Low Voltage Cascode Amplifier

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***Abstract*-A 0.8 V folded cascode amplifier was designed in 0.18-μm standard CMOS technology. Emphasis was placed on observing the low voltage design and using current driven bulk (CDB) technique to achieve this goal. The CDB technique was introduced as a method for low voltage design by reducing threshold voltage. This design achieves 141dB DC gain, 56Mhz 3dB band width and 65GHz gain band width, which is the working condition of pipeline ADCs.**

Index Terms – low voltage, ultra-low voltage operational amplifier, current driven bulk.

I. INTRODUCTION

Technology scaling is driving the supply voltages of digital circuits down to 1.2V by 2004 and to 0.9 V by 2008, according to the Semiconductor Industry Association's road map [1]. At the same time, the migration toward System-On-a-Chip (SoC) adds pressure on the analog circuits to follow that trend [2]. There are several approaches to ultra-low voltage supply circuit design which have recently been described; e.g., based on charge pumps [3], bulk drive [4], floating gates [5], limited common-mode range input circuits [6], [7], negative conductance [8] or CDB technique [9].

We can see the CDB technique, which is used as a method for compensating body effect [9], as means of reducing the threshold voltage in some transistors.

In this paper, we look to how CDB technique can reduce the threshold voltage in a standard CMOS process, and we use the reduced threshold voltage transistors to implement a 0.9-V folded cascode operational amplifier with compatible input- and output levels.

Section II gives an overview of CDB technique. Section III includes the design consideration of the folded cascode operational amplifier. Simulation results and measurements are presented in Section VI and finally conclusion is made in Section V.

II. CDB TECHNIQUE

Current Driven Bulk (CDB) as a technique to reduce the threshold voltage of MOS transistor in standard CMOS technology is shown in [9]. Equation (1) shows the relationship between threshold-voltage and V_{BS}, which is called bulk bias voltage.

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{2\Phi_F}) \quad (1),$$

where: V_{th0} : Zero bias threshold voltage

γ : Bulk effect factor

Φ_F : Fermi potential

The CDB technique [9] targets the absolute value of V_{BS}. We show, here, that technique is also applicable to transistors, which have no body effect; i.e V_{BS}=0.

Replacing this in equation (1) yields $V_{th} = V_{th0}$.

As this becomes evident, the bulk bias voltage does not play a significant role in threshold voltage. Our explanation for effectiveness of CDB technique is as follows. The relationship between threshold voltage and acceptor concentration (N_A) in NMOS can be expressed using the following equations:

$$V_{th0} = \Phi_{ms} + -2\Phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_I}{C_{ox}} \quad (2)$$

$$Q_{B0} = \sqrt{2q.N_A.\varepsilon_{si}|-2\Phi_F|} \quad (3)$$

Injecting a current into the bulk in NMOS would change the acceptor concentration (N_A), which in turn, causes a decrease in the threshold voltage of NMOS. Same understanding is valid for PMOS and donor concentration by extracting an electron from bulk.

In reality, the turn-on phenomenon is a gradual function of the gate voltage, making it difficult

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to define V_{th} clearly. In semiconductor physics, the V_{th} of an NMOS is usually defined as the gate voltage for which the interface is "as much *n*-type as the substrate is *p*-type." This definition cannot directly indicate whether the device is "on" or "off."[10] The drain current however can clearly indicate, whether the device is "on" or "off." To calculate the threshold voltage we used I-V characteristic, as follows:

$$I_{DS} = \mathrm{K}(V_{eff})^n + \alpha \qquad (4)$$

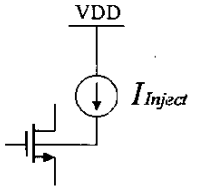
$$V_{eff} = V_{GS} - V_{th,n} \qquad (5)$$

From the equations (4) and (5) one observes that Let I_{DS1}, α_1, V_{eff1}, V_{GS1} and $V_{th0,n1}$ be the specifics of the MOS transistor without the bulk injection and I_{DS2}, α_2, V_{eff2}, V_{GS2} and $V_{th0,n2}$ be the specifics of the MOS transistor with the injection. IF $I_{DS1}=I_{DS2}$ and $\alpha_1 = \alpha_2$ then $V_{eff1}=V_{eff2}$ from eq. (5), one can observe that

$$(V_{GS1} - V_{th,n1}) = (V_{GS2} - V_{th,n2})$$

$$\Rightarrow \quad (V_{GS1} - V_{GS2}) = (V_{th,n1} - V_{th,n2}) \qquad (6)$$

Fig.1: NMOS CDB transistor



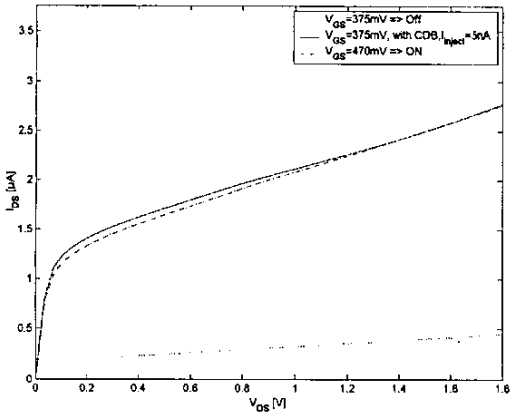


Fig.2: Transistors characteristic

Fig.2 shows I-V characteristic for transistor with and without bulk injection. The dotted curve is for a transistor without the bulk injection and with V_{GS}=375 mV. This transistor is in the off-mode.

This transistor would be in on-mode when V_{GS}= 470mV, as shown by dash-line in Fig.2. The solid line corresponds for a transistor which has lower V_{GS}=375mV, but with bulk injection (I_{inject}=5nA), although the V_{GS} of the latter transistor is smaller.

Using eq. (6) one can calculate the threshold voltage as the following example shows.

The transistor is in on-mode. However, one should appreciate the reduction in threshold voltage by approximately 100mV, using CDB technique.

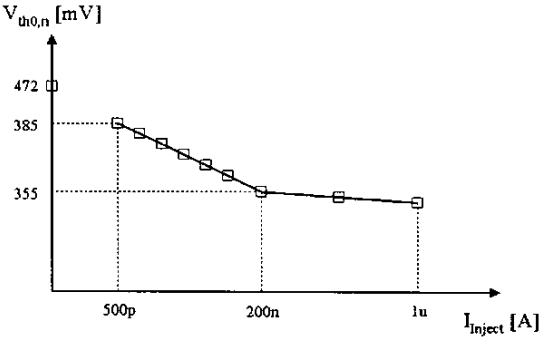


Fig.3: Effect of Inject current on threshold voltage

Fig.3 is a diagram of V_{th} *Vs.* I_{Inject}. It shows the approximate range of the current injected into the bulk by which the V_{th} is considerably changed. Here, I_{inject} ε {500pA ,200nA} results in a decline in $V_{th0,n}$ form 385mV to 355mV.

According to [9] there are some disadvantages in CDB technique such as Output Impedance, Low Frequency Pole-Zero Pair and Slew rate.

III. CASCODE AMPLIFIER

The typical folded-cascode amplifier is commonly preferred for high frequency applications since the parasitic capacitance and the transconductance of the folding transistor determine the non-dominant pole of this amplifier [11].

This configuration has two advantages: 1) high voltage gain 2) large bandwidth due to less Miller effect [10]. Fig. 4 shows our amplifier, which is a standard folded cascode amplifier

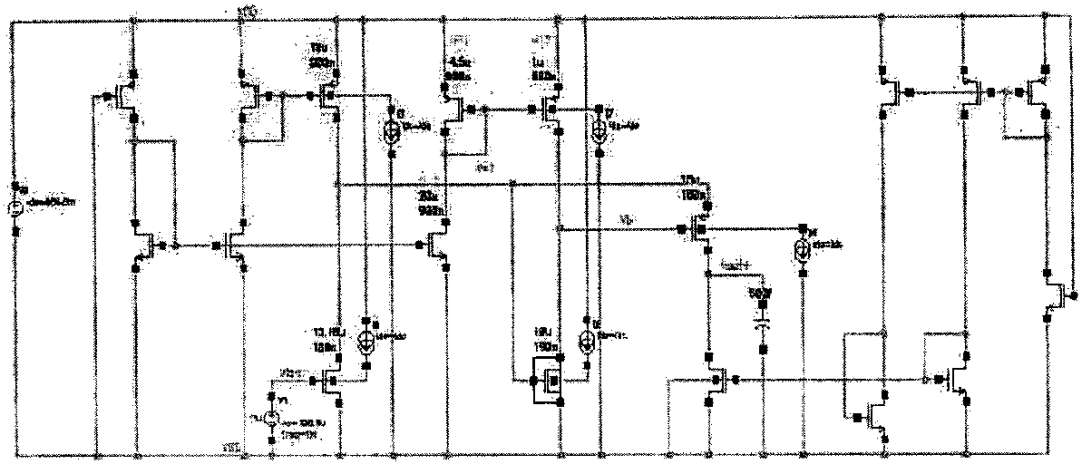


Fig.4: Schematic Diagram

with CDB transistors. Due to the concept of the CDB method, which is based on current bulk driven, we are injecting current into the circuit.
In such a low voltage-design, it is an advantage to operate the cascading transistor in sub-threshold, as that makes it easier to generate the bias voltages; however, it is not critical.
The other transistors should work in strong inversion mode. as good matching gives the lowest overall offset error.
The limited gain achievable in folded-cascode configuration has motivated the invention of gain-boosting techniques. These techniques are usually applied to cascade operational amplifiers to increase their gain with little degradation in speed [12],[13]. Transistor (M_{13}) plays a gain-boosting role in our design.

IV. Measurements

An experimental amplifier has been simulated in a standard 0.18μm CMOS technology. Numerical results extracted from the simulations for design are shown in this section in Table 2.

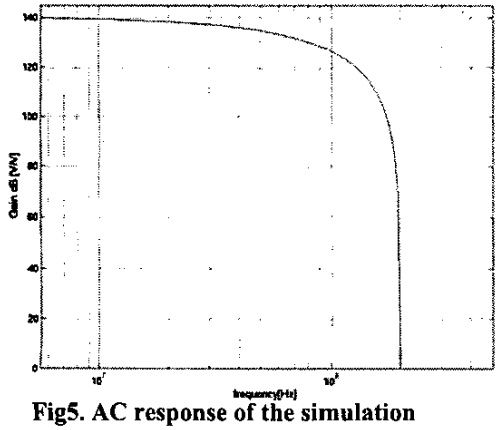


Fig5. AC response of the simulation

DC Gain	**141dB**
GBW	**65G**
3dB freq.	**56Mhz**
Power	**82uW**
VDD	**0.8V**
Output Level	**0.4V**
Load	**100pf**
I-Inject	**10nA to 200nA**

Tabel-1: Simulation result.

V. Conclusion

In this paper, we showed CDB technique as a method of reducing threshold voltage in any transistor and we designed an ultra-low voltage folded cascade, gain-boosted operational amplifier using CDB technique. At 0.8 volts power supply, it has a dc gain of 141 dB, 50MHz bandwidth and 56GHz gain bandwidth. This design is usable for pipeline ADCs. This design was made possible by CDB technique as a new method of reducing threshold voltage of transistor.

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