# A DC-SIDE FAULT-TOLERANT BIDIRECTIONAL AC/DC CONVERTER FOR POWER SYSTEM INTEGRATION OF LOW-VOLTAGE DC DISTRIBUTION SYSTEMS

by

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**A DC-Side Fault-Tolerant Bidirectional AC-DC Converter for Power System Integration of Low-Voltage DC Distribution Systems**

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# Abstract

With the rising potential for the employment of low- and medium-voltage direct-current (dc) electric power distribution systems, most notably for a more efficient integration of plug-in electric vehicles and such other distributed energy resources as photovoltaic (PV) panels, there is a need for robust ac/dc electronic power converters that can interface such dc distribution systems with the legacy alternating current (ac) power system. Thus, this thesis proposes a new single-stage low-voltage three-phase ac-dc power converter that is simple structurally, enables a bidirectional power exchanges between the ac and dc distribution systems, and can handle short-circuit faults at its dc as well as ac sides. The proposed converter consists of three legs, corresponding to the three phases of the host ac grid, each of which hosting two full-bridge submodule (FBSM), in an architecture that can be regarded as a special case of the so-called modular multi-level converter (MMC). Thus, at the dc port each FBSM is connected in parallel with a corresponding capacitor, while the ac voltage of each phase is synthesized by the coordinated sinusoidal pulse-width modulation (SPWM) of the two corresponding FBSMs. This architecture allows the generation of low-distortion ac voltage while it also provides the converter with the very important dc fault current blocking capability since, upon the detection of a short circuit across the converter dc port, the switches of the FBSMs are turned off and disallow the flow of any dc current. The thesis also presents a mathematical model for the converter, for analysis and control design purposes. Thus, the control for the regulation of the overall dc-side voltage, as well as those for the regulation of the dc voltages of the FBSMs are devised based on the aforementioned mathematical model and presented with details. It is further shown that the voltage conversion ratio of the proposed converter is the same as that offered by a conventional voltage-sourced converter (VSC), whereas the VSC is vulnerable to dc- side shorts. The proposed converter can be extended to medium-voltage levels by multiplying the number of FBSMs in each leg. The effectiveness of the proposed converter and its controls is demonstrated through time-domain simulation studies conducted on a topological model of the converter in PSCAD/EMTDC software environment.

**Keywords:** Control, dc-side fault, modeling, modular converter, distribution systems, bidirectional, simulation model.

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# Convention for Notations

For clarity and consistency, the following notations are used throughout the presented thesis.

- Circuit parameters are denoted by upper-case letters, for example, $R_{arm}$, $C$, etc.
- Instantaneous voltages, currents and powers are denoted by lower-case letters, for example $v_{dc}$, $i_{ext}$, $p_g$, etc.
- Real and reactive powers are denoted by upper-case letters, for example $P_g$, $Q_g$, etc.
- $dq$-transformed variables are denoted by lower-case letters and accompanied by applicable subscript of $d$ or $q$ referring to the d-or q-axis parameter, respectively, for example, $i_d$, $v_{gq}$, etc.
- Laplace transformed variables are denoted by upper-case letter and accompanied by $(s)$, for example, $V_{t\delta q}(s)$
- Subscript $\delta$ denotes a differential-mode parameter of the converter.
- Subscript $\sigma$ denotes a common-mode parameter of the converter.
- Subscript $t$ denotes a converter phase terminal variable.
- Subscript $g$ denotes a converter ac-side variable.
- Subscript $k$ denotes phase $a$, $b$, or $c$ of the converter.
- Subscript 1 denotes an upper-arm variable.
- Subscript 2 denotes a lower-arm variable.
- Subscript $j$ denotes 1, or 2, corresponding to the upper and lower arm of the corresponding leg of the converter.

# List of Abbreviations

| | |
|---|---|
| DC | Direct Current |
| AC | Alternating current |
| HVDC | High Voltage DC |
| PV | Photo-voltaic |
| LED | Light Emitting Diode |
| LVDC | Low Voltage DC |
| kV | Kilovolt |
| MG | Microgrid |
| PCC | Point of Common Coupling |
| IGBT | Insulated Gate Bipolar Transistor |
| CB | Circuit Breaker |
| DG | Distributed Generation |
| BESS | Batter Energy Storage System |
| EV | Electric Vehicle |
| AES | All-Electric Ship |
| IPS | Integrated Power System |
| FACTS | Flexible AC Transmission System |
| LV | Low Voltage |
| V | Voltage |
| MV | Medium Voltage |
| Hz | Hertz |
| DER | Distributed Energy Resources |
| ms | milliseconds |
| EMCB | Electromechanical Circuit Breaker |

# List of Abbreviations

| | |
|---|---|
| MCCB | Molded Case Circuit Breaker |
| VSC | Voltage-sourced converter |
| PWM | Pulse-width modulation |
| NPC | Neutral-Point Clamped |
| MMC | Modular-Multilevel Converters |
| PSCAD/EMTDC | Power Systems Computer Aided Design using Electromagnetic Transients including DC |
| FBSM | Full-Bridge Submodule |
| UPWM | Unipolar pulse-width modulation |
| BPWM | Bi-polar pulse-width modulation |
| PLL | Phase-Locked Loop |
| EXT | External |
| PI Compensator | Proportional-Integrator Compensator |
| RHP | Right-Half Plane |

# List of Symbols

| | |
|---|---|
| $v_{dc}$ | DC voltage |
| $v^*_{dc}$ | Reference value of the dc-side voltage |
| $v_{gk}$ | Grid voltage of the phase $k$ (k=a, b, and c) |
| $v_{sk}$ | Grid voltage phase $k$ at the point of common connection |
| $V_s$ | RMS line-to-line ac-side voltage at the POI |
| $v_{sd}$ | D-axis component of the voltage at PCC |
| $v_{sq}$ | Q-axis component of the voltage at PCC |
| $v_{tk}$ | Terminal voltage phase $k$ |
| $v_{t1k}$ | Terminal voltage of the upper arm FBSM of leg $k$ |
| $v_{t2k}$ | Terminal voltage of the lower arm FBSM of leg $k$ |
| $v_{C1k}$ | DC-side voltage of the upper arm FBSM of leg $k$ |
| $v_{C2k}$ | DC-side voltage of the lower arm FBSM of leg $k$ |
| $v^*_{t\sigma k}$ | Reference value of the common-mode terminal voltage of the $k$th leg |
| $v^*_{t\delta k}$ | Reference value of the differential-mode terminal voltage of the $k$th leg |
| $v_{t\sigma k}$ | Common-mode terminal voltage of the $k$th leg |
| $v_{t\delta k}$ | Differential-mode terminal voltage of the $k$th leg |
| $v_{t\delta d}$ | D axis component of the differential-mode terminal voltage |
| $v_{t\delta q}$ | Q axis component of the differential-mode terminal voltage |
| $e$ | equivalent Thevenin voltage seen from the ac side. |
| $y_{\sigma k}$ | Common-mode dc-side squared voltage of the FBSMs in the $k$th leg of the converter |
| $y_{\delta k}$ | Differential-mode dc-side squared voltage of the FBSMs in the $k$th leg of the converter |
| $\widehat{i}$ | Ac-side terminal current peak |

# List of Symbols

| | |
|---|---|
| $\varphi$ | Ac-side terminal current angle |
| $i_{dc}$ | Dc-side current of the converter |
| $i_k$ | Ac-side converter current of phase $k$ |
| $i_{gk}$ | AC grid current of phase $k$ |
| $i_{1k}$ | Current in the upper arm FBSM of leg $k$ |
| $i_{2k}$ | Current in the lower arm FBSM of leg $k$ |
| $i_d$ | Ac-side current $d$ component in $dq$-frame |
| $i_q$ | Ac-side current $q$ component in $dq$-frame |
| $i_d^*$ | Reference value of the $d$ component of the ac-side terminal current in $dq$-frame |
| $i_q^*$ | Reference value of the $q$ component of the ac-side terminal current in $dq$-frame |
| $i_{\delta k}$ | Differential-mode current of the phase $k$ |
| $i_{\sigma k}$ | Common-mode current of the phase $k$ |
| $i_{\sigma k}^{1*}$ | Reference value of the ac component of the common-mode current of phase $k$ |
| $i_{\sigma k}^{1}$ | AC component of the common-mode current of phase $k$ |
| $I_{\sigma k}^{0}$ | DC component of the common-mode current of phase $k$ |
| $i_{DC}$ | DC-side current of the proposed converter |
| $i_{ext}$ | External current |
| $\tilde{i}_{\sigma k}^*$ | Reference small-signal perturbation of the common-mode current of the $k$th leg. |
| $\tilde{i}_{\sigma k}$ | Small-signal perturbation of the common-mode current of the $k$th leg |
| $\hat{i}^1$ | Maximum value of the fundamental-frequency component of the common-mode current |
| $m_{\delta d}$ | D axis component of the differential-mode modulating signal |
| $m_{\delta q}$ | Q axis component of the differential-mode modulating signal |

# List of Symbols

$m_{\delta k}$ Differential-mode modulating signal of the $k$th phase of the converter

$m_{\sigma k}$ Common-mode modulating signal of the $k$th leg

$m_{1k}$ Modulating signal of the FBSM in the upper arm of the $k$th leg of the converter

$m_{2k}$ Modulating signal of the FBSM in the lower arm of the $k$th leg of the converter

$P_{ext}$ External power

$P_{dc}$ DC power going through the dc side of the converter

$P_t$ Ac-side terminal active power

$P_s^*$ Reference value of the active power exchanged between grid and the converter at PCC

$P_s$ Active power exchanged between grid and the converter at PCC

$P_{loss}$ Power loss in the converter

$P_{1k}$ Rate of change of energy stored in the dc-side capacitor of the FBSM in the upper arm of the $k$th leg of the converter

$P_{2k}$ Rate of change of energy stored in the dc-side capacitor of the FBSM in the

$P_{\sigma k}$ Common-mode active power of the FBSMs in the $k$th leg of the converter

$P_{\delta k}$ Differential-mode active power of the FBSMs in the $k$th leg of the converter lower arm of the $k$th leg of the converter

$Q_t$ Ac-side terminal reactive power

$Q_s^*$ Reference value of the reactive power exchanged between grid and the converter at PCC

$Q_s$ Reactive power exchanged between the grid and the converter at PCC

$Q_c$ Reactive power delivered by the capacitor of the LCL-filter at the PCC

$f_g$ Grid frequency

# List of Symbols

| | |
|---|---|
| $f_{sw}$ | Switching frequency of the converter |
| $\omega$ | Grid angular frequency |
| $\beta_k$ | Initial phase angle of $i^1_{\sigma k}$ |
| $\gamma_k$ | Phase displacement between $i^1_{\sigma k}$ and $v_{sk}$ |
| $C$ | DC-side capacitor of the converter and its FBSMs |
| $L$ | Arm inductance |
| $R$ | Arm resistance |
| $L_g$ | Grid inductance |
| $R_g$ | Grid resistance |
| $L_f$ | AC-side filter's series inductance |
| $R_f$ | Ac-side filter's series resistance |
| $C_f$ | Ac-side filter's shunt capacitance |
| $R_{fd}$ | Ac-side filter's damping resistor |
| $L^{'}$ | Equivalent inductance as seen from the PCC |
| $R^{'}$ | Equivalent resistance as seen from the PCC |
| $r_{on}$ | Online resistance of each switch |
| $K_{i\sigma k}(s)$ | Common-mode current controller of the $k$th leg |
| $K_{VDC}(s)$ | DC-side voltage controller of the proposed converter |
| $K_{p\sigma k}(s)$ | Common-mode FBSM power controller |
| $K_{P\delta k}(s)$ | Differential-mode FBSM power controller |
| $K_d(s)$ | D-axis ac-side current controller |
| $K_q(s)$ | Q-axis ac-side current controller |

# List of Symbols

$BRK1$ Breaker 1, connecting the ac-grid to the POI of the proposed converter

$BRK2$ Breaker 2, connecting the POI of the proposed converter to its terminal through the low-resistive path

$BRK3$ Breaker 3, connecting the POI of the proposed converter to its terminal through the high-resistive path

# Chapter 1

# Introduction

## 1.1 Background and Motivation

In late 1880s and early 1890s, *Thomas Alva Edison* and *George Westinghouse* publicly debated their proposed power transmission systems, i.e., direct-current (dc) based and alternating-current (ac) based power transmission systems, respectively. The aforementioned debate is known as the *battle of currents* in the literature. The result of the battle of currents was strongly influenced by the invention of a number of breakthrough ac-based devices by Nikola Tesla, and led to the global acceptance of ac-based power system as the main architecture for electricity generation, transmission, and distribution [1]. However, in the past couple of decades, dc-based systems started to return as high-voltage dc transmission systems (HVDC), especially for long distances due to their economical, technical, and environmental advantages[2]. Large-scale integration of renewable energy resources is another major influencer in the return of HVDC systems [3]. It must be mentioned that the invention of transistors had a great impact on the come-back pace of the dc systems. Although, initially, transistors were designed for the applications in computers and communications, as a by-product, they have enabled the transformation of dc voltages, and caused a revolution in power electronics [1].

Over the past two decades a number of trends in the electric power systems, has directed the attention to the use of dc in lower voltage levels. Among the most important trend the growth in photovoltaics (PV)-based power generation, rising interest in the LED lighting, and increasing focus on the sustainable and efficient energy leading to a shift from fossil fuel as the main source of electric power generation can be named [7]. Furthermore, the escalating interest in renewable and distributed generation systems, is another influencer in the growth of low-voltage dc systems [4]. In comparison to the available ac systems, LVDC has a higher power transmission capacity, no need for source synchronization, and doesn't have skin effect associated with it. Furthermore, LVDC networks can reduce the conversion losses by eliminating the redundant conversion stages for distributed renewables which inherently generate dc power [6]. Perhaps one of the earliest applications of low-voltage direct current (LVDC) in recent years, started in 2005 in Finland, with the development of 1-$kV$ intermediate LVDC distribution systems [5]. Employing dc systems can also benefit the customers which require dc, by eliminating the conversion stage. Fig. 1.1 presents some of the applications of dc in today's electricity market and the required voltage range for those applications [7].

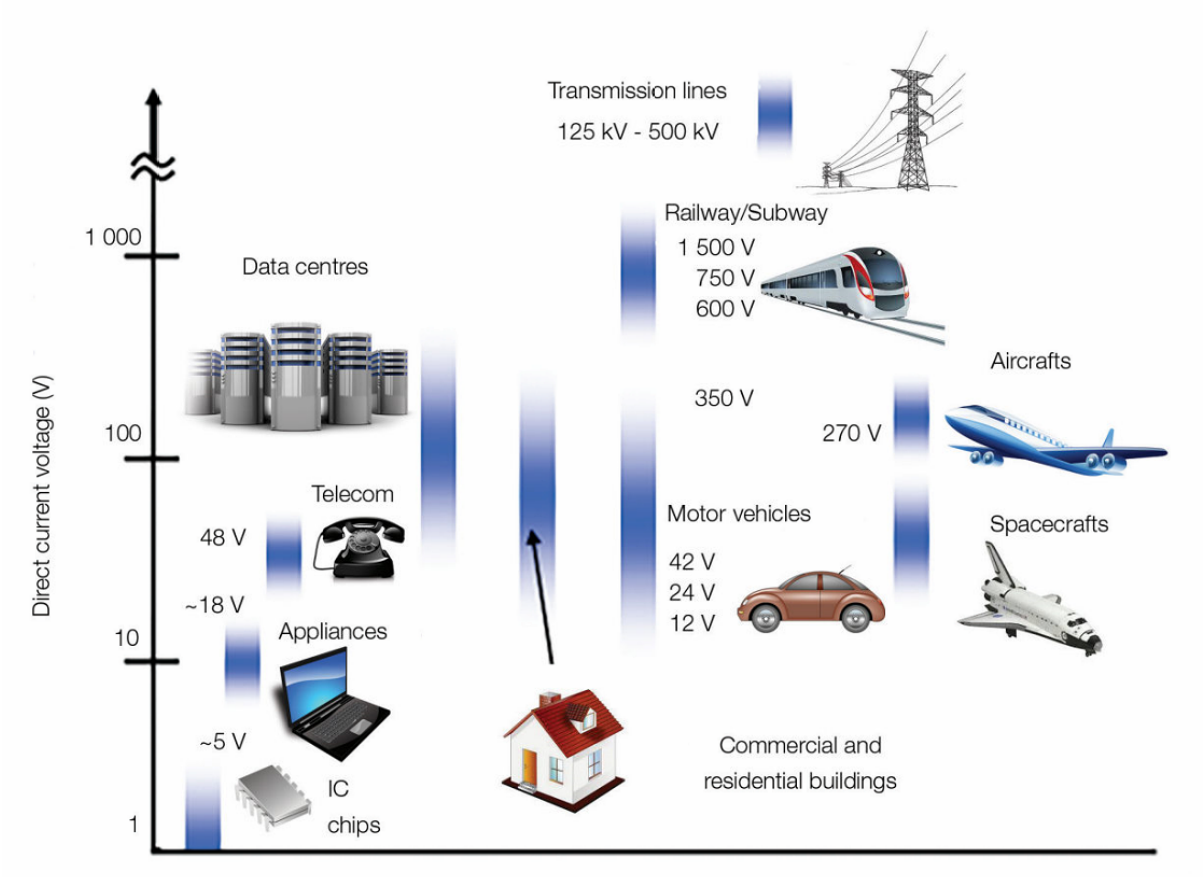


Figure 1.1: Voltage range for a number of dc application in today's electricity market[7].

Fig. 1.2 presents an example of a basic implementation of the LVDC system which is connected to the ac grid. The aforementioned connection between the dc and ac grid is done through the use of an ac/dc converter, which can be considered as one of the most critical components [11] and [12]. So far, the merits of the LVDC networks were discussed, but it must also be mentioned that LVDC systems have significant technical challenges associated with them in terms of dc-side fault detection and isolation [13]. None the less, ac-distribution systems also have their own merits, like the ability to use transformers, and mature technology of ac circuit breakers [8]. Thus, hybrid ac/dc electrical network through capitalizing the advantages of both ac- and dc-distribution systems is an answer to the needs in today's market [9] and [10]. The aforementioned networks must be interconnected and allow the bidirectional power flow between ac and dc grids. Furthermore, there have been many arguments addressing one of the most important shortcomings of dc grids, i.e., the lack of effective and economical fault-handling capability for dc systems. The proposed solutions can be mainly categorized in two groups: using DC circuit breaker or dc-fault tolerant converters [14]. The focus of this thesis is to propose a new topology and control method for a bidirectional ac/dc converter, with the dc-side fault handling capability.

This chapter, focuses on outlining the merits, problems, and structures of dc distribution and ac/dc power-converter systems. Followed by listing the problems which are addressed in

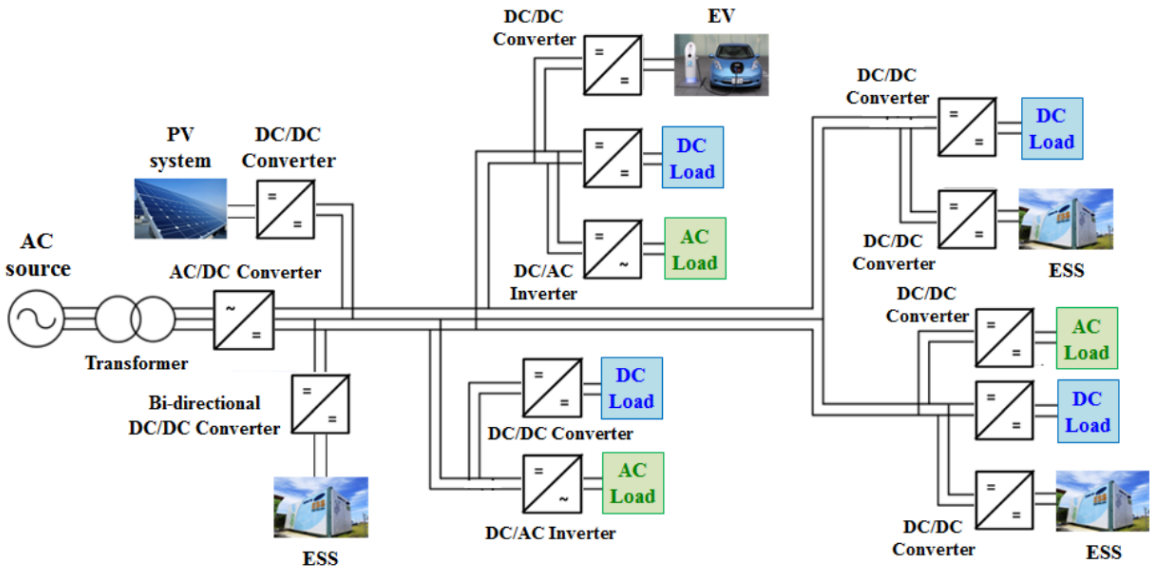


Figure 1.2: Concept of an LVDC distribution system [5].

the thesis, a literature survey of related prior work done in this area, and the scope of the thesis.

## 1.2 Statement of Problem and Overall Thesis Objectives

The use of dc networks in distribution systems is an emerging concept and not fully grown. Increasing presence of distributed generation and loads with strict power quality requirements, along with the interest to make the grid more resilient have impacted the characteristics of the traditional distribution systems, and has led to the increase in the popularity of LVDC systems, as they offer several advantages compared to LVAC grids [21]. The mentioned dc systems might even offer the ability to form an isolated power system which is known as microgrid (MG) in the literature [15]. However, even in that case the LVDC microgrid must be connected to its host ac grid through power converters. The connection between the dc and ac system is done through power converters and at the point of common coupling (PCC) [23]. Thus, power converters are responsible for the direction of the power flow. Previously and in the absence of a considerable distributed energy sources such as photovoltaics (PVs), fuel cell and etc. it would've been safe to assume a uni-directional power flow from the ac grid to the dc network. Never the less, with the growing interest in employment of DERs, the power must be able to transfer in both direction which requires a bi-directional converter.

It goes without saying that using LVDC networks, the behavior of the system during the normal operation and in presence of faults, defers from the conventional ac grid. Although, previously the dc section used to have limited extensions and as a result the probability of occurrence of a dc-side fault was considerably low and almost negligible, in recent years the LVDC networks are becoming much more complex and contain more extensions which further signifies the fault related problems on the dc system. The aforementioned issues need to be dealt with by proper and economical protection schemes. In contrary to the protection

technology designed for ac power systems, which is fully grown, achieving appropriate protection for dc power systems is still a challenge [22]. Most commonly suggested protection methods against dc-side faults at PCC are employing dc circuit breaker (CB) or incorporating fault-tolerant converters. At the connection point of ac and dc distribution systems it is desirable to have a bidirectional power flow, and thus bidirectional ac/dc converter using insulated gate bipolar transistor (IGBT) modules are mainly used. Morover, employment of bidirectional ac/dc converters with IGBT modules further complicates the protection system design due to their sensitivity to over-currents and their requirement for fast protection [23]. Although each one of the mentioned methods has a host of merits associated with it, this thesis focuses on the latter approach and presents a bidirectional ac/dc converter with the ability of blocking pole to pole and pole to ground short circuit faults at its dc-side terminal.

## 1.3 Literature Survey Pertinent to the Thesis Objectives

There are a number of literature currently available which investigate the structure and benefits of the low-voltage dc systems in comparison to its equivalent ac system, the problems associated with the mentioned LVDC systems [17] to [19], and topology of the front-end converters as a key equipment in LVDC. This section first presents a brief comparison between the low-voltage ac and dc grid, followed by further analyzing one of the biggest challenges in designing a complex LVDC system, i.e., the ability to handle the faults and the protection methods previously discussed in the literature. This section then moves on to exploring a number of previously proposed ac/dc converters and their effectiveness as a front-end converter in a LVDC system.

### 1.3.1 AC Versus DC Distribution Systems

Introduction of LVDC systems begins with addressing a number of available areas in the current distribution system infrastructure, in which the main ac-based power system has a number of shortcomings. In this subsection, first these areas are presented along with the merits of both dc- and ac-distribution systems in addressing the aforementioned problems.

- **Energy Storage, Distributed Generation, and Micro-grids:** In recent years, the trend in the growth of electric power system has increasingly been going towards distributed generations (DGs) , since they can lead to efficiency improvement in the system by producing the required energy in distributed manner and close to the demand and thus eliminating the transmission losses [8]. Employing dc system provide the opportunity for a more straightforward integration of distributed energy resources such as PVs, fuel cells, wind, battery energy storage systems (BESSs), etc. [24]. The mentioned dc systems can offer the ability to work independent from the main grid and in islanded mode and form a dc microgrid, which in comparison to the ac microgrid they are less costly while they can benefit from the other advantages of the LVDC systems [20].

- **Increasing Application of Electric Vehicles:** In recent years, there was a greath growth in the interest in electric vehicles (EVs), including fully electric vehicles and plug-in hybrid electric vehicles, due to the ecological aspects [25] and [26]. Increase in the

number of charging stations, can be named as one of the leading reasons in the growth of the EVs [27]. Furthermore, employing EVs can provide a potential to improve the grid resiliency and assist balance loads. [8] whilst it offers higher efficiency and less noise in comparison to the traditional gasoline vehicles [28].

- **Computers, Lighting, and Home Electronics:** Electric appliances in homes using power converters such as fridges, freezers, dish washers, washing machines, and modern air conditions, LED lighting, space and water heating with heat pumps or direct heating, etc. could be directly fed by dc power [3]. In the current configuration, each load has its own power supply. However, employing dc distribution systems can eliminate the redundant conversion of power from dc to ac and then back to dc, again [8].

- **Shipboard Power Systems:** In recent years, increasing the strictness on the government regulation of emissions while customers' fuel-efficiency requirements have risen, has led to the current trend toward the all-electric ship (AES). The most significant feature of the AESs is the concept of the integrated power system (IPS), which minimizes the number of generators in ships and it can be regarded as a large-scale, on-board microgrid [29].

DC-distribution power systems has properties that makes it more suited to address the aforementioned areas than ac-distribution systems. The mentioned properties can be categorized as follows

- **Incorporation of Renewable Energy Resources:** By using dc-distribution system, the incorporation of the renewable energy sources becomes much more simpler. The ease of connecting the renewable energy sources to a dc-distribution system can be justified by the fact that in order to connect an energy source to a dc system only the voltage has to be monitored and controlled. However, connecting renewable energy sources to the ac system requires the voltage magnitude, frequency and phase must match [30].

- **Reliability and Un-incorruptible Supplies:** Buildings such as hospitals and special offices such as banks and data centers are categorized as critical loads and require a "24-7" access to the electric power. Thus, special measures must be taken to ensure the smooth access to the electricity for critical loads. One measure is to utilize decentralized generation scheme instead of the more traditional centralized generation. By doing this more sources can be integrated to the network at various locations and closer to the critical loads [31]. The aforementioned measure can be done both using ac or dc power systems. However, in comparison to ac solutions, dc measures contain fewer conversion staged and thus increasing efficiency [30]. DC also enables connection of various sources without the need for synchronization which further simplifies the integration process [7] and enables the easy incorporation of more local energy storage and sources, either standby power generation, which are used when a fault occurs on the utility grid or distributed generation which can even work continuously [30].

- **Voltage Stability:** One of the key components in dc power systems are the power electronic converters. Depending on the type of the converter being used at the point of common coupling of ac and dc grid, it might be possible to control the reactive power

flow independently and according to the requirements of the system in order to achieve the required voltage stability and eliminating the use of other equipment with the sole purpose of controlling the reactive power flow such as capacitor banks and FACTS [8].

- **Lighting and Home Electronics:** As it was previously mentioned there are a number of equipment in the residential and commercial buildings which inherently uses dc power. Apart from the typical equipment such as freezers, dishwasher and etc. the fluorescent lighting electronic ballasts also require dc power [8]. These devices typically include a rectifier inside them which lets changed their ac input to the required dc. Thus, by building dc buildings all of those unnecessary power conversion stage will be eliminated. As a result, in recent years the possibility of dc homes have been the subject of many researches.

- **Power Quality:** Reactive power consumption and low-frequency current harmonics are two of the issues associated with power quality in traditional ac grids [7]. The power factor correction is one of the performed stages of dc power supplies. This will address the power quality problems associated with the consumption of reactive power. Moreover, by employing accurate design practices and filtering acceptable harmonic quality is also achievable [8].

- **Larger Power Transfer:** The low-voltage (LV) range for ac and dc systems are $5 - 1000\ V$ ac and $75 - 1500\ V$ dc, respectively. Thus, low-voltage dc systems have the ability to transfer larger power in comparison to low-voltage ac system. Moreover, since no reactive power is transferred through the dc grid, the losses are also reduced. The aforementioned property make it possible to even replace the low-power branch of the medium-voltage (MV) ac network by low-voltage dc distribution networks [38].

- **50/60-Hz Concerns:** Employing the dc-power system will lead to elimination of the potential health concerns of being exposed to 50/60-Hz ac-power systems [61].

The ac distribution networks also have its own advantages a number of which are mentioned in this part:

- **Voltage Transformation:** Historically the main advantage of the ac over dc is the ability to change the voltage levels in an ac systems through transformers [8]. However, even with the current developments in the field of power converters, still these solutions can be much more costly than a transformer.

- **Circuit Breaker Protection:** One of the most important aspects of any power system is its reliable operation. In case of ac distribution systems, circuit protection is more mature than that of dc systems. Moreover, periodic zero voltage crossings in ac systems greatly benefits the circuit protection of ac circuits. Since, during the zero crossing of the voltage, circuit breakers will have a better likelihood to extinguish a fault current arc [8].

Considering the advantages and shortcomings of both dc and ac distribution systems, and the maturity of current ac distribution system, one can conclude that the best approach is to

form a dc distribution system, in parallel with the current ac distribution system and connect them to one another wherever it's needed. As a result, the advantages of both systems can be used while trying to avoid their demerits.

### 1.3.2 Previously Proposed Protection Scheme for LVDC Systems

One of the critical issues associated with LVDC networks is designing a reliable protection system. Historically, LVDC systems used to be less complex, and as a result it was less likely to have a fault at the dc network. Furthermore, due to the lack of significant distributed energy resources (DERs) and simplicity of the LVDC networks a bidirectional power flow at the PCC was not a necessity, which enabled the use of grid-connected rectifiers with current limiting capabilities. However, due to the changes in the infrastructure of the distribution systems, the LVDC systems are becoming more complex, which leads to new requirements for the system, one of which is the ability to effectively detect and clear the dc-side faults [23].

Both the problems associated with interrupting faults without having natural zero crossing points, which is the case for the ac, and changes in the nature and transient response of the faults which are a consequence of employing complex LVDC networks, have made it more difficult to handle the dc-side faults. Previously done research in this area ([46] - [47]) show that a dc-side fault at terminals of a converter can result in a high short-circuit transient current with a magnitude of up to 35 times the steady-state fault current, and a duration of less than 4 $ms$. As a result, a significant thermal energy ($I^2t$) will flow through the network components. Hence, in the absence of an effective fault-current limiting device, the ratings of the components in the network must be higher, which in turn increases the costs of the plant [47].

There are a number of methods proposed in the literature to eliminate the dc side faults. These methods are briefly explained here.

- **Measuring the dc-side voltage and current and operating the ac-side breakers during the faults:** This method is an economical way to deal with the dc-side faults an is mostly used in HVDC systems. However, employing this method for dc distribution system leads to disconnecting the entire network from the grid until the available fast acting mechanical switch available on the dc system reconfigure the dc lines. Consequently, using the mentioned method can lead to problems associated with power quality and load stability [47].

- **Create zero-crossing points for dc fault currents:** This method employs a series reactor with the conventional electromechanical circuit breaker (EMCBs) on the dc side, to limit the magnitude of the dc-side fault current, and by causing it to oscillate create a zero crossing which then leads to fault current interruption by the EMCB during the first zero crossing. However, this method is not as reliable for high impedance faults, which require large reactors. Furthermore, addition of more reactance will increase the fault stress which is a result of releasing larger stored energy during the fault [47].

- **Direct elimination of dc-side fault using equipment that do not require zero crossing points:** Using fuses and EMCBs such as molded case circuit breakers (MCCBs), the fault current can be eliminated without using the zero-crossing points. However, the aforementioned devices have slower operation for dc in comparison to ac systems. As a

result these methods will not be able to protect the converters and other sensitive devices against the transient period of the discharge of the capacitors, and thus requires higher ratings for the devices. Moreover, the high transient current will also cause the dc-voltage to rapidly drop to zero and converters loosing the control. Furthermore, the undervoltage conditions during the transient period will make it more difficult to maintain the stability of local micro generators and avoid sympathetic tripping against remote dc faults [47].

Hence, there is a lack of fast yet mature and effective protection method for LVDC systems. As a result, recently more attention is payed to designing a converter with the ability to tolerate the faults at its dc side [48], which is the focus of this thesis.

### 1.3.3 Converter Typologies and DC-Side Fault Tolerability in Distribution-Level DC Systems

So far a number of advantages of the dc and ac distribution systems have been presented, and it was concluded that by building the two systems in parallel to each other the merits of both can be taken advantage of. It must be mentioned that these systems must be able to connect to each other at various locations, which is done through the use of power electronic converters. Thus, one of the key enabling components towards the realization of building a dc-distribution system along side the currently available low and medium voltage ac system, is the power-electronic converter. Moreover, as it was mentioned in the previous section, designing converter topologies with the ability to tolerate dc-side faults, will further solve the issues associated with the currently employed protection system for LVDC networks. There are various topologies suggested in the literature that would satisfy one or both network requirements previously mentioned in this chapter, i.e., bidirectional power flow and the ability to tolerate dc-side fault. This section of the thesis presents a summary of the aforementioned converter topologies which ranges from a thyristor bridge which is one of the most simple and economical solutions, to more complex designs like neutral-point clamped VSCs.

- **Three Phase Thyristor Rectifier:** One of the most basic and economical ac/dc converters is the thyristor rectifier which converts the ac input to a constant polarity dc. Figure 1.3 illustrates the schematic diagram of a three-phase thyristor rectifier. As it an be seen from Fig.1.3, the thyristor rectifier is a diode rectifier, where the diodes are replaced with thyristors. This converter is able to create a unidirectional power flow from the ac to dc system and can be used in feed and control of the dc motors among other applications. Since the thyristors do not let the current to pass in the reverse direction and there is no anti-parallel diodes in this scheme, the thyristor rectifiers have the ability to tolerate the dc-side faults. However, since thyristor rectifiers cannot enable the reversal of power flow, they can't be used as front-end converters in recent and more complex dc distribution systems with distributed generation. Moreover, they result in relatively high harmonics in the dc-side current and they require a transformer at their ac side in order to be able to change their ac-side voltage to the ac-grid voltage level and connect the converter to the grid, [32].

- **Voltage-Sourced Converter:** Figure 1.4 presents the schematic diagram of a three-phase voltage-sourced converter. Typically, in power-system applications the VSC is inter-

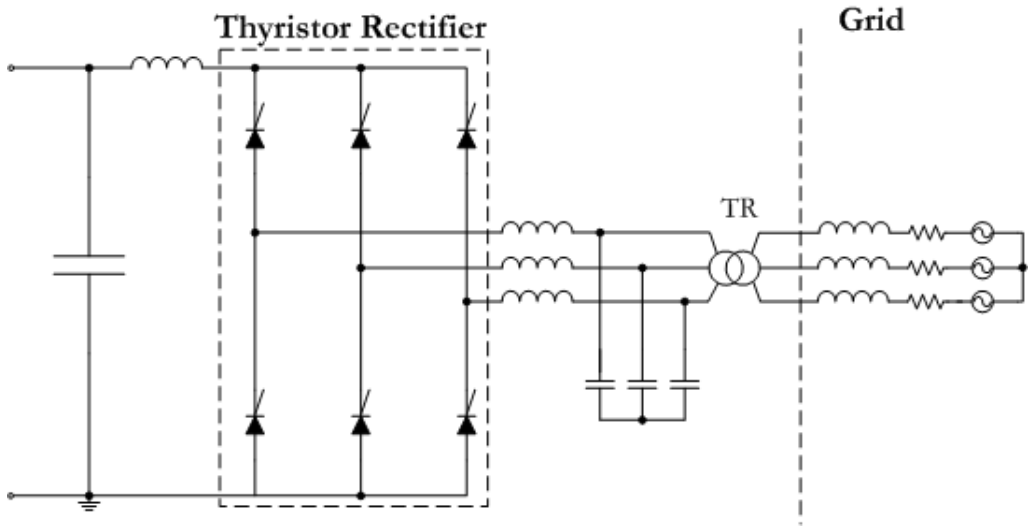


Figure 1.3: Schematic diagram of a thyristor rectifier.

faced with the ac grid through a transformer using a VSC as a front-end converter the bi-directional power flow from the ac grid to the dc side and vice versa. As it can be seen from Fig. 1.4 the VSCs consist of switches composing of anti-parallel connection of a fully controllable unidirectional switch and a diode [43]. The commutation of the aforementioned switches can be achieved through different modulation schemes, like pulse width modulation (PWM), and thus produces a low harmonic contribution. Moreover, using VSC the reactive power flow can be controlled independently. Hence, it has the ability to control the power factor and thus improving the voltage stability of the system. The applications of VSCs include HVDC light transmission, ac/dc converter in drives, and front-end converter in LVDC microgrids [32]. Hence it can be concluded that by employing a pulse width-modulated (PWM) voltage-sourced converter (VSC) operated as a controlled dc voltage power port the aforementioned shortcomings of the thyristor rectifier can be avoided.

However, upon occurrence of a fault at the dc-side of the VSC the dc-side capacitor will start to discharge which causes a fault current with a high magnitude and low rise time, and small duration. Furthermore, once the dc-link voltage drops to almost zero, which is the case during a short-circuit fault, the converter loses its capability to control the current. Consequently, fault current will start to go through the anti-parallel diodes of the isolated gate bipolar transistors. As a result, VSCs are vulnerable to dc-side faults, which in turn makes them unsuitable for current dc distribution systems [23].

- **Neutral-Point Clamped (NPC) VSC:** As it can be seen from Fig. 1.5 NPC is a combination of two-level half-bridge converters and two additional diodes. Similar to what has been previously mentioned regarding VSCs, NPCs not only have the ability to allow the bidirectional power flow, but also use various modulation schemes, like PWM, and thus result in low harmonics on the dc-side current. Neutral-point clamped (NPC) converters also require transformer at their ac side in order to connect to the ac grid [43]. Moreover, as it can be interpreted from Fig. 1.5, the NPC topology also results in bipolar dc-side

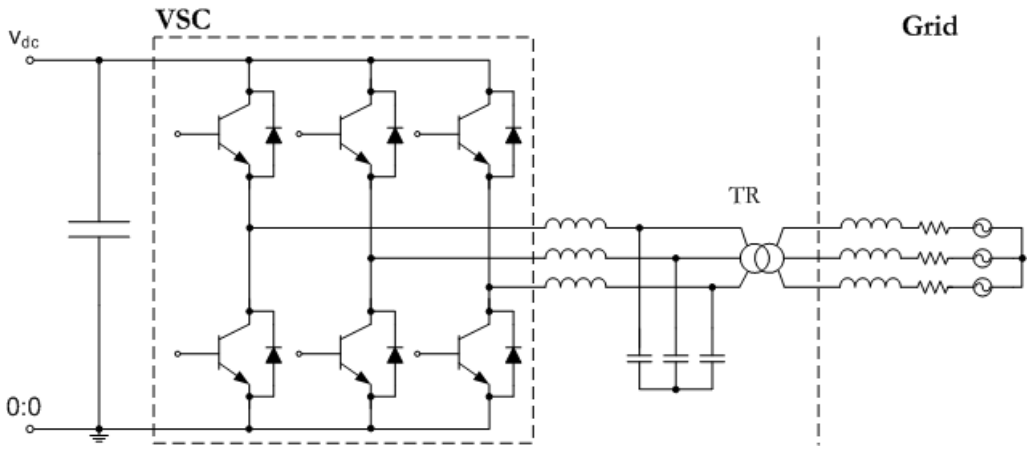

Figure 1.4: Schematic diagram of a three-phase, two-level voltage-sourced converter.

voltage. However, the same short circuit fault analysis previously described for VSCs can be applied to the NPC converters. Furthermore, the pole-to-ground short-circuit fault can travel through the clamping and anti-parallel diodes [48]. Consequently, similar to what was discussed for the VSCs, the ratings of the power electronic devices available in NPC converters must also be selected higher than what is required for normal applications, in order to be able to tolerate the thermal energy released during the short circuit faults and in absence of an effective protection scheme against the dc-side faults.

- **12-Pulse Thyristor Rectifier:** Figure 1.6 shows the typical configuration of a 12-pulse series-type thyristor rectifier, which consists of two identical six-pulse thyristor rectifiers. Hence, by employing the 12-pulse thyristor rectifiers, the merits of the simple thyristor converter including its ability to tolerate the dc-side fault is achievable. Furthermore, the dc-side current harmonics will be less than the 6-pulse thyristor rectifier, presented in Fig. 1.3, and results in bipolar dc-side voltage. However, in comparison to VSC and NPC, the

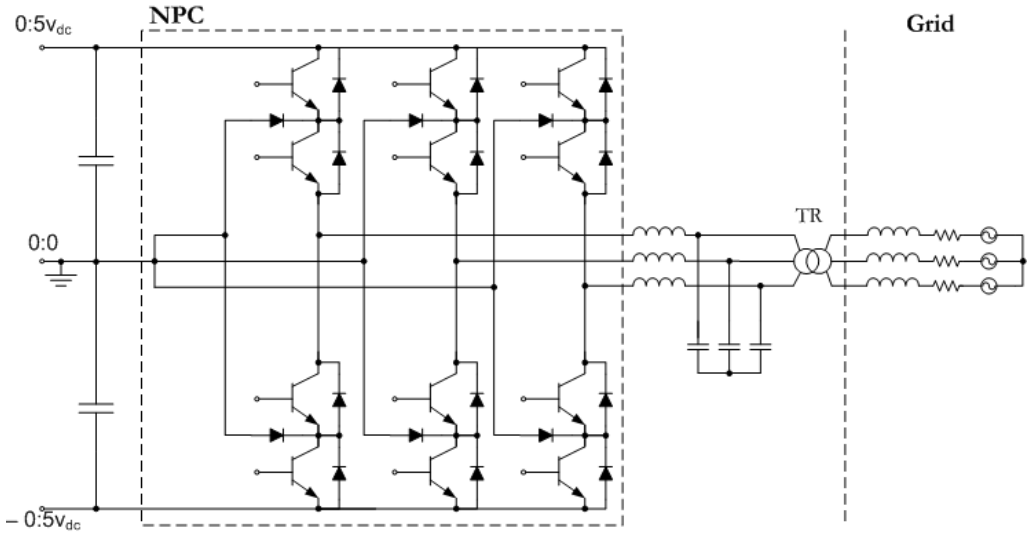

Figure 1.5: Schematic diagram of a three-level NPC.

dc-side current of the 12-pulse thyristor rectifier will still be considerably higher. It must also be mentioned that the 12-pulse thyristor rectifier requires a three-winding rectifier in order to be connected to the ac grid.

- **Two-stage VSC:** Previously the single-stage two-level VSC topology was analyzed, and it was outlined that one of the major problems associated with these type of the converters is their vulnerability to the dc-side faults. Hence, a new updated topology is presented here, which enables the user to benefit from the advantages of a typical single-stage VSC while providing protection against dc-side faults. The proposed design is a modified version of the discussed design in [33], where the H-bridge converter available in the second stage was replaced with a VSC. This design not only provides a path for bidirectional power flow between the ac and dc systems, and provides low harmonic output, but also is able to limit the short circuit current and behave as an electric dc breaker [33]. Figure 1.7 presents the discussed converter's topology. As it can be seen from the mentioned figure, the proposed two-stage converter consists of a series connection of a buck and VSC as the first and second stage of the converter, respectively. Furthermore, the presented two-stage VSC also leads to a reduction of the size of the dc-link capacitor [33]. However, all of the aforementioned merits are achieved by sacrificing the efficiency of the converter. Although employing a synchronous buck converter instead of a typical buck converter with diodes will lead to an increase in the overall efficiency, but it is still

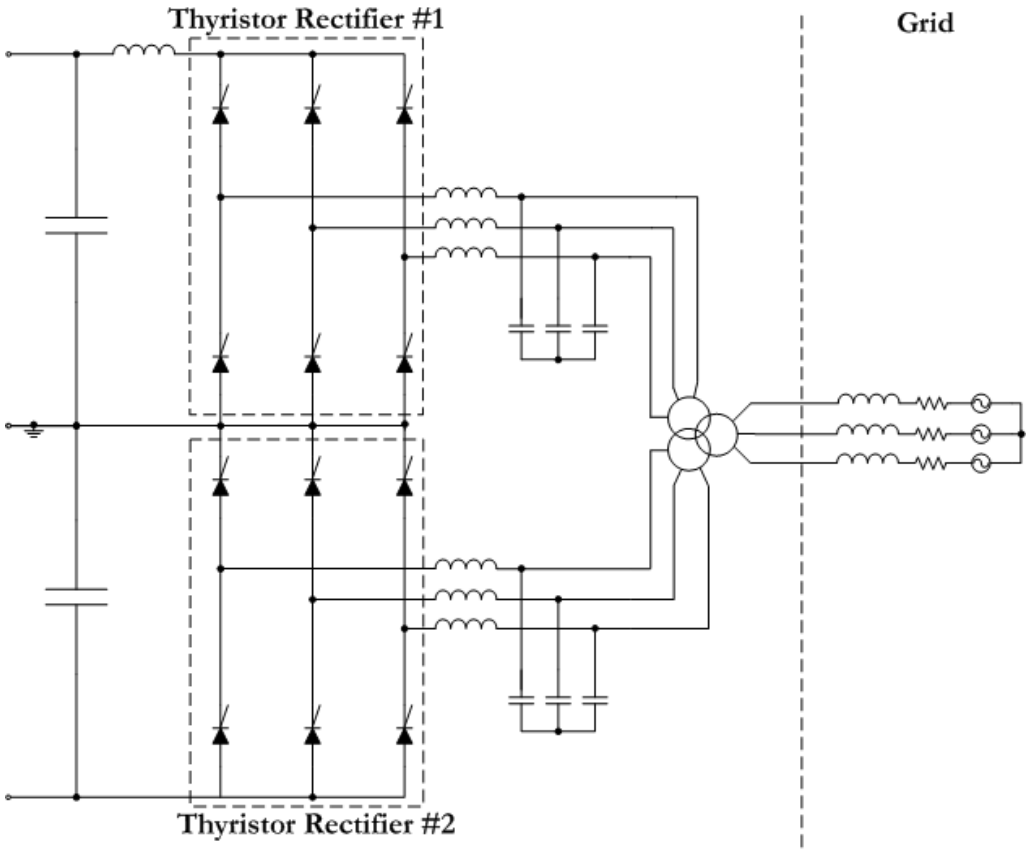


Figure 1.6: Schematic diagram of a 12-pulse thyristor rectifier.

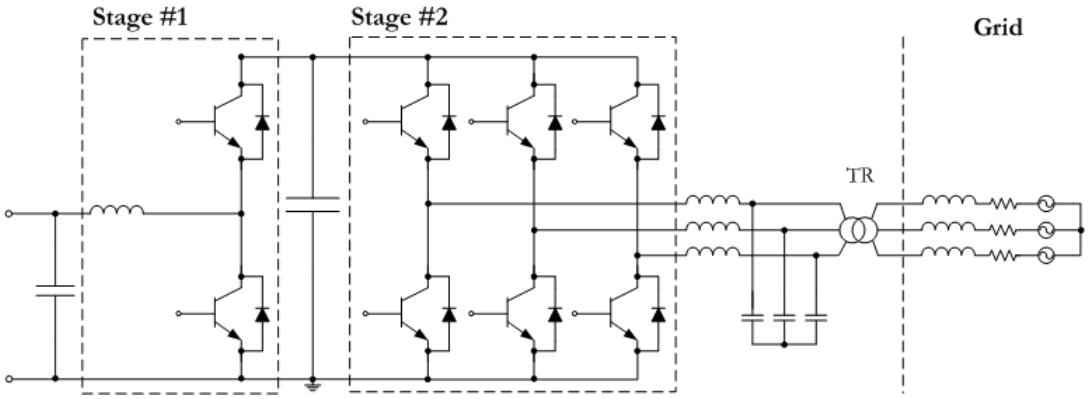

Figure 1.7: Schematic diagram of the proposed two-stage VSC in [33].

less than a single-stage VSC [49].

- **Two-stage NPC VSC:** Using the same strategy proposed for a two-stage VSC, a two stage NPC VSC can be designed, which is presented in Fig. 1.8. As it can be seen from Fig. 1.8 the two-stage NPC converter consist of cascading a step-down converter with the NPC converter shown in Fig. 1.5. Although, the aforementioned topology has the ability to tolerate dc-side faults, as well as offering the rest of the merits of the NPC, which were mentioned earlier, it consists of two stages, which in turn leads to decrease in the efficiency of the converter.

- **Series-type two-stage VSC:** As it can be seen from Fig. 1.9, series-type two-stage VSC analyzed here consists of the series connection of the sample two-stage VSC presented in Fig. 1.7. By employing the aforesaid settings, as well as benefiting from all the previously discussed advantages of the two-level VSCs, the bipolar dc side voltage can be achievable. However, a three-winding transformer is required in order to connect the

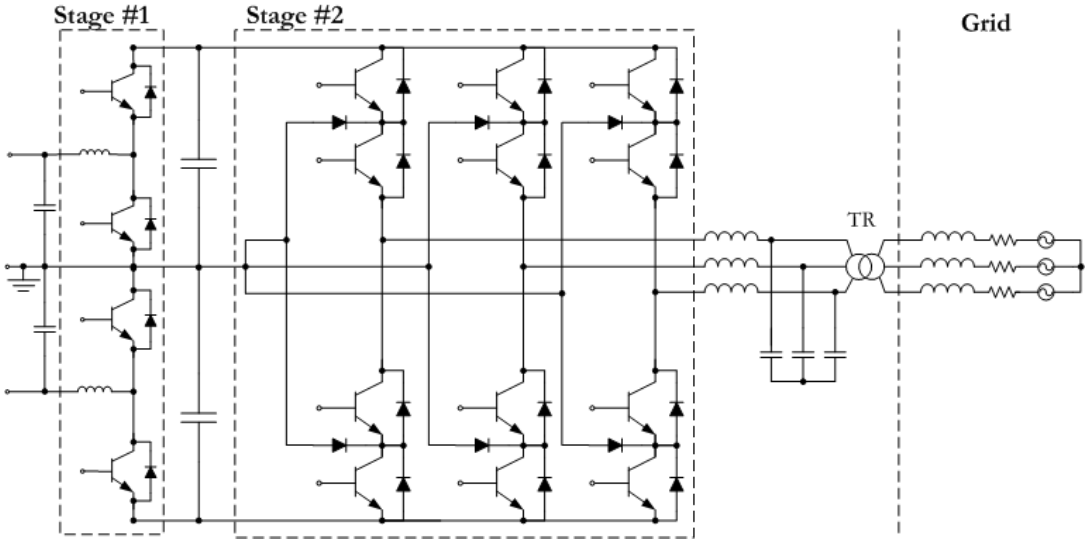

Figure 1.8: Schematic diagram of the proposed two-stage NPC VSC.

aforementioned converter to the ac-grid.

As it can be realized from the above explanations, majority of the most common ac/dc converters, used in LVDC systems, either are not able to tolerate the dc-side faults or have been upgraded to multiple-stage converters in order to achieve tolerance for such fault. Consequently, they have lower efficiencies. Furthermore, some of the topologies can not be used as a front-end converter in complex dc systems, as they do not offer bidirectional power flow between the ac and dc systems. As a result, this thesis proposes a unique single-stage bidirectional ac/dc converter, with the ability to tolerate faults at its dc side. The initial idea for this converter came from the design of the modular-multilevel converters (MMCs), which are wildly used in HVDC systems, [50] - [52].

## 1.4 Methodology

In order to achieve the objectives of this thesis, first a bidirectional ac/dc converter topology is proposed, whose structure makes it tolerant against dc-side short circuit faults. After mathematical modeling and achieving the effective controller design, the proposed converter was modeled in detail in the power systems computer aided design using electromagnetic transients

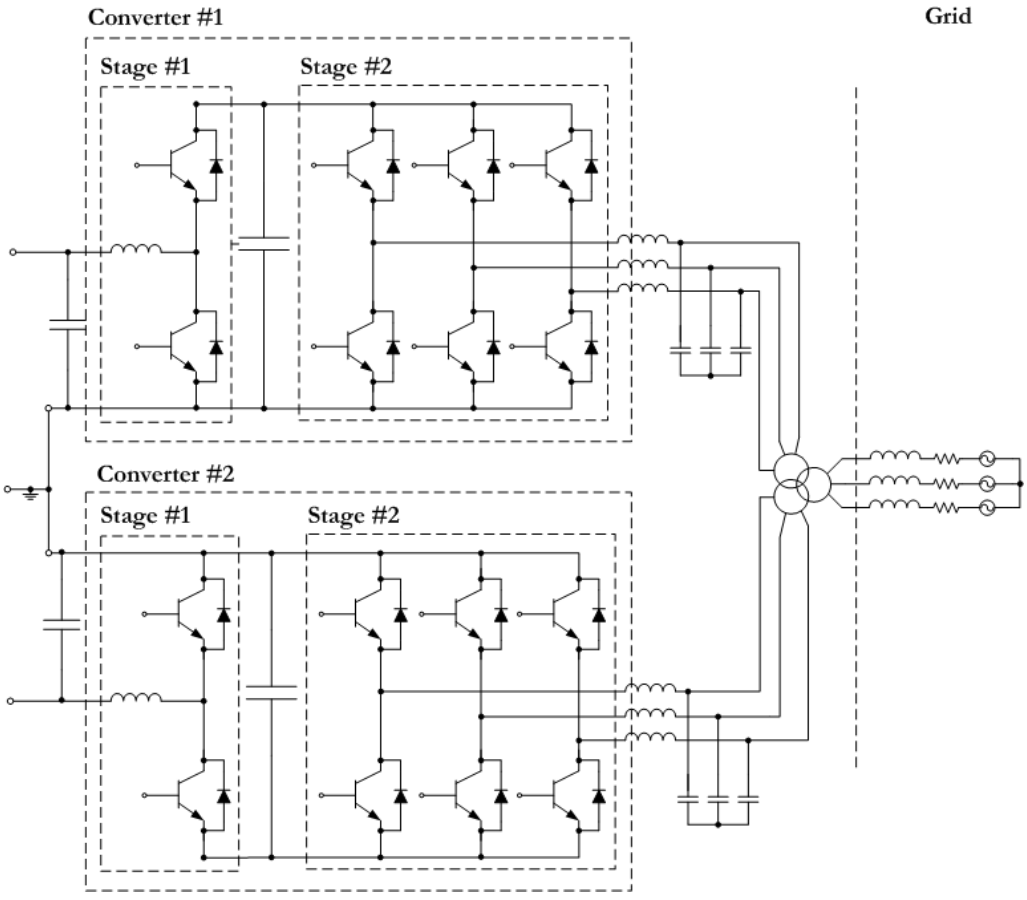


Figure 1.9: Schematic diagram of the series-type two-stage VSC.

including dc (PSCAD/EMTDC). The model is then used in order to evaluate the performance of the ac/dc converter and the effectiveness of the proposed control schemes through a number of case studies, using PSCAD/EMTDC software environment.

## 1.5 Thesis Contribution and Scope

As it was outlined in this chapter of the thesis, the protection of the low-voltage dc systems against short circuit currents is a challenge and although there are a number of methods currently proposed in the literature the lack of a mature, economical and effective protection method can still be seen. Among the proposed techniques, one can name the utilization of a converters with the ability to tolerate dc-side faults. Furthermore, by increasing the complexity of the LVDC systems, which is a result of the growing interest in DERs and microgrids, among others, having the possibility of bidirectional power flow between the ac and dc grid is a necessity. As a result, this thesis focuses on addressing the aforementioned challenge/requirements, and proposes a new topology and control method for a bidirectional ac/dc converter which can tolerate the dc-side faults.

The main contributions of this thesis are:

- This thesis proposes a new topology for a single-stage three-phase dc-side fault tolerant bidirectional ac/dc converter. The converter can provide clean outputs with low level of unwanted harmonics, and is also able to be current-controlled in a rotating reference frame, in the same way as a conventional VSC, as presented in [43] and, therefore, provides protection against ac faults.

- The effectiveness of the aforementioned converter topology and designed controllers are then evaluated by building a model of the ac/dc converter in the PSCAD/EMTDC software environment and testing it in various normal and faulted scenarios.

- The thesis then presents a comparison between the proposed model and the previously related works in the literature. Followed by discussing the future works that can be done to further improve the design and effectiveness of the converter.

## 1.6 Thesis Outline

The reminder of this thesis is organized as follows:

- In chapter 2, first, the power circuit of the proposed dc-side fault tolerant ac/dc converter is presented, and explained. Including the switching scheme used for the converter and the expected operation of the converter under both normal and dc-side fault operating conditions. Furthermore, the second chapter presents a detailed mathematical model of the aforementioned converter.

- Chapter 3 employs the mathematical model, presented in the second chapter, and designs an effective control scheme for the ac/dc converter. The proposed control strategy, is able to regulate the dc-side voltage of the converter and assures that the energy is uniformly

distributed among the sub-modules in all the legs, i.e., control and regulate the dc-side voltage of the sub-modules at their corresponding reference value, as well as protecting the converter from the dc-side faults.

- Chapter 4 is dedicated to presenting the results obtained from the simulation of the proposed converter, in PSCAD/EMTDC software environment for various normal and faulted scenarios. This chapter also presents a detailed explanation of the achieved results.
- Chapter 5 present the conclusion of the thesis, comparison of the proposed converter and previously done research in this area, along with the suggestions for the future research work.

# Chapter 2

# Topology of the Proposed Converter

## 2.1 Introduction

The focus of this chapter is to address, and analyze the power circuit topology of the proposed dc-side fault tolerant, bidirectional, ac/dc converter, hereinafter, referred to as *the converter*.

## 2.2 Power-Circuit Structure

This section focuses on presenting a detailed description of the power circuit of the proposed ac/dc converter, whose schematic diagram is shown in Fig. 2.1. As it is presented in the mentioned figure, the converter has three identical legs, corresponding to the three phases of the ac grid. Each leg, in turn, consists of an upper and a lower arm. Hereinafter, the parameters associated to the upper and lower arm are denoted by the subscripts of 1 and 2, respectively. Moreover, each arm hosts a series connection of a full-bridge converter, referred to as *Full-Bridge Sub-Module (FBSM)* throughout this thesis, and an arm reactor; the inductance and resistance of the arm reactor are denoted by $L$ and $R$, respectively. Each FBSM is connected in parallel with a capacitor, $C$, at its dc side. The voltage of the aforementioned capacitor is denoted by $v_{C1k}$ and $v_{C2k}$ in Fig. 2.1 for the upper and lower arm, respectively, and referred to as *submodule dc voltage* ($k = a$, $b$, and $c$). In order to ensure the energy balance in the proposed converter the dc-voltage of the FBSMs must be kept at their reference values. The voltage measured at the ac-side terminals of the each FBSM is denoted by $v_{t1k}$ and $v_{t2k}$, for upper and lower arm of the $k$th leg, respectively. As it can be illustrated from Fig. 2.1, during the steady-state operation of the proposed converter, and by ignoring the resistive losses associated with the converter, the arm voltage is almost equal to the terminal voltage of its FBSM.

As presented in Fig. 2.1 at the ac-side, converter is connected to the ac grid. The aforementioned grid can be assumed to be ideal or non-ideal. The latter can be modeled by a series connection of an ideal ac voltage source and grid impedance, $L_g$ and $R_g$. In order to mitigate the harmonics the converter is connected to the grid through a passive filter. The inductive filter can be a first-order L, second-order LC, or an LCL filter [53]. Using a simple inductive filter, will reduce the harmonics, but at the same time it requires either high switching frequency which in turn leads to higher switching losses, or requires a larger inductance [54]. The aforementioned filter is mainly used for single phase and/or low power converters [53]. LC filters will

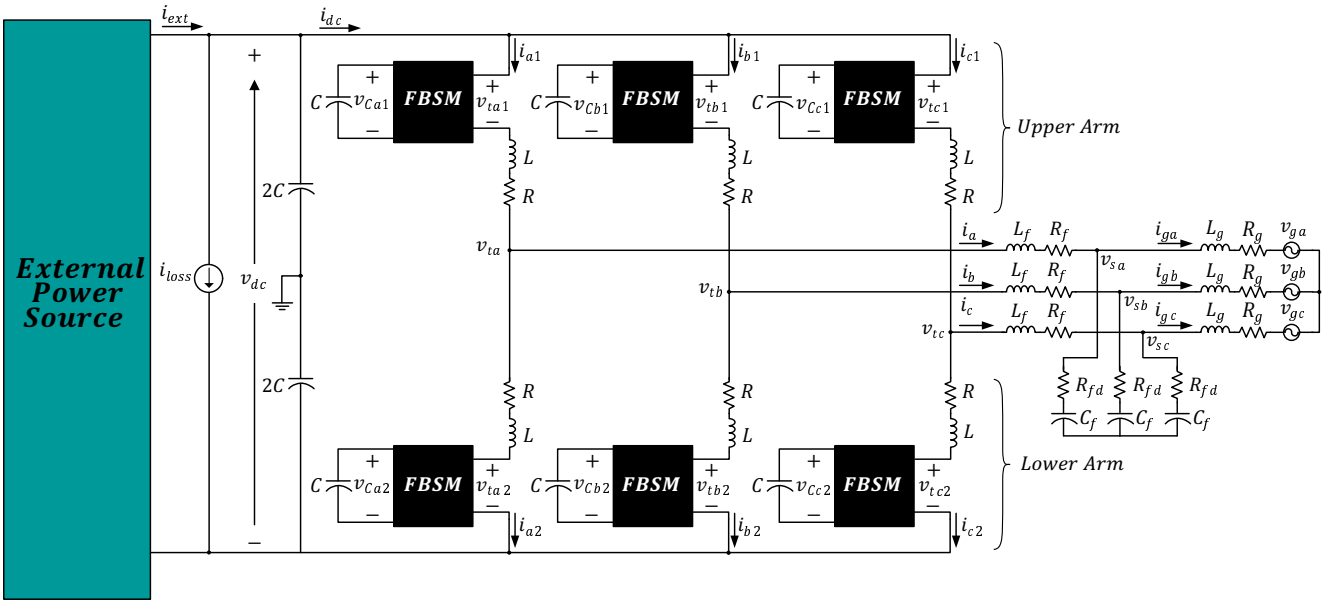


Figure 2.1: Schematic diagram of the proposed converter.

improve the performance and can generate nearly sinusoidal output. However, the LC filter is difficult to control and requires an effective damping method to deal with the resonance of the LC filter [55]. Thus, the LCL filter is attracting more attention due to its ability to mitigate the switching frequency harmonics while employing lower inductance. Hence, it is more suitable for higher power applications. Nevertheless, the LCL filters are even harder to control and they require many considerations in their design, such as the ripple current through the inductors, total impedance of the filter, resonance phenomenon, etc. [56]. Figure 2.1 illustrates the schematic diagram of the converter while connected to a non-ideal grid. As it can be seen, the per-phase inductance and capacitance of the LC filter at the point of common coupling (PCC) of the proposed converter and the ac grid is marked with $L_f$ and $C_f$. Furthermore, the resistive losses associated with the filter inductor is presented as $R_f$ in Fig. 2.1. As it was previously mentioned the LC filters require damping in order to circumvent the instabilities due to the filter resonance. The aforementioned is done through the series connection of the damping resistors, referred to as $R_{fd}$ hereinafter, with the capacitors of the LC filter in this thesis. The shunt capacitor provides a path with low impedance for the switching current harmonics that exist in the ac-side current of the converter. Thus, prevents the switching current harmonics from entering and decreasing the dependence of the grid impedance to the switching frequency harmonics. It must be mentioned that if the grid is assumed to be ideal, the shunt branch can be ignored, and a simple L filter would be used. Moreover, it must be considered that by employing the shunt branch the reactive power exchanged with the grid will change. As a result the real and reactive power transferred from the converter to the grid changes from $(P_s, Q_s)$ to $(P_s, Q_s + Q_c)$.

As Fig. 2.1 shows, the positive ac-side terminals of the three upper-arm FBSMs form the positive terminal of the converter's dc link, while the negative ac-side terminals of the lower-arm FBSMs constitute the negative dc link terminal. Moreover, the dc link of the converter

is connected in parallel with a dc-link capacitor whose capacitance is assumed, for simplicity, to be equal to the dc-link capacitors of the FBSMs. For the purpose of analysis, the dc-link capacitor in Fig. 2.1 is shown as the series connection of two identical capacitors, with a capacitance of 2C. Thus, the node common to the two capacitors, denoted by 0, is regarded as the potential reference for the converter, unless noted otherwise. Hence, in Fig. 2.1, the ac-side terminal voltage, the voltage at the point of common-coupling of the converter and the ac grid, and the ac-grid voltage are all referred to the virtual dc-side midpoint of the converter, are denoted by $v_{tk}$, $v_{sk}$, and $v_{gk}$, respectively ($k = a$, $b$, and $c$).

The upper and lower arm currents are defined separately and shown by $i_{1k}$ and $i_{2k}$, respectively. Figure 2.1 also illustrates the ac-side current of the converter and the ac grid current, denoted by $i_k$ and $i_{gk}$, respectively. Furthermore, the current transferred from the dc grid to the converter is referred to as the *external current* and shown by $i_{ext}$, while the current of the dc-side of the converter is called the *dc current* and denoted by $i_{dc}$. It must be mentioned that the value of the external current is not controllable through the converter.

## 2.3 Switching Scheme

The schematic diagram of the FBSMs used in the proposed converter is presented in Fig. 2.2. The FBSMs operate on the alternate switching of the switch pairs of [1, 4], and [3, 2], whose turning on and off commands are issued using *unipolar pulse-width modulation* (UPWM) strategy. This switching method is briefly explained in this section.

Using UPWM each FBSM requires two modulating signals, i.e., one for each switch pair in the FBSM. The aforementioned modulating signals of each FBSM have the same magnitude and are 180° out of phase with each other. The aforementioned signals will be compared to a common high-frequency periodic triangular signal, referred to as the carrier, and generate the gating signals for the upper two switches, as shown in Fig. 2.2. It goes without saying that in order to avoid short circuiting the dc-side of the FBSMs the gating signals for the lower switches of each leg of the FBSMs shown in Fig. 2.2 are complimentary to their corresponding upper switch.

The distinct characteristic of UPWM that makes it superior to other PWM techniques for the proposed converter is the fact that it will cause the minimum number of switching at any

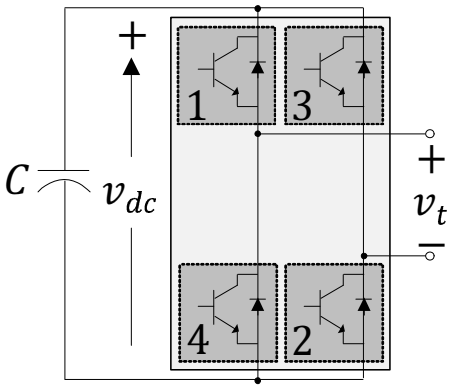


Figure 2.2: Schematic diagram of a FBSM.

time, which in turn reduces the switching losses [45]. Moreover, in terms of harmonics, when using the unipolar PWM technique, the lowest order of the undesirable harmonic is $2f_{sw} \pm 1$, which is much higher than the lowest order harmonic available when employing bi-polar PWM (BPWM), i.e. $f_{sw} \pm 1$. Figure 2.3 illustrates the gating signals generated by UPWM technique for the upper switches in both legs of the single-phase full bridge converter used as FBSM, Fig. 2.2, as well as the generated terminal voltage.

The fundamental frequency component of the output of each submodule, depends on the modulating signal of the corresponding FBSM as well as the carrier, while the undesirable harmonics only depend of the carrier. Furthermore, employing UPWM technique, the equivalent circuit of the converter, seen from the ac-side, is as presented in Fig. 2.4, where $e_k$, $R^{'}$, and $L^{'}$ are the Thevenin equivalent voltage, resistance and inductance of the converter, respectively, and their magnitudes are as follows

$$e_k = \frac{v_{t2k} - v_{t1k}}{2} \tag{2.1}$$

$$R^{'} = \frac{R + 2r_{on}}{2} + R_f \tag{2.2}$$

$$L^{'} = \frac{L}{2} + L_f \tag{2.3}$$

where k corresponds to legs a, b, and c. Considering (2.1) and by selecting a common carrier for both sub-modules in the upper and lower arm of each leg, the undesired harmonics of the upper and lower submodule in each leg, cancel each other out to a great deal. Thus, the output of the converter will be cleaner in comparison to the results obtained while employing two carriers with the same magnitude and 180 degrees phase displacement with one another.

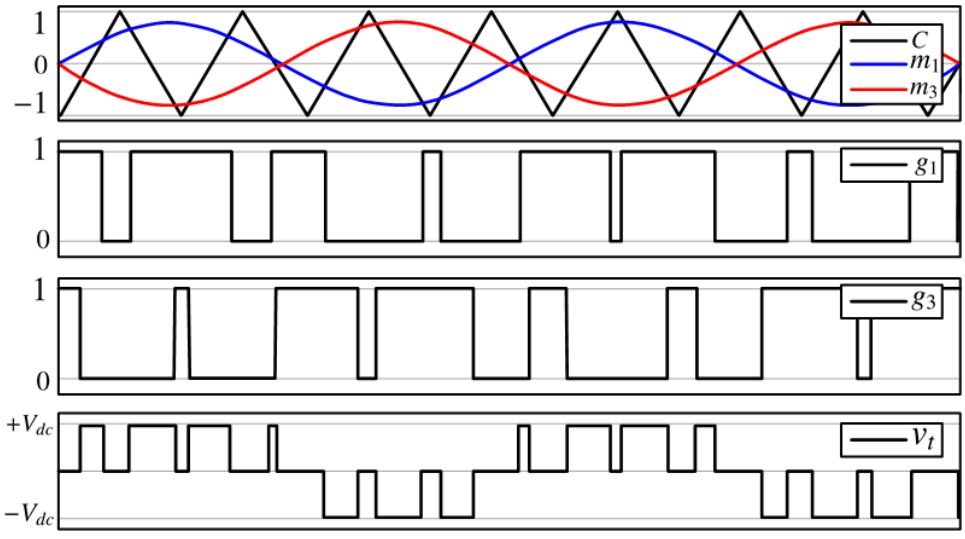


Figure 2.3: Waveforms of unipolar PWM.

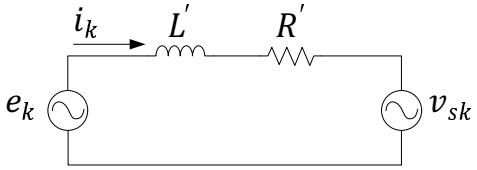

Figure 2.4: Simplified equivalent Thevenin circuit of the converter from as seen from the ac grid.

## 2.4 Principles of Operation

In this part of the thesis, the operation of the converter under the normal, and under the dc-side fault conditions is analyzed.

### 2.4.1 Operation Under the Normal Conditions

As it was previously mentioned, the ac-grid can be modeled by a balanced, sinusoidal three-phase voltage source, $V_{sabc}$. Under normal operating conditions, the proposed VSC, exchanges real- and reactive power components with the ac system, at the point of common coupling and is used as a dc-voltage power port, whose dc-side voltage is regulated through the control of the active power. As a result, the reactive-power can be regulated at its desired reference value separately.

During normal operations, each sub-module presented in Fig. 2.1, can be replaced by a dependent voltage source, whose voltage is equal to the terminal voltage of the corresponding FBSM, as shown in Fig. 2.5. The voltage of each of the illustrated dependent sources in Fig. 2.5, is $m_{jk}v_{Cjk}$, where $k = a, b$ and $c$, and $j$ is 1 or 2, for the upper and lower arm, respectively.

### 2.4.2 Operation Under DC-Side Short Circuit Faults

Upon occurrence of a dc-side fault, the switches will be turned off. Hence, the dc-side capacitors of the FBSMs will effectively be connected in series with the anti-parallel diodes. As a result, while experiencing dc-side fault the equivalent schematic diagram of the proposed converter will be as shown in Fig. 2.6. It must be mentioned that in Fig. 2.6, it was assumed that prior to the occurrence f the fault the converter was working in its steady-state conditions. As a result the FBSM capacitors are replaced by their pre-fault steady-state voltages, $v_C^0$. Hence, using Fig. 2.6 and assuming that prior to the dc-side fault the converter was working at its steady-state condition, i.e., FBSM capacitors were all fully charged, when a dc-side short circuit fault occurs the diodes will turn off and the arm current will drop to zero. Thus, as it is mentioned in the title of this thesis, the proposed converter has the ability to tolerate the dc-side fault, which in can eliminate the need for employing dc breakers.

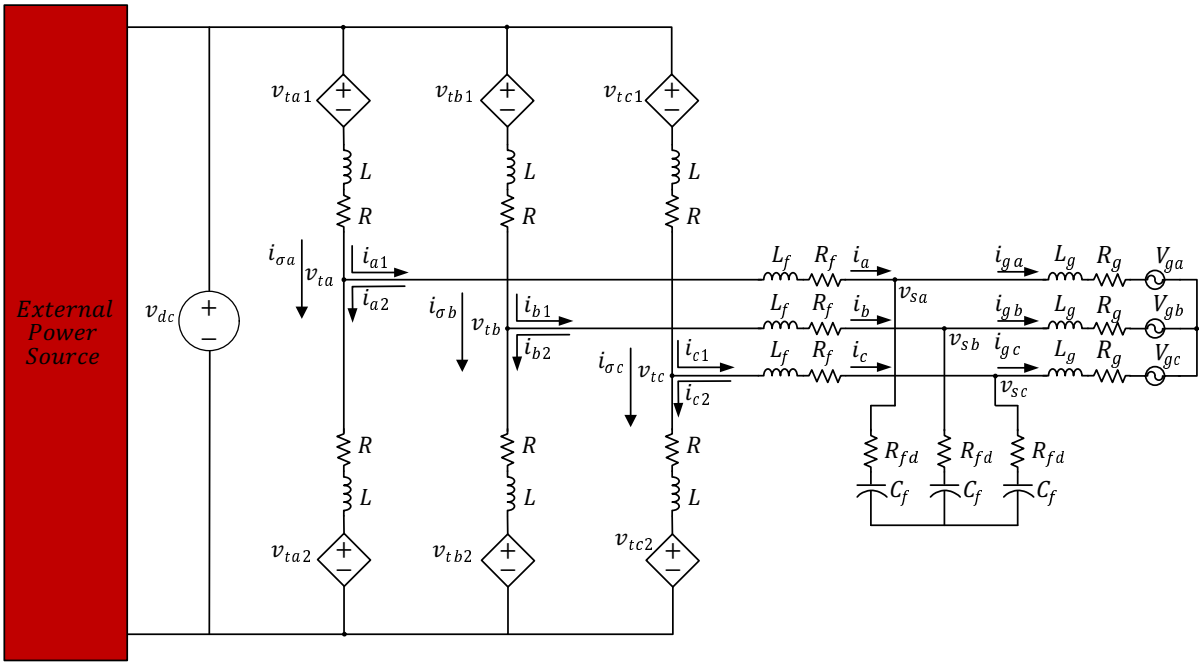


Figure 2.5: Schematic diagram of the proposed converter when the converter is operating under normal conditions.

## 2.5 Mathematical Modeling of the Proposed AC/DC Converter

In the previous sections, the power circuit, switching and operation schemes of the proposed converter were discussed. However, in order to achieve a stable and effective operation, under

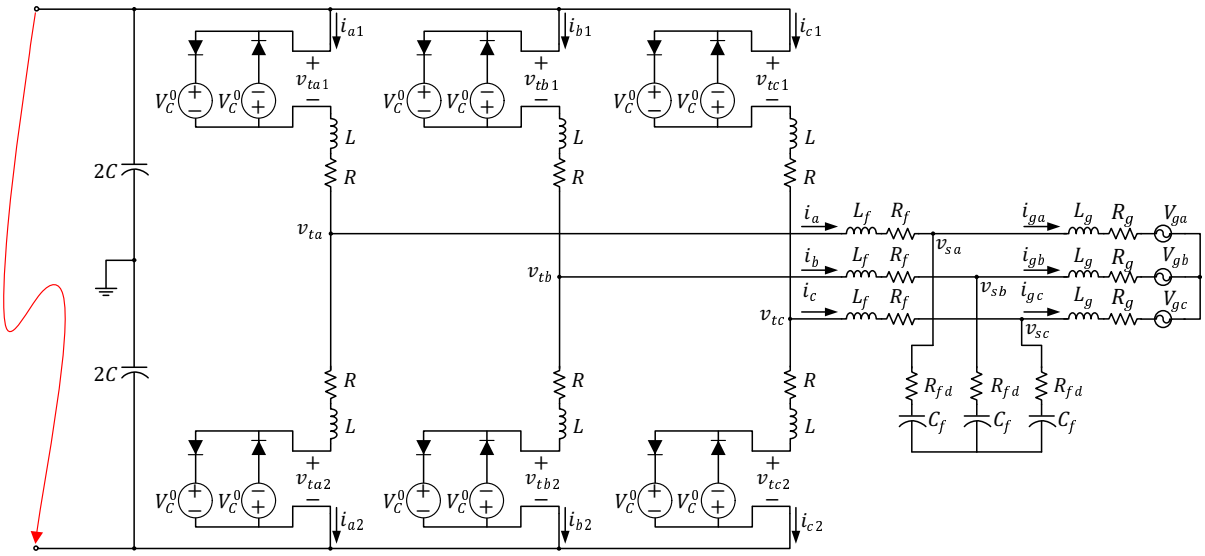


Figure 2.6: Schematic diagram of the proposed converter when the switches are turned off.

both transient and steady-state conditions, the converter must be accompanied by appropriate control methodology which would enable the bi-directional power flow between the ac and dc systems. In order to develop an effective control technique, first a detailed mathematical model of the proposed converter is required. Hence, this section is dedicated to finding the aforementioned mathematical model. The achieved model is then used in the third chapter of the thesis in order to propose an effective control method for the converter.

The modeling and control of the proposed converter, is divided in two separate categories, the common-mode and differential-mode values. Presented in (2.4) and (2.5), respectively.

$$\frac{A_{1k} + A_{2k}}{2} \tag{2.4}$$

$$\frac{A_{2k} - A_{1k}}{2} \tag{2.5}$$

where $A$ represents any quantity in the arm of the converter. It will be shown in this section that the differential-mode quantities are directly related to the ac-side parameters of the converter, while the common-mode values are related to the FBSMs in each leg.

As Fig. 2.1 shows and it was previously mentioned, each leg of the converter hosts two arms and each arm consists of FBSMs. Thus, the modeling begins with mathematical modeling of the FBSMs, as the building blocks of the proposed converter, and is then followed by a detailed explanation regarding the differential-mode parameters and results in a model which expresses the relation between the dc-side voltage of the converter and the reference active power transferred to the grid, which in turn is related to the d-axis value of the ac-side current of the converter. Furthermore, it is explained that in order to achieve a stable converter, the dc-side voltage of the submodules must be regulated, and the last part of this section is dedicated to finding an accurate model that explains the relation between the common-mode parameters and FBSMs' dc-side voltage.

Prior to beginning the modeling, it must be mentioned that in this section, the grid is assumed to be ideal and its connection with the proposed converter is done through the inductive filter. The discussions related to non-ideal grid and the RLC filter associated with it will be discussed in the fourth chapter of this thesis.

By employing the uni-polar pulse-width modulation (PWM) switching strategy for a full-bridge converter, as it was mentioned in 2.3, the ac-side terminal voltage of each FBSM can be approximated by

$$v_t = m v_C \tag{2.6}$$

Hence, in Fig. 2.1 each FBSM can be replaced by a dependent voltage source as illustrated in Fig. 2.7.

Using the Thevenin technique and (2.6), the Thevenin equivalent voltage of the $k$th leg of the converter, can be found as follows (k=a, b, and c)

$$e_k = \frac{m_{2k} v_{C2k} - m_{1k} v_{C1k}}{2} \tag{2.7}$$

where $e_k$, $m_{1k}$, $m_{2k}$, $v_{C1k}$, and $v_{C2k}$ present the Thevenin equivalent voltage, modulating signals and the dc-side voltage of the FBSMs in the upper and lower arm of the $k$th leg of the converter, respectively.

Moreover, as it was previously mentioned, using the appropriate controller, the dc-side voltage of the FBSM's can be regulated at their reference value, $v_{dc}$ with small perturbations. Hence, in steady-state conditions (2.7) can be approximated by (2.8)

$$e_k \simeq \frac{v_{t2k} - v_{t1k}}{2} = v_{dc}\frac{m_{2k} - m_{1k}}{2} \tag{2.8}$$

Using the definition of the differential-mode signals, the *differential-mode modulating signals* for the $k$th leg, $k = a, b$, and $c$, (2.8) can be rewritten as $\frac{m_{2k}-m_{1k}}{2}$

$$e_k = v_{dc}m_{\delta k} \tag{2.9}$$

Equation (2.9) indicates that in order to obtain a balanced three-phase voltage and consequently line current at the ac-side of the converter, the differential-mode modulating signals of each leg must be constituted of a balanced three-phase sinusoidal function of time with required amplitude, phase angle, and frequency. As a result, the differential-mode modulating signals are assumed to have the following form and are delivered by closed-loop ac-side current controller, which will be fully explained in chapter 3.

$$m_{\delta a} = \hat{m}(t)cos\left[\varepsilon(t)\right] \tag{2.10}$$

$$m_{\delta b} = \hat{m}(t)cos\left[\varepsilon(t) - \frac{2\pi}{3}\right] \tag{2.11}$$

$$m_{\delta c} = \hat{m}(t)cos\left[\varepsilon(t) + \frac{2\pi}{3}\right] \tag{2.12}$$

where $\varepsilon(t)$ contains the phase-angle and frequency information.

In Fig. 2.5 the ac-side current is shown by $i_k$. Using this figure, the ac-side current can be written in terms of the upper and lower arm currents of the $k$th leg, i.e.,

$$i_k = i_{1k} - i_{2k} \tag{2.13}$$

Considering the definition of the differential-mode components, i.e., $\frac{A_{2k}-A_{1k}}{2}$, the *differential-mode arm current*, denoted by $i_{\delta k}$ throughout this thesis, can be defined as presented in ([**?**]). The aforementioned currents are shown in Fig. 2.5.

$$i_{\delta k} = \frac{i_{2k} - i_{1k}}{2} \tag{2.14}$$

Using (2.14) and (2.13) the ac-side current of the $k$th phase can be re-written as follows:

$$i_k = -2i_{\delta k} \tag{2.15}$$

The active and reactive power exchanged with the grid, are denoted by $P_s$ and $Q_s$, respectively, and can be expressed as follows

$$P_s(t) = Re\left\{\frac{3}{2}\overrightarrow{V}(t)\overrightarrow{i}^{*}(t)\right\} \tag{2.16}$$

$$Q_s(t) = Im\left\{\frac{3}{2}\overrightarrow{V}(t)\overrightarrow{i}^{*}(t)\right\} \tag{2.17}$$

Through the use of a Phase-lock loop (PLL) the values of $\omega$ and $\rho$ will be fixed at $\omega_0$ and $\omega_0 t+\theta_0$. Hence, by using a PLL and abc- to dq- frame transformation the $v_{sq}$ can be regulated at zero. Thus, the active and reactive power at the ac-side of the converter will be directly linked to the d- and q-axis components of the ac-side current, respectively. Hence, the reference value of the d- and q-axis currents of the converter can be found as presented in (2.18) and (2.19), respectively. For more information regarding the abc- to dq-frame transformation or PLL mechanism please consult [43]

$$i_d^* = \frac{P_s^*}{1.5v_{sd}} \tag{2.18}$$

$$i_q^* = \frac{-Q_s^*}{1.5v_{sd}} \tag{2.19}$$

Considering the aforementioned fact and by using Fig. 2.4 the dynamics of the ac side of the proposed VSC system in dq frame is presented in 2.20 and 2.21.

$$L^{'}\frac{di_d}{dt} = L^{'}\omega_0 i_q - R^{'}i_d + m_{\delta d}v_{dc} - \hat{V}_s \tag{2.20}$$

$$L^{'}\frac{di_q}{dt} = -L^{'}\omega_0 i_d - R^{'}i_q + m_{\delta q}v_{dc} \tag{2.21}$$

In (2.20) and (2.21), $i_d$ and $i_q$ are the state variables, $m_{\delta d}$ and $m_{\delta q}$ are the control inputs and $\hat{V}_s$ is the disturbance input. Moreover, due to the presence of $L^{'}\omega_0$ terms in (2.20) and (2.21), dynamics of $i_d$ and $i_q$ are coupled. In order to decouple the aforementioned dynamics, $m_{\delta d}$ and $m_{\delta q}$ are defined as presented in (2.22) and (2.23).

$$m_{\delta d} = \frac{u_d - L^{'}\omega_0 i_q - \hat{V}_s}{v_{dc}} \tag{2.22}$$

$$m_{\delta q} = \frac{u_q + L^{'}\omega_0 i_d}{v_{dc}} \tag{2.23}$$

Equations (2.22) and (2.23) are the basis of the ac-side current controller designed for the proposed converter, which will be presented in chapter 3.

Throughout this thesis the average value of the arm currents in each leg is denoted by $i_{\sigma k}$, (k=a, b, and c), and referred to as the *common-mode current*. As can be seen in Fig.

2.5, the terminal voltages of FBSMs in the upper and lower arm of each leg appears with the same polarity. Thus, it can be concluded that the common-mode current circulates through the corresponding leg of the converter without directly affecting the *ac-side terminal* voltage.

It must be taken into consideration that the common-mode and differential-mode currents are decoupled from one another, and thus they can be independently controlled.

Using Fig. 2.5, and considering the fact that the common-mode currents have the same polarity in both arms, the upper and lower arm currents of the $k$th leg, $i_{1k}$ and $i_{2k}$, respectively, can be found as:

$$i_{1k} = \frac{i_k}{2} + i_{\sigma k} \tag{2.24}$$

$$i_{2k} = -\frac{i_k}{2} + i_{\sigma k} \tag{2.25}$$

Applying KVL to the equivalent circuit presented in Fig. 2.5 yields

$$\frac{v_{dc}}{2} = \frac{v_{t1k} + v_{t2k}}{2} + (R + 2r_{on})\, i_{\sigma k} + L\frac{di_{\sigma k}}{dt} \tag{2.26}$$

Term $\frac{v_{t1k}+v_{t2k}}{2}$ in (2.26) represents the *common-mode terminal voltage* for the $k$th leg. In order to control the common-mode current, the common-mode modulating signal of each leg are used as the control inputs in designing the control scheme, more explanation on the aforementioned controller is presented in chapter 3.

Common-mode modulating signal of the $k$th leg is defined as

$$m_{\sigma k} = \frac{m_{1k} + m_{2k}}{2} \tag{2.27}$$

Hence, the modulating signal for the FBSM in the upper and lower arm of the $k$th leg, $m_{1k}$ and $m_{2k}$, respectively, are as follows

$$m_{1k} = m_{\sigma k} - m_{\delta k} \tag{2.28}$$

$$m_{2k} = m_{\sigma k} + m_{\delta k} \tag{2.29}$$

As it can be seen from Fig. 2.7, the converter is in parallel with an external power source. The power exchanged between the aforementioned external power source and the converter is called the *external power* and denoted by $P_{ext}$. The external power is an exogenous signal and cannot be controlled by the proposed converter. Furthermore, the external power is also subjected to losses, hereinafter referred to as $P_{loss}$. The remaining portion of the external power going through the converter is known as the *dc power* and is denoted by $P_{DC}$ in this thesis. To ensure the power balance, dc power must be controlled using the converter.

The overall power balance equation of the proposed converter is formulated as

$$P_{ext} - P_{loss} - \frac{d}{dt}\left(0.5Cv_{dc}^2\right) = P_{dc} \tag{2.30}$$

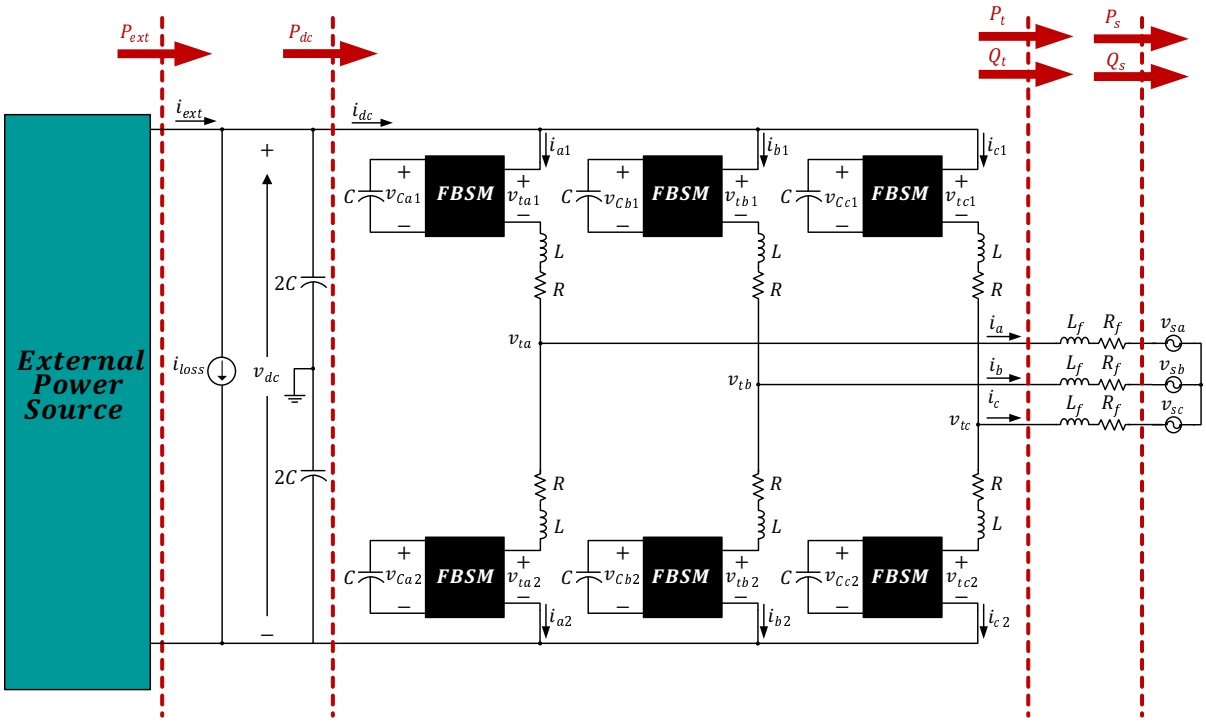


Figure 2.7: Schematic diagram of the proposed ac/dc converter illustrating the powers exchanged.

Ignoring the losses in the converter the dc power is found as

$$P_{dc} = P_t + \Sigma P_{sm} \tag{2.31}$$

However, $\Sigma P_{sm}$ represents the accumulated power of the FBSMs. Since, FBSMs are not connected to a power source to a power source at their dc-side, by ignoring their losses the value of $\Sigma P_{sm}$ in comparison to the terminal power of the converter will be negligible. Thus, it can be assumed that the dc power going to the converter is equal to the terminal power of the converter. Furthermore, the overall power dissipated by the can be ignored. and by substituting $P_{dc} = P_t$ in (2.30), it can be deduced that

$$\frac{d}{dt}(0.5Cv_{dc}) = P_{ext} - P_t \tag{2.32}$$

Using Fig. 2.4, it can be concluded that the terminal power of the converter can be written in terms of the power dissipated in the Thevenin equivalent inductance and resistance, and the power exchanged between the converter and the grid at the POI. However, the power dissipated by the Thevenin equivalent resistance is negligible and can be ignored. At the same time, in order to reduce the switching losses, the switching frequency of the converter must be limited. As a result, the inductance value at the ac-side of the converter must be sufficient enough to suppress the switching harmonics. Consequently, the instantaneous power absorbed by the

three-phase inductance can become significant during the transient conditions and cannot be ignored. Thus, the terminal power of the converter, can be written as presented in (2.33), for more information please refer to [43].

$$P_t \simeq P_s + \left(\frac{2L^{'}}{3\hat{V_s}^2}\right) P_s \frac{dP_s}{dt} + \left(\frac{2L^{'}}{3\hat{V_s}^2}\right) Q_s \frac{dQ_s}{dt} \tag{2.33}$$

By substituting the terminal power from (2.33) in (2.32) the following will be achieved.

$$\frac{dv_{dc}^2}{dt} = \left(\frac{2}{C}\right) P_{ext} - \left(\frac{2}{C}\right) P_{loss} - \left(\frac{2}{C}\right)\left[P_s + \left(\frac{2L^{'}}{3\hat{V_s}^2}\right) P_s \frac{dP_s}{dt}\right] - \left(\frac{2}{C}\right)\left(\frac{2L^{'}}{3\hat{V_s}^2}\right) Q_s \frac{dQ_s}{dt} \tag{2.34}$$

Based on (4.1), $v_{dc}^2$ is the output, $P_s$ is the control input, and $P_{ext}$, $P_{loss}$, and $Q_s$ are the disturbance inputs. Equation (4.1) is further used in chapter 3 in order to design the effective controller to regulate the dc-side voltage of the converter.

Using the model presented in this part the dc-side voltage of the converter can be linked to the active power exchanged between the converter to the grid. Thus, the dc-side voltage is in turn linked to the d-axis component of the ac-side current. Using the aforementioned link, the dc-side voltage can be regulated to its reference value by regulating the d-axis component of the current, which is completely explained in the third chapter of this thesis.

### 2.5.1 Energy Balance Analysis

In order to achieve a balanced three-phase ac/dc converter system, it must be ensured that the energy is uniformly distributed among each leg, and between the upper and lower arms of each leg [57]. Hence the energy balance analysis presented in this thesis first focuses on achieving uniform energy distribution among the three legs of the converter and then moves on to proposing an algorithm for ensuring the balance of energy between the FBSMs of the upper and lower arms of each leg. The aforementioned is done through independently regulating the dc-side voltage of the FBSMs at the value of the dc-side voltage of the converter as presented in (2.35), where k=a, b, and c.

$$v_{C1k} = v_{C2k} = v_{dc} \tag{2.35}$$

To regulate a submodule dc-side voltage, one must regulate the dc (average) power exchanged with the FBSMs' capacitor at zero. Furthermore, by ignoring the submodule conduction and switching power losses the dc power of the FBSMs is almost equal to its ac-side power. Therefore, by controlling the active power of the FBSMs, their dc-side voltages can be regulated. The exchange of power between the dc grid and the converter is done through the arm currents, which consists of differential- and common-mode components. Based on (2.15), the differential-mode current components are the scaled versions of the converter's ac-side currents and are sinusoidal, by assuming a ripple-free dc-link voltage, a differential current

component cannot give rise to any non-zero average power flow to or from the dc distribution system. Hence, power exchange between the converter and the dc distribution system is only possible through the common-mode current components, indicating that each common-mode current component must at least have a dc component. The aforesaid dc-component will ensure that the energy is uniformly distributed among the three legs.

Next step is to achieve the energy balance between the upper and lower arm of each leg. Considering, the ac-terminal voltage of the FBSMs in the upper and lower arms of the $k$th leg are as presented in (2.36) and (2.37), respectively, it can be seen that the terminal voltage of each FBSM consist of a sinusoidal and a dc component, corresponding to the sinusoidal differential current component and the dc common-mode component, respectively. consequently, the average ac-side power of each FBSM is uncontrollable and non-zero, since the differential and common-mode current components are fixed by the powers exchanged with the host ac grid and the dc distribution system, respectively.

$$v_{1k} = \frac{v_k}{2} + v_{\sigma k} \tag{2.36}$$

$$v_{2k} = -\frac{v_k}{2} + v_{\sigma k} \tag{2.37}$$

Thus, in order to achieve arm energy balance a fundamental-frequency sinusoidal component is added to the common-mode current. The fundamental frequency component of the common-mode current leads to a power flow between the FBSMs in the upper and lower arm in each leg and ensures that the energy balance between the corresponding FBSMs is achieved.

Considering the above explanations, the common-mode current of the $k$th leg can be found as follows:

$$i_{\sigma k} = I^0_{\sigma k} + i^1_{\sigma k} \tag{2.38}$$

where $I^0_{\sigma k}$ and $i^1_{\sigma k}$ represent the dc and ac component of the common-mode current of the $k$th leg, respectively.

In the following parts of this section, the mathematical modeling of the converter used in the control design process for the common-mode components are presented. The achieved mathematical models are further used in Chapter 3 to design the corresponding controllers.

### Leg Energy Transfer Analysis of the Converter

Ignoring the voltage drop across the inductance and resistances, the average power flowing into the upper and lower FBSMs can be found as the difference of the power exchanged with the host ac grid and the power delivered by the positive and negative dc link rail, respectively, as presented in (2.40) and (2.40).

$$P_{1k} \approx \frac{1}{2} v_{dc} I^0_{\sigma k} - \overline{v_{sk} \underbrace{\left( \frac{i_k}{2} + i^1_{\sigma k} \right)}_{i_{1k}}} \tag{2.39}$$

$$P_{2k} \approx \left( -\frac{1}{2} v_{dc} \right) \left( -I^0_{\sigma k} \right) - \overline{v_{sk} \underbrace{\left( \frac{i_k}{2} - i^1_{\sigma k} \right)}_{i_{2k}}} \tag{2.40}$$

Ignoring the power losses of the FBSMs, $P_{1k}$ and $P_{2k}$ are equal to the rates of change of the energies stored in their corresponding FBSMs' capacitors. Using this knowledge, (2.40) and (2.40) the common-mode average power of the FBMSs in the $k$th leg can be found as

$$\frac{C}{2} \frac{d}{dt} y_{\sigma k} \approx \frac{v_{dc} I^0_{\sigma k} - \overline{v_{sk} i_k}}{2} \tag{2.41}$$

where

$$y_{\sigma k} = \frac{1}{2} \left( v^2_{C2k} + v^2_{C1k} \right) \tag{2.42}$$

The term $v_{sk} i_k$ at the right hand-side of the equation represent the active power that is delivered to the corresponding phase of the ac grid, which, under balanced condition, constitutes one third of the three-phase active power that the converter delivers to the host ac grid.

As it can be seen from (2.42), the common-mode squared dc-side voltages of each leg of the converter, $y_{\sigma k}$, is controlled by using the dc component of the common-mode current. Thus, based on (2.42), $y_{\sigma k}$ is the output, $I^0_{\sigma k}$ is the control input, and $\frac{\overline{v_{sk} i_k}}{2}$ is the disturbance input. The aforesaid is further used in Chapter 3 in order to design the controller for the common-mode squared dc-side voltages of each leg of the converter.

### Arm Energy Transfer Analysis of the Converter

The energy-balance in each leg of the proposed converter was achieved in the previously described. However, each leg consists of two identical arms. Hence, next step in ensuring the energy balance of the whole converter is to achieve the uniform energy distribution among the arms. The aforementioned can be done by independently controlling the dc-side voltages of the FBSMs. Using the model presented in the previous subsection the $\frac{v^2_{C1k} + v^2_{C2k}}{2}$ can be controlled. Thus, by finding a way to model and control the $\frac{v^2_{C1k} - v^2_{C2k}}{2}$, the dc-side voltage of each FBSM can be controlled. The aforesaid is achieved through the energy transfer between the arms of each leg, which in turn is a result of addition of a fundamental frequency component to the common-mode current and enabling the power transfer between the upper and lower FBSMs in each leg.

The average power following into the upper and lower FBSMs of the $k$th leg were previously presented in (2.40) and (2.40). Subtracting (2.40) from (2.40), will result in the

*differential-mode average power* of the FBSMs. Ignoring the losses of the FBSMs the differential-mode average power of the FBSMs can be written as

$$\left(\frac{C}{2}\right)\frac{d}{dt}\frac{\left(v_{C2k}^2 - v_{C1k}^2\right)}{2} \approx \overline{v_{sk} i_{\sigma k}^1} \tag{2.43}$$

Defining $y_{\delta k} = \frac{\left(v_{C2k}^2 - v_{C1k}^2\right)}{2}$ (2.43) can be re-written as

$$\left(\frac{C}{2}\right)\frac{d}{dt} y_{\delta k} \approx \overline{v_{sk} i_{\sigma k}^1} \tag{2.44}$$

where $i_{\sigma k}^1$ is the fundamental frequency component of the common-mode current of the $k$th leg of the converter. Hence, $i_{\sigma k}^1$ can be replaced by $\hat{i}^1 cos\,(\omega t + \beta_k)$, where $\hat{i}^1$ and $\beta_k$ present the maximum and initial phase values of the fundamental-frequency component of the common-mode current, respectively. As a result the term in the right hand side of (2.44) can be re-written as

$$P_{\delta k} \approx \sqrt{\frac{2}{3}}\, V_s \widehat{i_{\sigma k}^1} \cos\gamma_k \tag{2.45}$$

where $V_s$ is the rms line-to-line ac-side voltage at the POI, $\gamma_k$ is the phase displacement between $i_{\sigma k}^1$ and $v_{sk}$, and $P_{\delta k}$ denotes the differential-mode active power of the FBSMs in the $k$th leg. Considering, (2.44), (2.45) can be written as

$$P_{\delta k} = \left(\frac{C}{2}\right)\frac{d}{dt} y_{\delta k} = \sqrt{\frac{2}{3}}\, V_s \widehat{i_{\sigma k}^1} \cos\gamma_k \tag{2.46}$$

Furthermore, considering (2.44) the minimum peak value of the fundamental frequency component of the circulating current for a required power transfer can be achieved when the aforementioned fundamental frequency component of the common-mode current and the ac-side voltage of the corresponding leg of the converter are in phase with each other, i.e., when the power factor, $\cos\gamma_k$, equals to unity.

In practice, voltage drops across the reactors require $i_{\sigma k}^1$ to be in-phase with $v_{\delta k}$, instead of $v_{sk}$. Therefore, in an ideal condition $\gamma_k$ must be equal to the phase angle of $v_{\delta k}$. The difference, however, is hardly remarkable, since, in a well-designed converter, there is a negligible phase difference between $v_{\delta k}$ and $v_{sk}$.

Equation (2.46) is further used in the next chapter of this thesis in order to design the differential-mode dc-side squared voltage controller. Based on (2.46), $y_{\delta k}$ is the output, and $\widehat{i_{\sigma k}^1}$ is the control input.

It must be mentioned that the resulting common-mode current from the $y_{\delta k}$, $i_{\sigma k}^1$, is considerably smaller than the common-mode current achieved from the leg energy balance control, $I_\sigma^0$. Moreover, the latter is mainly dc, while the former is an ac quantity. Thus, employing the $y_{\delta k}$ controller will have a negligible effect on the leg energy balance control.

In summary, in order to achieve effective energy balance among all the FBSMs the common-mode current of the converter must be regulated at the sum of the dc and ac component of the corresponding leg, i.e.,

$$i_{\sigma k} = I^0_{\sigma k} + i^1_{\sigma k} \tag{2.47}$$

### 2.5.2 Voltage Conversion Ratio

So far a detailed description of the power circuit and the proposed converter along with its mathematical modeling has been discussed. Another deciding factor in the effectiveness of an ac/dc converter is its conversion ratio. Hence, in this part, the conversion ratio of the proposed converter is calculated.

In Fig. 2.1, $v_{sa}$, $v_{sb}$, and $v_{sc}$ are ac voltages of phase a, b, and c, respectively. The aforementioned voltages can be found as

$$v_{sk} = \hat{v}_s cos\left(\omega_0 t + \theta_0 + \Phi_k\right) \tag{2.48}$$

Moreover, as it was previously discussed, the terminal voltage of the upper-leg FBSM in the $k$th can be found as

$$v_{t1k} = v_{t\sigma k} - v_{t\delta k} \simeq \frac{v_{dc}}{2} - v_{t\delta k} \tag{2.49}$$

In the steady-state operation of the converter, and by ignoring the resistive loses, the differential-mode terminal voltage, i.e., the Thevenin equivalent voltage given in Fig. 2.4, is almost equal to the grid voltage, $v_{t\delta k} \simeq v_{sk}$. Furthermore, the terminal voltage of each FBSM can be found as $v_{tjk} = m_{jk} v_{cjk}$, where k=a,b, and c, and j is 1 or 2, corresponding to the upper, or lower arm of the $k$th leg, respectively. Using the controllers which are discussed in chapter 3, the dc-side capacitor voltage of each FBSM can be regulated to the value of the dc-side voltage of the converter. Hence, (2.49) can be written as (2.50) for the $k$th phase

$$m_{k1} v_{dc} \simeq \frac{v_{dc}}{2} - v_{sk} = \frac{v_{dc}}{2} - \sqrt{\frac{2}{3}} V_s cos\left(\omega t + \Theta_0 + \Theta_k\right) \tag{2.50}$$

By rearranging (2.50), the modulating signal for the upper sub-module in the leg a will be found as presented in (2.51).

$$m_{k1} = \frac{1}{2} - \sqrt{\frac{2}{3}} \frac{V_s}{v_{dc}} cos\left(\omega t + \Theta_0 + \Theta_k\right) \tag{2.51}$$

Moreover, considering that the modulating signal of each FBSM is between $-1$ and 1, it can be concluded that

$$-1 \leqslant \frac{1}{2} - \sqrt{\frac{2}{3}}\frac{V_s}{v_{dc}} cos\,(\omega t) \leqslant 1 \tag{2.52}$$

Hence, by solving (2.52), the ratio of the converter is found as follows, where $V$ is the line-to-line rms voltage of the grid,

$$\frac{V_s}{v_{dc}} = 0.612 \tag{2.53}$$

# Chapter 3

# Control of the Proposed Converter

## 3.1 Introduction

This chapter focuses on addressing and analyzing the control techniques employed for the proposed ac/dc converter.

As it was mentioned in Chapter 2, the differential- and common-mode quantities of the converter are independent from one another. Therefore, the control of the proposed converter is achieved by two independent sets of controllers, one for differential-mode and another one for common-mode variables. The aim of the former set of controllers is to regulate the dc-side voltage of the converter, and thus provide a balance between the power exchanged with the converter at its ac and dc sides. While, the latter set, is employed for the regulation of the dc-side voltage of the individual capacitors, which in turn ensures that the energy is uniformly distributed inside the converter.

## 3.2 Real- and Reactive-Power Controller

As it can be seen from Fig. 3.1, the proposed converter is connected to an external power source and the grid, at its dc and ac side, respectively. In this section the closed-loop control structure used for regulation of the dc-side voltage of the proposed converter is presented. The purpose of the aforementioned controller is to regulate the power that is exchanged with the converter and the ac grid, i.e., $P_s(t)$. Moreover, it will also be shown that the reactive power transferred to the grid can be controlled independently.

### 3.2.1 Dynamic Model of Real-/Reactive-Power Controller

In order to regulate the dc-side voltage of the converter and the active and reactive power exchanged with the ac grid, different approaches may be used, like *current-mode control* and the *voltage-mode control* methods, both of which are further discussed in [43]. In this thesis, the former method, *current-mode control*, is used. Figure 3.2 illustrates the current-mode control scheme for the proposed converter. Using the current-mode control technique, the ac-side terminal voltages are used to control the line current at the ac side and as a result the real and reactive power transferred from the external power source to the grid, or vice

versa are regulated through the magnitude and phase angle of the line current of the proposed voltage source converter. The current-control mode offers several advantages in comparison to voltage-controlled VSC, for example using the former, the output current is directly controlled, which in turn leads to inherent protection against ac-side faults, whereas the latter requires external hardware. Moreover, while the current-controlled VSCs independently control the active and reactive power, there is a cross-coupling between the active and reactive power in the voltage-controlled VSCs [58]. The current-controlled VSC has more merits such as its robustness against variations in parameters of the converter and ac grid, better dynamic performance, and high control precision [43]. The current control scheme is done in *dq*-frame. Hence, $P_s(t)$ and $Q_s(t)$ are independently controlled by the d-axis and q-axis components of the ac-side current. To do so, the feedback and feed-forward signals measured at the ac side are transformed to d- and q-axis components, which are then used by the designed compensators in order to generate the control signals in *dq*-frame. Then the aforementioned control signals are transformed back to the *abc*-frame and produce the differential-mode modulation signals for each leg of the converter. By using dc-frame transformation, under the steady-state conditions instead of dealing with the ac signals the controllers will deal with dc values, which in turn leads to much simpler controllers and lower dynamic orders.

As it was previously discussed in chapter 2, using the equivalent Thevenin model of the proposed VSC the dynamics of the ac side of the converter can be found as follows.

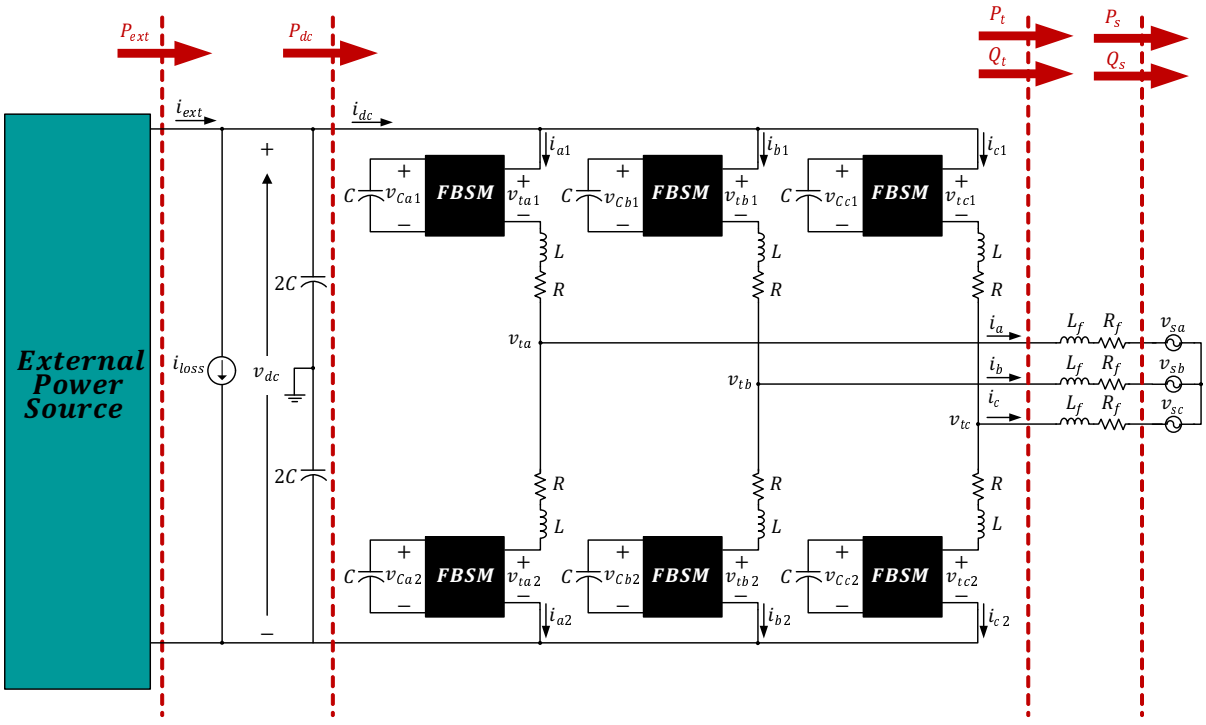


Figure 3.1: Schematic diagram of the proposed ac/dc converter illustrating the powers exchanged.

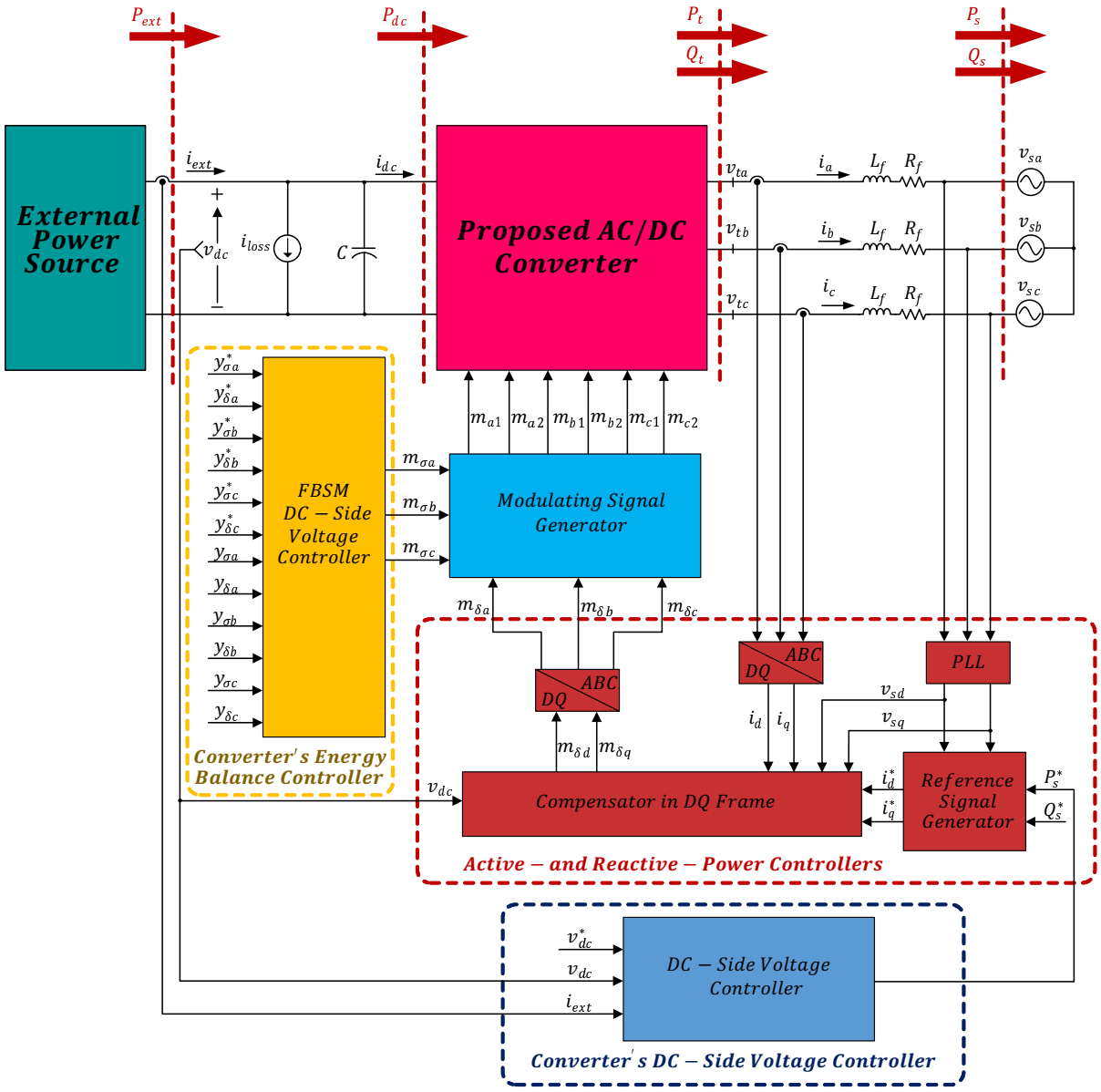


Figure 3.2: Schematic diagram of the proposed converter using current-controlled real-/reactive power controller.

$$L^{'}\frac{di_d}{dt} = L^{'}\omega_0 i_q - R^{'}i_d + m_{\delta d}V_{dc} - \hat{V}_s \tag{3.1}$$

$$L^{'}\frac{di_q}{dt} = -L^{'}\omega_0 i_d - R^{'}i_q + m_{\delta d}V_{dc} \tag{3.2}$$

Equations (3.1) and (3.2) describe two decoupled, linear, first order systems. According to (3.1) and (3.2), using $m_{\delta d}$ and $m_{\delta q}$, $i_d$ and $i_q$ can be regulated at their desired reference

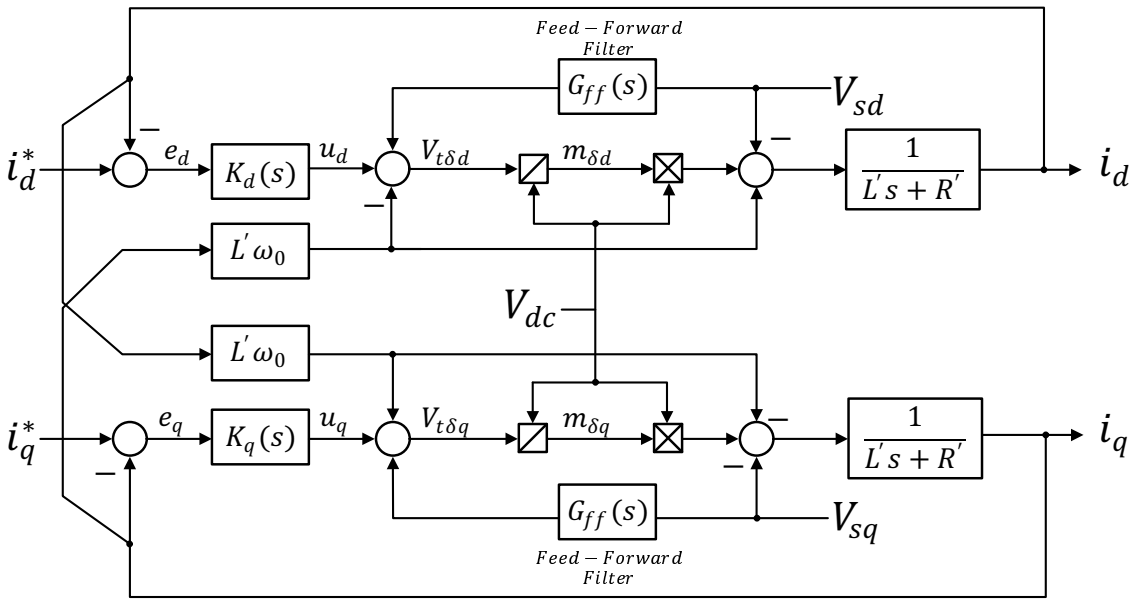


Figure 3.3: Control block diagram of the d- and q-axis ac-side current controller for the proposed converter.

values, respectively. Figure 3.3 illustrates the block diagram of the d- and q-axis ac-side current controllers of the proposed converter. Using the control scheme, the d- and q-axis components of the differential mode modulating signal are found, which are then multiplied using the VSC by the factor of $v_{dc}$ and results in the d- and q-axis components of the terminal voltage of the converter, that in turn generate the d- and q-axis component of the ac-side current, respectively.

### 3.2.2 Design of the Real-/Reactive-Power Controller

As it was previously mentioned, in order to increase the robustness of the proposed VSC, it employs current-mode control method, which in turn uses decoupled dc-frame control. The aforementioned approach consists of two loops, one inner loop for controlling the d- and q- axis current components, which is relatively fast, and an outer loop for controlling the dc voltage, which is slower than the aforesaid inner loop [59]. The focus of this subsection is to design the fast control loop for regulating the real-/reactive-power of the proposed converter. The design of the dc-side voltage controller is then presented in the following sections of this chapter.

Since dq-frame transformation is used for the inner-loop ac-side current controller of the proposed converter, the required reference signals for the aforementioned controller, $v_{sd}$ and $v_{sq}$ which are the dq-frame transformation of the ac-side voltage are all dc values. The aforementioned further simplifies the controller design for the a-side current controller and as a result a proportional-integrator (PI) compensator with the generic form of $K(s) = \frac{k_p s + k_i}{s}$ will be sufficient. The integral term of this compensator will guarantee that the current tracks its reference value with zero steady-state error, in spite of the disturbance. Based on Fig. 3.4 the open-loop gain of the proposed converter has a stable pole at $p = -\frac{R_r}{L'}$. Since, $p$ is typically close to the origin. The magnitude and phase angle of the uncompensated d- and q-axis current

control loop starts to drop from a fairly low frequency, i.e., the open loop system has a slow natural response. Thus, in order to improve the characteristics of the plant, the zero of the employed PI compensator is used to cancel out the inherent pole of the system. Hence, $\frac{K_p}{L'} = \frac{1}{\tau_i}$ and $\frac{k_i}{k_p} = \frac{R_r}{L_r}$, where $\tau_i$ is the desired time-constant of the closed loop system. $\tau_i$ is typically selected in the range of 0.5 and 5 $ms$. Choosing $\tau_i = 1\ ms$ the values of the proportional gain and integral time constant of the PI compensator will be found equal to 0.15 and 9. Figure 3.4 shows the bode plot of the uncompensated and compensated open-loop gain of the ac-side current controller. Equation (3.3) illustrates the transfer function of the d- and q-axis component of the ac-side current controller shown in Fig. 3.4. It must be taken in to consideration that the control loops of the d- and q-axis components of the current are identical, and thus the same compensator is employed for both loops. Using the aforementioned controller, the closed loop transfer function would be equal to what is shown in (3.4).

$$K_d(s) = K_q(s) = \frac{0.15s + 9}{s} \tag{3.3}$$

$$G_{i_\delta}(s) = \frac{i_d(s)}{i_d^*(s)} = \frac{i_q(s)}{i_q^*(s)} = \frac{P_s(s)}{P_s^*(s)} = \frac{Q_s(s)}{Q_s^*(s)} = \frac{1}{\tau_i s + 1} = \frac{1}{10^{-3}s + 1} \tag{3.4}$$

Equation (3.4) will be used in designing the dc-side voltage controller, which is explained in the upcoming part of this chapter.

## 3.3 DC-Side Voltage Controller

The main objective of the controlled dc-voltage power port is to regulate the dc-bus voltage, $v_{dc}$, at its desired reference value[43]. The schematic diagram of the current controlled dc-voltage power port was previously presented in Fig. 3.2. As it can be seen from Fig. 3.2 a feedback

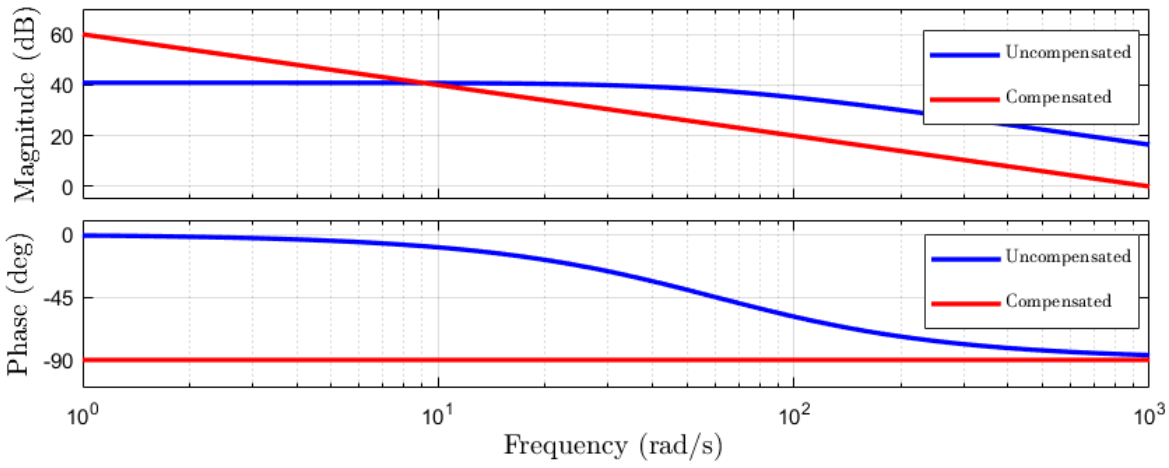


Figure 3.4: Bode plot of the uncompensated and compensated open-loop gain of the ac-side current controller.

signal is used to compare $v_{dc}$ with its reference command and accordingly adjusts $P_s(t)$, such that the net power exchanged with the dc-side capacitor of the proposed converter is kept at zero. It needs to be mentioned that the reactive power, $Q_s$, is independently controlled.

The model of controlled dc-voltage power port was presented in the second chapter of this thesis, which eventually led to the following

$$\frac{dv_{dc}^2}{dt} = \left(\frac{2}{C}\right)P_{ext} - \left(\frac{2}{C}\right)P_{loss} - \left(\frac{2}{C}\right)\left[P_s + \left(\frac{2L'}{3\hat{V}_s{}^2}\right)P_s\frac{dP_s}{dt}\right] - \left(\frac{2}{C}\right)\left(\frac{2L'}{3\hat{V}_s{}^2}\right)Q_s\frac{dQ_s}{dt} \tag{3.5}$$

Based on (3.5), $v_{dc}^2$ is the output, $P_s$ is the control input, and $P_{ext}$, $P_{loss}$, and $Q_s$ are the disturbance inputs. Figure 3.5 illustrates the resulting schematic diagram of the dc-bus voltage controller with feed-forward compensation when the $P_{loss}$ is neglected.

Unlike $P_s$, the reactive power exchanged with the grid, $Q_s$, is independently controlled, i.e., depending on the reactive power required by the grid it can be set to positive, negative or zero values.

Due to the presence of the terms $P_s\frac{dP_s}{dt}$ and $Q_s\frac{dQ_s}{dt}$ the plant described by (3.5) is non linear. Linearizing the aforementioned about its operating point results in

$$\frac{d\tilde{v}_{dc}^2}{dt} = \left(\frac{2}{C}\right)\tilde{P}_{ext} - \left(\frac{2}{C}\right)P_{loss} - \left(\frac{2}{C}\right)\left[\tilde{P}_s + \left(\frac{2L'}{3\hat{V}_s{}^2}\right)P_s^0\frac{d\tilde{P}_s}{dt}\right] - \left(\frac{2}{C}\right)\left(\frac{2L_{eq}}{3\hat{V}_s{}^2}\right)Q_s^0\frac{d\tilde{Q}_s}{dt} \tag{3.6}$$

In (3.6) subscript ~ and superscript 0 represents the small-signal perturbations and steady-state values of the variables, respectively. Hence,

$$G_v(s) = \frac{\tilde{v}_{dc}^2(s)}{\tilde{P}_s(s)} = -\left(\frac{2}{C}\right)\frac{\tau s + 1}{s} \tag{3.7}$$

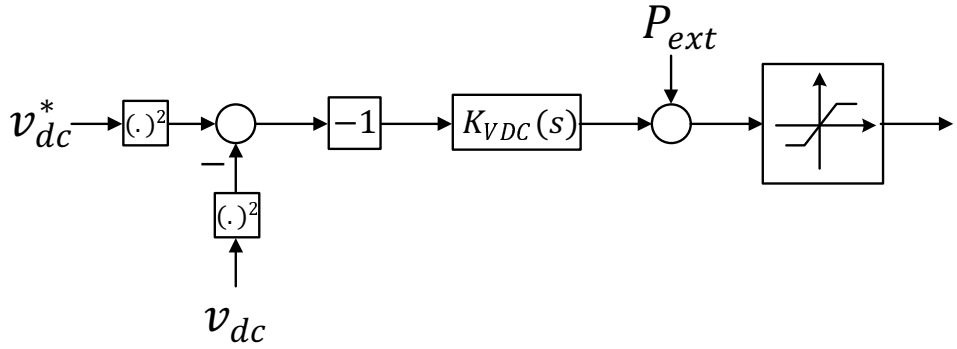


Figure 3.5: Schematic diagram of the dc-bus voltage controller with feed-forward compensation.

where the time constant $\tau$ is

$$\tau = \frac{2L' P_s^0}{3v_{sd}^2} \tag{3.8}$$

It can be understood from (3.8) that the time constant in the dc-bus voltage control loop of the proposed converter is directly proportional to the steady-state real power exchanged with the grid, denoted by $P_s^0$. By neglecting the losses in the converter it can be assumed that $P_s^0$ is equal to the steady-state real power exchanged between the converter and the external power source, i.e., $P_{ext}^0$. As a result, the time constant would become insignificant and make the plant predominantly an integrator if the value of $P_{ext}^0$ is small enough. By increasing the steady-state power drawn from the external power source, $\tau$ increases and makes a change in the phase of the plant. The aforementioned phase shift can either add to the phase of $G_v(s)$ or reduce it, corresponding to inverting and rectifying mode of operation, respectively. Based on (3.8), during the rectifying mode of operation, the value of $\tau$ would become negative, i.e., would result in a zero in the right half plane (RHP). Hence, during the rectifying operation mode the controlled dc-voltage power port is a non-minimum-phase system. The aforementioned must be taken into considerations during its controller design process.

In Fig. 3.2, the external power is added to the control loop as a feed-forward signal, so that the changes in the external power are rapidly reflected in the reference value of the active power exchanged with the grid. Hence, eliminating the impacts of the changes in the external power on the dc-side voltage of the converter. Figure 3.2 also shows that the reference power achieved using the dc-side controller is passed through a saturation block, before being used to generate the d-axis component of the reference value of ac-side current. The aforementioned saturation block will protect the converter from the potential over currents that might be caused due to the significant differences between the actual and reference value of the dc-side voltage, or large changes in the power exchanged with the converter and the power source connected to the dc side of the converter.

The rated power of the converter system was chosen equal to 160 $kW$. The power controller dynamics shown in Fig. 3.6, is the same as the closed-loop transfer function of the ac-side current previously given in (3.4). Using dc-side voltage controller shown in Fig. 3.6, the open-loop gain can be found as presented in (3.9).

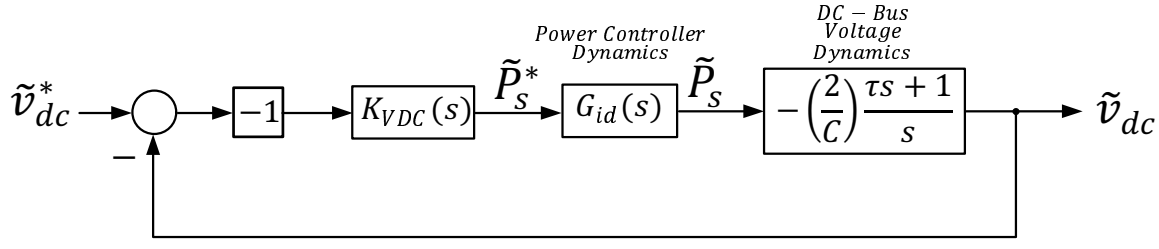


Figure 3.6: Control block diagram of dc-bus voltage controller based on linearized model.

$$\ell_{VDC}(s) = -K_{VDC}G_{id}(s)\left[\left(\frac{-2}{C}\right)\frac{\tau s+1}{s}\right] \tag{3.9}$$

where $G_{id}(s)$ is the closed-loop transfer function of the control loop of the d-axis ac-side current and is given by (3.4).

As it was previously mentioned in this part, the dc-bus voltage dynamics depend on the operating point of the converter. Consequently, $K_{VDC}$ must be designed for the worst-case operating scenario, i.e., $P^0_{ext} = -160\ kW$, which causes the converter system to become a non-minimum phase plant.

The compensator used in the dc-side voltage control loop, shown in Fig. 3.2, must include an integral term to ensure zero steady-state error in the $v^2_{dc}$ and eliminate the effects of $P_{loss}$ term in (3.5). As it was previously discussed, the impact of the external power on the dc-side voltage is mostly eliminated by using the feed-forward compensation. Consequently, $K_{VDC}(s)$ can be rewritten as

$$K_{VDC} = N_{VDC}(s)\left[\frac{k_{VDC0}}{s}\right] \tag{3.10}$$

where $N_{VDC}(s)$ and $k_{VDC0}$ are proper transfer function with no zeros at the origin, and constant gain, respectively. Substituting (3.10) for the dc-side voltage compensator in (3.9), will lead to

$$\ell_{VDC}(s) = -N_{VDC}(s)\left[\frac{k_{VDC0}}{s}\right]\left[\frac{1}{\tau_i s+1}\right]\left[\left(\frac{-2}{C}\right)\frac{\tau s+1}{s}\right] \tag{3.11}$$

Using (3.4) the bandwidth of the closed-loop d-axis current control system is found equal to 1000 $rad/sec$. Hence, in order to avoid excessive phase lag in the dc-side voltage control loop, its cross-over frequency is chosen to be one fifth of the bandwidth of $G_{id}(s)$, i.e., 200 $rad/s$.

First, assuming $N_{VDC}(s) = 1$, the value of the constant gain of the compensator corresponding to $\omega_{c_{VDC}} = 200\ rad/s$ is found as $-200.6$, and the open-loop gain can be rewritten as

$$\ell_{VDC}(s) = \left[\frac{193.747}{s}\right]\left[\frac{1}{\tau_i s+1}\right]\left[\left(\frac{2}{C}\right)\frac{\tau s+1}{s}\right] \tag{3.12}$$

Equation (3.15), is referred to as the uncompensated loop gain of the dc-side voltage controller. Fig. 3.7 represents the magnitude and phase plot of the uncompensated loop gain corresponding to the $P^0_{ext} = -160\ kW$ operating point. The phase margin of the uncompensated loop gain is $-197.5^\circ$ which indicates that the closed-loop system is unstable.

In order to achieve a stable closed-loop system $N_{VDC}(s)$ must be designed to correct the phase margin of the uncompensated loop gain. Thus, $N_{VDC}(s)$ must be a lead compensator. Assuming a desired phase margin of 60 degrees, the lead filter would be found as

$$N_{VDC}(s) = 12.1406\left[\frac{s+16.47}{s+2428}\right] \tag{3.13}$$

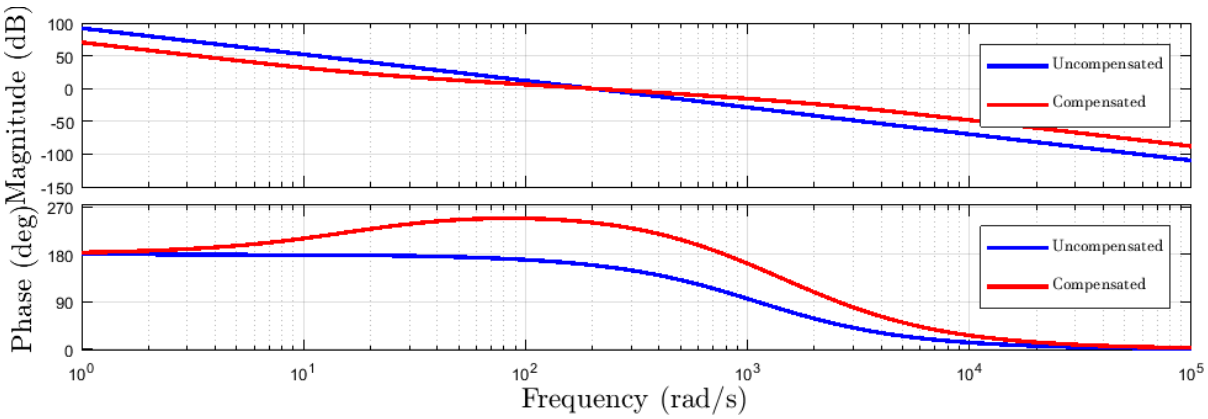


Figure 3.7: Bode plot of the uncompensated and compensated open-loop gain of the dc-bus voltage controller for $P_{ext} = -160\ kW$.

Hence, the dc-side voltage controller is eventually found as

$$K_{VDC}(s) = 2352.2\left[\frac{s + 16.47}{s\,(s + 2428)}\right] \tag{3.14}$$

Using (3.14), as the dc-side voltage controller, the compensated loop gain is found as

$$\ell_{VDC}(s) = 2352.2\left[\frac{s + 16.47}{s\,(s + 2428)}\right]\left[\frac{1}{\tau_i s + 1}\right]\left[\left(\frac{2}{C}\right)\frac{\tau s + 1}{s}\right] \tag{3.15}$$

The magnitude and phase plot of the uncompensated- and compensated-loop gain of the dc-bus voltage controller are presented in Fig.3.7.

$$K_{VDC} = 2352.2\left[\frac{s + 16.47}{s\,(s + 2428)}\right] \tag{3.16}$$

As a result, by employing (3.16) the closed-loop system is stable for $P_{ext} = -160\ kW$, i.e., the worst-case scenario. In order to be thorough the bode plots of the uncompensated and compensated of the open-loop gain of the DC-bus voltage controller for $P_{ext} = 160$, and $0\ kW$ are also presented in Fig. 3.8 and 3.9, respectively. The $\angle \ell_{VDC}(j200)$ corresponding to $P_{ext} = 160$, and $0\ kW$ are $-101.5°$ and $-110.6°$ , respectively, which confirms the aforementioned statement that $P_{ext} = -160\ kW$ is the worst case and designing a controller for this situation leads to stability of the closed-loop system under all operating conditions.

## 3.4 Energy Balance Controller

In the previous sections, the control technique used for regulating the dc-side voltage of the proposed converter was explained. It was shown that the dc-side voltage of the converter,

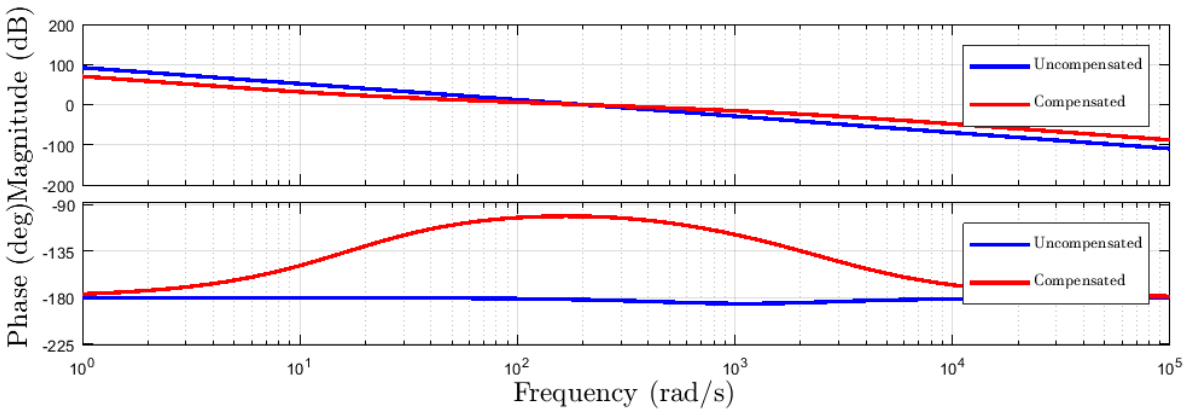


Figure 3.8: Bode plot of the uncompensated and compensated open-loop gain of the dc-bus voltage controller for $P_{ext} = 160\ kW$.

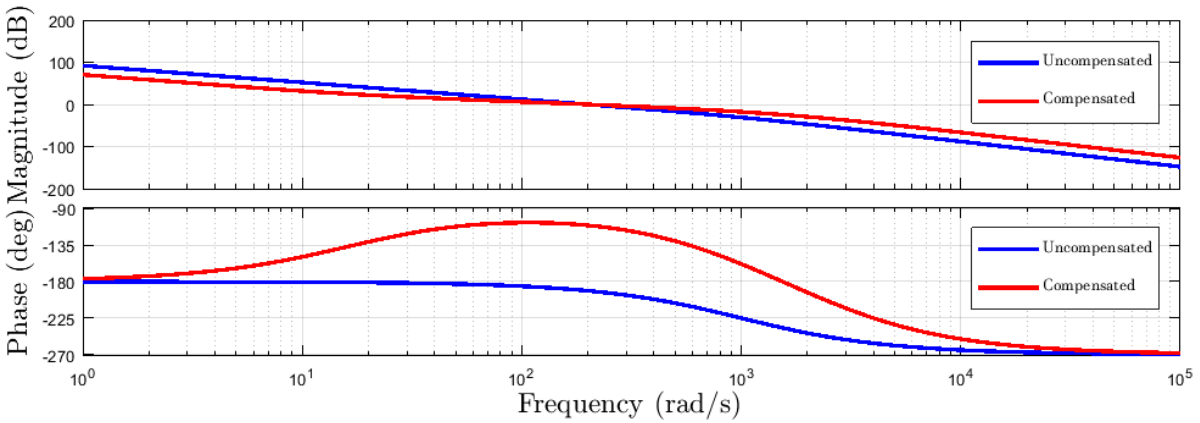


Figure 3.9: Bode plot of the uncompensated and compensated open-loop gain of the dc-bus voltage controller for $P_{ext} = 0\ kW$.

is controlled trough the ac-side current. In order to reach a balanced three-phase voltage-sourced converter systems, the energy must be uniformly distributed among the FBSMs of the proposed converter. Hence, next step is to ensure the balanced operation of the converter under all conditions. To achieve the aforementioned, the dc-side voltage of the FBSMs needs to be regulated at the value of the dc-side voltage of the converter. The dc-side FBSM voltage control is done through two control loops, whose outputs would generate the reference common-mode current for each leg. The first one regulates the common-mode power of the FBSMs in each leg, and consequently regulates the common-mode squared dc-side voltage of each leg. The second control loop, focuses on regulating the differential-mode active power of the FBSMs in each leg, by doing so the differential-mode squared dc-side voltages of the corresponding submodules are regulated. Both of the aforementioned algorithms are fully discussed in the next two sub sections of this thesis.

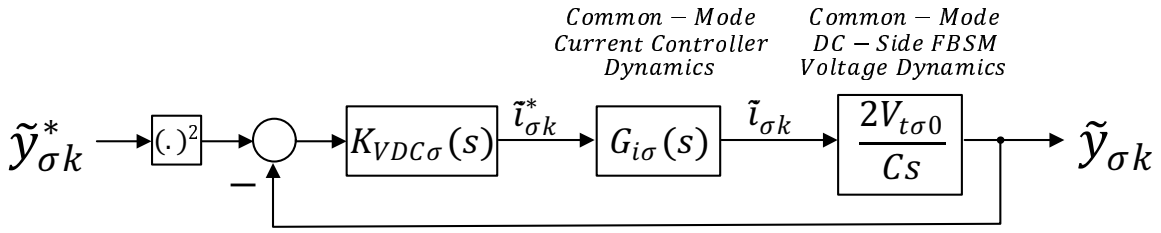


Figure 3.10: Control scheme figure for the common-mode dc-side squared voltage controller.

### 3.4.1 Leg Energy Balance Controller

It was previously mentioned in Chapter 2, that the common-mode powers of the submodules in each leg are used to achieve the leg energy balance. As it was shown in Chapter 2, the common-mode power of the FBSMs in the $k$th leg, can be found as (3.17). In (3.17), the losses of the upper and lower submodule of the $k$th leg are ignored, and it is assumed that the rate of change of the energy of the dc-side capacitor of each FBSM is equal to its terminal power.

$$\frac{1}{2}C\frac{d}{dt}y_{\sigma k} = \frac{P_{DCk} - P_{tk}}{2} \tag{3.17}$$

where $P_{DCk} = v_{DC}i_{\sigma k} = 2v_{t\sigma k}i_{\sigma k}$. Thus, (3.17) can be rewritten as

$$\frac{1}{2}C\frac{d}{dt}y_{\sigma k} = \frac{2v_{t\sigma k}i_{\sigma k}}{2} - \frac{P_{tk}}{2} \tag{3.18}$$

Equation (3.18) describes dynamics of the dc-side common-mode squared voltage of the FBSMs in the $k$th leg of the converter. Based on (3.18), $y_{\sigma k}$ is the output signal, $i_{\sigma k}$ is the control input, $P_{tk}$ is the disturbance input. However, the control plant described by (3.18), is non-linear due to the presence of the term $v_{t\sigma k}i_{\sigma k}$. After linearizing (3.18) about its steady-state operating point, (3.18) can be re-written as

$$\frac{1}{2}C\frac{d}{dt}\tilde{y}_{\sigma k} = \frac{v^0_{t\sigma k}\tilde{i}_{\sigma k}}{2} + \frac{\tilde{v}_{t\sigma k}i^0_{\sigma k}}{2} - \frac{P^0_{tk}}{2} - \frac{\tilde{p}_{tk}}{2} \tag{3.19}$$

Hence, in order to control the sum of the common-mode dc-side squared voltage of the FBSMs in each leg, the control scheme presented in Fig. 3.10 can be used.

Transforming (3.19) to Laplace domain gives the following transfer function from $\tilde{i}_{\sigma k}$ to $\tilde{v}_{C\sigma k}$ as

$$\frac{\tilde{y}_{\sigma k}(s)}{\tilde{i}_{\sigma k}(s)} = \frac{v^0_{t\sigma k}}{Cs} \tag{3.20}$$

The control scheme shown in Fig. 3.10, is composed of a controller, $K_{VDC\sigma}(s)$, the common-mode current controller dynamics, denoted by $G_{i\sigma}(s)$, and the control plant representing the

common-mode dc-side FBSMs' squared voltage dynamics. As Fig. 3.10 illustrates, in order to design the common-mode squared dc-side voltage controller of each leg, first the common-mode current control loop must be formed. Thus, the subsections below, will first discuss the common-mode current controller and then focuses on the design of the common-mode dc-side FBSMs' squared voltage controller.

### Common-Mode Current Controller Design

The common-mode current in each leg of the converter, is the current going through both arms of the corresponding leg and as it was previously mentioned in Chapter 2 it can be calculated using (3.21). The reference value of the common-mode current of each leg can be found by regulating the dc-side voltage of the FBSMs in the leg. Thus, in order to achieve the FBSMs' dc-side voltage control, the common-mode current must be able to effectively track its reference value, which is done using the common-mode current controller. In this section the design of the aforementioned controller is presented.

$$i_{\sigma k} = \frac{i_{1k} + i_{2k}}{2} \tag{3.21}$$

As it was previously shown in Chapter 2, the ac-side current of the converter is given by

$$i_k = i_{1k} - i_{2k} = -2i_{\delta k} \tag{3.22}$$

Equation (3.22) shows that the ac-side current of the converter only depends on the differential-mode current of the corresponding leg. Thus, the common-mode quantities do not have any effect on the ac-side variables of the converter, and as a result they can be independently controlled.

The simplified equivalent circuit of the $k$th leg of the converter as seen from the dc side was presented in Chapter 2 and is represented in Fig. 3.11 for ease of use.

From Fig. 3.11 and using KVL method it can be found that

$$\frac{v_{dc}}{2} = v_{t\sigma k} + (R + 2r_{on})\, i_{\sigma k} + L\frac{d}{dt} i_{\sigma k} \tag{3.23}$$

where $v_{t\sigma k} = \frac{v_{t1k}+v_{t2k}}{2}$ and $i_{\sigma k} = \frac{i_{1k}+i_{2k}}{2}$.

Transferring (3.23), to the Laplace domain gives the following transfer function from $v_{t\sigma k}$ to $i_{\sigma k}$

$$G_{i\sigma k} = \frac{i_{\sigma k}}{v_{t\sigma k}} = \frac{-1}{Ls + (R + 2r_{on})} \tag{3.24}$$

Figure 3.12 illustrates the control block diagram of the common-mode current control loop for the $k$th leg, when all the capacitors are replaced by dc-voltage sources.

Next step, is to design the common-mode current controller for the proposed converter using the control loop presented in Fig. 3.12. Since the common-mode current is mainly dc

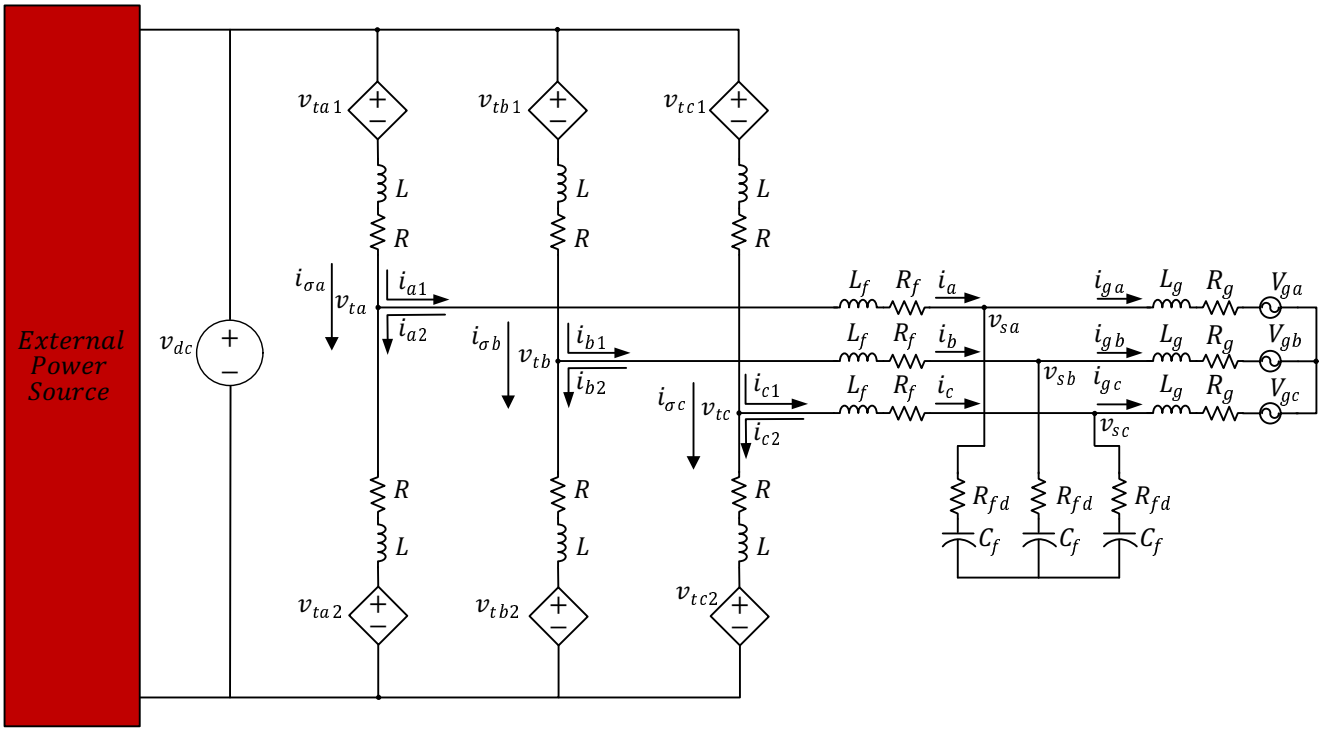


Figure 3.11: Schematic diagram of the proposed converter when the converter is operating under normal conditions.

and $v_{dc}$ is also a dc voltage, a proportional-integrator (PI) compensator with the generic form of $K(s) = \frac{k_p s + k_i}{s}$ will be sufficient. as it was mentioned earlier in this chapter, the integral term of this compensator will guarantee that the current tracks its reference value with zero steady-state error, in spite of the disturbance of $v_{dc}$ . Based on Fig. 3.12 the open-loop gain of the proposed converter has a stable pole at $p = -\frac{R+2r_{on}}{L}$. The PI compensator is designed in a manner that would increase the speed of the control loop. Hence, $\frac{K_p}{L} = \frac{1}{\tau_{i\sigma}}$ and $\frac{k_i}{k_p} = \frac{R+2r_{on}}{L}$, where $\tau_{i\sigma}$ is the desired time-constant of the closed loop system. Choosing $\tau_{i\sigma} = 1\ ms$ the values of the proportional gain and integral time constant of the PI compensator will be found equal to 0.1

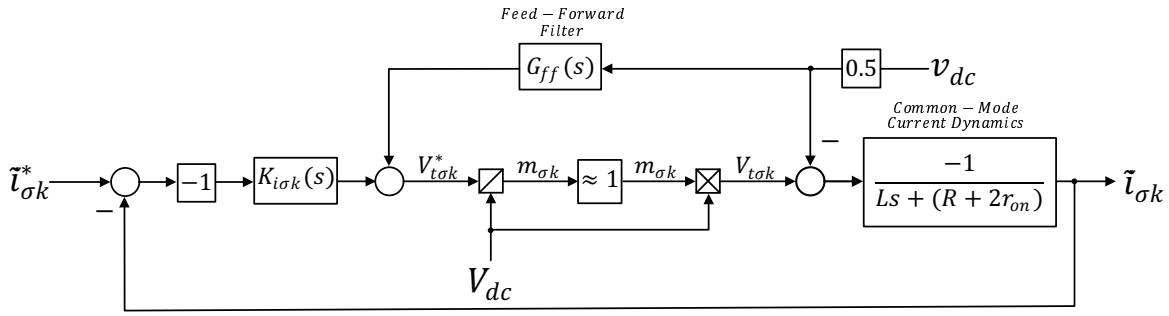


Figure 3.12: Control block diagram of the common-mode current controller for the *k*th leg of the proposed ac/dc converter.

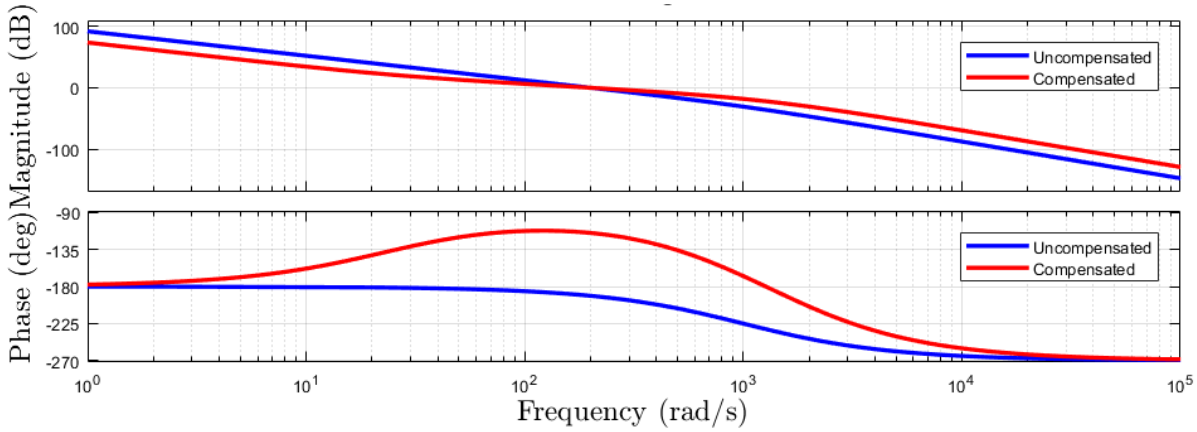


Figure 3.13: Bode plot of the uncompensated and compensated open-loop gain of the common-mode current controller.

and 14, respectively.

Figure 3.13 shows the bode plot of the uncompensated and compensated open-loop gain of the common-mode current controller. Equation (3.25) illustrates the transfer function of the common-mode current controller shown in Fig. 3.12.

$$K_{i\sigma}(s) = -\frac{0.1s + 14}{s} \tag{3.25}$$

Using the aforementioned controller, the closed loop transfer function would be equal to what is shown in (3.26).

$$G_{i\sigma}(s) = \frac{1}{\tau_{i\sigma}s + 1} = \frac{1000}{s + 1000} \tag{3.26}$$

Using Fig. 3.13, it can be seen that the phase margin of the common-mode current control loop is 90° and the gain cross-over frequency is 1000 $rad/s$. Hence, the system is stable with an appropriate time constant.

### Common-Mode Power Controller Design

The closed-loop transfer function of the common-mode current control loop, $G_{i\sigma}(s)$, shown in Fig. 3.10, was calculated in the previous subsection and presented in (3.26). Hence, using (3.26), the open-loop gain for the common-mode instantaneous FBSM power control loop is found as

$$\ell_{p\sigma k}(s) = K_{p\sigma k}(s)\left[\frac{1}{\tau_{i\sigma}s + 1}\right]\left[\frac{2v^0_{t\sigma k}}{Cs}\right] \tag{3.27}$$

In order to ensure zero steady-state error in spite of the available disturbances, the common-mode FBSM power controller must include an integral term. Thus, $K_{p\sigma k}(s)$ can be rewritten as

$$K_{p\sigma k}(s) = N_{p\sigma k}(s)\left[\frac{k_{p\sigma k0}}{s}\right] \tag{3.28}$$

where $N_{p\sigma k}$ and $k_{p\sigma k0}$ are proper transfer function without any zeros at the origin and constant gain, respectively. In order to design the compensator, first it is assumed $N_{p\sigma k}(s) = 1$ and the value of the constant gain of the common-mode power compensator corresponding to the gain cross-over frequency of one-fifth of the bandwidth of the $G_{icm}$, i.e., 200 $rad/s$. Hence, the instantaneous common-mode FBSM power controller for each leg is chosen as a simple gain, in order to set the cross-over frequency at 200 $rad/s$, i.e., one fifth of the bandwidth of common-mode current control loop. Moreover, the steady-state value of the common-mode voltage, denoted by $v^0_{t\sigma k}$ in (3.27) is half of the steady-state value of the dc-side voltage. Hence, (3.27) can be rewritten as

$$\ell_{p\sigma k}(s) = K_{p\sigma k}(s)\left[\frac{1000}{s+1000}\right]\left[\frac{v_{dc}}{Cs}\right] \tag{3.29}$$

In order to ensure zero steady-state error, $K_{p\sigma k}$ must have an integral term. Hence, the general form of $K_{p\sigma k}$ can be assumed as follows

$$K_{p\sigma k}(s) = N_{p\sigma k}(s)\frac{k_{p\sigma k0}}{s} \tag{3.30}$$

In (3.30), $N_{p\sigma k}(s)$ is a proper transfer function without any zeros at the origin, and $k_{p\sigma k0}$ is a constant gain. Substituting the compensator presented in (3.30) in (3.29) would lead to

$$\ell_{p\sigma k}(s) = N_{p\sigma k}(s)\frac{k_{p\sigma k0}}{s}\left[\frac{1000}{s+1000}\right]\left[\frac{v_{dc}}{Cs}\right] \tag{3.31}$$

Assuming $N_{p\sigma k}(s) = 1$, the value of $k_{p\sigma k0}$ corresponding to the cross-over frequency of 200 $rad/s$ can be calculated using the fact that at the cross-over frequency the magnitude of the open-loop gain is equal to one. Hence,

$$k_{p\sigma k0} = 196.3123 \tag{3.32}$$

Using the value given in (3.32), the open-loop gain is calculated as follows, still considering $N_{pcmi} = 1$

$$\ell_{p\sigma k}(s) = \frac{196.3123}{s}\left[\frac{1000}{s+1000}\right]\left[\frac{v_{dc}}{Cs}\right] \tag{3.33}$$

Equation (3.31) is referred to as the uncompensated loop gain of the common-mode instantaneous FBSM power. The bode plot of the uncompensated open-loop gain of the instantaneous

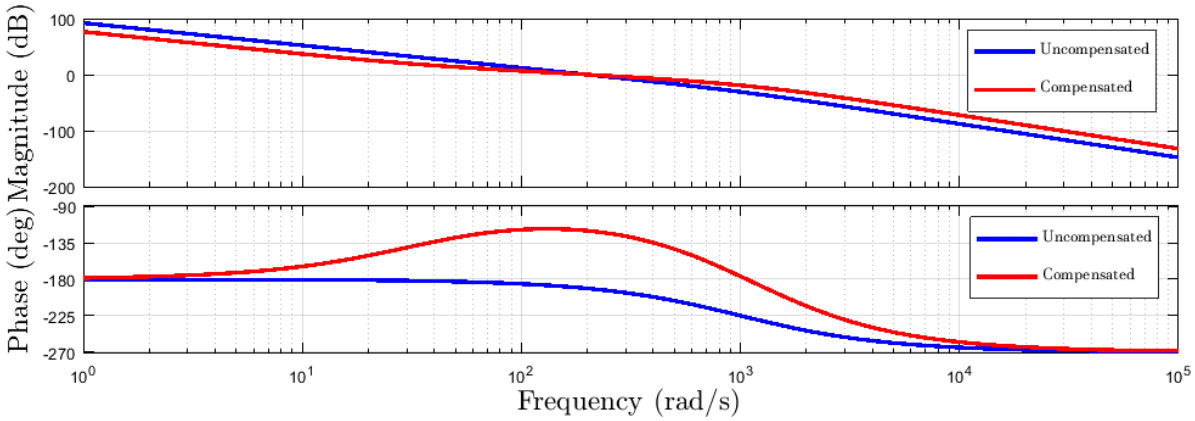


Figure 3.14: Bode plot of the uncompensated and compensated open-loop gain of the instantaneous common-mode FBSM power controller.

common-mode FBSM power controller is illustrated in Fig. 3.14. Using Fig. 3.14, the phase margin of the uncompensated system is found equal to $-11.3°$, which means the closed-loop system is unstable. Thus, in order to achieve stability in the closed-loop system, $N_{p\sigma k}$ must be a lead compensator. Setting the desired phase margin to 60°, the aforementioned lead compensator is found as follows

$$N_{p\sigma k}(s) = 6.0767\frac{s + 32.91}{s + 1215} \tag{3.34}$$

Hence, the $K_{p\sigma k}$ controller shown in Fig.3.14 has a final form of

$$K_{p\sigma k}(s) = 1192.9\frac{s + 32.91}{s\,(s + 1215)} \tag{3.35}$$

Using the proposed compensator in (3.35), the leg energy balance of the proposed converter is achieved, and the open-loop gain of the common-mode instantaneous FBSM power controller will be as follows

$$\ell_{p\sigma k}(s) = 1192.9\left[\frac{s + 32.91}{s\,(s + 1215)}\right]\left[\frac{1000}{s + 1000}\right]\left[\frac{V_{dc}}{Cs}\right] \tag{3.36}$$

Fig. 3.14 also illustrates the bode plot of the compensated loop gain of the common-mode instantaneous power controller. As it can be observed from Fig. 3.14 $\angle\ell_{p\sigma k}(j200) = 120°$, i.e., the closed loop system is stable with a phase margin of 60°.

### 3.4.2 Differential-Mode Active Power Controller

As it was previously mentioned, in order to ensure that the energy is evenly distributed among the FBSMs, the dc-side voltages of all the submodules must be regulated to the value of $v^*_{dc}$.

To achieve the aforementioned goal, first the common-mode FBSM power is regulated, which in turn regulates the common-mode squared dc-side voltage of the submodules in each leg. Then the differential-mode squared dc-side voltage of the submodules is regulated by enabling power transfer among the FBSMs in each leg. As a result, the dc-side voltage of the individual FBSMs in each leg can be regulated.

As it was illustrated in the second chapter, the power transferred between the upper and lower submodule in the $k$th leg is found as

$$P_{\delta k} = \frac{1}{2}\hat{i}_{\sigma 1k}\hat{v}_{t\delta} cos\left(\gamma - \alpha\right) \tag{3.37}$$

where $P_{\delta k} = \frac{\Delta P_k}{2}$. Moreover, ignoring the power loss in each full-bridge submodule, $P_{\delta k}$ can be rewritten as

$$P_{\delta k} = \frac{1}{2}C\frac{d}{dt}y_{\delta k} \tag{3.38}$$

Hence,

$$\frac{1}{2}C\frac{d}{dt}y_{\delta k} = \frac{1}{2}\hat{i}_{\sigma 1k}\hat{v}_{t\delta} cos\left(\gamma - \alpha\right) \tag{3.39}$$

The minimum fundamental frequency component of the current can be achieved by ensuring that the common-mode current and terminal voltage of the same leg are in phase with one another. Hence, (3.39) can be rewritten as

$$\frac{C}{s}y_{\delta k} = \hat{i}_{\sigma 1k}\hat{v}_{t\delta} \tag{3.40}$$

Equation (3.40) is non-linear due to the presence of the term $\hat{i}_{\sigma 1k}\hat{v}_{t\delta}$. By linearizing(3.40) about its steady-state operating point (3.40) can be rewritten as

$$\frac{C}{s}\tilde{y}_{\delta k} = \tilde{\hat{i}}_{\sigma 1k}\hat{v}_{t\delta 0} + \hat{i}_{\sigma 1k}\tilde{\hat{v}}_{t\delta 0} \tag{3.41}$$

Transforming (3.41) to Laplace domain gives the following transfer function from $\tilde{\hat{i}}_{\sigma 1k}$ to $\tilde{y}_{\delta k}$

$$\frac{\tilde{y}_{\delta k}}{\tilde{\hat{i}}_{\sigma 1k}} = \hat{v}_{t\delta 0}\frac{1}{Cs} \tag{3.42}$$

Equation (3.42) describes the dynamics of the differential-mode active power of the FBSMs in the $k$th leg, which will be used in the upcoming section of this thesis to design the differential-mode active power controller for the $k$th leg.

**Design of the Differential-Mode Active-Power Controller**

Figure 3.15 illustrates the control block diagram of the common-mode current controller for the $k$th leg. As it can be illustrated from Fig. 3.15 regulating $y_{\delta k}$ results in a fundamental frequency common-mode current denoted by $i^1_{\sigma k}$, which in turn enables an active power transfer between the full-bridge submodule in the upper and lower arm of the $k$th leg called the differential-mode active power. The direction of the aforementioned common-mode current and consequently the power transfer is decided by the dc-side voltage of the FBSMs in each leg, i.e., if the dc-side voltage of lower FBSM is higher than the dc-side voltage of the upper FBSM, a fundamental frequency current from the lower to the upper arm will be formed, this current will lead to discharging the capacitor of the FBSM in the lower arm of the $k$th leg, while at the same time charging the capacitor at the dc-side of the FBSM in the upper arm of the $k$th leg, and vice versa.

It must be mentioned that $\hat{v}_{t\delta 0}$ represents the maximum steady-state value of the differential-mode terminal voltage. Ignoring the resistive losses at the ac side of the converter, under steady-state operation the value of the $\hat{v}_{t\delta 0}$ can be assumed to be equal to the maximum value of the ac voltage at the point of common connection of the converter and the grid. As it can be seen from Fig. 3.15 the effect of $\hat{v}_{t\delta 0}$ is implemented externally rather than being accounted for in the controller.

Furthermore, from Fig. 3.15, and using (3.26) and (3.42) , the open-loop gain of the differential-mode FBSM active power control loop is fund as

$$\ell_{P\delta k}(s) = -K_{P\delta k}(s)\left[\frac{1}{\tau_{i\sigma}s+1}\right]\left[\frac{1}{Cs}\right]\hat{v}_{t\delta 0} \tag{3.43}$$

Setting $K_{P\delta k}(s) = 1$ in (3.43) leads to the uncompensated open-loop gain of the differential-mode active power controller. Choosing a simple P controller as $K_{P\delta k}(s)$ ensures the regulation of the $v_{C\delta k}$ at its desired reference value, i.e., 0. Thus $K_{P\delta k}(s)$ will adopt the general form of

$$K_{P\delta k}(s) = k_{P\delta 0} \tag{3.44}$$

where $k_{P\delta k0}$ is a constant gain. Moreover, the cross-over frequency of the differential-mode active power control loop is chosen equal to one fifth of the bandwidth of the common-mode

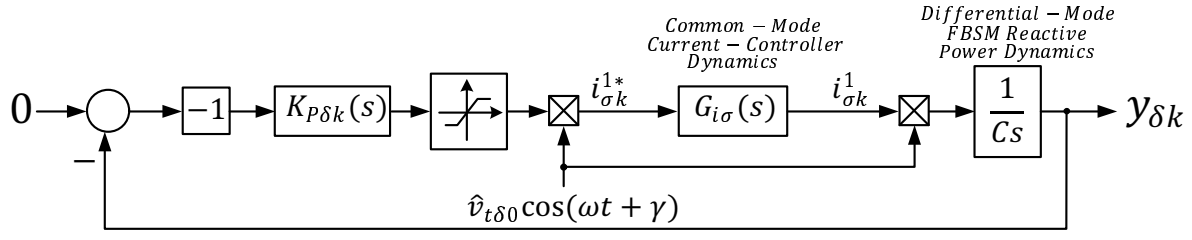


Figure 3.15: Control block diagram of the differential-mode dc-side squared voltage controller for the $k$th leg of the proposed ac/dc converter.

current controller, i.e., 200 $rad/s$. Using the fact that $|\ell_{P\delta k}(j200)| = 1$, the constant gain of the differential-mode active power controller is found equal to 0.9814. Thus,

$$K_{P\delta k}(s) = 0.9814 \tag{3.45}$$

Using (3.45), the open-loop compensated loop gain can be found as follows

$$\ell_{P\delta k}(s) = 0.9814 \left[\frac{1}{\tau_{i\sigma} s + 1}\right]\left[\frac{1}{Cs}\right] \tag{3.46}$$

Using the controller presented in (3.45), the phase margin is 78.7° which indicates that the system is stable.

The resulting common-mode current is negligible in comparison to the common-mode current resulting from the common-mode power controller, which was discussed in previous sections. Thus, it will not affect the results of the aforementioned control loop.

## 3.5 Summary of the Control

In this chapter the control strategy of the proposed converter was analyzed. As Fig. 3.2 illustrates, there are two independent control input sets for each leg of the converter, i.e., the differential- and common-mode modulating signals. The former is used in order to regulate the dc-side voltage of the proposed converter, by regulating the amount of the power exchanged with the grid, denoted by *DC-Bus Voltage Controller with Feed-Forward Compensation* and *Real- and Reactive Power controller* in Fig. 3.2. However, the common-mode modulating signal of each leg is achieved by regulating the dc-side voltage of the individual building blocks of the proposed converter, shown with *FBSM DC-Side Voltage Controller* in Fig. 3.2. The *Modulating Signal Generator* in Fig. 3.2 uses the differential- and common-mode modulating signals are then used to generate the modulating signal required for each individual sub-module. The relationship between the differential- and common-mode modulating signals of the $k$th leg and the modulating signals of each of the submodules in the same leg, was presented in the second chapter, and it is being repeated in Fig. 3.16 for the ease of use:

$$m_{1k} = m_{\sigma k} - m_{\delta k} \tag{3.47}$$

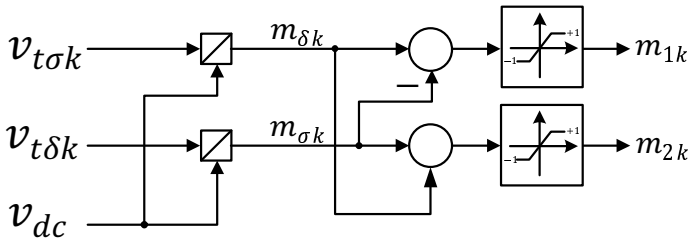


Figure 3.16: Schematic diagram of the modulating signal generator of the $k$th leg of the proposed converter.

$$m_{2k} = m_{\sigma k} + m_{\delta k} \tag{3.48}$$

# Chapter 4

# Simulation Results

## 4.1 Introduction

Chapters 2 and 3 focused on presenting the mathematical model and control methodology for the proposed bidirectional ac/dc converter. To evaluate the performance of the converter and the effectiveness of its controllers under various normal and faulted operation scenarios, a model of the converter has been simulated and tested in PSCAD/EMTDC software environment. The following sections of this chapter, discuss the test system configurations, defines various study cases and presents the obtained results from simulating the converter's model under the aforementioned scenarios in PSCAD/EMTDC environment.

## 4.2 Test System Configurations

This section discusses the configurations of the test system simulated in the PSCAD/EMTDC environment. The schematic diagram of the proposed converter was previously presented in this thesis and is shown again in Fig. 4.1 for ease of use. It must be mentioned that the converter shown in Fig. 4.1 is connected to an external power source at its dc side, which is not shown. The external power source is implemented in the simulations by a current source, whose current is subjected to stepwise changes in order to simulate an actual uncontrollable dc power source. As it can be seen from Fig. 4.1 the converter is connected in parallel with dc-side capacitor at its dc-side. However, during the simulations the dc-side capacitor was modeled by a series connection of two identical capacitors, marked by $2C$ whose capacitance is $2 \times 9625\ \mu F$. By doing so, the virtual neutral point of the converter will be achievable during the simulations. At the ac side the converter interfaces with the host ac grid that is modeled by a series connection of ideal ac voltage source with the grid reactor, which includes both the grid's inductance and its losses. The aforementioned are marked by $v_g$, $L_g$ and $R_g$, respectively, and present a non-ideal grid. The proposed converter is designed for distribution level systems. Thus, the voltage of the ac grid was chosen as 208 $V$, line-to-line rms. While the magnitude of the grid inductance and resistance are chosen equal to $3.6 \times 10^{-5}\ H$ and $0.0135\ \Omega$, respectively, which corresponds to $X_{Rg} = X_{Lg} = 0.05\ pu$. As it was mentioned in Chapter 2, at the point of common connection of the ac grid and the converter an LC filter is used. The three-phase capacitor branch of the filter is equipped with damping resistors and provides a path for

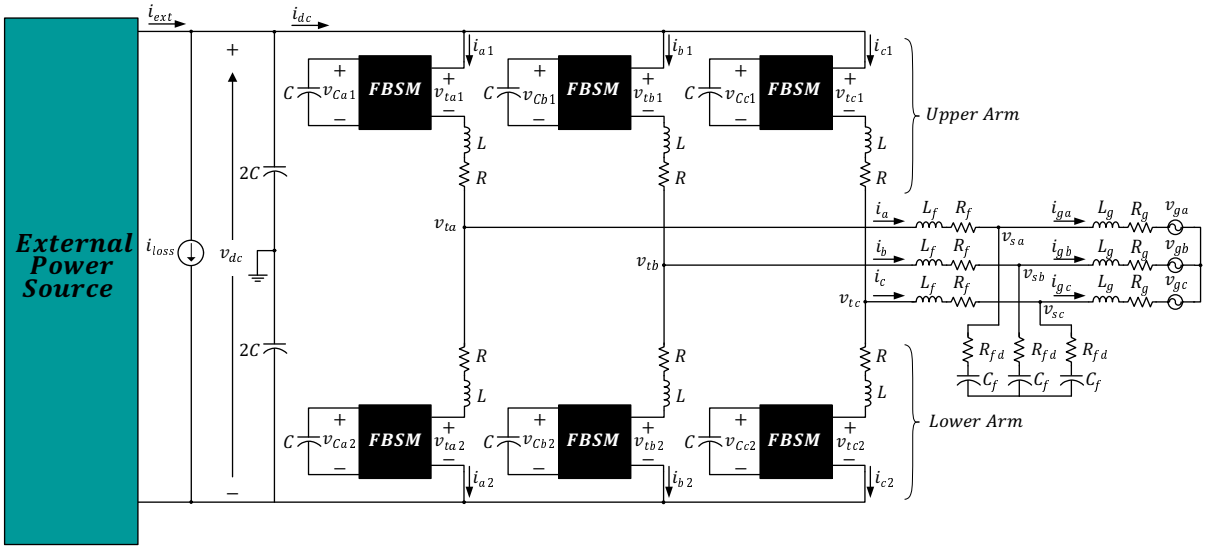


Figure 4.1: Schematic diagram of the proposed converter when connected to a non-ideal grid.

the high-frequency harmonic components of the current, the capacitance and resistance of the aforementioned shunt capacitor branch are referred to as $C_f$ and $R_fd$ in Fig. 4.1 and their magnitudes are 100 $\mu F$ and 0.1 Ω, respectively. Moreover, the magnitude of the inductance of the LC filter, marked with $L_f$ on Fig. 4.1, was chosen equal to $10^{-4}$ $H$. The losses associated with the filter is presented as $R_f$ in Fid 4.1 and has a resistance of 2.0 $mH$. The converter was also simulated while connected to an ideal ac grid, which can be modeled by a three-phase ideal ac voltage source. As it can be seen from Fig. 4.1 each arm of the converter consists of a series connection of a full-bridge submodule and the RL branch. The values of the inductance and the resistance of the arm reactor are 0.1 $mH$ and 3 $m\Omega$, respectively. FBSMs are connected to a capacitor at their dc-side. shown by $C$ in Fig. 4.1. The capacitance of all the dc-side capacitors in the proposed converter have the same value of 9625 $\mu F$. The aforementioned circuit variables are also presented in A.

For the control of the proposed converter, the common-mode current control strategy, dc-side voltage and the real- and reactive-power control schemes previously discussed in Chapter 3 were adopted. The controller parameters are also presented in B for the ease of use.

Thus, the upcoming sections of this chapter focuses on describing the different case studies simulated in PSCAD/EMTDC software environment. Followed by presenting the obtained results and their interpretations.

‘

## 4.3 Study Cases and Simulation Results

The operation of the proposed bidirectional ac/dc converter was analyzed in PSCAD/ EMTDC software environment. This section of the thesis first defines each simulation scenario and then presents the obtained results and justifies them. It must be mentioned that the case studies aim to subject the test system to difficult conditions to evaluate its responses and are not necessarily

similar to real-time scenarios.

The aforementioned case studies can be divided in two main groups, i.e., normal conditions, and operation under fault conditions, all of which are further explained here.

### 4.3.1 Case 1: Converter Operating Under Normal Conditions

Normal conditions refers to the operation of the converter in ideal or non-ideal conditions while connected to an ideal or non-ideal grid, and without any ac- or dc-side faults. The normal operation of the converter includes various steady-state and transient scenarios, including the start-up transient studies, dc-voltage level change, change of the external power, and the change of the reactive power exchanged between the converter and the grid.The aforementioned are explained in the upcoming subsections.

#### Case 1.1: Start Up

This case study demonstrates the response of the converter to the start-up process. As can be seen from Fig. 4.1, the proposed converter consist of 8 capacitors (as it was previously mentioned the dc-side capacitor of the proposed converter is modeled as a series connection of two caacitors), all of which are fully discharged prior to starting simulations and the start-up transient refers to transient conditions during which all of the capacitors in the proposed converter get charged. Hence, the start-up process of the converter aims to rise the capacitor voltages to their rated values [60] and skipping this stage will result in drawing too much current from the grid and overshoot in the capacitors' voltages, and thus putting extra stress on the converter. As a result, it can be concluded that the start up procedure must be designed to decrease the speed of the charging process and as a result avoiding the aforementioned stress.

Prior to the start up of the converter the power exchanged between the external-power source and the ac grid is zero, the gating signals of the voltage-sourced converter are blocked, all the controllers are inactive, and the breaker connecting the converter to the ac grid at the point of common coupling is at open state. As it is mentioned in [60], the pre-charging scheme of the capacitors consists of "uncontrolled rectifier" and "constant dc-voltage control" stage. During the former, the power is transferred from the ac grid to the converter to pre-charge the capacitors, while the latter stage is used to unblock the converter and its controllers. Thus, the first operation step of the proposed converter is to connect it to the host ac grid and charging up the capacitors inside the converter, i.e., the un-controlled rectifier start-up stage. Initially, the breaker at PCC, referred to as $BRK1$ in Fig. 4.2, and $BRK3$ close and $BRK2$ opens, which in turn establishes the connection between the converter and the ac grid through the high resistive path. The resistance of the aforementioned path is presented with $R_{st}$ in Fig. 4.2 and is chosen equal to 0.03 Ω. Employing the start-up resistance limits the current drawn from the grid for charging up the capacitors and leads to a smoother start-up procedure. As it can be seen from Fig. 4.19 during the uncontrolled rectifier stage a maximum current of about 380 $A$ is drawn from the converter, i.e., the converter won't face any over-current issues at this stage, and the capacitors will charge up to the peak line-to-line value of the ac-side voltage (293 $v$). Then, at $t = 0.08$ $s$ the controllers and gating signals are unblocked, while the value of reference dc-side voltage keeps to gradually increase to 380 $v$. It must be mentioned that during the start-up procedure no power is transferred between the external power source and converter.

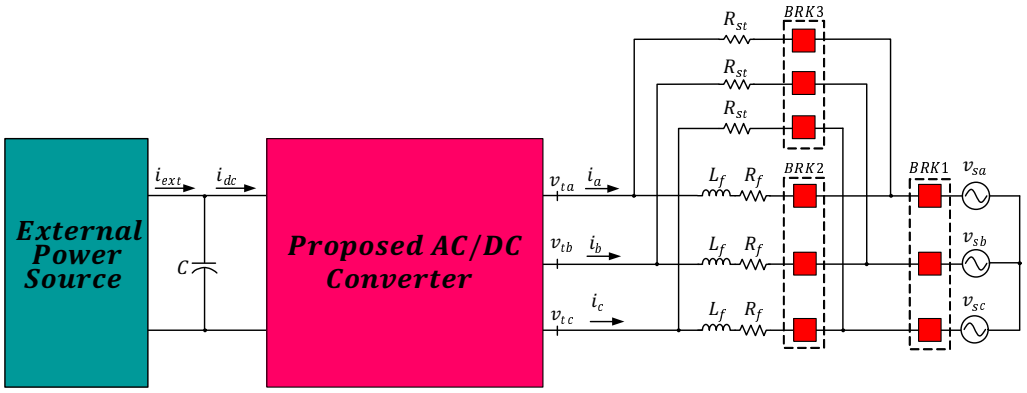


Figure 4.2: Schematic diagram of the proposed converter, along with the start-up resistors and breakers

At $t = 0.07$ the gating signals are unblocked, all controllers are activated, while at the same time the reference value of the dc-side voltage is slowly increasing to reach its final value or 0.38 $kV$. The aforementioned increase in the reference value of the dc-side voltage must be done slowly in order to achieve a clean $v_{dc}$ and avoid over-voltage stresses on the capacitors. Moreover, it must be mentioned that the starting point of the ramp of the reference value of the dc-side voltage at the moment of unblocking the gating signals must have a value around the magnitude of the pre-charged voltage of the capacitors. At about $t = 0.15$ $s$, the dc-side voltage of the converter and the voltage of the capacitors at the dc side of the FBSMs are regulated at their steady-state values, i.e., $v_{dc}^{*} = 0.38$ $kV$, as presented in Fig. 4.3, and the values of the active and reactive power transferred to the grid at the point of common connection drops to zero. Figure 4.4 and 4.5 present the dynamic response of the dc- and ac-side currents and modulating signals of the converter achieved during the start-up procedure while Fig. 4.6 presents the $P_{ext}$, reference and actual values of the active and reactive power exchanged between the converter and ac grid during the aforementioned scenario.

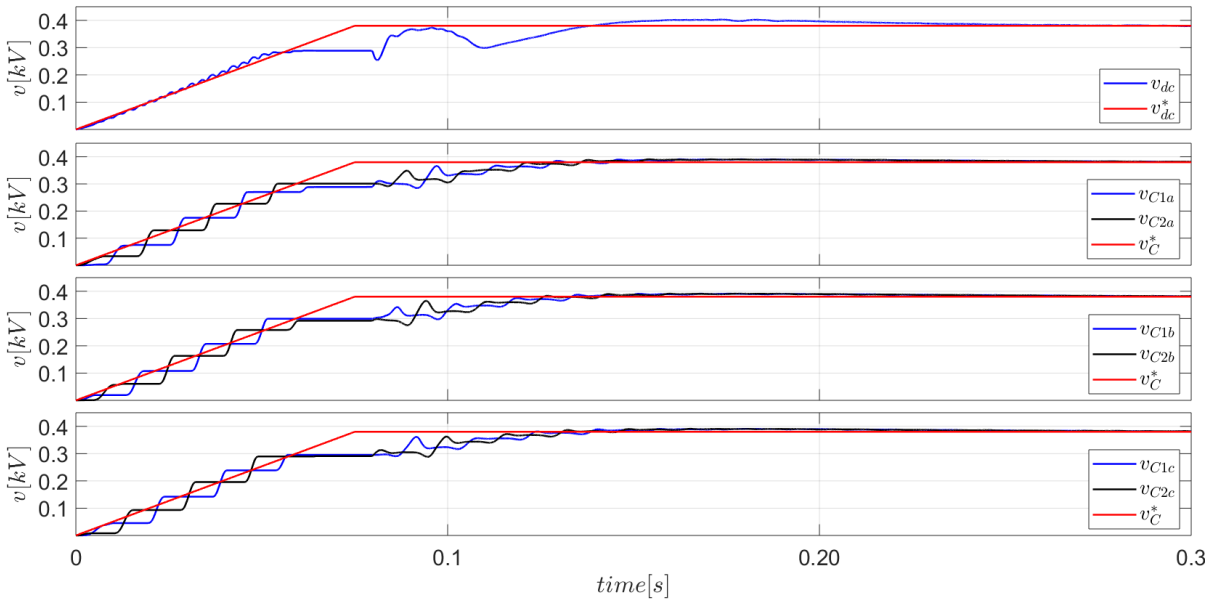


Figure 4.3: Dynamic response of the dc-side voltage of the converter and the FBSMs during the start-up procedure under ideal conditions.

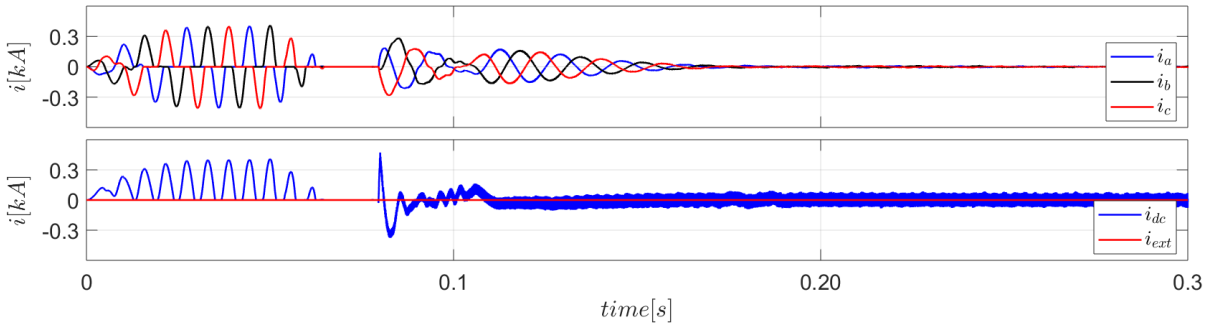


Figure 4.4: Dynamic response of the dc- and ac-side currents during the start-up procedure of the proposed converter under ideal conditions

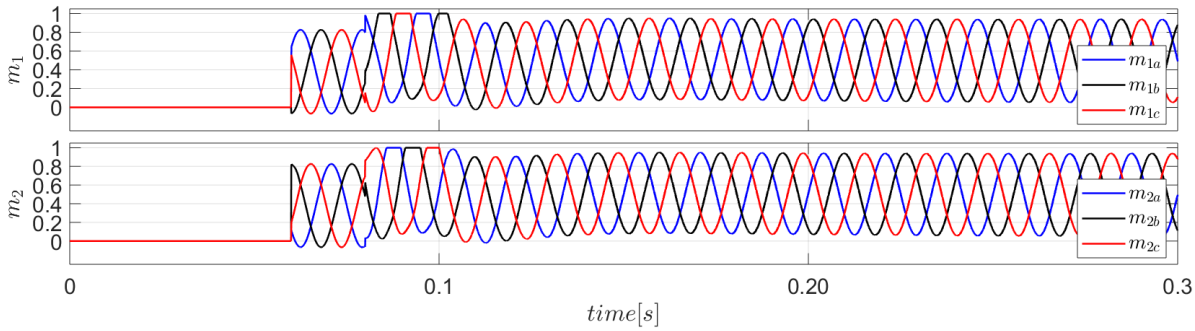


Figure 4.5: Modulating signals of the FBSMs of the converter during the start-up procedure of the proposed converter under ideal conditions

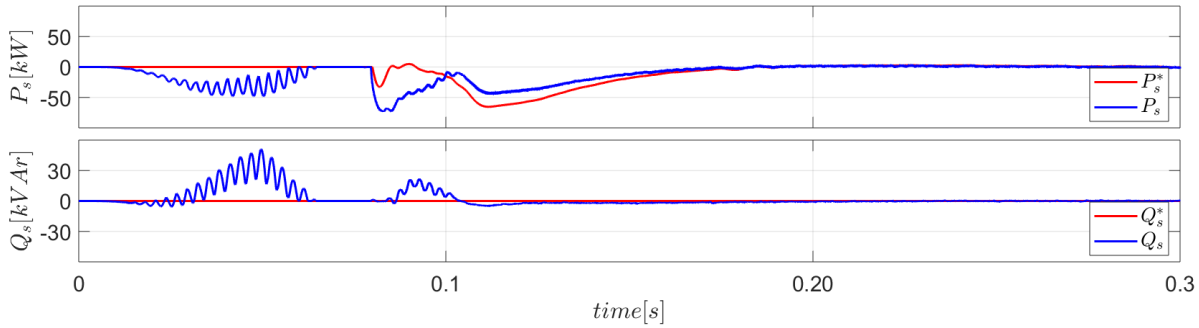


Figure 4.6: Dynamic response of the $P_{ext}$, $P_s$, $P_s^*$, $Q_s$, and $Q_s^*$ during the start-up procedure of the proposed converter under ideal conditions

**Case 1.2: DC-Voltage Reference Level Change**

As it was discussed in previous chapters, the converter employs dc-side voltage controllers, for the capacitor at the dc-side of the main converter and the capacitors at the dc-side of each FBSM. Hence, the focus of this case is to analyses the response of the converter to changes in its reference dc voltage and to evaluate the effectiveness of the proposed control methodology while subjected to changes in the dc-side voltage. In this study, after the converter reaches the steady-state conditions, at $t = 0.45\ s$, the reference value of the dc-side voltage increases by 20%. Figures 4.7 to 4.10 present the results obtained by simulating the converter under the mentioned scenario. The achieved results are further explained here.

During the steady-state conditions of the converter, the power balance is achieved and thus the power exchanged between the converter and the grid is almost equal to the value of the external power. However, as it can be seen increasing the reference value of the dc-side voltage leads to a sudden drop in the value of the reference active power exchanged with the grid and makes it negative which means that now the current is traveling from the ac gird to the converter. The sudden change in the direction of the current will charge up the capacitors to their new reference value. Once the capacitors reach their new steady-state voltage, $P_s^*$ starts to increase and the power balance will be achieved again. As it can be seen from the results, the transient period for changing the reference value of the dc-side voltage is about 0.05 $s$. Next step would be to confirm the effectiveness of the control methodology while operating under the new dc-side voltage. To do so, at $t = 0.6\ s$ the external power drops to $-160\ kW$, and once the converter reaches the steady state, at $t = 0.75\ s$ the reference value of the reactive power changes from 0 to 100 $kVAr$. Furthermore, $t = 0.95\ s$ the reference value of the reactive power drops from 100 to $-100\ kVAr$. As it can be seen from Fig. 4.7 to 4.10 the designed controllers can effectively control the converter under the aforementioned scenario.

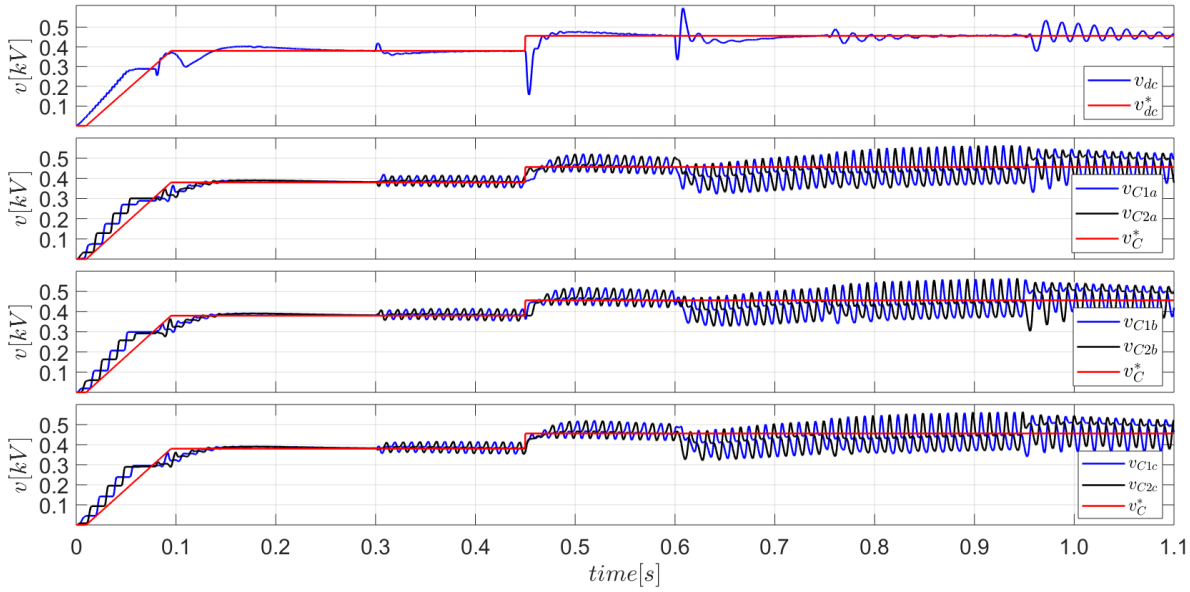


Figure 4.7: Dynamic response of the dc-side voltage of the converter and the FBSMs while facing changes in their reference values under ideal conditions.

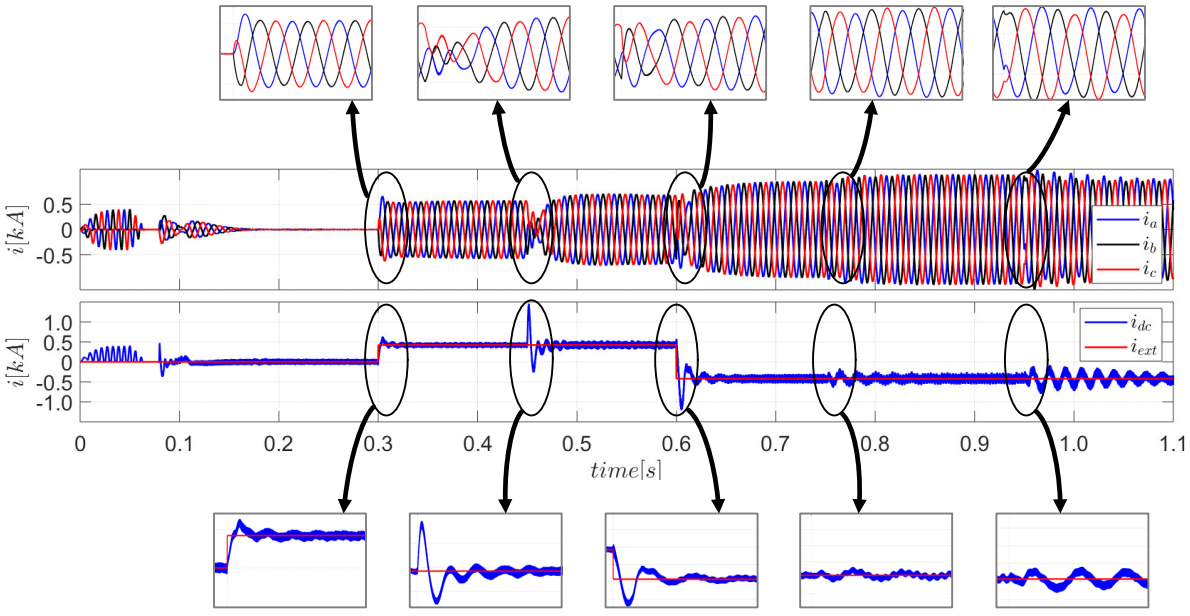


Figure 4.8: Dynamic response of the dc- and ac-side current while facing changes in $v_{dc}^*$ under ideal conditions

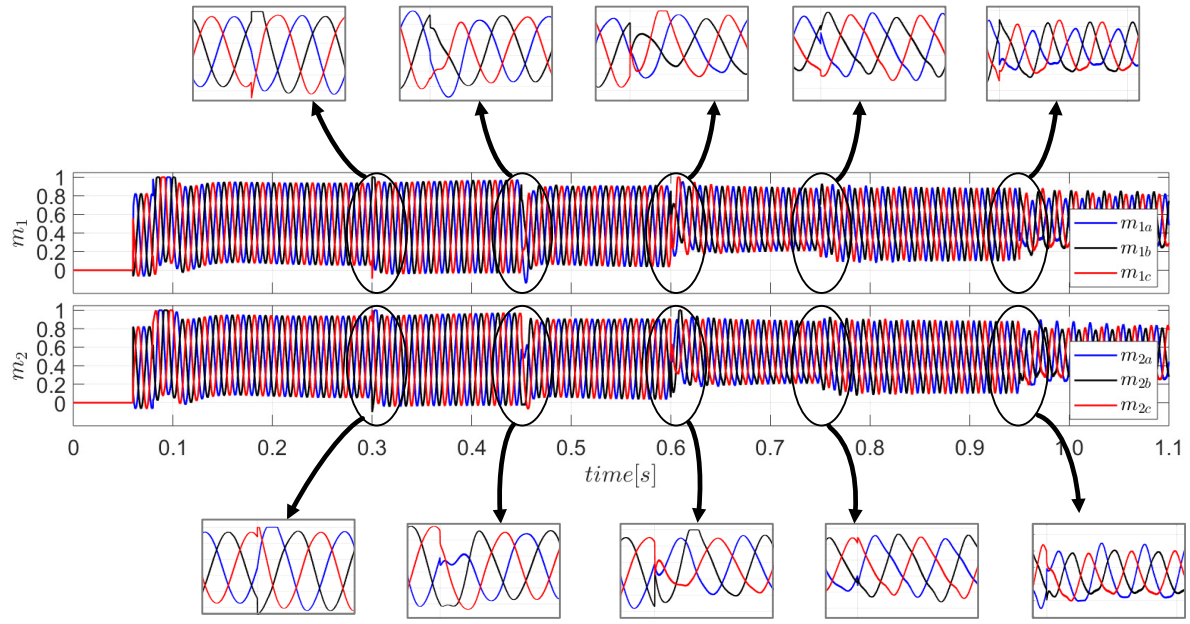


Figure 4.9: Modulating signals of the FBSMs of the converter while facing changes in $v^*_{dc}$ under ideal conditions

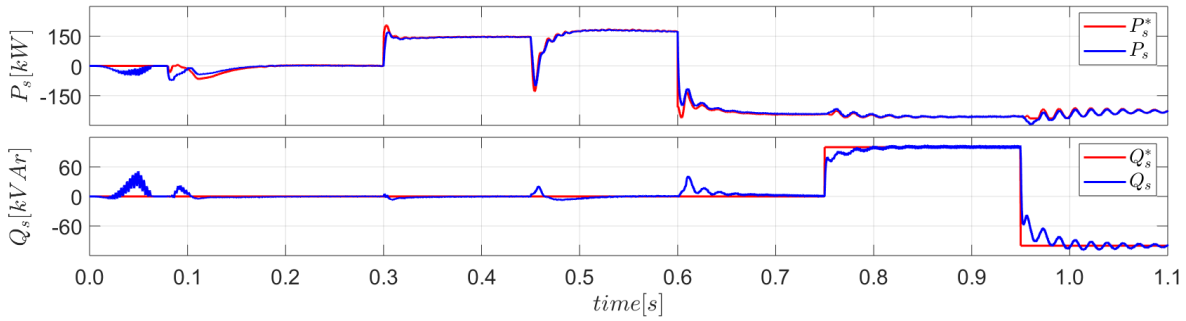


Figure 4.10: Dynamic response of the $P_{ext}$, $P_s$, $P^*_s$, $Q_s$, and $Q^*_s$ while facing changes in $v^*_{dc}$ under ideal conditions

### Case 1.3: Change of the Value of the External Power

Initially, the dc power source connected to the dc side of the converter is inactive, that is $P_{ext} = 0\ kW$. At this condition and once the converter reaches its steady-state operation the value of the $P_s$ assumes a small value which corresponds to the power loss of the converter. However, as it was previously mentioned, the external power source is not controllable through the converter. As a result, it is very important to analyze the response of a converter to the sudden changes in the $P_{ext}$. To achieve the aforementioned, at $t = 0.3\ s$, the external power transferred to the converter from the dc power source is changed step-wise from 0 to $-160$ $kW$. As it can be seen from Fig. 4.11, at this time the dc-side voltage has an undershoot which makes the controllers to react and drop $P^*_s$. Once the converter reaches its steady-state operation again, at $t = 0.45\ s$, the external power has another step-wise change, this time

from $-160\ kW$ to $160\ kW$. The aforementioned change causes an overshoot to the dc-side voltage, which in turn leads to an overshoot in $P_s^*$ in order to reduce the dc-side voltage. It must be mentioned that the dc-bus controller designed in Chapter 3, employs a feed-forward compensation of the external power which rapidly communicates any changes in $P_{ext}$ to $P_s^*$. Figure 4.11 also presents the dynamic response of the dc-side voltages of the FBSMs available in each leg of the converter. As it can be seen from the figure, once the external power changes from $0\ kW$ the upper and lower capacitors in each leg start to partially charge and discharge, respectively, or vice versa. The aforementioned process is controlled by the ac-component of the common-mode current and as a result the average dc-side FBSMs voltages are regulated at their desired values. Figure 4.12 illustrates the ac-side current of the converter. As it can be seen from the aforementioned figure that the ac-side current of the proposed converter is a clean sinusoidal current with fast transient response. Furthermore, the modulating signals of the FBSMs in the upper and lower arms of the converter are shown in Fig. 4.13. As it was previously mentioned in Chapters 2 and 3 the modulating signal consists of two components: The common-mode and differential-mode modulating signals. The aforesaid can be seen from Fig. 4.13, since each modulating signal has an ac component and a dc offset, corresponding to the differential- and common-mode modulating signal, respectively.

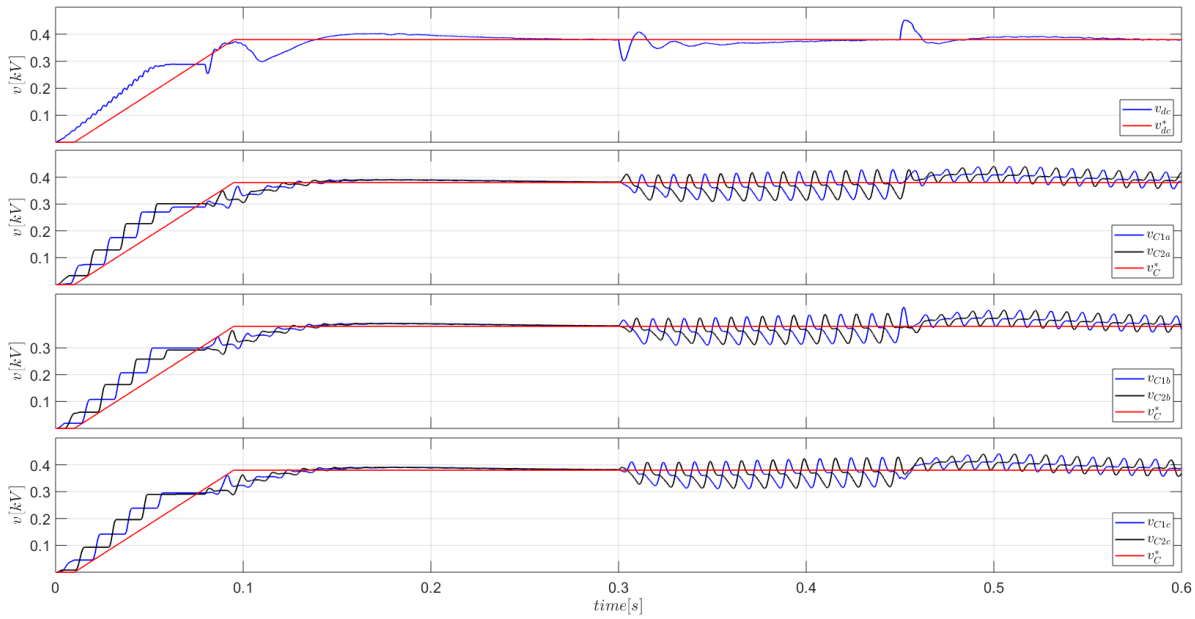


Figure 4.11: Dynamic response of the dc-side voltages of the converter and its FBSMs while facing changes in the external power under ideal conditions

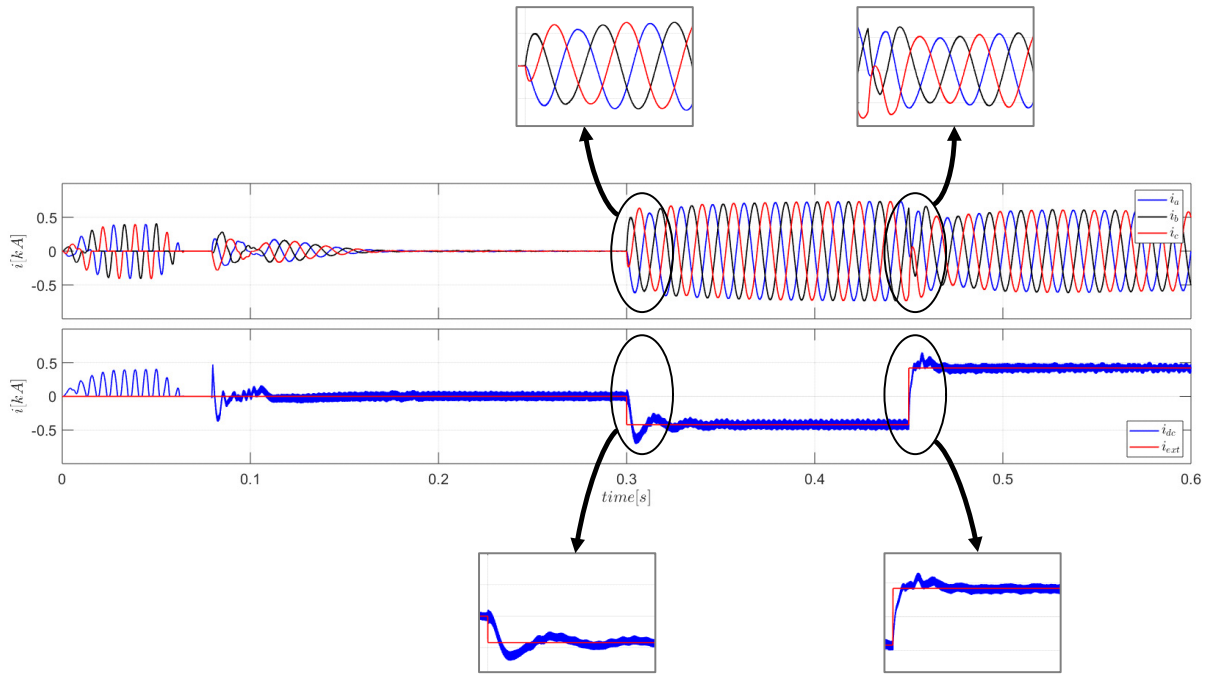


Figure 4.12: Dynamic response of the dc- and ac-side current while facing changes in the external power under ideal conditions

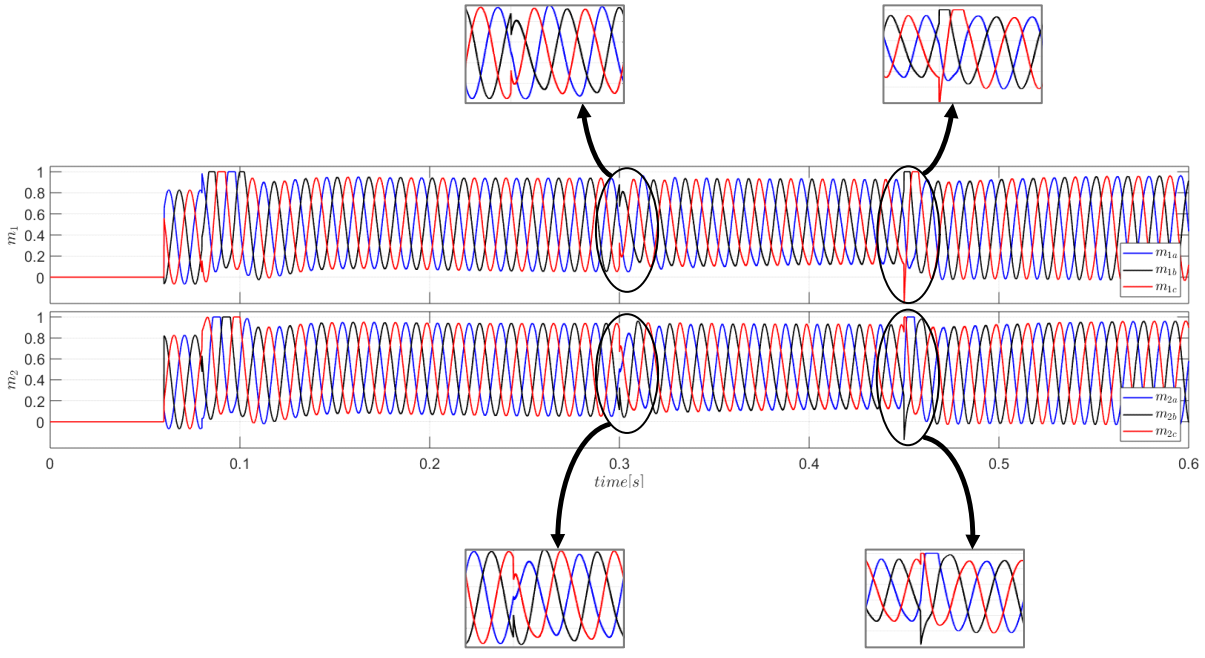


Figure 4.13: Modulating signals of the FBSMs of the converter while facing changes in the external power under ideal conditions

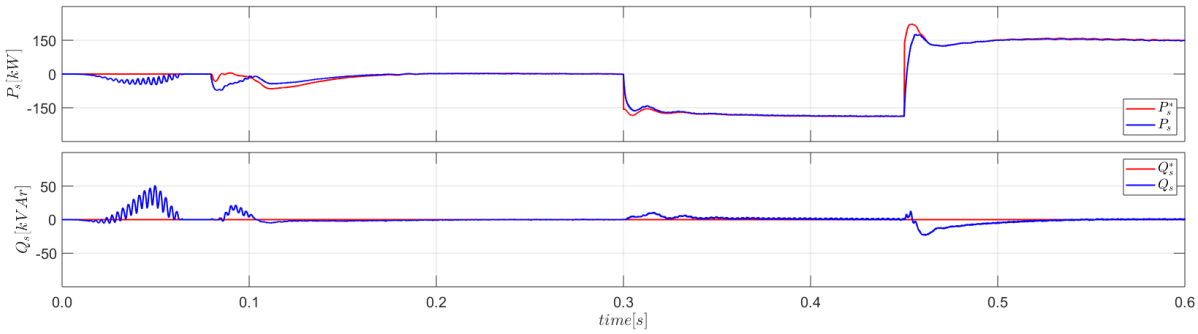


Figure 4.14: Dynamic response of the $P_{ext}$, $P_s$, $P_s^*$, $Q_s$, and $Q_s^*$ while facing changes in the external power under ideal conditions

**Case 1.4: Change of The Reactive Power Exchanged Between the Converter and AC Grid**

As it was previously mentioned, one of the advantages of the proposed converter is its ability to independently control the reactive power exchanged between the converter and ac grid can be independently controlled. Thus*Case 1.4* is dedicated to analyzing the transient and steady-state response of the converter while faced with changes in the reactive power exchanged between the converter and the ac grid. During Case 1.4, $P_{ext}$ and consequently $P_s$ is kept constant. Initially, the dc power source connected to the dc side of the converter is inactive and the reference value of the reactive power transferred to the grid, $Q_s$ is set to zero. After the successful startup of the converter, and once all the capacitors are fully charged first the external power source connected to the dc side of the converter is activated at $t = 0.25\ s$ and $P_{ext}$ changes from 0 to $-160\ kW$. The effect of the aforementioned was analyzed in the previous section. Once the converter reaches steady-state conditions, at $t = 0.4\ s$, the reference value of the reactive power transferred to the grid assumes a step-wise change from 0 to $-100\ kVAr$ While $P_{ext}$ is kept constant, as shown in Fig. 4.18. After a small transient, the converter reaches its new steady-state operation. Then, at $t = 0.6\ s$ the reference value of the reactive power has another step change from $-100\ kVAr$ to $100\ kVAr$. The dc-side voltage of the converter and the dc-side voltage of the FBSMs are presented in Fig. 4.15. Furthermore, Fig. 4.16 and 4.17 show the dc- and ac-side currents of the converter and the modulating signals of the FBSMs for the during obtained from simulating the converter under the conditions described as Case 1.4 in PSCAD/EMTDC software environment, respectively.

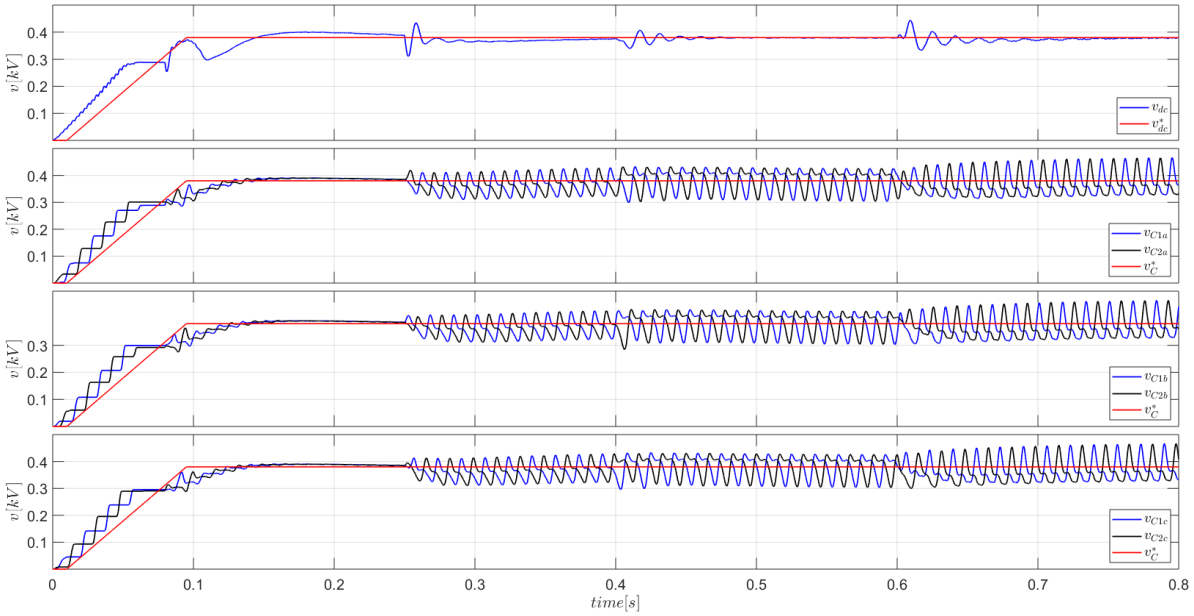


Figure 4.15: Dynamic response of the dc-side voltages of the converter and the FBSMs while facing changes in the reference value of the reactive power exchanged with the grid under ideal conditions

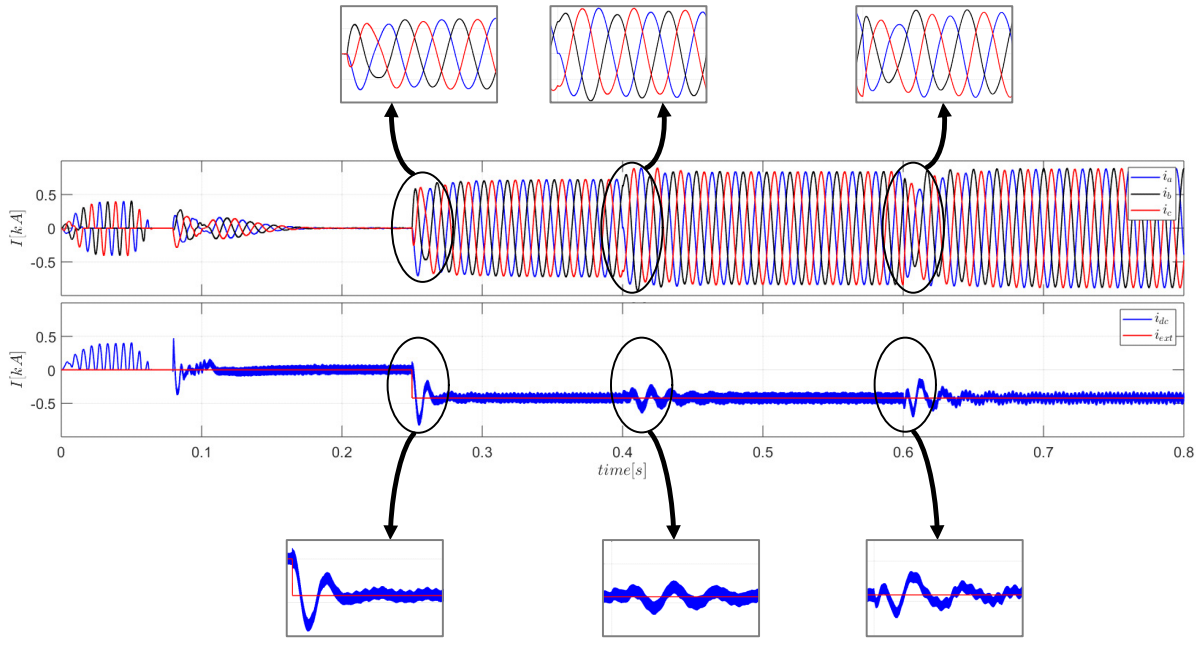


Figure 4.16: Dynamic response of the dc- and ac-side current while facing changes in the reference value of the reactive power exchanged with the grid under ideal conditions

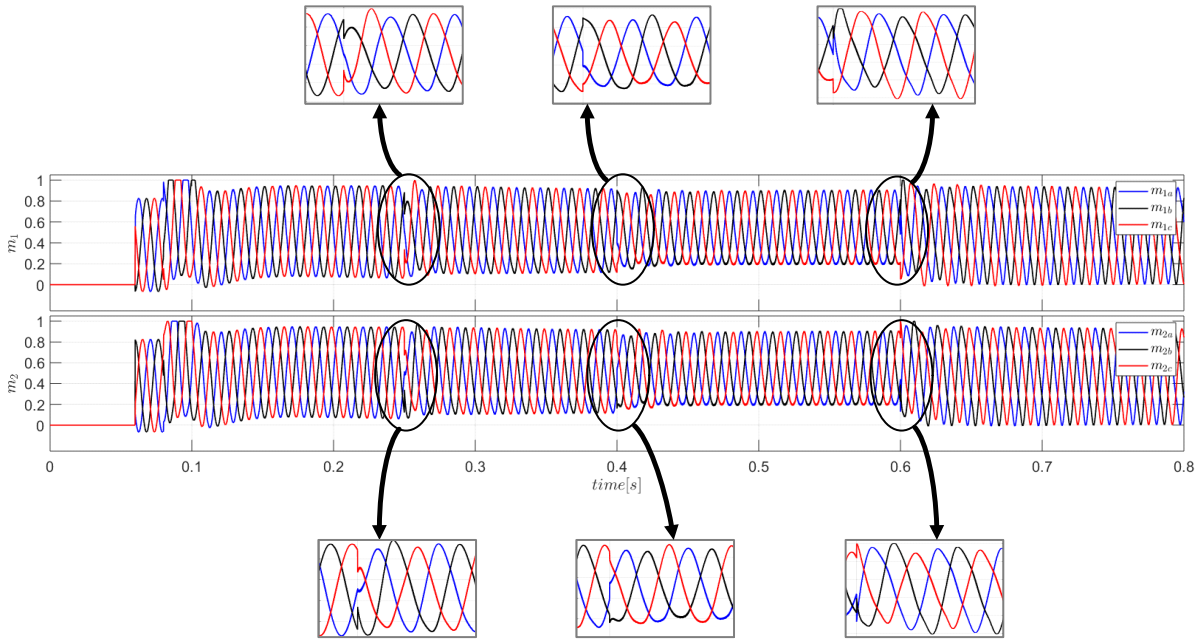


Figure 4.17: Modulating signals of the FBSMs of the converter while facing changes in the reference value of the reactive power exchanged with the grid under ideal conditions

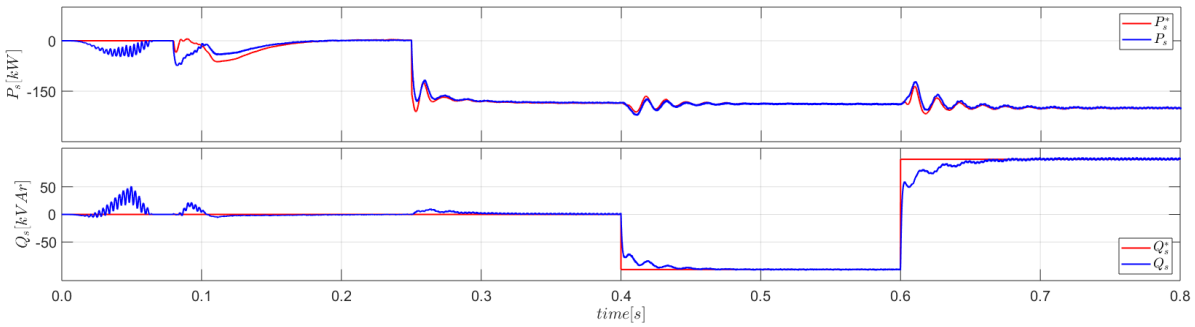


Figure 4.18: Dynamic response of the $P_{ext}$, $P_s$, $P_s^*$, $Q_s$, and $Q_s^*$ while facing changes in the reference value of the reactive power exchanged with the grid under ideal conditions

### 4.3.2 Case 2: Non-Ideal Conditions

In the normal operating scenarios, it was assumed that both the converter and the grid are ideal. However, in actual applications the aforementioned is not achievable. Thus, during the course of this research special attention were paid to simulating the converter under more practical situations, which can be divided in two groups:

1. Un-ideal converter
2. Un-ideal ac grid

Each of the above scenarios and the results obtained by simulating the converter in PSCAD/EMTDC software environment are explained in more details in this section section.

**Case 2.1: Non-Ideal Converter**

It is a well-known fact that no two component available in the market are exactly the same. Thus, in order to prove the stable operation of the converter in real applications, the control topology must be able to function sufficiently in spite of any noise or disturbances. In *Case 2.1*, the effects of asymmetry in the proposed converter is examined. The aforementioned is done by paralleling a resistor with the dc-side capacitor of a random FBSM in the converter, denoted hereinafter by $R_c$. Fig. 4.19 shows the schematic diagram of the proposed converter under asymmetric condition. The resistance value of the $R_c$ is chosen equal to 30 Ω.

Figure 4.20 to 4.23 present the results obtained while simulating the non-ideal converter. As it can be seen from the fig. 4.23 initially the power exchanged with the grid is set to zero, and the capacitors are charged through the grid, following the same procedure previously explained in Section 4.3.1. At $t = 0.3\ s$ the external power has a step-wise change from 0 to $-160\ kW$, which causes an undershoot in the dc-side voltage, as presented in Fig. 4.20, this in turn makes the compensators to react and drop the $P_s^*$. Then, once the converter reaches the steady-state operation again, at $t = 0.45\ s$, the external power is changed from $-160\ kW$ to $160\ kW$, and leads to an overshoot in the dc-side voltage. In order to bring the dc-side voltage back to its reference value the $P_s^*$ also experiences an overshoot.

At $t = 0.6\ s$ and $t = 0.8\ s$, $Q_s^*$ has two step-wise changes from 0 to 100 $MVAr$ and from 100 $MVAr$ to $-100\ MVAr$, respectively. However, these changes have no significant effect on the dc-side voltages, which can be explained by using the following equation, which was previously discussed in Chapter 2. As it can be seen from (4.1), the contribution of $Q_s$ on $\frac{dv_{dc}^2}{dt}$ has a weight of $\frac{2}{C}\frac{2L'}{3\hat{v}_s^{\,2}}$, which is typically small.

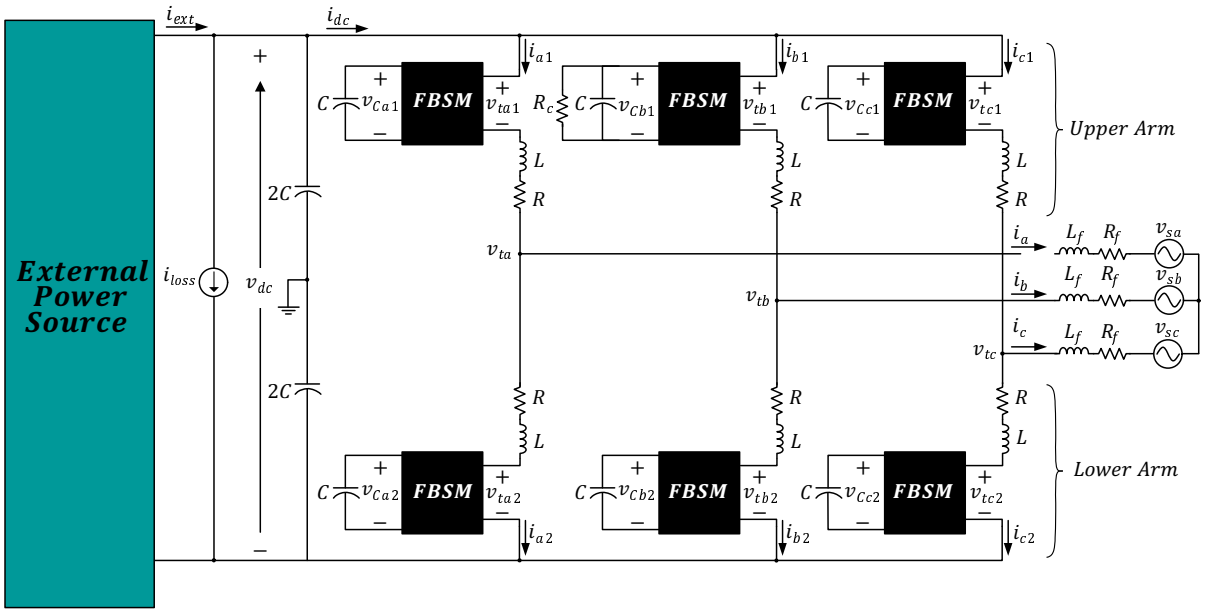


Figure 4.19: Schematic diagram of the proposed ac/dc converter under asymmetric condition.

$$\frac{dv_{dc}^2}{dt} = \left(\frac{2}{C}\right)P_{ext} - \left(\frac{2}{C}\right)P_{loss} - \left(\frac{2}{C}\right)\left[P_s + \left(\frac{2L'}{3\hat{v}_s^{\,2}}\right)P_s\frac{dP_s}{dt}\right] - \left(\frac{2}{C}\right)\left(\frac{2L'}{3\hat{v}_s^{\,2}}\right)Q_s\frac{dQ_s}{dt} \tag{4.1}$$

Figures 4.21 presents the ac-side current of the converter. As it can be seen from this figure, the current is a clean sinusoidal current with short transient periods, in spite of the asymmetry in the converter itself.

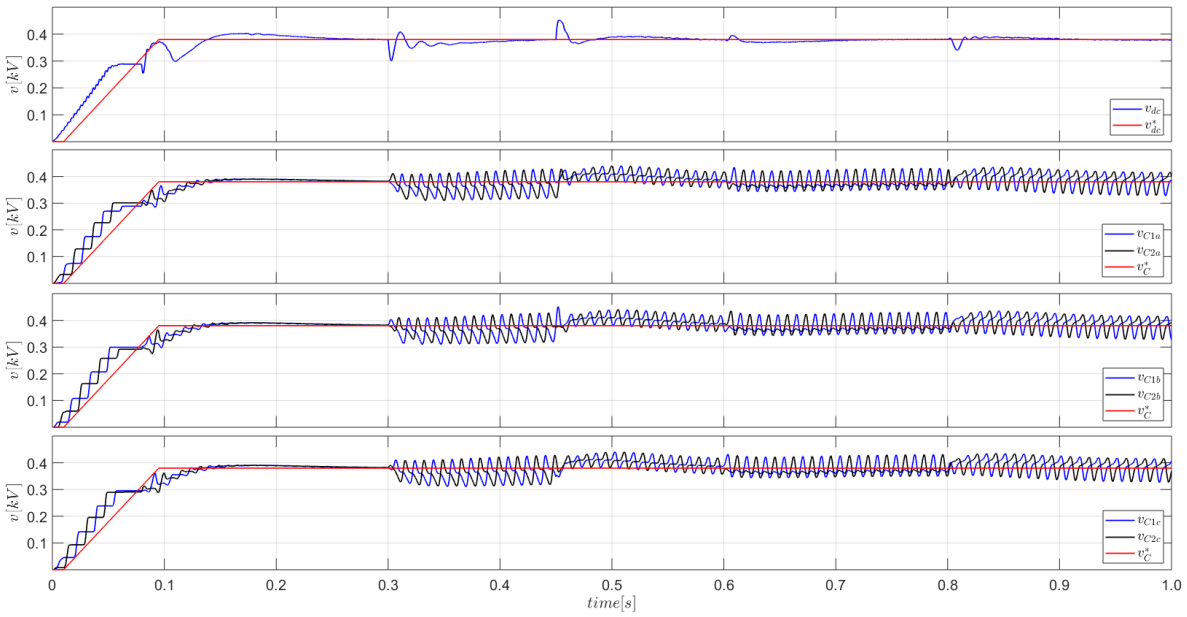


Figure 4.20: Dynamic response of the dc-side voltages of the proposed converter and its FB-SMs of the non-ideal converter while facing changes in external power at the dc-side and reference reactive power at PCC.

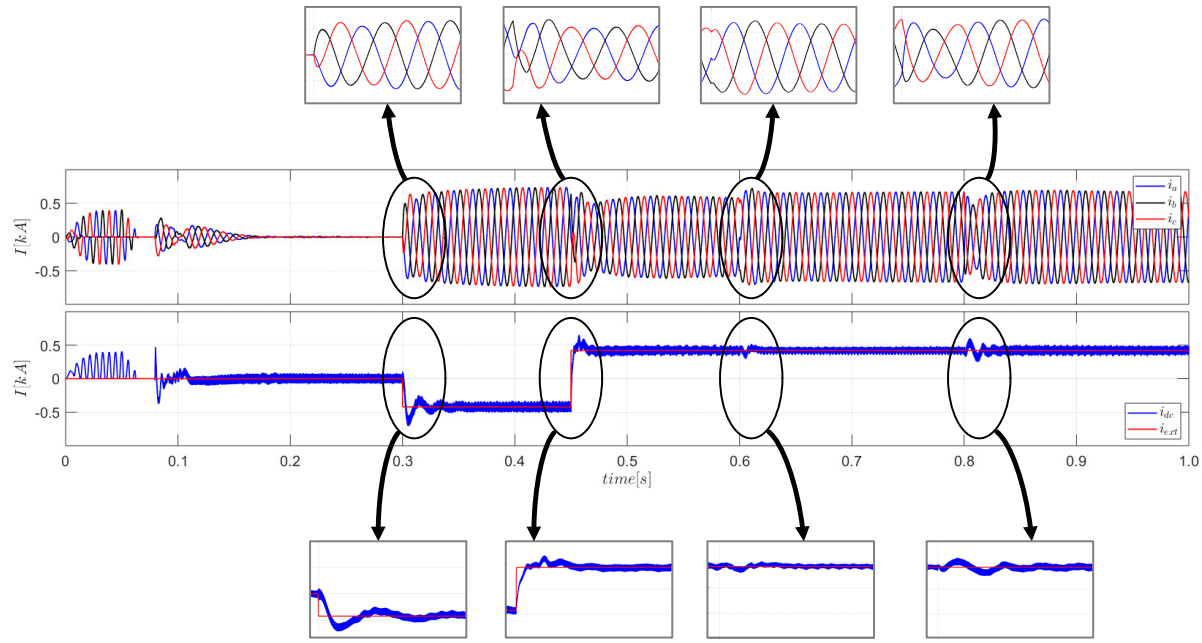


Figure 4.21: Dynamic response of the dc- and ac-side current of the non-ideal converter while facing changes in external power at the dc-side and reference reactive power at PCC.

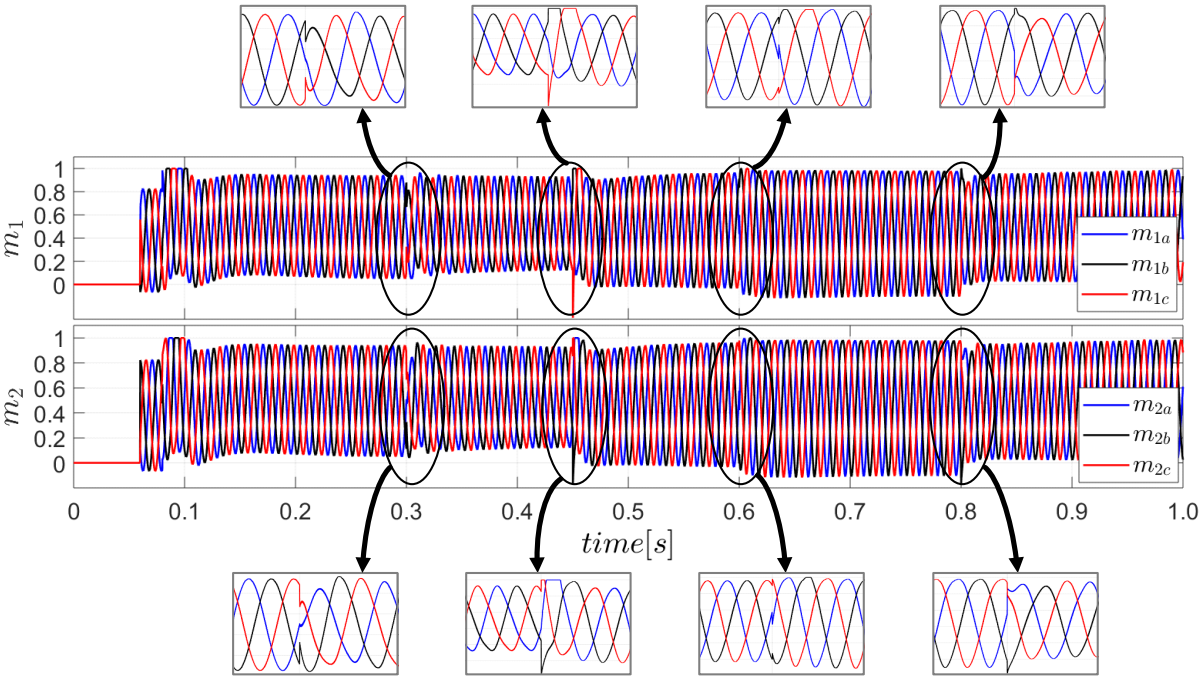


Figure 4.22: Modulating signals of the FBSMs of the non-ideal converter while facing changes in external power at the dc-side and reference reactive power at PCC.

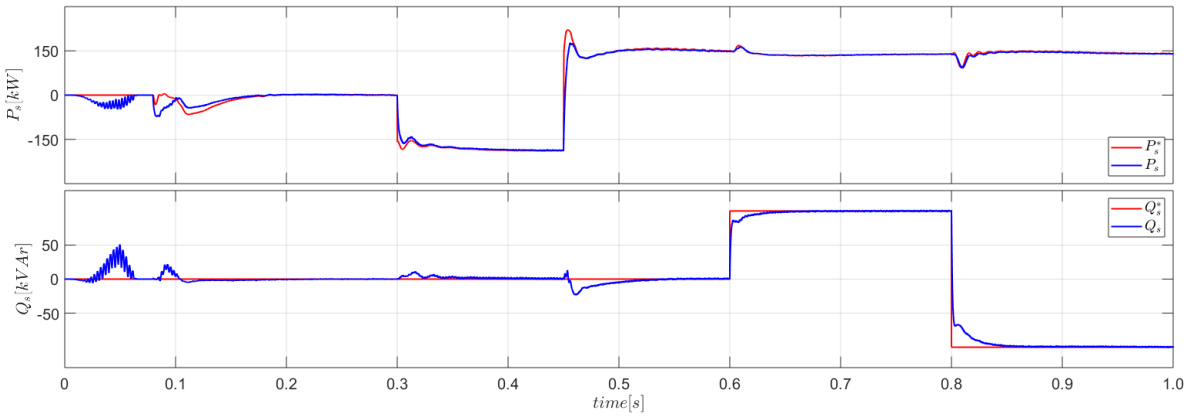


Figure 4.23: Dynamic response of the $P_{ext}$, $P_s$, $P_s^*$, $Q_s$, and $Q_s^*$ of the non-ideal converter while facing changes in external power at the dc-side and reference reactive power at PCC.

### Case 2.2: Non-Ideal Grid

During all the previous cases, it was assumed that the converter was connected to an ideal grid at its ac side. However, in order to simulate the converter under more accurate scenarios, *Case 2.2* assumes that the converter is connected to a non-ideal ac grid, which can be modeled by an ideal ac voltage source connected to a series RL branch, corresponding to the impedance of the grid and denoted by $L_g$ and $R_g$. it must be mentioned that $L_g$ represents the inductance of not only the line but also any interface transformer (not presented in the figure). The connection between the non-ideal grid and the proposed converter is done at the point of common coupling (PCC), and its voltage is referred to as $v_{sabc}$. In contrary to the ideal grid model, which could be connected to the converter via a simple series RL branch, in order to be able to achieve clean sinusoidal output while connecting the proposed converter to a non-ideal grid, an inductor-capacitor (LC) filter has been chosen. The presence of the shunt capacitors, hereinafter denoted by $C_f$, will provide a path for the high frequency harmonics of the current and prevents them from penetrating in to the ac grid. However, the aforementioned will introduce the resonant problem to the system and thus there will be a need for damping in the converter, which can be done through active or passive method. For the purposes of this thesis a passive damping using damping resistors, referred to by $R_{fd}$ hereinafter, was proven sufficient and is put in series with the shunt capacitors and used to suppress the resonance of the used LCL filter at the ac side of the converter which consists of the aforementioned LC filter and the inductance of the ac grid. Figure 4.19 shows the schematic diagram of the proposed converter connected to a non-ideal grid through the discussed LC filter.

Figures 4.24 to 4.27 present the results of simulating the converter, while connected to a non-ideal grid, in the PSCAD/EMTDC software environment. Similar to previously discussed scenarios, at $t = 0\ s$ the controllers are blocked, and the converter is connected to the grid through the high-resistive path, and the start-up procedure begins. Once the dc-side voltages of the capacitors are charge to peak line-to-line value of the ac-side voltage they remain steady until the controllers unblock, which will allow the capacitors to get fully charged. At $t = 0.3\ s$, which is sufficient enough for the converter to reach its steady-state conditions after the start-up procedure, the external power has a step-wise change from 0 to $-160\ kW$, which leads to an

undershoot in the dc-side voltage, and thus the compensators react and drop $P_s^*$. Then after the converter reaches its new steady-state conditions, at $t = 0.45$ the external power has another step-wise change from $-160\ kW$ to $160\ kW$. The aforementioned causes an overshoot in the dc-side voltage of the capacitors, which in turn forces the compensators to react and cause an overshoot in $P_s^*$ in order to regulate the dc-side voltage at its reference value once again. At $t = 0.6$, $Q_s^*$ has a sudden jump from 0 to $100\ kVAr$, after this jump the converter reaches its new steady-state conditions in about $0.05\ s$. Furthermore, at $t = 0.8\ s$ the reference value of the reactive power exchanged with the grid at PCC has another step-wise change from 100 to $-100\ kVAr$. The dc-side voltage of the converter, dc-side voltages of the FBSMs available in the converter, and the external power, $P_s^*$, $P_s$, $Q_s^*$ and $Q_s$ are shown in Fig. 4.24, and 4.27, respectively. Moreover, as it can be seen from Fig. 4.25, the ac-side current of the converter is a clean-sinusoidal current. Figure 4.26 presents the modulating signals achieved for controlling the proposed converter under the scenario described in Case 2.2.

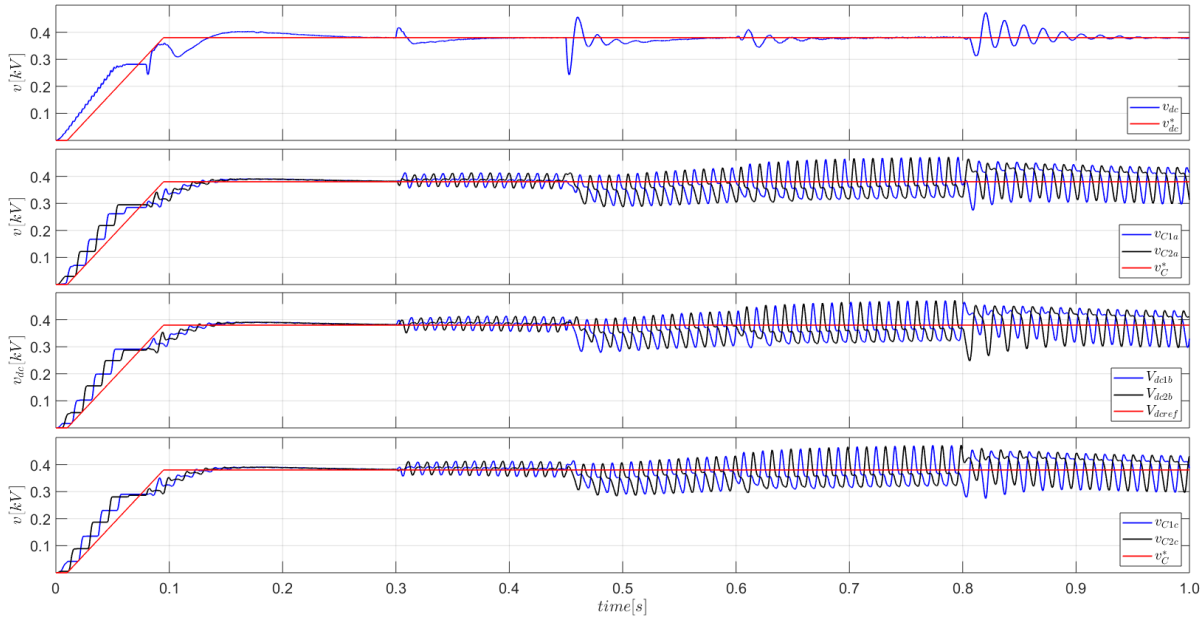


Figure 4.24: Dynamic response of the dc-side voltages of the converter and the FBSMs of the converter, while connected to a non-ideal grid, to the changes in external power at the dc-side and reference reactive power at PCC.

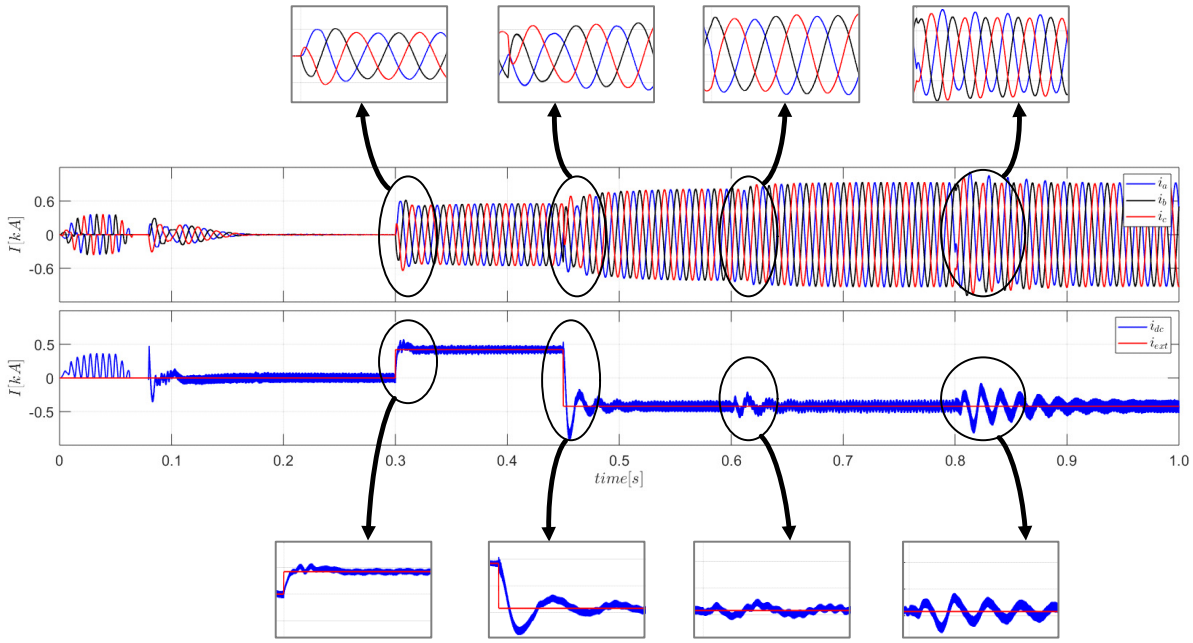


Figure 4.25: Dynamic response of the dc- and ac-side current of the converter, while connected to a non-ideal grid, to the changes in external power at the dc-side and reference reactive power at PCC.

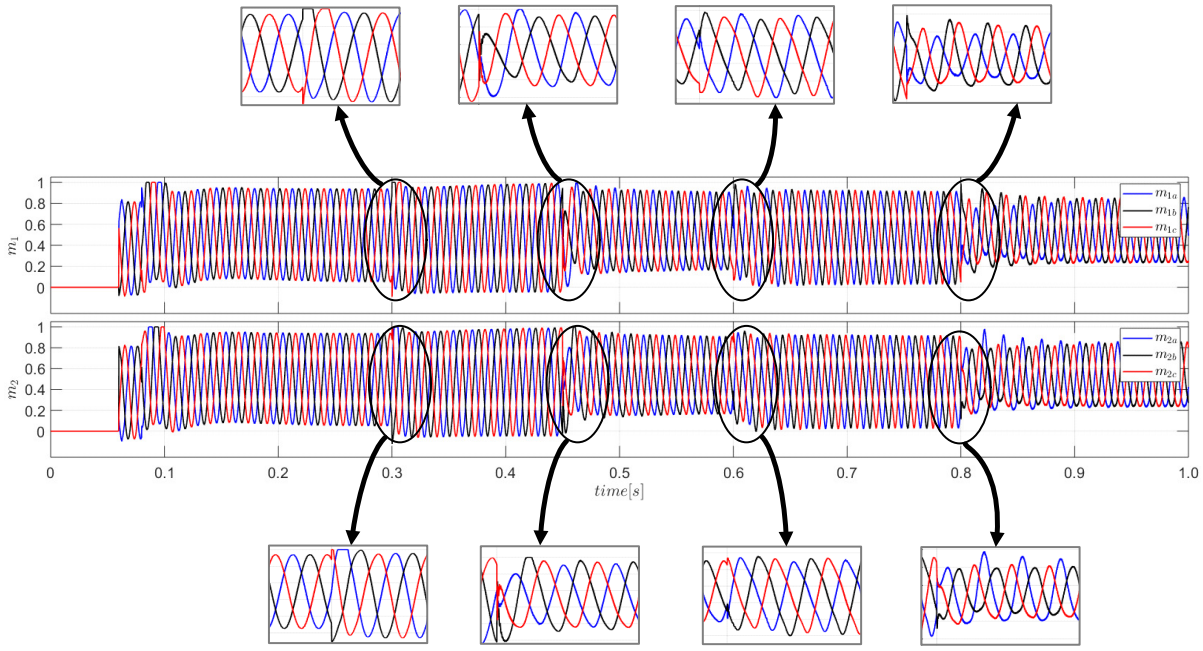


Figure 4.26: Modulating signals of the FBSMs of the converter, while connected to a non-ideal grid, to the changes in external power at the dc-side and reference reactive power at PCC.

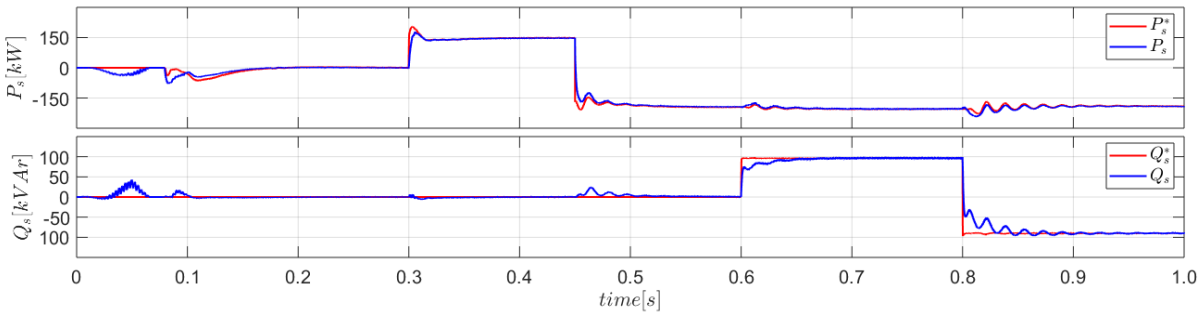


Figure 4.27: Dynamic response of the $P_{ext}$, $P_s$, $P_s^*$, $Q_s$, and $Q_s^*$ of the converter, while connected to a non-ideal grid, to the changes in external power at the dc-side and reference reactive power at PCC.

### 4.3.3 Case 3: Converter Operation Under DC-Side Short Circuit Faults

Cases 1 and 2 focused on the operation of the converter under normal and non-ideal conditions, respectively. As it was mentioned in the previous chapters of this thesis, one of the main advantages of the proposed topology for the bidirectional ac/dc converter, is its tolerance to the dc-side short circuit faults. Thus, in this simulation scenario the converter is subjected to short-circuit fault while operating under steady-state conditions. Once the short-circuit fault occurs, and the dc-side voltage drops below 0.7 *pu* the modulating and signal get blocked. However, in actual applications this cannot be done immediately, and as a result during the simulations a time delay of 15 *ms* between the short-circuit fault and blocking the modulating signals has been considered.

In the following parts of this section, response of the ideal converter, non-ideal converter connected to ideal grid and ideal converter connected to non-ideal ac grid to dc-side short-circuit fault are analyzed and their corresponding simulation results are presented.

#### Ideal Converter Under DC-Side Fault

Figure 4.29 to 4.30 present the results obtained while subjecting the ideal-converter connected to an ideal ac-grid to dc-side short circuit fault at $t = 0.4$ *s*. The dc-side voltage of the proposed converter, shown in Fig. 4.28, drops from its steady-state value, i.e., 380 *v*, to 0 *v* immediately after the fault, which is expected. This sudden drop in the dc-side voltage forces the compensators to react and drop the $P_s^*$, however, the saturation block available in the dc-side voltage controller, which was previously discussed in Chapter 3, prevents it to go lower than $-170$ *kW*, as presented in Fig. 4.31. Furthermore, as it can be seen from Fig. 4.29 as soon as the dc-side fault happens the current starts to increase. However, as it was mentioned before the FBSMs will be turned off with a delay of 15 *ms* after the fault. By turning off the FBSMs their capacitors which were in their steady-state condition and fully charged prior to the fault will be connected in series with the anti-parallel diodes, which in turn leads to turning off the anti-parallel diodes and eliminating the ac-side current contributions to the dc-side fault, illustrated in Fig. 4.29. The modulating signals for this scenario are shown in Fig. 4.26. As it was previously mentioned, in the proposed control topology for the converter the modulating signals also get blocked once the dc-side voltage drops to below 0.7 *pu*, but the tolerance of

the dc-side fault of the converter is irrelevant to this since the gating signals also get blocked and thus regardless of the value of the modulating signals for each FBSMs their switching devices would not be turned on. Figure 4.28 also presents the dc-side voltage of the FBSMs available in the proposed converter. As it can be seen from this figure, during the dc-side short circuit fault the capacitors do not discharge and worsen the situation, whereas they remain fully charged and close to their reference values which then can block the fault current path using the explanation presented earlier in this paragraph.

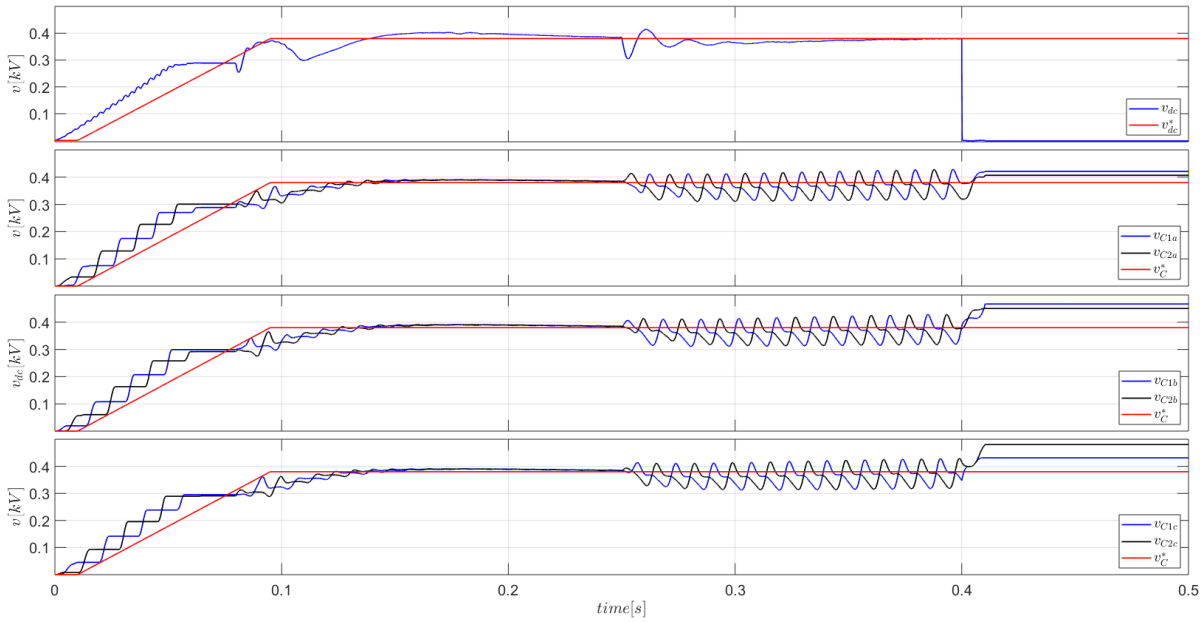


Figure 4.28: Dynamic response of the dc-side voltages of the converter and the FBSMs of the ideal converter, while subjected to dc-side fault.

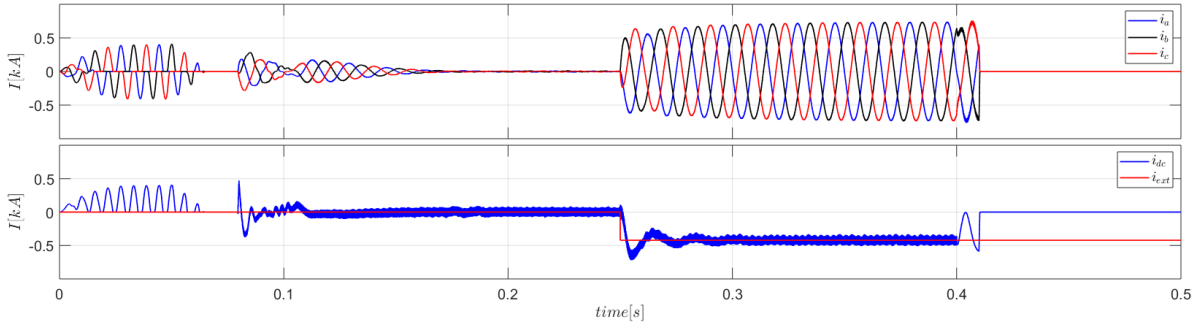


Figure 4.29: Dynamic response of the dc- and ac-side current of the ideal converter, while subjected to dc-side fault.

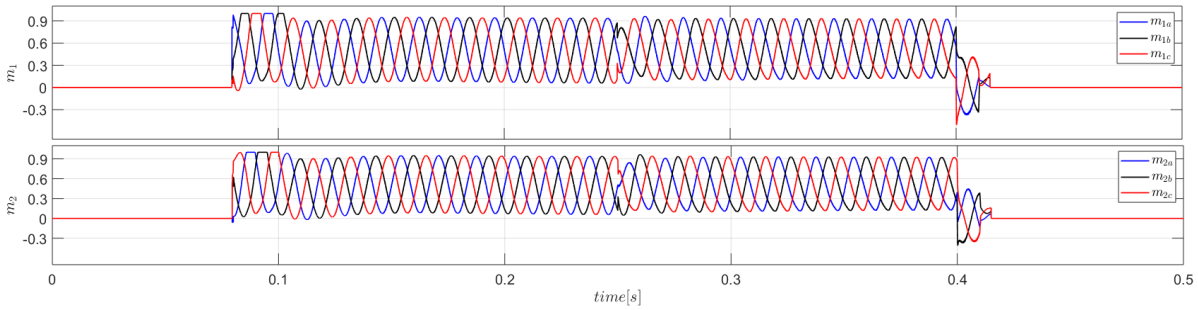


Figure 4.30: Modulating signals of the FBSMs of the ideal converter, while subjected to dc-side fault.

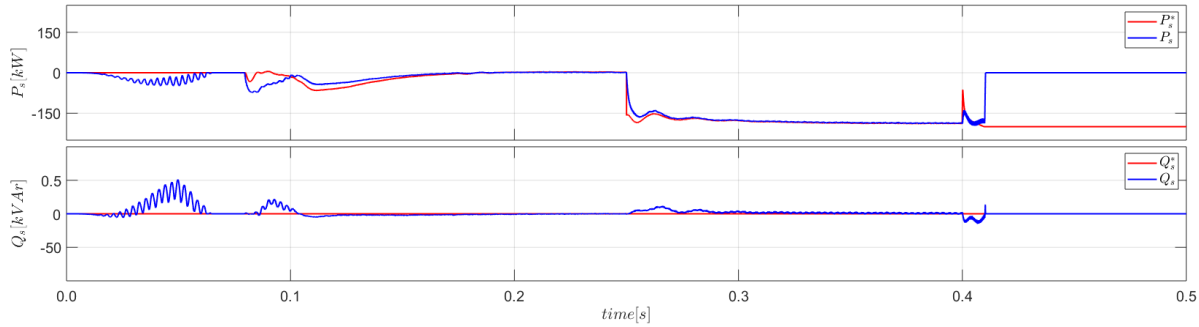


Figure 4.31: Dynamic response of the $P_{ext}$, $P_s$, $P_s^*$, $Q_s$, and $Q_s^*$ of the ideal converter, while subjected to dc-side fault.

### Non-Ideal Converter Under DC-Side Fault

It was previously mentioned in this chapter that in order to evaluate the operation of the converter in more realistic scenarios, it was modeled in non-ideal conditions, where the dc-side capacitor of a random FBSM was paralleled with a resistor. In this part, the aforementioned non-ideal converter was subjected to dc-side short circuit fault and its ability to tolerate the dc-side fault was analyzed.

Figures 4.32 to 4.35 present the dynamic response of the dc-side voltage of the converter, dc-side voltage of the FBSMs, ac-side currents, modulating signals of the FBSMs, and actual and reference values of the powers exchanged between the converter and dc and ac grid, respectively. As it can be seen illustrated from the figures, upon occurrence of a dc-side fault, the gating signals of the switches available in the converter are blocked, and the dc-side capacitors of the FBSMs are put is series with the anti-parallel diodes, and the path for the ac-side current to contribute to dc-side fault is blocked. In another word the results prove that the non-ideal converter has the ability to tolerate dc-side faults.

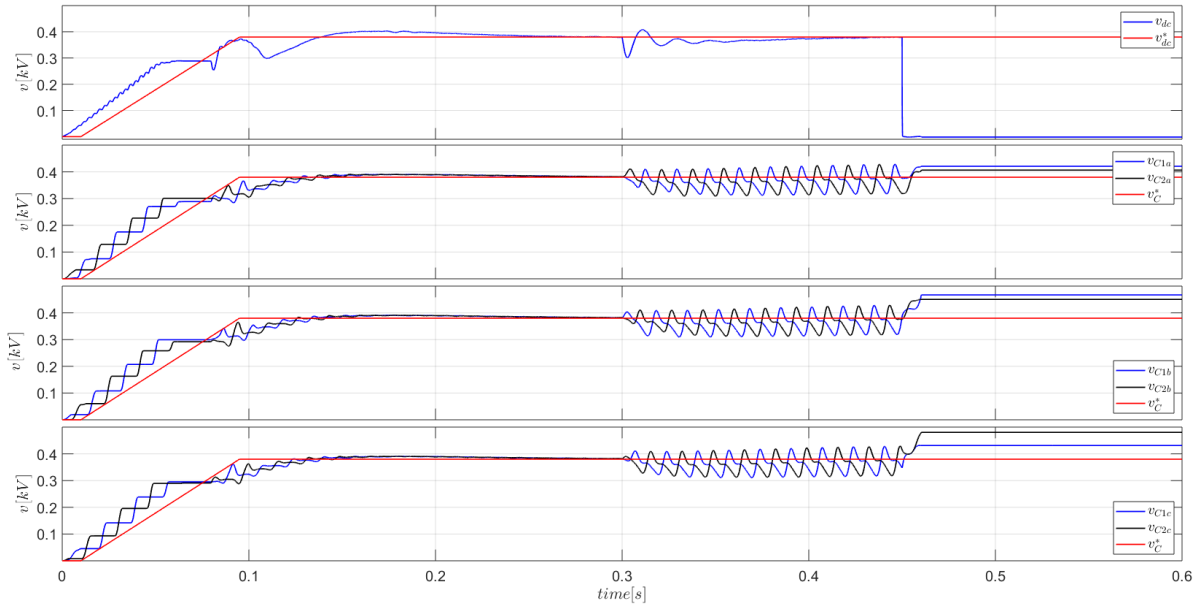


Figure 4.32: Dynamic response of the dc-side voltages of the converter and the FBSMs of the non-ideal converter, while subjected to dc-side fault.

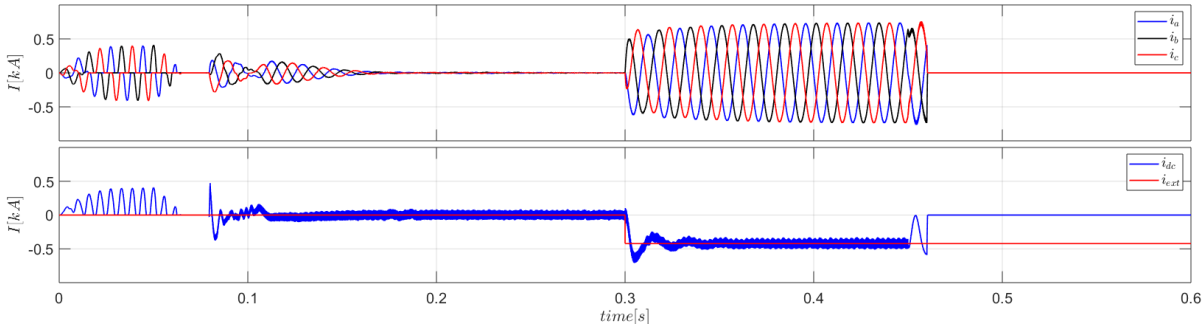


Figure 4.33: Dynamic response of the dc- and ac-side current of the non-ideal converter, while subjected to dc-side fault.

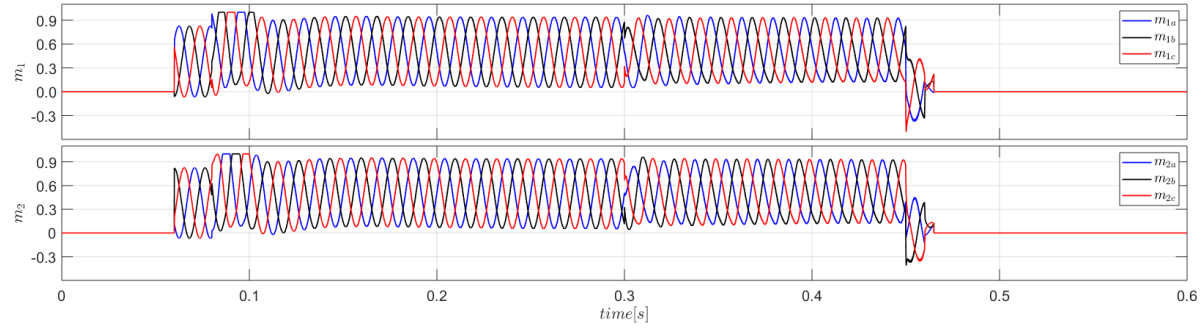


Figure 4.34: Modulating signals of the FBSMs of the non-ideal converter, while subjected to dc-side fault.

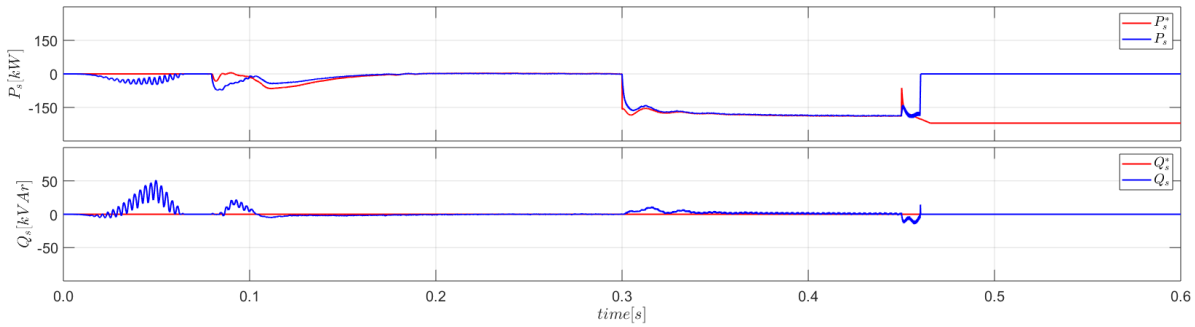


Figure 4.35: Dynamic response of the $P_{ext}$, $P_s$, $P_s^*$, $Q_s$, and $Q_s^*$ of the non-ideal converter, while subjected to dc-side fault.

**Ideal Converter Connected to a Non-Ideal AC Grid Under DC-Side Fault**

As it was previously discussed in this chapter, in actual applications the ac-grid is not an ideal voltage source and as a result in order to simulate the converter in more realistic conditions the actual structure of the ac-grid must be taken in to considerations. Hence, the converter was analyzed while connected to a non-ideal ac-grid, modeled with a series connection of an ideal voltage source and the grid impedance. In this part, converter was subjected to dc-side short circuit fault while connected to a non-ideal ac grid and its ability to eliminate the fault at its dc-side terminals was analyzed.

Figures 4.36 to 4.39 present the dynamic response of $v_{dc}$, dc-side voltage of the FBSMs, ac-side currents, modulating signals of the FBSMs, and actual and reference values of the powers exchanged between the converter and dc and ac grid, respectively. As it can be seen interpreted from the figures, once the converter is subjected to dc-side fault, after a 15 $ms$ delay, the gating signals get blocked by the controller, and the capacitors available at the dc-side of the FBSMs become series with the anti-parallel diodes, and thus the diodes are turned off and the ac-side current drops to zero. Hence, similar to the two previous scenarios, the converter has the ability to eliminate the ac-side contribution to the faults at its dc-side.

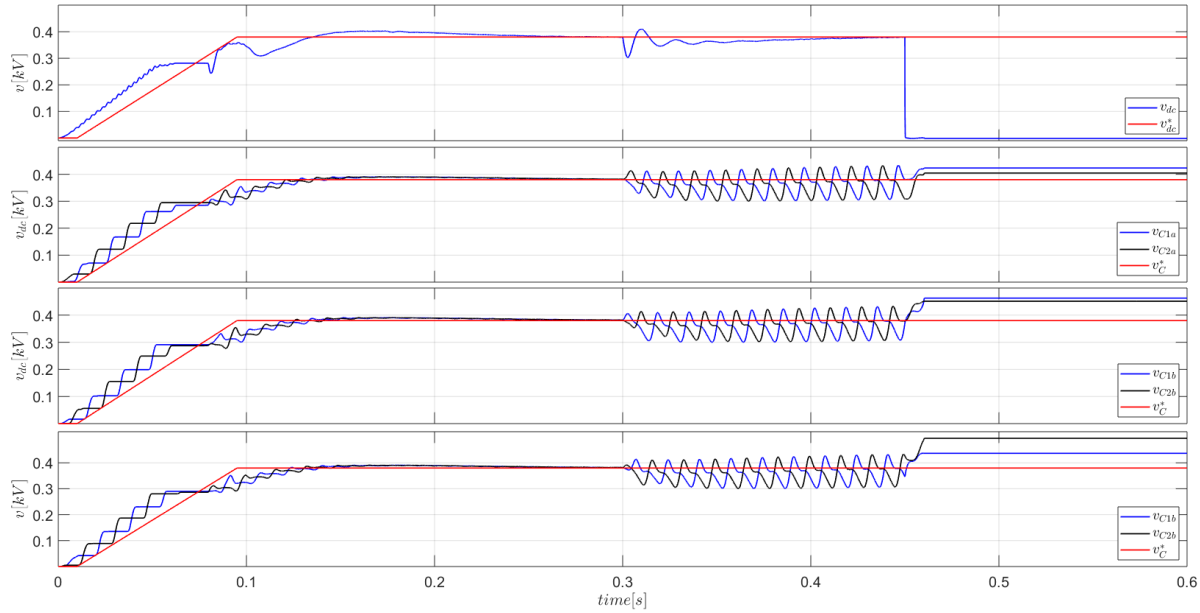


Figure 4.36: Dynamic response of the dc-side voltages of the converter and the FBSMs of the ideal converter, while subjected to dc-side fault.

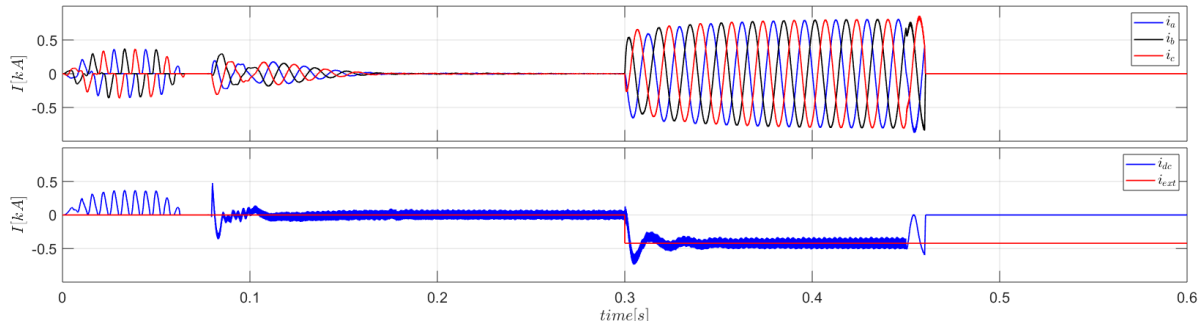


Figure 4.37: Dynamic response of the ac-side current of the ideal converter, while subjected to dc-side fault.

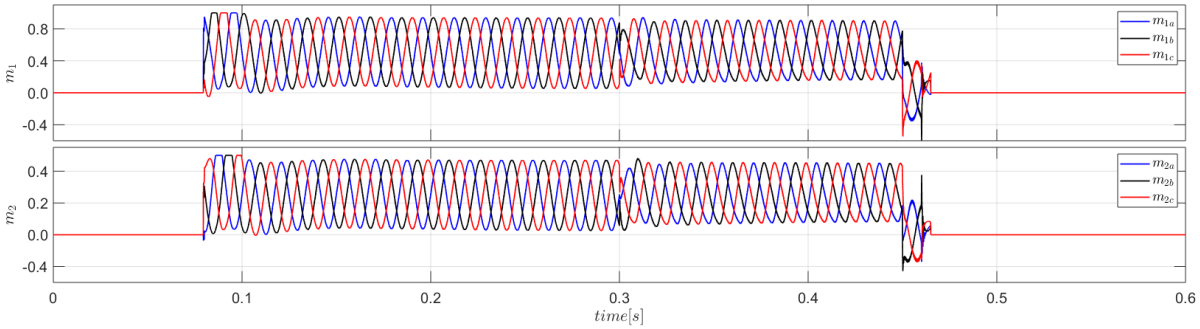


Figure 4.38: Modulating signals of the FBSMs of the ideal converter, while subjected to dc-side fault.

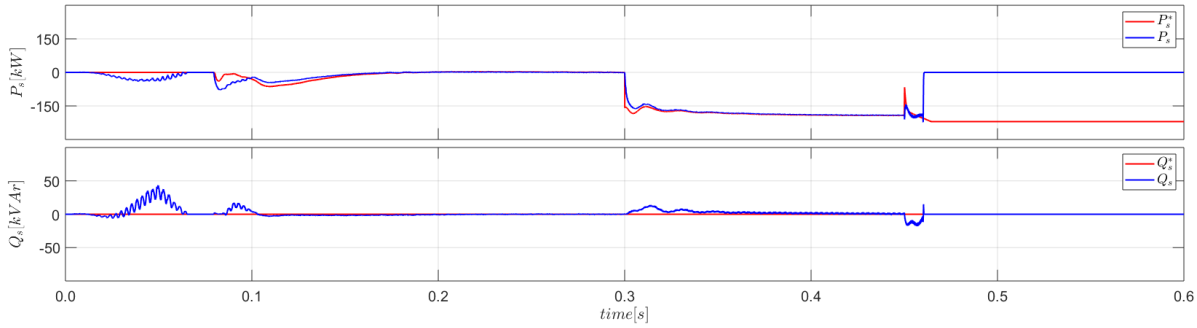


Figure 4.39: Dynamic response of the $P_{ext}$, $P_s$, $P_s^*$, $Q_s$, and $Q_s^*$ of the ideal converter, while subjected to dc-side fault.

# Chapter 5

# Conclusion and Future Work

In the previous chapters of this thesis the power circuit, control topology and simulation results of the proposed single-stage bi-directional ac/dc converter were discussed. This chapter presents the final conclusions achieved during the course of this research, followed by exploring the possible areas for further enhancing the proposed converter and make it more suitable for the market.

## 5.1 Conclusions

The overall aim of this thesis is to propose an answer to the current need for a bi-directional converter at the point of interconnection (POI) of dc- and ac-distribution system, whilst providing the required protection against potential dc-side short circuit faults. As a result, this thesis proposed the power circuit topology and control methodology of a single-stage bi-directional ac/dc converter with the ability to effectively tolerate dc-side short circuit faults, thus eliminating the need for expensive and complicated dc circuit breakers. The proposed converter was then modeled in detail in the PSCAD/EMTDC software environment. The following general conclusions were drawn from the studies:

- The thesis proposed a converter with two H-bridge sub-modules in each phase and a total of 7 dc-side capacitors, one for the dc-side of the converter and 6 for the mentioned sub-modules. Through the use of the decoupled dq-frame current control and dc-link voltage control schemes the converter is able to ensure the power balance between the external power source available at the dc-side of the converter and the ac grid. The aforementioned control schemes were referred to as the differential-mode controllers in this thesis. Furthermore, through the use of a separate control scheme, denoted by common-mode control scheme, the energy balance inside the converter was ensured by regulating the current traveling through both FBSMs in each leg.

- It was shown through mathematical modeling, that the modulating signals for the proposed converter must be consisted of two independent parts, i.e., ac and constant dc values, resulting from the differential-mode, and common-mode control schemes, respectively. Hence, it was proven that the two control schemes are independent from each other.

- It was mathematically proven that the ac-side parameters of the converter, only depend on the differential-mode components. Hence, by employing the same carrier for the FBSMs in the upper and lower arm of each leg of the converter, the switching harmonics transferred to the ac grid were reduced, and a clean sinusoidal ac current was achieved.

- It was shown that by employing a relatively high resistance path, gradual increase of the reference value of the dc-side voltage, and blocking the controllers during the start-up conditions, and gating signals until the capacitors are partially charged the converter is able to have a smooth and fast start-up without causing any additional stress on the converter. Once the capacitors of the converter are fully charged the high resistive path is opened and the connection between the converter is done through the RL branch, in order to avoid extra losses in the system.

- The converter was tested while facing sudden changes in the power exchanged with the converter and the external source at its dc-side and changed in the reference value of the reactive power exchanged between the converter and the grid at PCC. The obtain results proved that the converter is able to tolerate and follow the aforementioned changes.

- The converter was also faced with sudden changes in its desired dc-side reference voltage and it was shown the converter is able to function normally and follow the changes in a fast and effective manner. It must be mentioned that this only applies when the change in the reference value of the dc-side voltage does not drop below the voltage conversion ratio below its minimum value as discussed in Chapter 2.

- Then the thesis evaluated the effectiveness of the proposed control methodology, while the converter was not ideal. To do so, one of the dc-side capacitors of the converter was paralleled with a resistor which would dissipate power and thus an asymmetry was introduced to the converter topology and make it closed to an actual converter. The simulation results proved that the proposed control methodology was effective enough to regulate the non-ideal converter.

- In the next step, the converter was assumed to be connected to a non-ideal ac grid, modeled by series connection of an ideal ac voltage source and the line impedance. In this scenario the connection between the converter and ac-grid was done through an LC filter, since the use of shunt capacitors would provide a path for high frequency harmonics of the current. Furthermore, in order to avoid the resonance between the inductance of the filter and the grid and the capacitance of the filter a passive damping resistor was used. Doing the aforementioned allowed to analyze the converter under a more realistic scenario and proved that the controller is still effective.

- Finally, it was proven that upon occurring a fault at the dc-terminals of the converter, and blocking the gating signals with a short delay (in order to account for the controller delays in actual applications) the converter is able to eliminate the ac-side contribution to the fault, under all ideal and non-ideal scenarios. The fault elimination is done by turning the anti-parallel diodes through putting the fully-charged dc-side capacitors of the FBSMs in series with the anti-parallel diodes.

## 5.2 Future Works

The potential research topics related to the subject discussed in this thesis are as follows:

- Making refinements to the proposed LC filter for connecting the converter to the non-ideal ac grid which employs active damping method.
- Studying the possibility of upgrading the control methodology to enable the ability of self-restoration after fault clearance.
- Studying the efficiency of the proposed converter and searching for possibilities in further improving it.

# Appendix A

# Converter Paramters

Table A.1, presents a list of the parameters of the proposed converter.

Table A.1: Compensator parameters

| Parameter | Value |
|---|---|
| $V_s$ | 208 $V\ RMS$ |
| $v_{dc}$ | 380 |
| $L_g$ | $3.6 \times 10^{-5}\ H$ |
| $R_g$ | 0.0135 Ω |
| $C_f$ | 100 $\mu F$ |
| $R_{fd}$ | 0.1 Ω |
| $L_f$ | $1 \times 10^{-4}\ H$ |
| $R_f$ | 0.002 Ω |
| $L$ | $1 \times 10^{-4}\ H$ |
| $R_f$ | 0.003 Ω |
| $R_{st}$ | 0.03 Ω |
| $R_c$ | 30 Ω |

# Appendix B

# Compensators

Table B.1 presents a list of the designed compensators used in the control of the proposed converter, their corresponding descriptions and their transfer function.

Table B.1: Compensator parameters

| Compensator | Description | Transfer Function |
|---|---|---|
| $K_d(s)$ | D-axis ac-side current controller | $\left(\frac{0.15s+0.9}{s}\right)$ |
| $K_q(s)$ | Q-axis ac-side current controller | $\left(\frac{0.15s+0.9}{s}\right)$ |
| $K_{VDC}(s)$ | DC-side voltage controller | $2352.2\left(\frac{s+16.47}{s(s+2428)}\right)$ |
| $K_{i\sigma}(s)$ | Common-mode current controller | $-\left(\frac{0.1s+14}{s}\right)$ |
| $K_{P\sigma k}(s)$ | Common-mode FBSM power controller | $1192.9\left(\frac{s+32.91}{s(s+1215)}\right)$ |
| $K_{P\delta k}(s)$ | Differential-mode FBSM power controller | –0.9814 |

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