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# CMOS active inductors and transformers for wireless applications

Adrian Tang
*Ryerson University*

# CMOS ACTIVE INDUCTORS AND TRANSFORMERS FOR WIRELESS APPLICATIONS

Adrian Tang

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Ryerson University
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RYERSON UNIVERSITY

DEPARTMENT OF ELECTRICAL ENGINEERING

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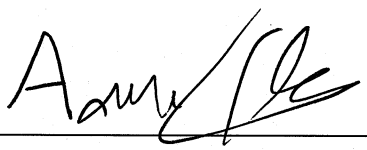

# Abstract

CMOS Active Inductors and Transformers for Wireless Applications

Adrian Tang, MASc, Program of Electrical and Computer Engineering,

Ryerson University, Toronto, Ontario, Canada. 2008.

This thesis first reviews existing work in CMOS active inductors focusing on two implementations, Wu gyrator-C and differential floating active inductors. It then proposes a new method of quantifying the performance of active inductors by introducing a figure of merit called "mean quality factor" that is better suited to the large signal behavior of active inductors. New CMOS constant-$Q$ active inductors are proposed that are intended specifically for applications where a large signal operation is required. The thesis then proposes CMOS active transformers that are the active circuit equivalents of two magnetically coupled coils. Four applications of constant-$Q$ active inductors and active transformers namely a 2.4 GHz voltage-controlled oscillator with -119.5dBc/Hz phase noise at 1 MHz offset, a 2.4 GHz current-mode phase-locked loop with -116dBc/Hz phase noise at 1 MHz offset and 80ns lock time, a 5 MHz 100X oversampled current-mode sigma-delta modulator with 50dB dynamic range and 65dB SNR, and a 1.6 GHz QPSK phase modulator with -101dBc/Hz phase noise at 1 MHz offset are presented.

# Acknowledgment

Thanks to my family and supervisors.

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# List of Abbreviations

| | |
|---|---|
| ADC | Analog to Digital Converter |
| CCO | Current Controlled Oscillator |
| CMOS | Complementary Metal Oxide Semiconductor |
| CTM | Capacitor Two Metal |
| DAC | Digital to Analog Converter |
| DFF | D-Flip Flop |
| FFT | Fast Fourier Transform |
| MOS | Metal Oxide Semiconductor |
| PLL | Phase-Locked Loop |
| PSD | Power Spectral Density |
| QPSK | Quadrature Phase Shift Keying |
| QVCO | Quadrature Voltage Controlled Oscillator |
| SNR | Signal to Noise Ratio |
| TSMC | Taiwan Semiconductor Manufacturing Company |
| VCDL | Voltage Controlled Delay Line |
| VCO | Voltage Controlled Oscillator |

# CHAPTER 1

# INTRODUCTION

## 1.1 Motivation

In analog circuit design the necessity for fabricating passive components on-chip remains critical while the direction and evolution of deep sub-micron CMOS technology continues to be influenced mostly by digitally oriented applications. For this reason special mixed-mode CMOS layers are often employed for the implementation of passive elements such as the CTM metal-to-metal capacitor layer and the low-silicide poly options to implement large valued resistors. One of the more challenging passive elements to implement in CMOS technology are inductors. Inductors are typically constructed on-chip for RF applications and employ a planar spiral structure using the top metal layer. These spiral inductors appear in a variety of geometries including stacked spiral inductors, which contain windings stacked on multiple metal layers to provide a larger inductance than is possible with a single planar spiral structure. CMOS spiral inductors have found a broad range of applications in analog signal processing and RF systems. The effectiveness of these inductors, however, is affected by a number of drawbacks that are intrinsic to their spiral layout and CMOS technologies. These drawbacks include a low quality factor due to the skin-effect induced ohmic loss, a low self-resonant frequency due to the large parasitic capacitance with the substrate, a small and non-tunable inductance due to the planner structure of these inductors,

and the need for a prohibitively large chip area. More recently, CMOS on-chip transformers have appeared in which two spiral or stacked inductors are placed in a configuration that permits magnetic coupling. The use of CMOS spiral transformers for RF applications in power amplifiers and VCOs have emerged recently.[1, 2, 3, 4, 5, 6, 7, 8, 9]. The intrinsic deficiencies of spiral inductors, however, are inherited by these on-chip spiral transformers.

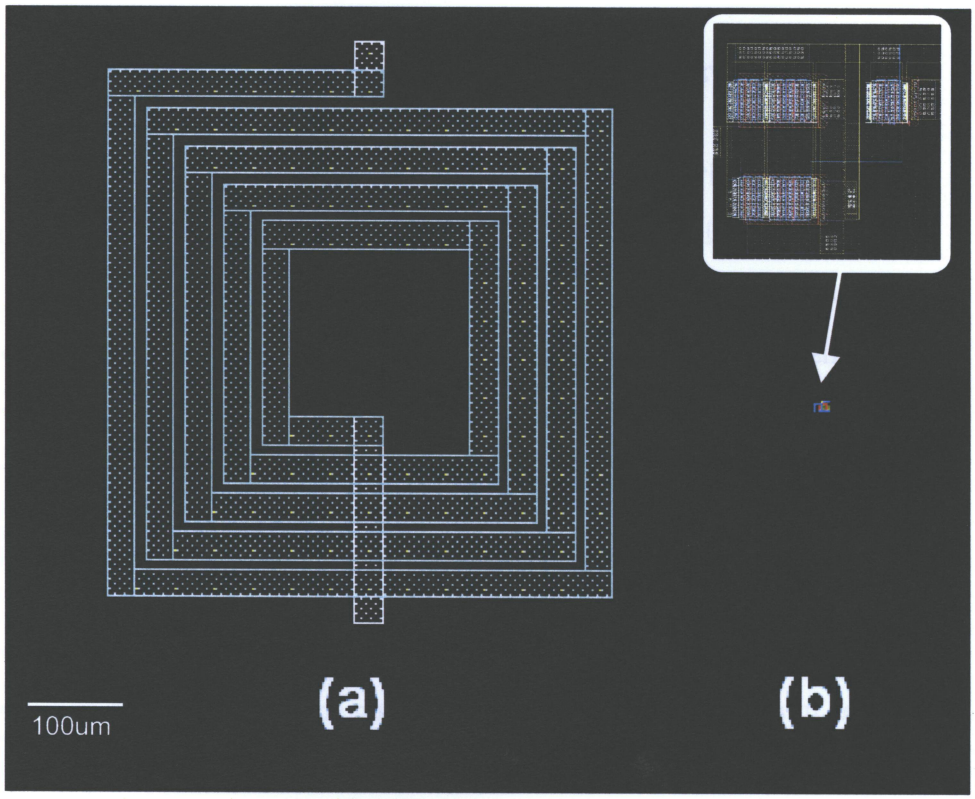



Figure 1.1: (a) 8 nH Spiral inductor. (b) An equivalent 8 nH active inductor.

Active inductors that are synthesized using active devices offer many unique advantages over their passive spiral counterparts including virtually no silicon area requirement, a large and variable inductance, a tunable quality factor, and full compatibility with digitally oriented CMOS technologies. These inductors have been used successfully in many applications where inductors are required,

such as SONET OC-48 optical receivers with 3GHz bandwidth [10], 2.5Gbps optical front-ends [11], VCOs for 4Gbps clock and data recovery [12], 5 GHz VCOs with -81 dBc/Hz phase noise at 500kHz offset [13], low-noise amplifiers with 1 GHz bandwidth and 2~3 dB noise figure [14], optical pre-amplifiers [15], and Gbps serial links [16], to name a few. Active inductors however still have several limitations including a higher level of noise associated with active devices and increased distortion due to their limited dynamic range. Active inductors also exhibit higher levels of power consumption then their passive counterparts. The purpose of this thesis is to improve the distortion and noise performance of CMOS active inductors to a level comparable with that of spiral inductors.

## 1.2 Contributions

The work in this thesis has made the following contribution in active inductors, specifically:

- A new figure-of-merit called "mean quality factor" is introduced to take into account the large signal behavior of active inductors.
- A new constant-$Q$ active inductor, that offers the advantage of a large and nearly constant quality factor in the presence of a large signal swing.
- CMOS active transformers are proposed.
- High-speed phase-lock loops employing CMOS active transformers and constant-Q active inductor CCOs that provide phase noise comparable to that of phase-locked loops with spiral inductors, tunability and locking performance while occupying only a small silicon area.

- A new sigma-delta modulator employing CMOS active transformers to provide an SNR performance comparable to that of sigma-delta modulators with a passive loop filter while occupying a much smaller silicon area.

- A new active transformer-based QPSK phase modulator that exhibits phase noise comparable to that of QPSK modulators with spiral inductors, and optimizes carrier bandwidth, while occupying only a small silicon area.

The work presented in this thesis has also led to the following publications:

- A. Tang, F. Yuan, and K.L.E. Law,, "A new CMOS QPSK modulator with optimal transaction bandwidth control," *IEEE Transactions on Circuits and Systems II*, Vol 55. No. 1, pp. 11-15 Jan 2008.

- D. DiClemente, F. Yuan, and A. Tang, "Current-mode phase-locked loops with CMOS active transformers," *IEEE Transactions on Circuits and Systems II*, Accepted for publication in Jan 2008.

- A. Tang, F. Yuan, and K.L.E. Law,, "Class AB CMOS active transformers with applications in LC oscillators," *Proc. Int. Symp. on Circuits, Systems and Electronics*, pp. 501-504, Montreal. Aug 2007.

- A. Tang, F. Yuan, and K.L.E. Law,, "Low-noise CMOS active transformer voltage-controlled oscillators," *Proc. IEEE MWSCAS*, pp. 1441-1444, Montreal. Aug 2007.

- D. DiClemente, F. Yuan, and A. Tang, "CMOS active transformer current-mode phase-locked loops," *Proc. IEEE MWSCAS*, pp. 1528-1531, Montreal. Aug 2007.

- A. Tang, F. Yuan, and K.L.E. Law,, "A New WiMAX Sigma-Delta Modulator with Constant-Q Active Inductors," *Proc. IEEE International Symposium Circuits and Systems 2008*, Accepted for publication in Jan. 2008. Seattle.

- A. Tang, F. Yuan, and K.L.E. Law,, "A new CMOS BPSK modulator with optimal transaction bandwidth control," *IEEE Int. Symp. Circuits and Systems*, pp 2550-2553, New Orleans. May 2007.

- A. Tang, F. Yuan, and K.L.E. Law,, "3-5 GHz Active Inductor Oversampling Sigma Delta Modulator for WiMAX Applications," *CMC Microsystems Symposium 2007* Ottawa Ontario. Oct. 2007.

- A. Tang, F. Yuan, and K.L.E. Law,, "CMOS binary phase modulator with active transformers," *CMC Microsystems Symposium 2006* Ottawa Ontario. Nov. 2007.

- A. Tang, F. Yuan, and K.L.E. Law,, "A Low Phase-Noise Current-Mode Phase-Locked Loop with Constant-Q Active Inductor CCO and Active Transformer Loop Filter," *Analog Integrated Circuits and Signal Processing.* Revised in March 2008.

- A. Tang, F. Yuan, and K.L.E. Law,, "A new constant-Q active inductor with applications in low-noise oscillator," *Analog Integrated Circuits and Signal Processing.* Submitted in Jan 2008.

- A. Tang, F. Yuan, and K.L.E. Law,, "CMOS active transformers and applications," *Analog Integrated Circuits and Signal Processing.* Submitted in July 2007.

## 1.3 Organization

The basic characteristics of ideal and on-chip spiral inductors, spiral transformers and published work on active inductors in particular, the Wu gyrator-C active inductor, and differential active inductor are briefly reviewed in chapter 2. A new method of quantifying the performance of active inductors with a figure-of-merit called "mean quality factor" and CMOS constant-$Q$ active inductors are proposed in chapter 3. CMOS active transformers are proposed in chapter 4. Four applications are presented in chapter 5, including a 2.4 GHz VCO with -119.5dBc/Hz phase noise, a 2.4 GHz current-mode phase-lock loop with -116dBc/Hz phase noise and 80ns lock time, a 5 MHz 100X oversampled current-mode sigma-delta modulator with 50dB dynamic range and 65dB SNR, and a 1.6 GHz QPSK phase modulator with -101dBc/Hz phase noise. The thesis is concluded and future work is commented on in chapter 6.

# CHAPTER 2

# LITERATURE REVIEW

## 2.1 A Review of Ideal and Spiral Inductors

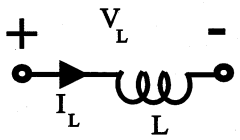



Figure 2.1: Ideal inductor.

Fig.2.1 shows the symbol of an ideal inductor with inductance L. The voltage $V_L$ is related to the current $I_L$ by $V_L = L\frac{dI_L}{dt}$. In the sinusoidal steady state this can be expressed as $v_L = j\omega L i_L$. The Bodé plots of the ideal inductor are shown in Fig.2.2.

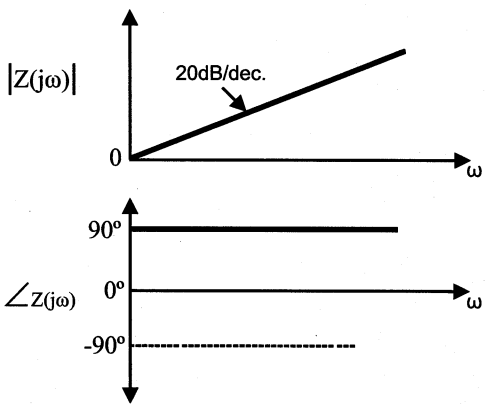



Figure 2.2: Bodé plot of ideal inductors.

Currently the best on-chip implementation of inductors are spiral inductors

that employ a planar spiral structure using the top metal layer. The top metal layer is chosen to maximize the distance from the substrate, minimizing the parasitic shunt capacitance. Spiral inductors also contain a small inter-winding capacitance because of their planar structure, and a series resistance due to skin effect-induced losses and the sheet resistance of the metal layer itself. Fig.2.3 shows the lumped circuit model of CMOS spiral inductors[17]. In this model L is the effective inductance, $R_{sub}$ models the losses due to the close proximity of the substrate, $R_{wind}$ models the ohmic losses due to the skin effect and sheet resistance, $C_{sub1}$ and $C_{sub2}$ model the capacitance to the substrate, and $C_{wind}$ models the inter-winding capacitance.

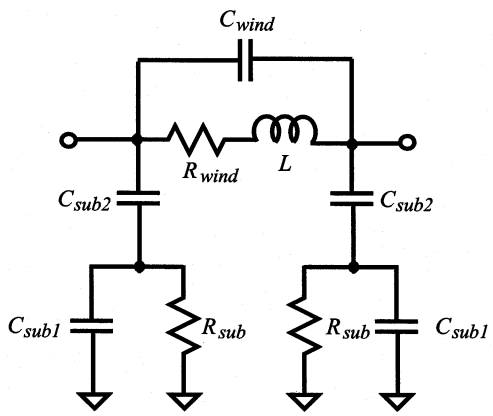



Figure 2.3: Lumped equivalent circuit of CMOS spiral inductors.

Fig.2.4 shows the Bodé plot for the spiral inductor model. The impedance contribution from $C_{wind}$ is small compared with that from $C_{sub}$ and can be neglected. As $R_{wind}$ is dominated by the skin effect loss its contribution to the impedance remains small at low frequencies, allowing the spiral to follow the behavior of the ideal inductor in the low frequency range. The spiral self resonates with the parasitic capacitances at frequency $\omega_o$ , and beyond this frequency range provides a capacitive behavior as the poles generated by $C_{sub1}$ and $C_{sub2}$ dominate the impedance.

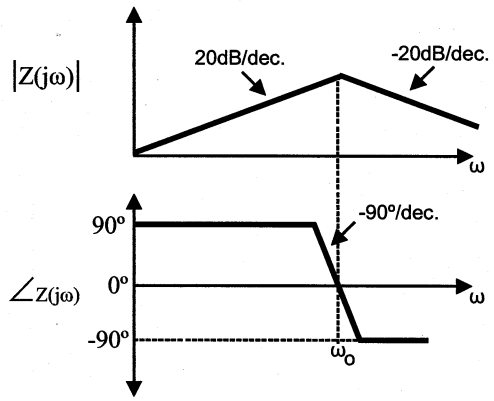



Figure 2.4: Bodé plots of CMOS spiral inductors.

## 2.2 Ideal Linear Transformers

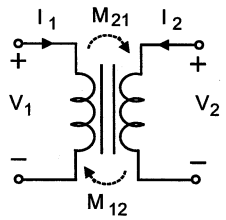



Figure 2.5: Symbol of ideal linear transformers.

An ideal linear transformer with its symbol shown in Fig.2.5 consists of a primary winding and a secondary winding, both wound on the same magnetic core. Each winding itself is an inductor. The magnetic core allows the magnetic flux of the two inductors to be shared, enabling a current passing through one winding to affect the voltage of the other. In the frequency domain the terminal voltages of linear transformers are quantified by

$$\begin{aligned} V_1 &= sL_{11}I_1 + sM_{12}I_2, \\ V_2 &= sL_{22}I_2 + sM_{21}I_1, \end{aligned} \tag{2.1}$$

where $L_{11}$ and $L_{22}$ are the self-inductance of the primary and that of the secondary windings, respectively, $M_{21}$ and $M_{12}$ are the mutual inductance from the primary winding to the secondary winding and that from the secondary winding to the primary winding, respectively, $V_1$ and $I_1$, $V_2$ and $I_2$ are the voltage and current of the primary and those of the secondary windings, respectively. The mutual inductance $M_{21}$ can also be expressed in terms of a coupling coefficient $K_{21}$

$$M_{21} = K_{21}\sqrt{(L_{11})(L_{22})}. \tag{2.2}$$

Similarly $M_{12}$ is given by

$$M_{12} = K_{12}\sqrt{(L_{11})(L_{22})}. \tag{2.3}$$

CMOS spiral transformers inherit the same self-resonance and ohmic loss characteristics of spiral inductors when implemented in CMOS technology due to their planar structure and proximity to the substrate. Fig.2.6 shows the lumped equivalent circuit model commonly used for spiral transformers. In this model $L_1$ and $L_2$ are the self-inductances, $R_{sub}$ is the loss due to the close proximity with the substrate, $R_{wind1}$ and $R_{wind2}$ model the ohmic losses due to the skin effect and sheet resistance of the primary and secondary windings respectively, $C_{sub1}$ and $C_{sub2}$ model the capacitances to the substrate, $C_{wind1}$ and $C_{wind2}$ model the inter-winding capacitances, $C$ models the capacitance between primary and secondary windings, $M_{12}$ and $M_{21}$ model the mutual inductances, and $R_{c12}$ and $R_{c21}$ model the coupling losses of the transformer. The Bodé plots of the transimpedance of the spiral transformer are the same as those for the impedance of spiral inductors

given in Fig.2.4.

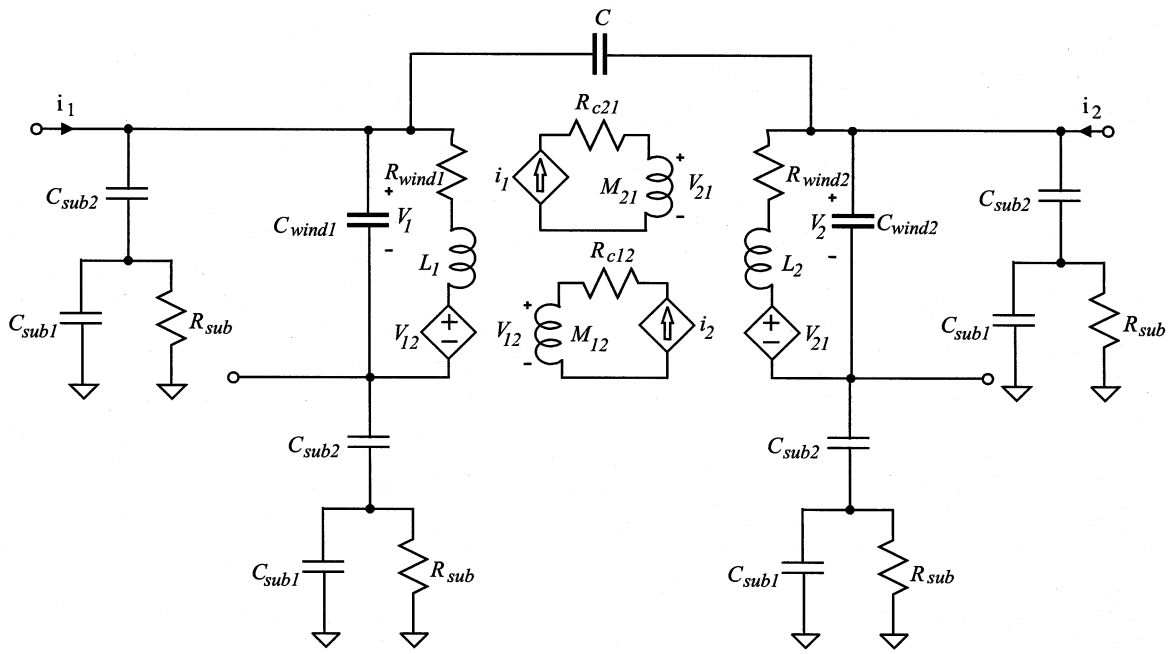



Figure 2.6: Lumped equivalent circuit of spiral transformers.

## 2.3 Quality Factor of Inductors

Quality factor is a parameter that describes the behavior of RLC circuits and can be computed using several definitions. For band-pass filters, the definition of quality factor $Q_{BPF}$ relates the half-power bandwidth $\omega_{3dB}$ to the center frequency $\omega_o$ of the filter,

$$Q_{BPF} = \frac{\omega_o}{\omega_{3dB}}. \tag{2.4}$$

This definition does not apply to situations where a bandpass characteristic is not present. In these situations the quality factor $Q$ is defined as

$$Q = \frac{E_{stored}}{E_{dissipated}}, \tag{2.5}$$

where $E_{stored}$ and $E_{dissipated}$ are the energy stored and dissipated per cycle. For a passive circuit with input impedance $Z(j\omega)$ this can be expressed as

$$Q = \frac{Im[Z(j\omega)]}{Re[Z(j\omega)]}, \tag{2.6}$$

where Im[ ] and Re[ ] denote the mathematical operation of extracting the imaginary and real components of an expression respectively. Applying this expression to a non ideal-inductor with a series resistance $R_s$ and inductance $L$, the $Q$ of the inductor can be given by

$$Q_{ind} = \frac{\omega L}{R_s}. \tag{2.7}$$

In applications where the phase selectivity of the circuit is most important such as oscillators where the phase sensitivity affects phase noise performance, the quality factor is usually expressed as the rate of the change of phase $\phi(j\omega)$ with respect to frequency[17]

$$Q(\omega) = \frac{\omega_o}{2}\frac{\partial\phi(\omega)}{\partial\omega}. \tag{2.8}$$

## 2.4 Gyrator-C Configuration Active Inductors

The most common configuration of active inductors is the gyrator-C configuration, which consists of two trans-conductors known as gyrators connected back-to-back with a capacitive load, as shown in Fig.2.7.

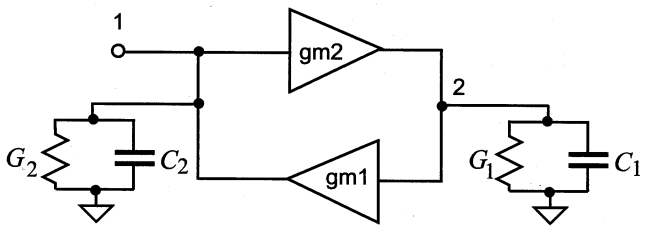



Figure 2.7: Gyrator-C active inductors.

With ideal gyrators whose input impedance assumed to be infinite we can obtain the KCL expressions at nodes 1 and 2

$$\begin{aligned} -I_{in} - g_{m1}V_2 + G_2V_1 + sC_2V_1 &= 0 \\ -g_{m2}V_1 + G_1V_2 + sC_1V_2 &= 0. \end{aligned} \tag{2.9}$$

where $V_1$ and $V_2$ are the voltages at nodes 1 and 2 respectively and $I_{in}$ is the current entering the port at node 1. Isolating $\frac{I_{in}}{V_1}$ in (2.9) we obtain the conductance at the port of the active inductor,

$$\frac{I_{in}}{V_1} = sC_2 + G_2 + \frac{1}{s\frac{C_1}{g_{m1}g_{m2}} + \frac{G_1}{g_{m1}g_{m2}}}. \tag{2.10}$$

The passive circuit shown in Fig.2.8 has an input of conductance

$$\frac{I_{in}}{V_{in}} = sC + G + \frac{1}{sL + R_s}. \tag{2.11}$$

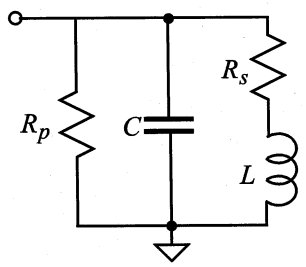



Figure 2.8: Equivalent circuit of single-ended gyrator-C active inductors.

Noting the similar structure of (2.10) and (2.11), we can equate the circuit parameters and obtain an equivalent circuit,

$$
\begin{aligned}
R_p &= \tfrac{1}{G_2}, \\
C &= C_2, \\
R_s &= \tfrac{G_1}{g_{m1}g_{m2}}, \\
L &= \tfrac{C_1}{g_{m1}g_{m2}}.
\end{aligned}
\tag{2.12}
$$

Assuming that $R_p >> Rs$ and considering the impedance of the active inductor in terms of the equivalent circuit parameters we can invert (2.11) and obtain

$$
Z(s) = \frac{R_s}{C_p L} \frac{s\frac{L}{R_s} + 1}{s^2 + s(\frac{1}{C_p R_p} + \frac{R_s}{L}) + \frac{R_p + R_s}{C_p L R_p}}. \tag{2.13}
$$

Extracting the poles of the input impedance provides the resonant frequency located at $\omega_o \approx \frac{1}{\sqrt{C_p L}}$. $Z(s)$, the input impedance also contains a zero at $\omega_Z = \frac{R_s}{L}$, providing the lower bound for the frequency range of the active inductor. This suggests the input impedance is resistive for $\omega < \omega_z$, inductive for $\omega_z < \omega < \omega_o$ and capacitive for frequencies $\omega > \omega_o$. Fig.2.9 shows the Bodé plots of the input impedance of the active inductor with the resistive, inductive, and capacitive regions identified.

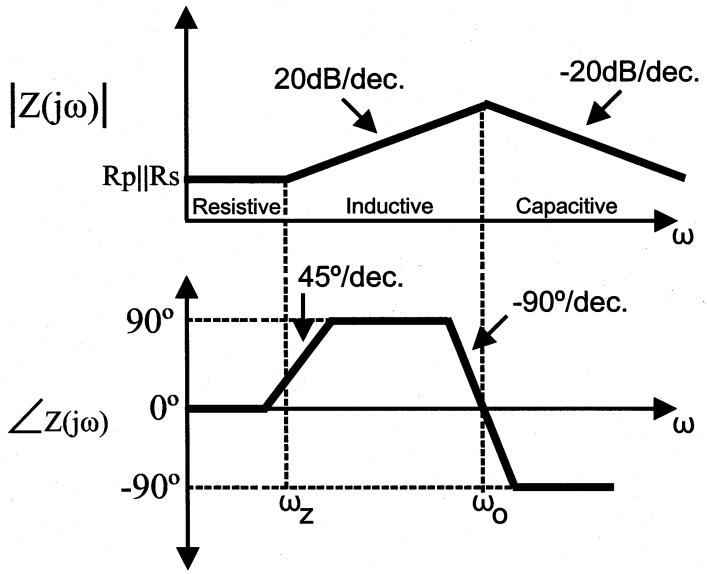



Figure 2.9: Bodé plot of the input impedance of gyrator-C active inductors.

## 2.5 Wu Active Inductors

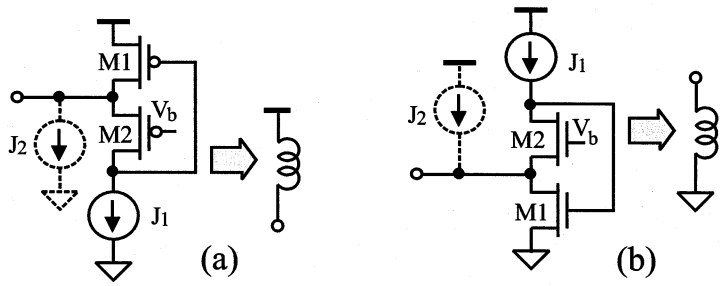



Figure 2.10: Wu current reuse active inductors. (a) PMOS and (b) NMOS configurations shown. Circuit parameters for simulation: $W_1 = 30\mu$m, $W_2 = 30\mu$m, $L = 0.18\mu$m for all transistors.

One of the widely used active inductors are the Wu current reuse active inductors [18] shown in Fig.2.10 with both PMOS and NMOS configurations. Wu active inductors are of gyrator-C configuration and employ a common source amplifier M1 and common gate amplifier M2 to form trans-conductors, and rely on the intrinsic gate to source capacitance of MOS devices to form the capacitive load. Current source $J_2$ boosts the trans-conductance of the common source stage to increase the quality factor of the active inductor. Fig.2.11 shows the small signal equivalent circuit of the Wu active inductor. Writing the KCL expressions at nodes 1 and 2 we obtain

$$\begin{aligned} I_{in} &= g_{o2}(V_1 - V_2) + g_{o1}V_1 + g_{m2}V_1 + g_{m1}V_2 + V_1 sC_{gs2}, \\ 0 &= g_{o2}(V_2 - V_1) - g_{m2}V_1 + sC_{gs1}V_2. \end{aligned} \tag{2.14}$$

Again isolating $\frac{I_{in}}{V_1}$ and using (2.10), the gyrator-C equivalent circuit parameters for Wu inductors can be found: $C = C_{gs2}, R_p = \frac{1}{g_{m2}}, L = \frac{C_{gs1}}{g_{m1}g_{m2}}$ and $R_s = \frac{g_{o1}+g_{o2}}{g_{m1}g_{m2}}$. Extracting the self resonant frequency of Wu active inductors from

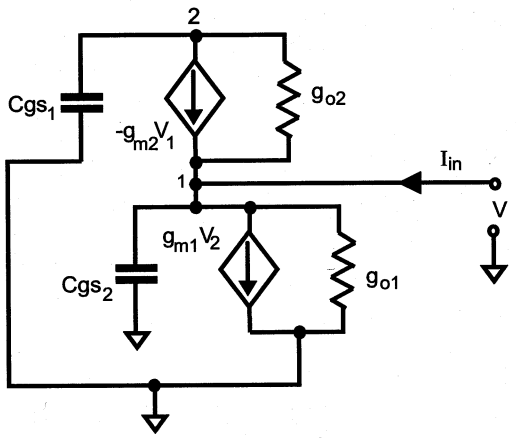



Figure 2.11: Small signal equivalent circuit of Wu active inductors.

these parameters we obtain $\omega_o = \frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}$. The simulated inductance of Wu active inductors is shown in Fig.2.12. As both transistors are biased in saturation with identical dimensions and biasing, $C_{gs1} = C_{gs2} = C_{gs}$, $g_{m1} = g_{m2} = g_m$, $g_{o1} = g_{o2} = g_o$ can be assumed. Using the equivalent circuit parameters we can find the input impedance of the Wu active inductor from (2.13),

$$z_{in}(s) = \frac{g_o}{C_{gs}^2} \frac{s\frac{C_{gs}}{g_o} + 1}{s^2 + s\frac{g_m}{C_{gs}} + \frac{g_m^2}{C_{gs}^2}}. \tag{2.15}$$

## 2.6 Differential Active Inductors

Unlike Wu current reuse active inductors, differential active inductors do not have one terminal of the inductor connected to ground or the supply. Instead, differential active inductors provide two terminal inductors with both terminals accessible as shown in Fig.2.13. Differential active inductors employ current source-loaded differential pairs to form the trans-condutors and rely on the gate to source capacitance of the input pair to provide the capacitive load. Fig.2.14

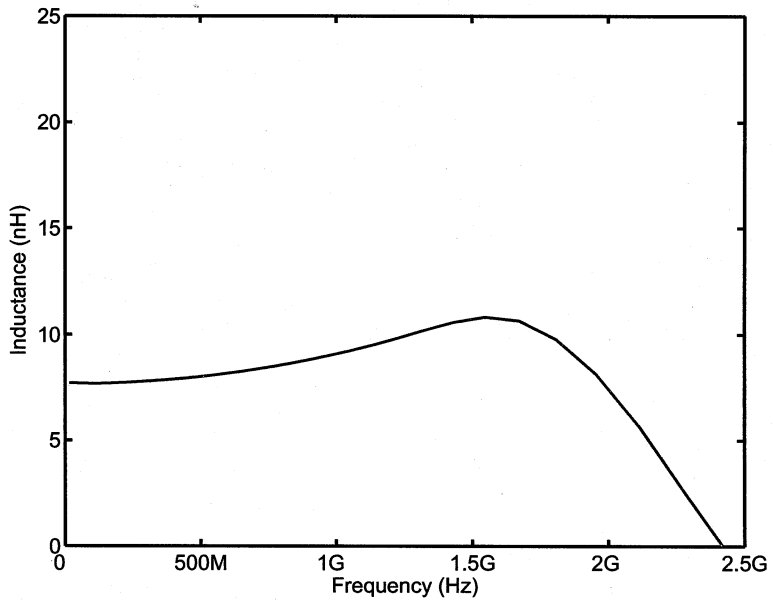



Figure 2.12: Simulated inductance of NMOS Wu current reuse active inductors.

shows the simulated inductance of the differential active inductor in Fig.2.13.

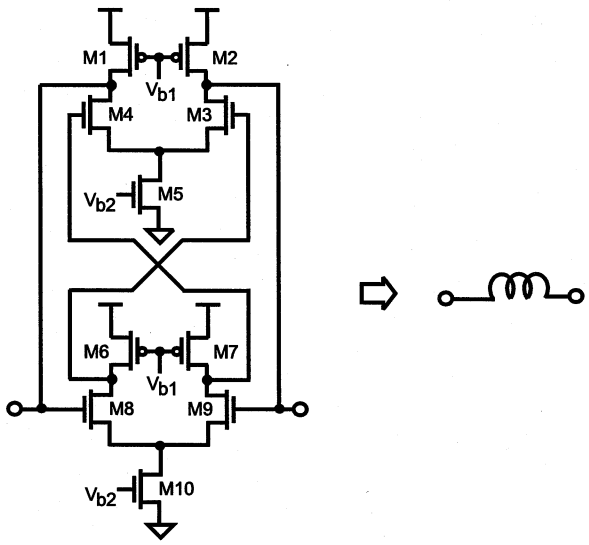



Figure 2.13: Differential active inductors. Circuit parameters : $W_1 = 100\mu$m, $W_2 = 100\mu$m, $W_3 = 30\mu$m, $W_4 = 30\mu$m, $W_5 = 60\mu$m, $W_6 = 100\mu m$, $W_7 = 100\mu m$, $W_8 = 30\mu$m, $W_9 = 30\mu m$, $W_{10} = 60\mu m$, $L = 0.18\mu$m for all transistors.

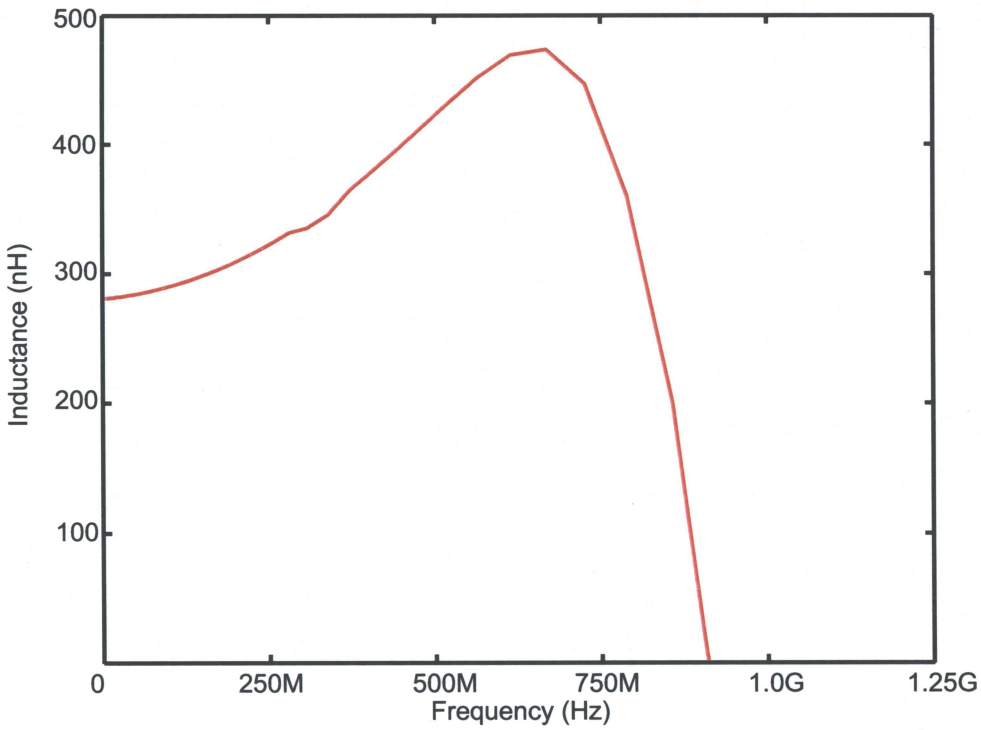



Figure 2.14: Inductance of differential floating active inductors.

# CHAPTER 3

# CONSTANT-Q ACTIVE INDUCTORS

## 3.1 Mean Quality Factor

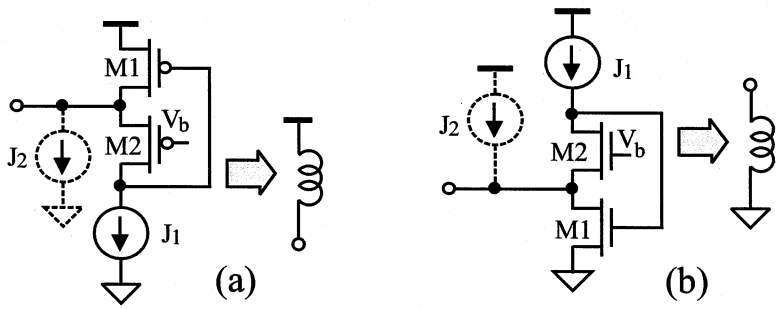



Figure 3.1: Wu current reuse active inductors. (a) PMOS and (b) NMOS configurations shown. Circuit parameters for simulation: $W_1 = 30\mu$m, $W_2 = 30\mu$m, $L = 0.18\mu$m for all transistors.

In this section, a new quantity called *mean quality factor* is introduced to quantify the quality factor of active inductors. Fig.3.1 shows the schematic of the well-known Wu's active inductors [18, 20]. It was shown earlier that the parameters of the RLC equivalent circuit of Wu's active inductor are given by $C_p = C_{gs2}$, $R_p = \frac{1}{g_{m2}}$, $L = \frac{C_{gs1}}{g_{m1}g_{m2}}$, and $R_s = \frac{g_{o1}+g_{o2}}{g_{m1}g_{m2}}$. The inductance $L$, the parasitic series resistance $R_s$, and parasitic parallel resistance $R_p$ are functions of $g_{m1}$ and $g_{m2}$, which are determined by the channel current of M1 and M2. The quality factor given by [21]

$$Q = \left(\frac{\omega L}{R_s}\right)\frac{R_p}{R_p + R_s\left[1 + (\frac{\omega L}{R_s})^2\right]}\left[1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p\right] \tag{3.1}$$

is also greatly affected by $g_{m1}$ and $g_{m2}$. The channel current of M2, which determines $g_{m2}$ and is given by $J_1 + I_{in}$, is greatly affected by the input current $I_{in}$, especially when $I_{in}$ is large. As a result, both the inductance and quality factor of the active inductor are strong functions of input current swing. This is evident in Fig.3.2 where the instantaneous quality factor of Wu's active inductor is evaluated at 2.4 GHz using the definition of the quality factor of LC tanks given in (2.8) at each level of the current of the active inductor.

The quality factor of a LC tank with a passive inductor is given by $Q \approx \frac{1}{R_p}\sqrt{\frac{L}{C_p}}$. When the LC tank is placed in a LC oscillator, the quality factor of the oscillator is independent of the current of the inductor. Unlike passive LC tanks, the quality factor of active inductors varies with the swing of their signals. The fact that the instantaneous quality factor of active inductors varies with their signal swing suggests that this *instantaneous quality factor* can not be used as a measure to quantify the performance of LC oscillators employing active inductors. We introduce the *mean quality factor* of active inductors defined as

$$Q_m(\omega_o) = \frac{1}{(I_{max} - I_{min})}\int_{I_{min}}^{I_{max}} Q(\omega_o, J)dJ, \tag{3.2}$$

where $I_{min}$ and $I_{max}$ are the minimum and maximum input currents of the active inductor, $Q(\omega_o, J)$ is the instantaneous quality factor of the active inductor at frequency $\omega_o$, and $J$ is the input current, as a measure to quantify the performance of oscillators with active inductors.

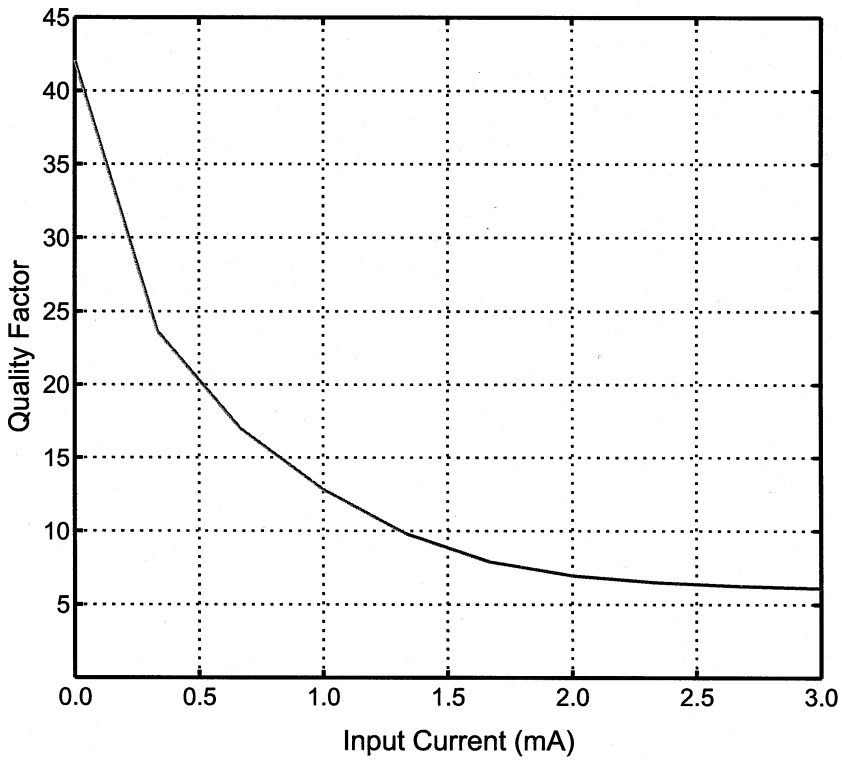
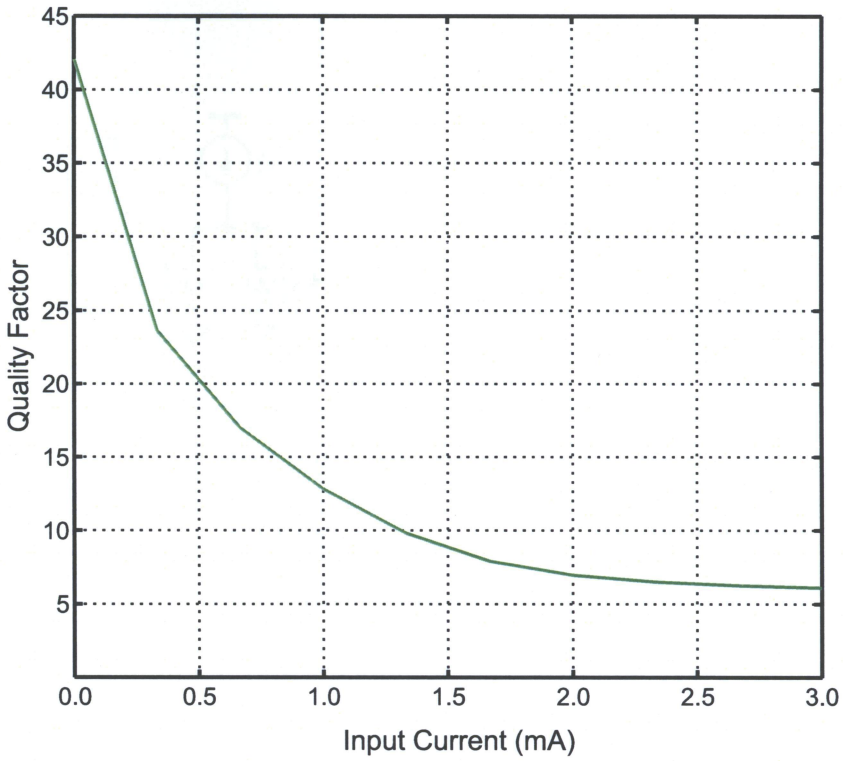



Figure 3.2: Dependence of the quality factor of Wu's active inductors on its input current at 2.4 GHz.

## 3.2 Constant-Q Active Inductors

In this section CMOS Constant-$Q$ active inductors which provide a nearly constant Q with the presence of a large input signal swing are presented. Constant-$Q$ active inductors have evolved from Wu's original gyrator-C active inductor shown in Fig.3.3a. Fig.3.3b shows the schematic of the proposed constant-$Q$ active inductor consisting of a Wu's active inductor and a current feedback network. Transistor M3 mirrors the current of M2, i.e. $i_{D3} = i_{D2}$. Current source $J_2$ is set to the maximum input current swing $I_{in,max}$, which results in $i_{D4} = I_{in,max} - i_{D2}$. Current mirrors M4-M5 and M6-M7 have a unity current gain such that $i_{D7} = I_{in,max} - i_{D2}$. M7 injects the negative feedback current $i_{D7}$ to

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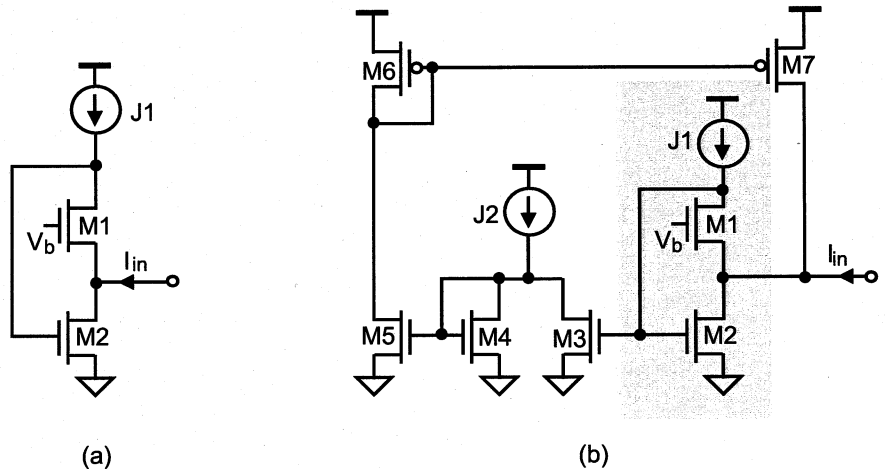


Figure 3.3: (a) Wu's current reuse active inductors. (b) Proposed constant-$Q$ active inductor. Circuit parameters : $J_1 = 400\mu$A, $J_2 = 3$mA, $W_1 = 30\mu$m, $W_2 = 25\mu$m, $W_3 = 25\mu$m, $W_4 = 20\mu$m, $W_5 = 20\mu$m, $W_6 = 30\mu m$, $W_7 = 30\mu m$, $L = 0.18\mu$m for all transistors.

the input terminal of the active inductor and maintains the drain current of M2 at a constant level, ensuring that both the inductance and quality factor of the active inductor remain unchanged in the presence of a input current swing. The inductance of the proposed active inductor is shown in Fig.3.4. The instantaneous quality factor of Wu's active inductors and the proposed constant-Q active inductor at 2.4 GHz are plotted in Fig.3.5 to provide a comparison. The use of a current feedback network which mirrors the large input current increases the power consumption to 3 times that of the original Wu active inductors.

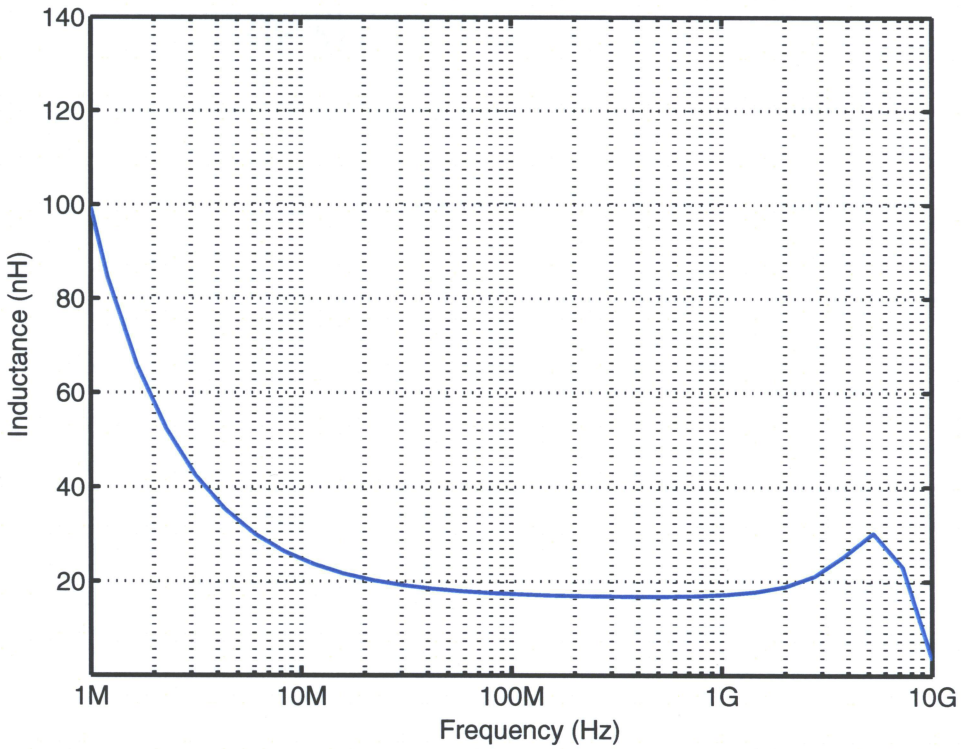


Figure 3.4: Inductance of the proposed constant-Q active inductor.

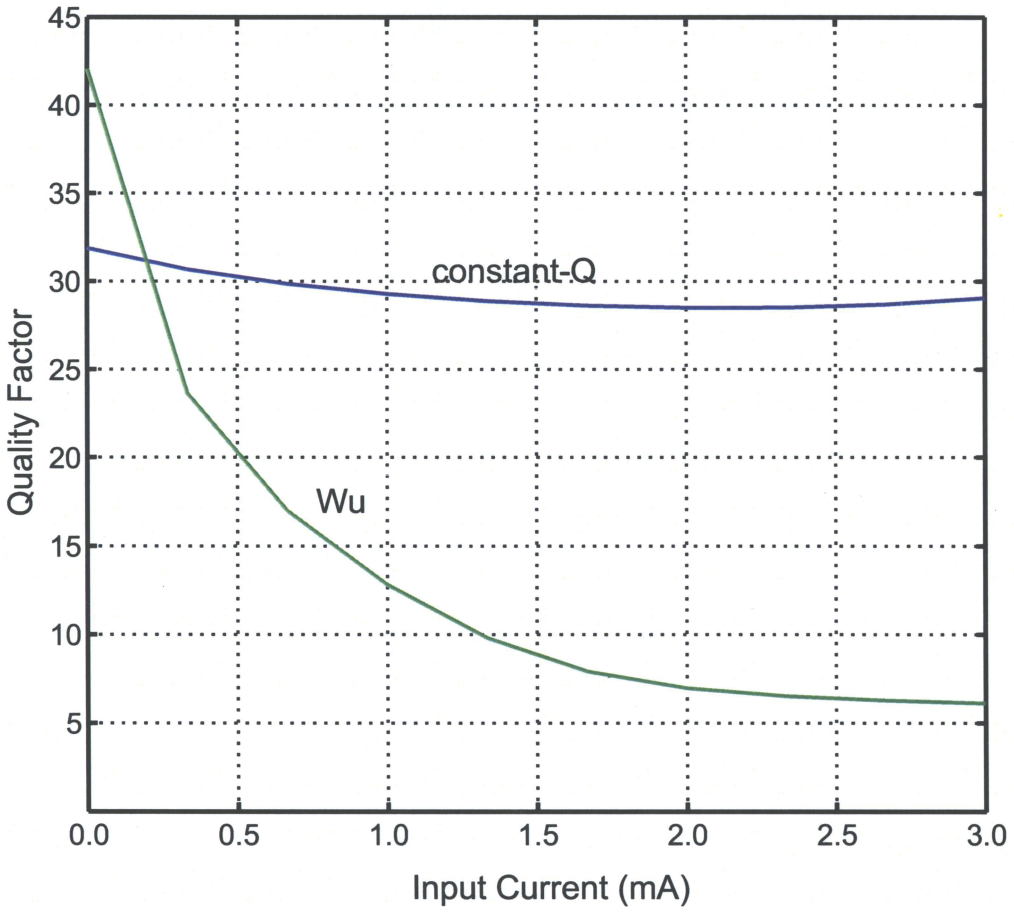


Figure 3.5: Dependence of the quality factor of Wu's active inductors and the proposed constant-Q active inductor on their input currents at 2.4 GHz.

# CHAPTER 4

# CMOS ACTIVE TRANSFORMERS

## 4.1 CMOS Linear Active Transformer Circuits and Characterization

In this section, CMOS linear active transformers are proposed which have evolved from Wu's original gyrator-C active inductors shown in Fig.4.1a. The input impedance of Wu's active inductors is given by

$$z_{in}(s) = \frac{g_o}{C_{gs}^2} \frac{s\frac{C_{gs}}{g_o} + 1}{s^2 + s\frac{g_m}{C_{gs}} + \frac{g_m^2}{C_{gs}^2}}, \tag{4.1}$$

where $C_{gd}$ and parasitic junction capacitances were neglected and $C_{gs1} = C_{gs2} = C_{gs}$, $g_{m1} = g_{m2} = g_m$, $g_{o1} = g_{o2} = g_o$ were assumed as all transistors have identical dimension and biasing. The frequency of the zero and the self-resonant frequency of the active inductor are given by $\omega_{z,p} = \frac{g_o}{C_{gs}}$ and $\omega_{o,p} = \frac{g_m}{C_{gs}}$, respectively. The active inductor is inductive when $\omega_{z,p} < \omega < \omega_{o,p}$ with the inductance $L \approx \frac{C_{gs}}{g_m^2}$. The schematic of the proposed CMOS linear active transformer is shown in Fig.4.1b with both PMOS and NMOS configurations. The transformer consists of a primary winding with its terminal P and a secondary winding accessed via the terminal S. The coupling from primary to secondary is achieved using a voltage-

controlled current source link via the gate of $M_3$ such that there is no direct current path from the primary winding to the secondary winding. It should be noted that the mutual inductance is unidirectional, from the primary winding to the secondary winding. The coupling coefficient, $K_{21}$ is given by $K_{21} = \frac{W_3 L_1}{W_1 L_3}$, the gain of the current mirror.

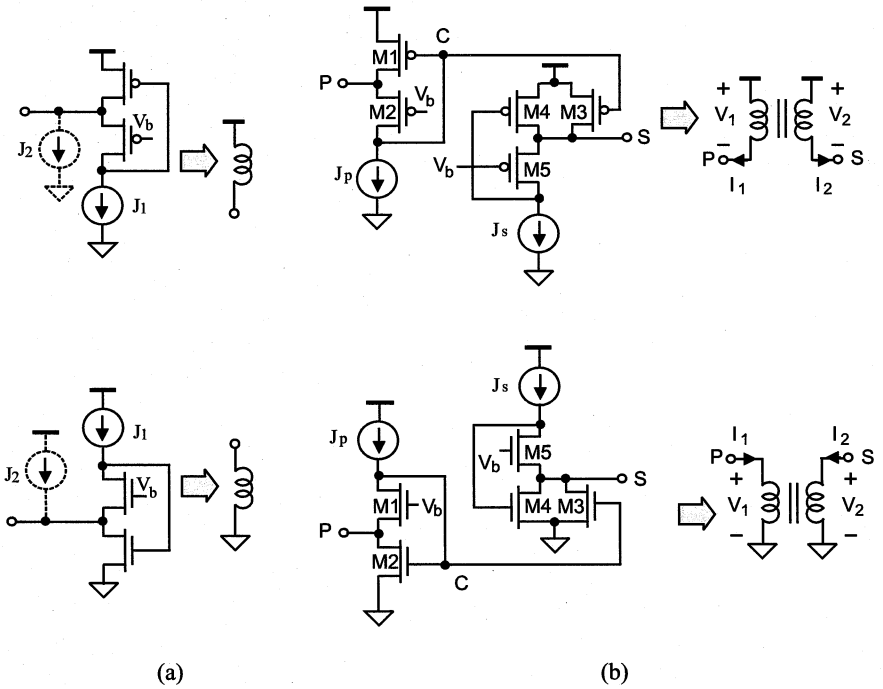


Figure 4.1: (a) Wu's original active inductors. (b) Proposed unidirectional single-winding linear active transformers. Circuit parameters for simulations : $W_1 = 45\mu$m, $W_2 = 50\mu$m, $W_3 = 50\mu$m, $W_4 = 50\mu$m, $W_5 = 40\mu$m. $L = 0.18\mu$m for all transistors.

The self-inductance of the primary winding is given by $L_p \approx \frac{C_{gs}}{g_m^2}$. The loading effect of the secondary winding via the gate-source capacitance of $M_3$ increases the self-inductance of the primary winding but lowers it's self-resonant frequency. The expression for $V_c$, the voltage at the coupling node labeled C in Fig.4.1 is obtained by isolating $V_2$ in (2.15) of the primary winding as $V_{2p} = V_c$

$$V_c(s) \approx \frac{g_m}{C_{gs}^2} \frac{I_1}{s^2 + s\frac{g_m}{C_{gs}} + \left(\frac{g_m}{C_{gs}}\right)^2}. \tag{4.2}$$

Note that $g_o \ll g_m$ was utilized in derivation of (4.2).

Transistors $M_{3\sim4}$ have the same output impedance $g_o$, gate-source capacitance $C_{gs}$, and transconductance $g_m$. $C_{gs3}$ is in parallel with $C_{gs1}$ and has been considered in the analysis of the primary winding. The channel current of $M_3$ is controlled by $V_c$ from the primary winding. Adjusting (2.15) to include the current source link from the primary to secondary we have

$$\begin{aligned} I_{in} &= g_o(V_1 - V_2) + g_o V_1 + g_m V_1 + g_m V_2 + V_1 s C_{gs} + g_m V_c \\ 0 &= g_o(V_2 - V_1) - g_m V_1 + s C_{gs} V_2. \end{aligned} \tag{4.3}$$

Solving for $V_1$ we obtain the voltage at the secondary terminal $V_{sec}$,

$$V_{sec}(s) = \frac{g_o}{C_{gs}^2} \frac{(s\frac{C_{gs}}{g_o} + 1) g_m V_c + (s\frac{C_{gs}}{g_o} + 1) I_2}{s^2 + s\frac{g_m}{C_{gs}} + \frac{g_m g_{m5}}{C_{gs}^2}}. \tag{4.4}$$

This expression has a zero at frequency $\omega_{z,s} = \frac{g_o}{C_{gs}}$ and the self-resonant frequency $\omega_{o,s} = \frac{\sqrt{g_m g_o}}{C_{gs}}$ indicating that the secondary winding is inductive when $\omega_{z,s} < \omega < \omega_{o,s}$. Note that $\omega_{o,s} < \omega_{o,p}$.

Fig.4.2 shows the self inductance and Fig.4.3 shows the mutual inductance from the primary winding to the secondary winding of the proposed linear active transformer for the NMOS configuration. Fig.4.4 plots the DC coupling from the

primary winding to the secondary winding of the proposed active transformer for the NMOS configuration showing that the windings are well isolated for small DC currents.

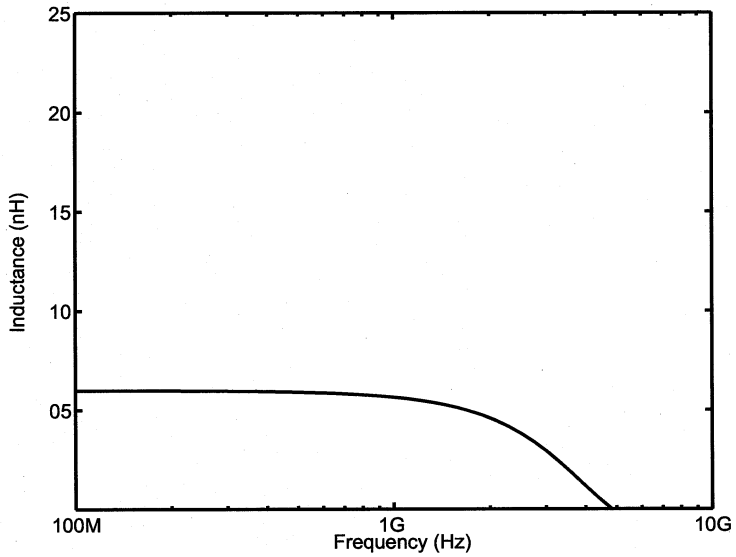


Figure 4.2: Self inductance of the proposed CMOS linear active transformer.

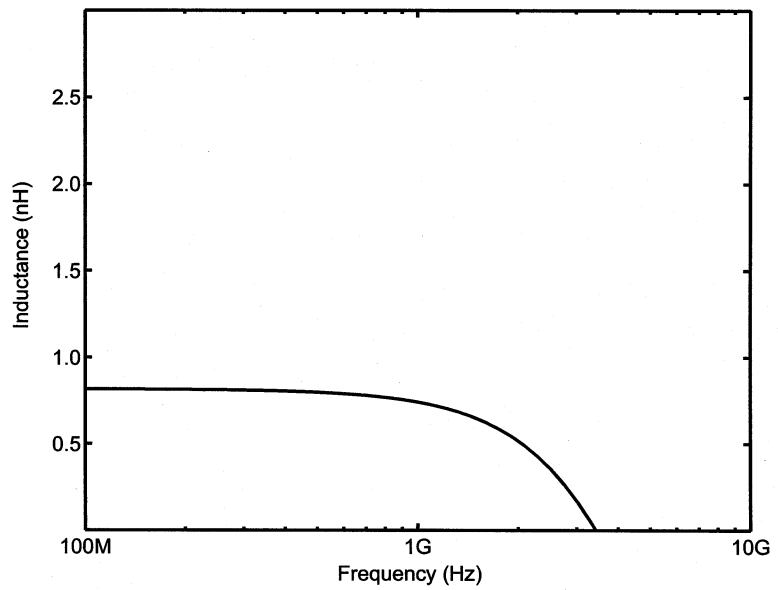


Figure 4.3: Mutual inductance of the proposed CMOS linear active transformer.

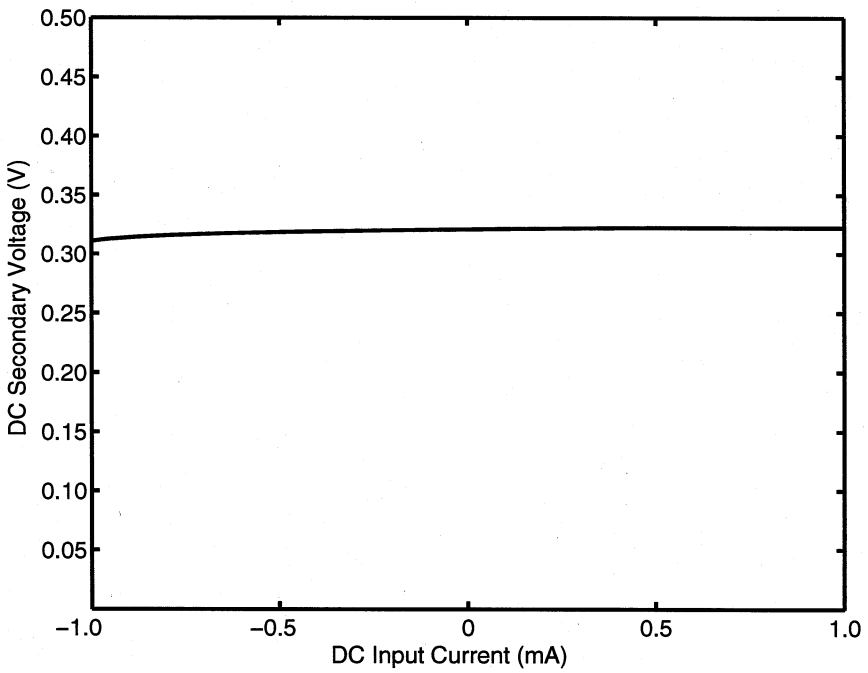


Figure 4.4: DC coupling of the proposed CMOS linear active transformer from primary to secondary winding.

### 4.1.1 Noise

The thermal and flicker noise of transistor $j$ are represented by an equivalent noise current source in the channel with its power given by,

$$\overline{i_{n,j}^2} = (4kTg_m\gamma + \frac{K_f I_j}{f})\Delta f, \tag{4.5}$$

where $k$ is the Boltzmann's constant, $T$ is the temperature in degrees Kelvin, $K_f$ is a CMOS process dependent constant, and $I_j$ is the dc biasing current of the transistor.

To quantify the total noise of the linear active transformer, a noise-voltage generator $\overline{v_n^2}$ and a noise-current generator $\overline{i_n^2}$ at the input of the primary winding are employed to quantify the overall effect of all the noise sources of the transformer at the secondary winding terminal, as shown in Fig.4.5. $\overline{v_n^2}$ and $\overline{i_n^2}$ can be obtained using the conventional approach given in [22]. The noise-current generator is given by,

$$\overline{i_n^2} \approx \left(\frac{g_m}{g_o}\right)^2 [\left(\frac{g_m}{4g_o}\right)^2 \overline{i_{n1}^2} + \frac{1}{16}\overline{i_{n2}^2} + \frac{1}{16}\overline{i_{n3}^2} + \frac{1}{4}\overline{i_{n4}^2} + \overline{i_{n5}^2}]. \tag{4.6}$$

Following similar procedures, one can show that the value of the input-referred noise voltage generator is given by,

$$\overline{v_n^2} \approx \frac{1}{g_o^2}\overline{i_{n2}^2} + \frac{1}{4g_m^2}\overline{i_{n3}^2} + \frac{1}{4g_m^2}\overline{i_{n4}^2} + \frac{1}{g_m^2}\overline{i_{n5}^2}. \tag{4.7}$$

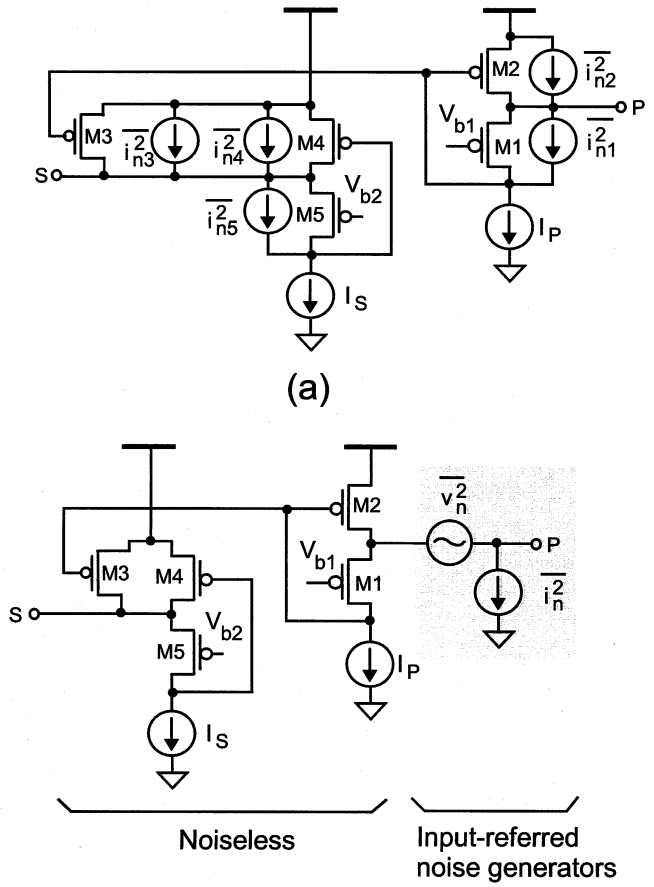


Figure 4.5: (a) Equivalent circuit of linear active transformers with noise sources shown. (b) Referred noise-voltage and noise-current generators.

### 4.1.2 Power Sensitivity.

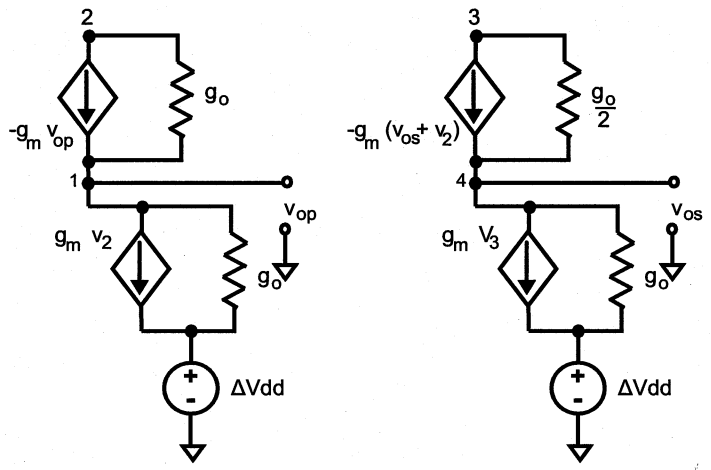


Figure 4.6: Equivalent circuit of linear active transformers with $V_{DD}$ fluctuations shown.

When switching noise exists, the supply voltage is changed from $V_{DD}$ to $V_{DD}+\Delta V_{DD}$, where $\Delta V_{DD}$ is a random variable with $E[\Delta V_{DD}] = 0$, where $E[.]$ denotes mathematical mean operation. Power sensitivity, denoted by $S_{V_{DD}}^{v_o}$ and defined as $S_{V_{DD}}^{v_o} = \frac{\partial v_o}{\partial V_{DD}}$, quantifies the effect of the variation of the supply voltage on the performance of active transformers. For practical circuits, because $\Delta V_{DD} \ll V_{DD}$ holds, the small-signal analysis approach shown in Fig.4.6 can be employed to compute $S_{V_{DD}}^{v_o}$. Writing the KCL for nodes 1 2,3 and 4 in Fig.4.6

$$
\begin{aligned}
g_m v_2 + (v_{op} - \Delta V_{DD})g_o + (v_{op} - v_2)g_o + g_m v_{op} &= 0, \qquad (4.8)\\
-g_m v_{op} + (v_2 - v_{op})g_o &= 0,\\
-g_m(v_{os} + v_2) + \frac{1}{2}g_o(v_3 - v_{os}) &= 0,\\
g_m v_3 + g_m(v_{os} + v_2) + g_o(v_{os} - \Delta V_{DD}) + \frac{1}{2}g_o(v_{os} - v_3) &= 0,
\end{aligned}
$$

and isolating both $\frac{v_o p}{\Delta V_{DD}}$ and $\frac{v_o s}{\Delta V_{DD}}$ the sensitivities of the voltage of the primary and secondary winding terminals, denoted by $S_{V_{DD}}^{v_p}$ and $S_{V_{DD}}^{v_s}$, can be found

$$\begin{aligned} S_{V_{DD}}^{v_p} &= \frac{\partial v_p}{\partial V_{DD}} \approx \frac{g_o}{g_m}, \\ S_{V_{DD}}^{v_s} &= \frac{\partial v_s}{\partial V_{DD}} \approx \frac{2g_o}{g_m} + \frac{g_o^2}{g_m^2} \end{aligned} \tag{4.9}$$

Eq.(4.9) reveals that the secondary winding is more sensitive to supply voltage fluctuation. This is because of the output impedances $g_{o3}$,$g_{o4}$ contributed from M3 and M4 are in parallel. The second term represents the contribution of $\Delta V_{DD}$ from primary to secondary winding and is quite small. Fig.4.7 shows the die photo of the linear active transformer implemented in TSMC CMOS 0.18$\mu$m technology.

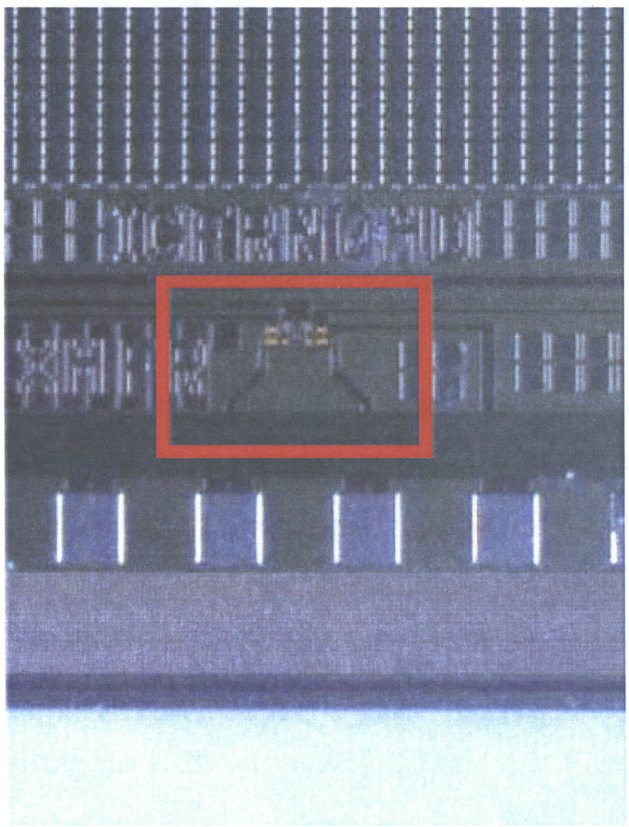

Figure 4.7: Die photo of CMOS linear active transformer in TSMC CMOS 0.18$\mu$m technology.

## 4.2 CMOS Linear Active Transformers with Multiple Windings

Linear active transformers can be constructed with multiple secondary windings as shown in Fig.4.8. The loading effect created by multiple secondary windings contributes to the gate capacitance of $M_1$, lowering the self-resonant frequency of the primary winding. Note that the coupling ratio between the primary winding and each secondary winding can be different and tuned by varying the dc biasing condition of the secondary winding or the current mirror dimensions. Active transformers can also be constructed with multiple primary windings and a single secondary winding as shown in Fig.4.8. Linear active transformers can also be constructed in a bidirectional configuration as shown in Fig.4.9. This configuration provides coupling in both directions between the primary and secondary windings. Fig.4.10 shows the self and mutual inductance of the bidirectional configuration.

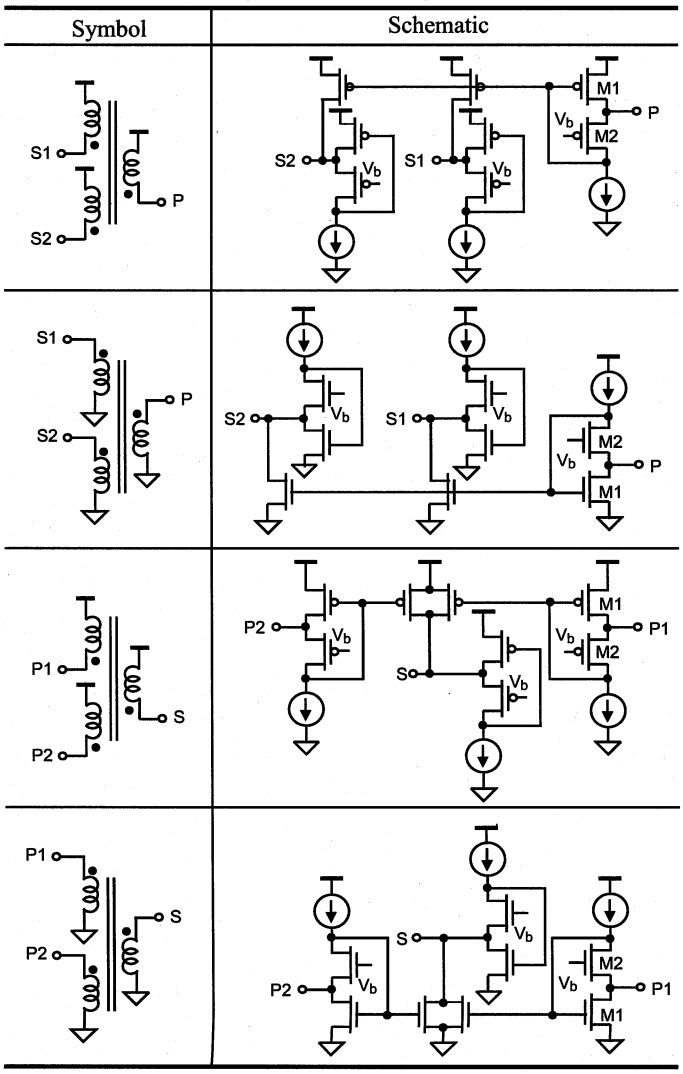


Figure 4.8: Unidirectional CMOS linear active transformers with multiple windings.

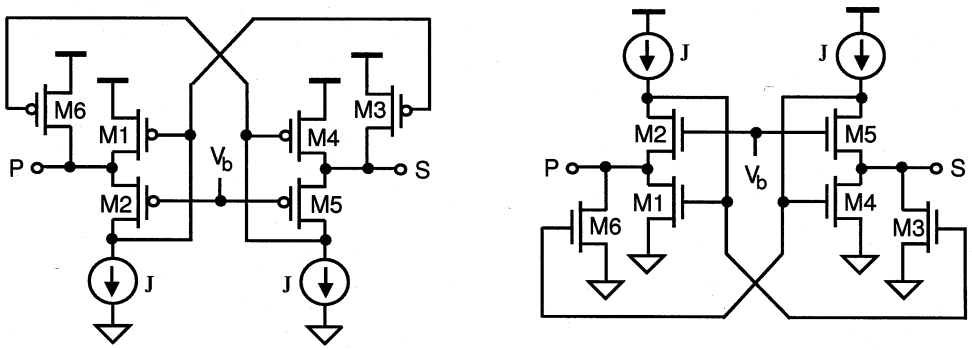


Figure 4.9: Bidirectional linear active transformers with single winding. Circuit parameters for simulations : $W_1 = 40\mu$m, $W_2 = 45\mu$m, $W_3 = 20\mu$m, $W_4 = 50\mu$m, $W_5 = 45\mu$m, $W_6 = 20\mu$m, $J = 550\mu A$.

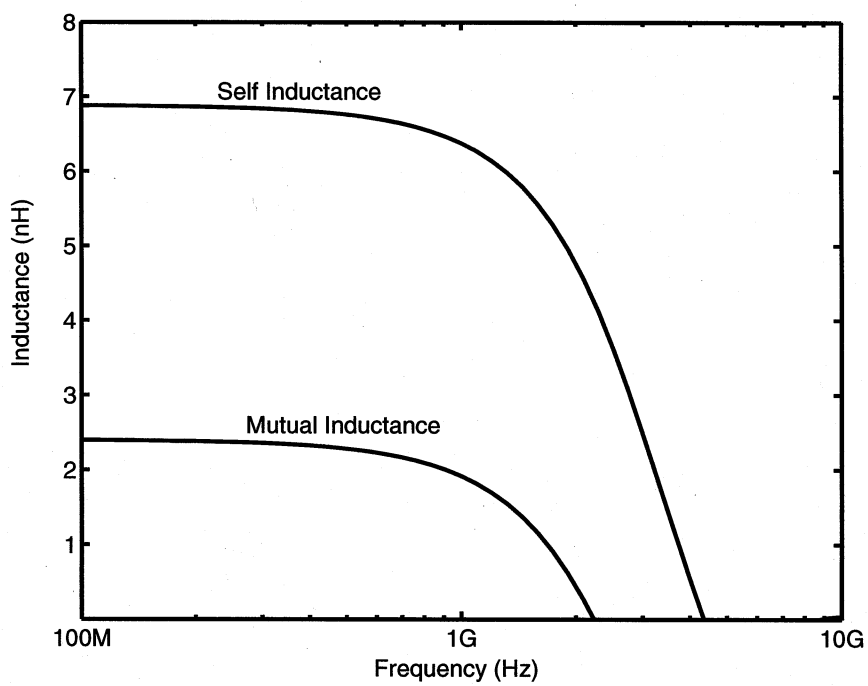


Figure 4.10: Self and mutual inductance of bidirectional CMOS linear active transformer.

## 4.3 Cascode Active Transformer Circuits and Characterization

This section proposes CMOS cascode active transformers, which employ a cascode configuration to improve the supply sensitivity and inductance characteristics of the linear active transformer. The schematic of the proposed CMOS cascode active transformers is shown in Fig.4.11. The transformer consists of a primary winding with its terminal $P$ and a secondary winding accessed via the terminal $S$. The primary is realized using Wu's current-reuse active inductors. The coupling from the primary winding to the secondary winding is achieved using a voltage-controlled current source link via the gate of $M_3$ such that there is no direct current path from the primary winding to the secondary winding. As a result, both windings can be biased and tuned individually. $M_{1\sim3}$ form a low input-impedance current mirror between the primary and secondary windings with the input impedance seen from the primary winding given by

$$z_{in,p} \approx \frac{1}{g_{m1}(g_{m2}r_{o2})} \tag{4.10}$$

at low frequencies [21], where the subindex $p$ identifies the primary winding. It should be noted that in the proposed cascode active transformers the mutual inductance is unidirectional, from the primary winding to the secondary winding. This is the same as the linear active transformer discussed earlier.

The primary winding is identical to Wu's current-reuse active inductors presented earlier. Note that the loading effect of the secondary winding via the gate-source capacitance of $M_3$ increases the self-inductance of the primary winding but lowers it self-resonant frequency. The expression for $V_c$, the voltage at

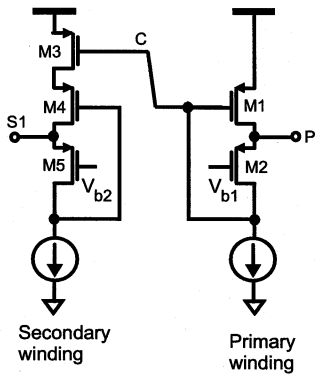


Figure 4.11: CMOS cascode active transformer. PMOS configuration shown. Circuit parameters for simulations: all transistors $W = 50\mu$m, $L = 0.18\mu$m.

the coupling node labeled C in Fig. 4.11 is obtained by solving the primary winding small signal equivalent circuit. Assuming all transistors have the same dimensions, biasing conditions, and the same tranconductance $g_m$ the voltage at the coupling node is given by

$$V_c \approx \frac{g_m}{(2C_{gs})^2} \frac{I_1}{s^2 + s\frac{g_m}{2C_{gs}} + \left(\frac{g_m}{2C_{gs}}\right)^2}. \tag{4.11}$$

Note that $g_o \ll g_m$ was utilized in derivation of (4.11).

Fig.4.12 shows the small-signal equivalent circuit of the secondary winding of the proposed cascode active transformer. As the circuit differs from the original Wu active inductor, it is necessary to develop the basic small-signal expressions. All transistors are biased in the saturation with identical dimension. As a result, $M_{3\sim5}$ have the same output impedance $g_o$, gate-source capacitance $C_{gs}$, and transconductance $g_m$. The $C_{gs}$ of M3 is in parallel with the $C_{gs}$ of M1 and has been considered in the analysis of the primary winding. The channel current of $M_3$ is controlled by $V_c$ from the primary winding. Write KCL at nodes 1, 2, and

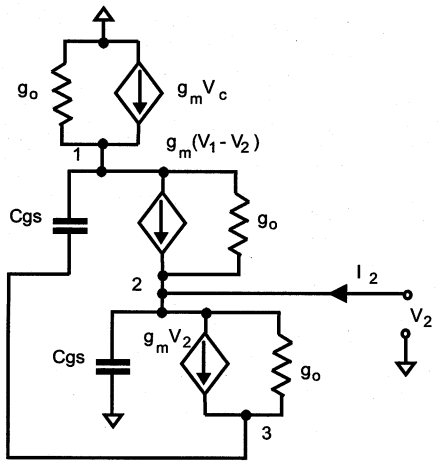


Figure 4.12: Small-signal equivalent circuit of the secondary winding of the proposed active transformer.

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$$(sC_{gs} + g_m + 2g_o)V_1 - g_o V_2 - (sC_{gs} + g_m)V_3 = -g_m V_c,$$

$$-(g_m + 2g_o)V_1 + (sC_{gs} + g_m + g_o)V_2 - (g_m - g_o)V_3 = I_2,$$

and

$$-sC_{gs}V_1 - (g_m + g_o)V_2 + (sC_{gs} + g_o)V_3 = 0. \tag{4.12}$$

To simplify analysis, we assume $g_m \gg g_o$. From (4.12)

$$V_3 \approx \frac{sC_{gs}}{sC_{gs}+g_o}V_1 + \frac{g_m}{sC_{gs}+g_o}V_2. \tag{4.13}$$

Substituting (4.13) into (4.12), we arrive at

$$g_o V_1 - g_m V_2 = -\frac{g_m(sC_{gs}+g_o)}{sC_{gs}+g_m}V_c. \tag{4.14}$$

Eq.(4.12) is simplified to

$$-g_m V_1 + (sC_{gs}+g_m)V_2 + g_m V_3 = 0. \tag{4.15}$$

Substituting (4.13) into (4.15), we arrive at

$$-g_m g_o V_1 + (s^2C_{gs}^2 + sC_{gs}g_m + g_m^2 + g_m g_o)V_2 = (sC_{gs}+g_o)I_2. \tag{4.16}$$

Solve (4.14) and (4.16) for $V_2$

$$\begin{aligned} V_2 &= \frac{sC_{gs}+g_o}{s^2C_{gs}^2 + sC_{gs}g_m + g_m g_o}I_2 \\ &- \frac{g_m^2(sC_{gs}+g_o)}{(sC_{gs}+g_m)(s^2C_{gs}^2 + sC_{gs}g_m + g_m g_o)}V_c. \end{aligned} \tag{4.17}$$

Examining (4.17) in detail :

- The expression for $V_c$ was already obtained by solving the primary winding

of the cascode transformer and is given by (4.11).

- When $V_c = 0$, i.e. the primary winding is in the dc steady state and the secondary winding is excited by $I_2$. The input impedance looking into the secondary winding is given by

$$z_{in2} = \frac{sC_{gs} + g_o}{s^2C_{gs}^2 + sC_{gs}g_m + g_m g_o}. \tag{4.18}$$

It has a zero at frequency

$$\omega_{z,s} = \frac{g_o}{C_{gs}} \tag{4.19}$$

and the self-resonant frequency

$$\omega_{o,s} = \sqrt{\frac{g_m g_o}{C_{gs}^2}}. \tag{4.20}$$

The secondary winding is therefore inductive when $\omega_{z,s} < \omega < \omega_{o,s}$. Note that because $g_o < g_m$, $\omega_{o,s} < \omega_{o,p}$. The secondary winding has a lower self-resonant frequency as compared with that of the primary winding.

- When $I_2 = 0$, $V_2$ is solely due to $V_c$, which comes from the primary winding. In this case, the zero is at the frequency

$$\omega_z = \frac{g_o}{C_{gs}} \tag{4.21}$$

and the dominant pole is at

$$\omega_p = \frac{g_m}{C_{gs}}. \tag{4.22}$$

As seen in Fig.4.13 the inductance of the cascode active transformer is much higher than that of the linear active transformer although the upper frequency limit is lower.

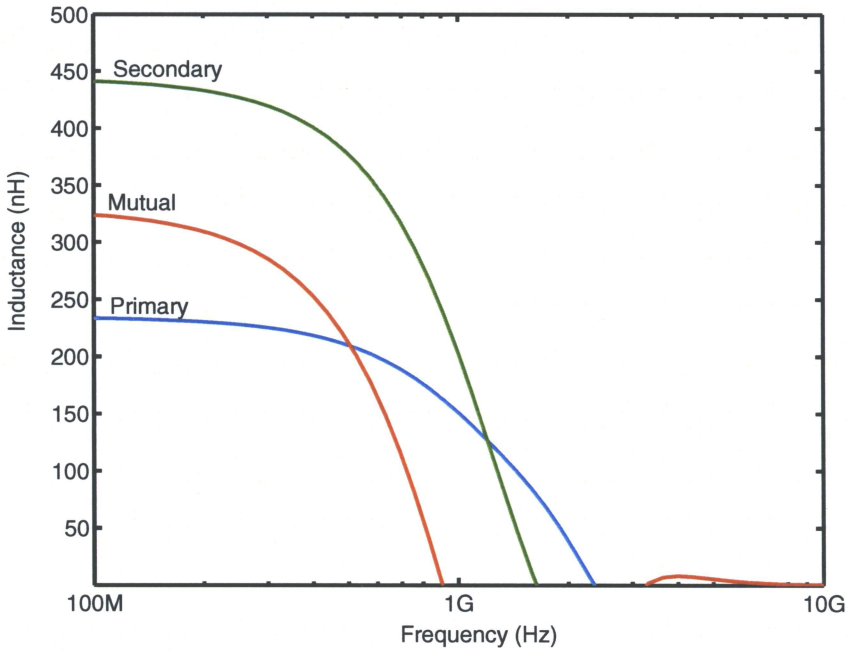


Figure 4.13: Inductance of cascode active transformers.

### 4.3.1 Noise

As in the noise analysis of the linear transformer, the thermal and flicker noise of transistor $j$ are represented by an equivalent noise current source in the channel with its power given by

$$\overline{i_{n,j}^2} = (4kTg_m\gamma + \frac{K_f I_j}{f})\Delta f, \tag{4.23}$$

where $k$ is Boltzmann's constant, $T$ is the temperature in degrees Kelvin, $K_f$ is a process dependent constant, and $I_j$ is the dc biasing current of the transistor. To quantify the total noise of the active transformer, a noise-voltage generator $\overline{v_n^2}$ and a noise-current generator $\overline{i_n^2}$ at the input of the primary winding are employed to quantify the overall effect of all the noise sources of the transformer at the secondary winding terminal, as shown in Fig.4.14. $\overline{v_n^2}$ and $\overline{i_n^2}$ can be obtained using the conventional approach given in [22]. The output noise power measured at the secondary winding due to all the noise sources of the transformer with the primary winding terminal open-circuited is given by

$$\overline{v_o^2} = \frac{\overline{i_{n1}^2}}{g_m^2} + \left(\frac{g_o}{g_m}\right)^2 \frac{\overline{i_{n2}^2}}{g_m^2} + \frac{\overline{i_{n3}^2}}{g_m^2} + \left(\frac{g_o}{g_m}\right)^2 \frac{\overline{i_{n4}^2}}{g_m^2} + \frac{\overline{i_{n5}^2}}{g_m^2}. \tag{4.24}$$

The output noise measured at the secondary winding with only $\overline{i_n^2}$ applied to the primary winding terminal and all internal noise sources of the transformer removed is given by

$$\overline{v_o^2} = \left(\frac{1}{g_m}\right)^2 \overline{i_n^2}. \tag{4.25}$$

Equating (4.24) and (4.25) yields

$$\overline{i_n^2} = \overline{i_{n1}^2} + \overline{i_{n3}^2} + \overline{i_{n5}^2} + \left(\frac{g_o}{g_m}\right)^2\left[\overline{i_{n2}^2} + \overline{i_{n4}^2}\right], \tag{4.26}$$

$$\tag{4.27}$$

Following similar procedures, one can show that the power of input-referred noise voltage generator is given by

$$\overline{v_n^2} = \left(\frac{g_o}{g_m}\right)^2\left[\frac{1}{g_m^2}(\overline{i_{n2}^2} + \overline{i_{n3}^2} + \overline{i_{n5}^2}) + \left(\frac{g_o}{g_m}\right)^2\overline{i_{n4}^2}\right]. \tag{4.28}$$

The preceding results reveal that because $g_m \gg g_o$, $\overline{i_{n1}^2}$, $\overline{i_{n3}^2}$, and $\overline{i_{n5}^2}$ dominate both $\overline{i_n^2}$ and $\overline{v_n^2}$.

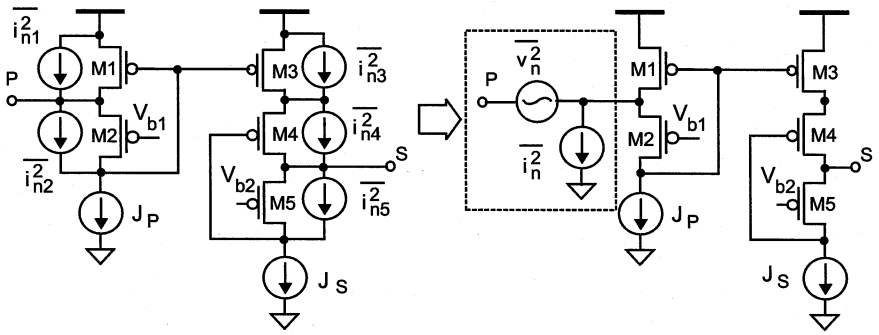


Figure 4.14: Noise equivalent circuit of cascode active transformers.

### 4.3.2 Power Sensitivity

When switching noise exists, the supply voltage is changed from $V_{DD}$ and $V_{DD} + \Delta V_{DD}$, where $\Delta V_{DD}$ is a random variable with $E[\Delta V_{DD}] = 0$, where $E[.]$ denotes mathematical mean operation. Power sensitivity, denoted by $S_{V_{DD}}^{v_o}$ and defined as

$$S_{V_{DD}}^{v_o} = \frac{\partial v_o}{\partial V_{DD}}, \tag{4.29}$$

quantifies the effect of the variation of the supply voltage on the performance of active transformers. For practical circuits, because $\Delta V_{DD} \ll V_{DD}$ holds, the small-signal analysis approach can be employed to compute $S_{V_{DD}}^{v_o}$. It can be shown using the same procedure as in section 4.1.2 that the sensitivities of the voltage of the primary and secondary winding terminals, denoted by $S_{V_{DD}}^{v_p}$ and $S_{V_{DD}}^{v_s}$, respectively, are given by

$$\begin{aligned} S_{V_{DD}}^{v_p} &= \frac{\partial v_p}{\partial V_{DD}} \approx \frac{g_o}{g_m}, \\ S_{V_{DD}}^{v_s} &= \frac{\partial v_s}{\partial V_{DD}} \approx \left(\frac{g_o}{g_m}\right)^2, \end{aligned} \tag{4.30}$$

Eq.(4.30) reveals that the primary winding is more sensitive to supply voltage fluctuation than the secondary winding. This is different behavior than the linear active transformer where the secondary is more sensitive to supply fluctuation. This is due to the cascode shielding effect of $M_3$. $S_{V_{DD}}^{v_s}$ can be written as,

$$S_{V_{DD}}^{v_s} = \frac{S_{V_{DD}}^{v_p}}{g_m r_o}, \tag{4.31}$$

which clearly shows the cascode shielding effect of $M_3$ in the denominator.

## 4.4 Cascode Active Transformers with Multiple Windings.

Cascode active transformers can be constructed with multiple secondary windings as shown in Fig.4.15. The loading effect created by multiple secondary windings contributes to the gate capacitance of $M_1$, lowering the self-resonant frequency of the primary winding. Note that the coupling ratio between the primary winding and each secondary winding can be different and tuned by varying the dc biasing condition of the secondary winding.

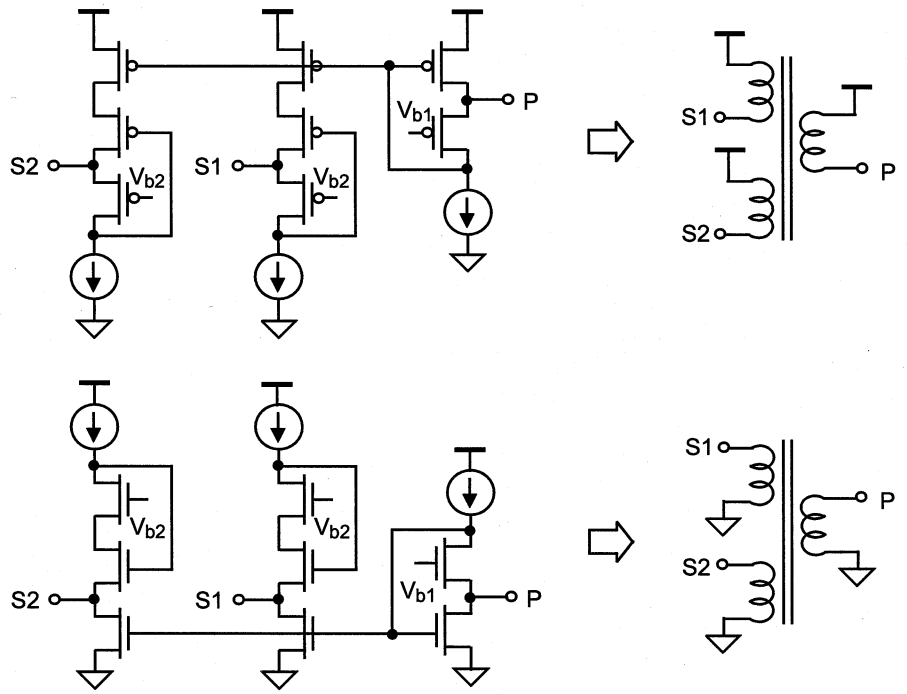


Figure 4.15: Cascode active transformers with one primary winding and multiple secondary windings.

Active transformers can also be constructed with multiple primary windings and single secondary winding as shown in Fig.4.16. The cascode active transformer can also be implemented as a bidirectional transformer as shown in

Fig.4.17 and enable signals to flow in both directions.

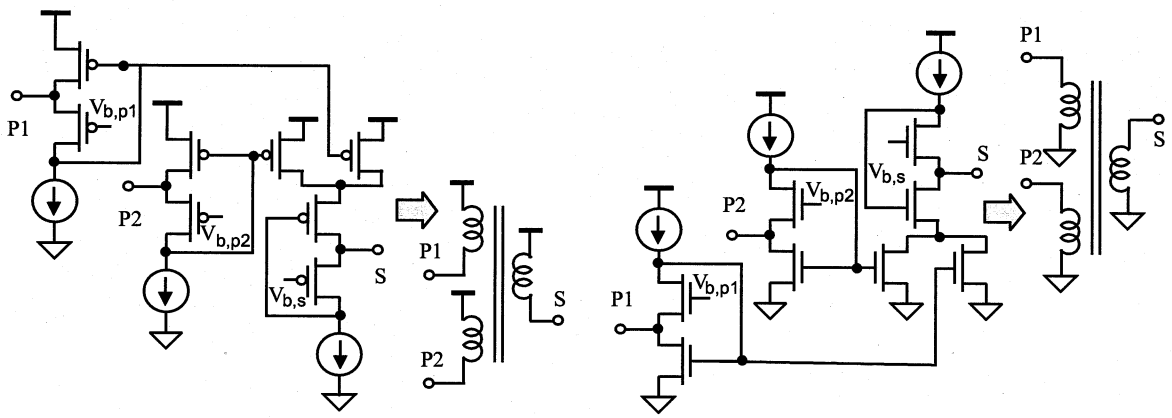


Figure 4.16: Cascode active transformers with multiple primary windings and one secondary winding.

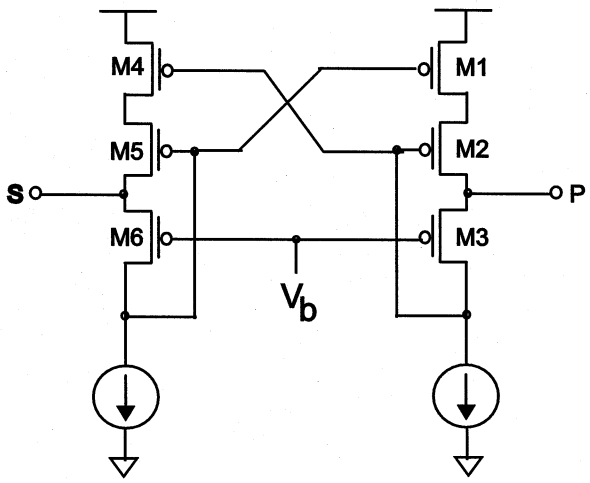


Figure 4.17: Bidirectional cascode active transformer.

## 4.5 Class-AB CMOS Active Transformers.

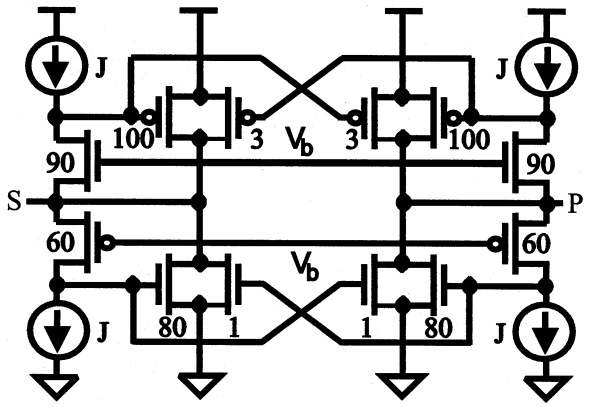


Figure 4.18: Class AB CMOS active transformer. All device length is 180nm, widths are as shown.

Active inductors and active transformers suffer from a higher level of distortion than their passive counterparts, particularly the distortion in class A CMOS active transformer VCOs when the swing is made large, contributes greatly to the phase noise. Reducing the swing to provide a linear output again will increase the levels of phase noise as the carrier power will decrease. In this section a class AB active transformer is proposed that permits larger output swing without the high distortion levels associated with class A linear active transformers. Fig. 4.18 shows the proposed class AB active transformer. Fig.4.19 shows the self-inductance of the primary and secondary windings (identical due to symmetry) and the mutual inductance between primary and secondary windings. Fig.4.20 shows the input impedance of the primary and secondary windings (identical due to symmetry) and trans-impedance between the primary and secondary windings.

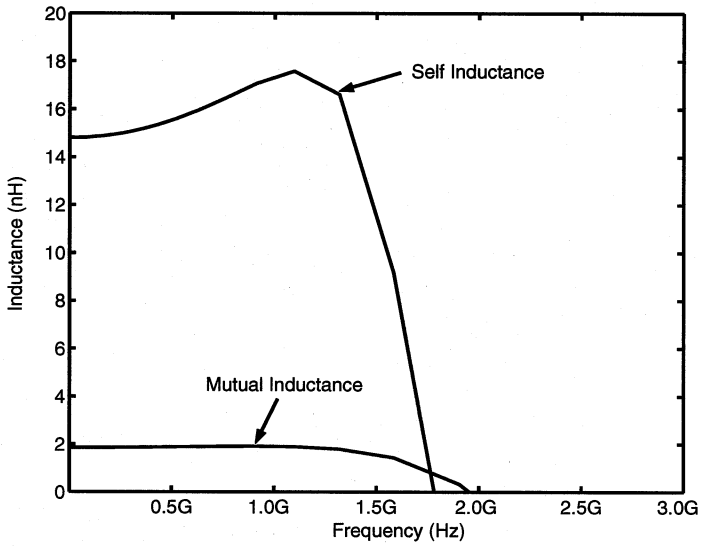


Figure 4.19: Self and mutual inductance of the proposed Class AB CMOS active transformer.

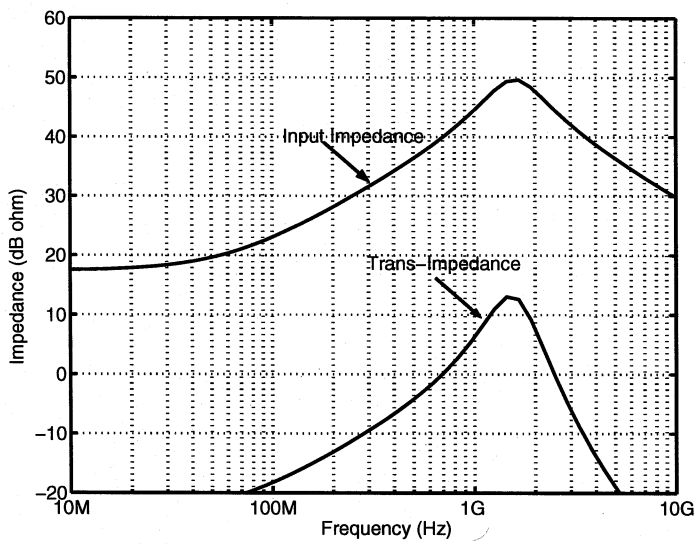


Figure 4.20: Input impedance and trans-impedance of class AB CMOS active transformer.

# CHAPTER 5

# APPLICATIONS

## 5.1 2.4 GHz Voltage Controlled Oscillator

The original proposed application of Wu's active inductors was the construction of LC tank voltage controlled oscillators (VCOs) for RF applications. VCO performance is an excellent way of comparing noise and tuning performance characteristics of active inductors. Five LC oscillators have been constructed as shown in Fig.5.1, an original Wu active inductor LC oscillator, a linear active transformer oscillator, a class AB active transformer oscillator, a constant Q oscillator, and a spiral inductor oscillator. Each oscillator was implemented in TSMC-0.18$\mu$m 1.8V CMOS technology and analyzed using SpectreRF from Cadence Design Systems with BIM3V3 device models that account for device parasitics and high-order effects.

The current J in Fig.5.1 is provided by the same input transconductor structure for each oscillator and is shown in Fig.5.2. The simulations for the tuning range of each oscillator are referred to the transconductor's input voltage.

Table 5.1: Comparison of active and spiral inductor VCOs.

| Feature | Wu | Constant-Q | Spiral | AT | Class AB |
|---|---|---|---|---|---|
| Power | 23.2mW | 37.8mW | 8.4mW | 22.6mW | 25.4mW |
| Area | $680\mu m^2$ | $1440\mu m^2$ | $175000\mu m^2$ | $2140\mu m^2$ | $2720\mu m^2$ |
| MQF | 15 | 28 | 36 | 19 | 23 |

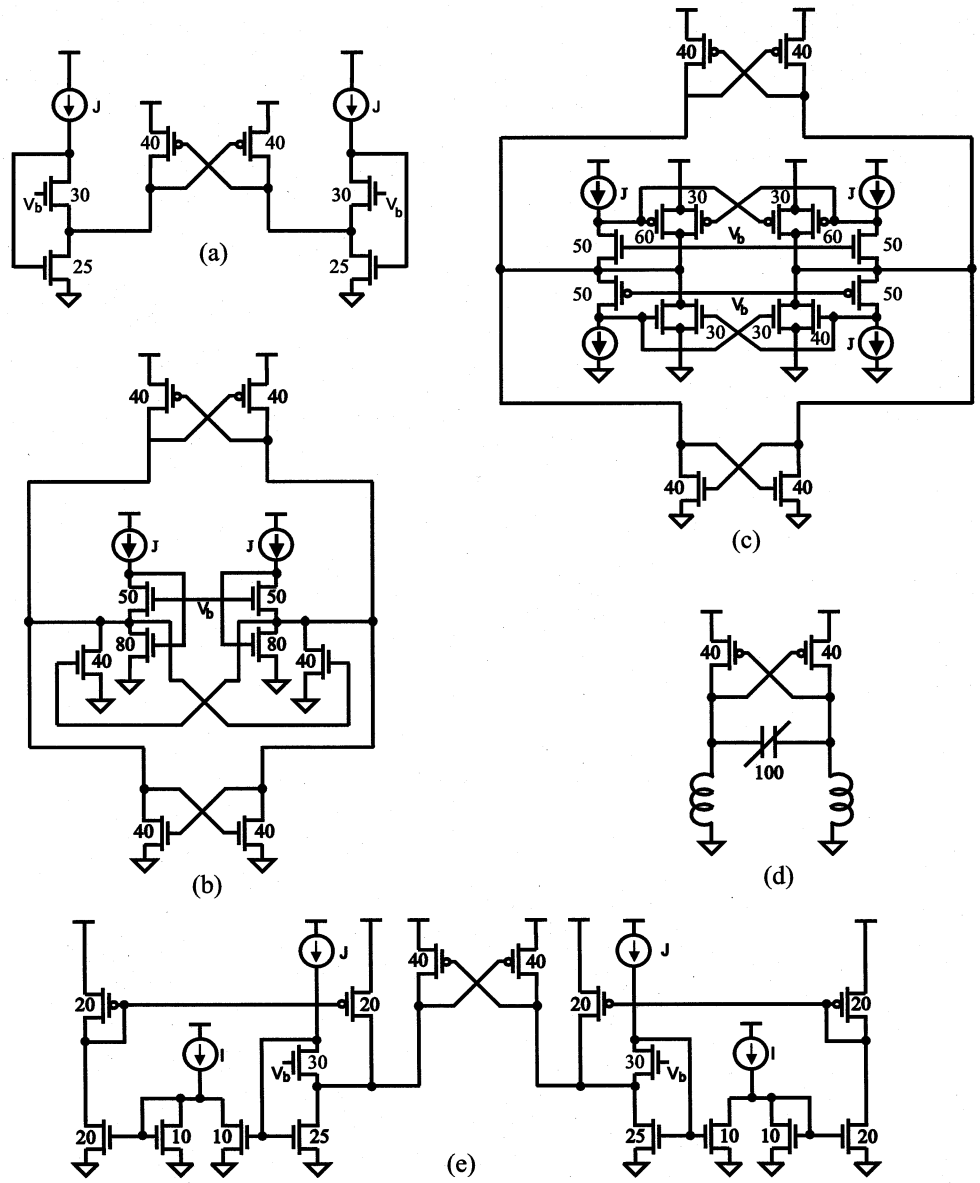


Figure 5.1: (a) Wu active inductor oscillator. (b) Linear active transformer oscillator. (c) Class AB active transformer oscillator. (d) Spiral inductor oscillator. (e) Constant-$Q$ active inductor oscillator. Device dimensions are as shown. $L = 0.18$ for all devices.

The phase noise of the five oscillators is plotted in Fig.5.3. The spiral inductor clearly provides the best phase noise performance, as it is a passive device with no internal noise sources. The constant-Q active inductor oscillator is the quietest

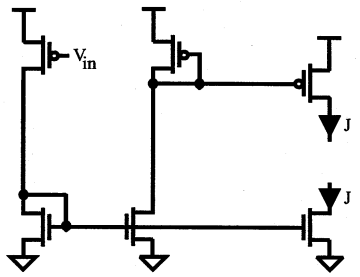


Figure 5.2: Input transconductor.

of the active inductor oscillators with a phase noise of -119.5 dBc/Hz at 1 MHz offset from the carrier. The linear active transformer exhibits a phase noise of -107 dBc/Hz while the class AB active transformer has a phase noise -113.7 dBc/Hz. The original Wu active inductor oscillator is the noisiest of the oscillators with a phase noise of -93 dBc/Hz at 1 MHz offset from the carrier.

The tuning range for each of the five oscillators is plotted in Fig.5.4. The spiral inductor due to its fixed inductance is tuned with a CMOS varactor and has a poor frequency range limited to the 2.4 GHz band. The active inductor based oscillators are all tunable from the 500MHz range to the 2.4 GHz range. Table 5.1 compares the power consumption, silicon area and mean quality factor of the five oscillators. While the constant-$Q$ oscillator does provide the best phase noise performance of the active inductor oscillators, its power consumption is much higher.

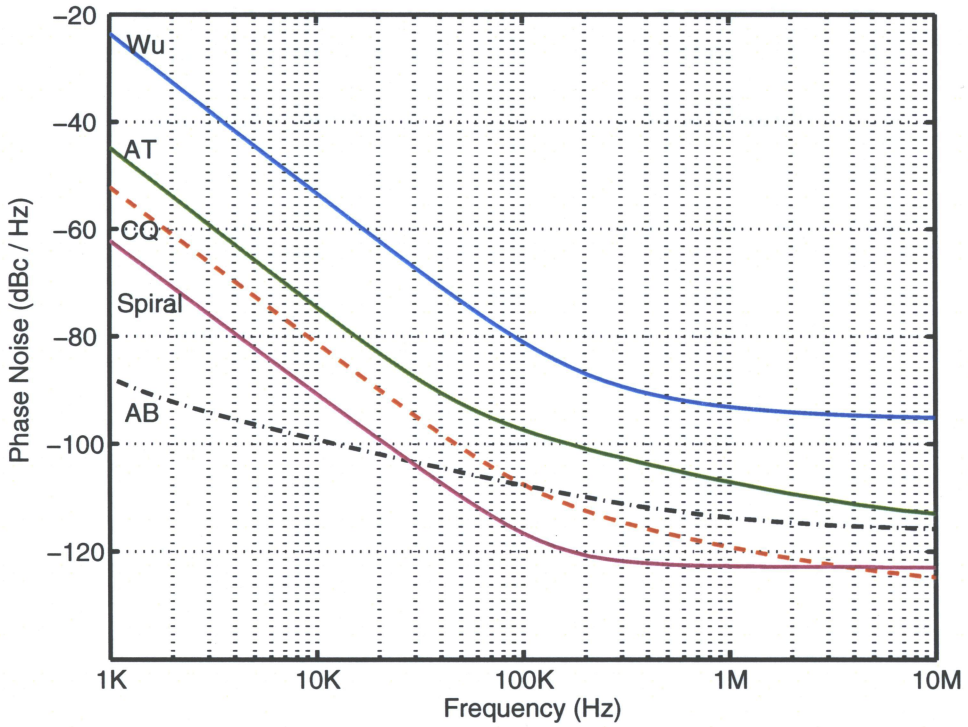


Figure 5.3: Phase noise of active inductor oscillators and spiral oscillators. AT-Linear active transformer, CQ-Constant-$Q$, Wu-Wu active inductor, Spiral-Spiral Inductor, AB-Class AB active transformer.

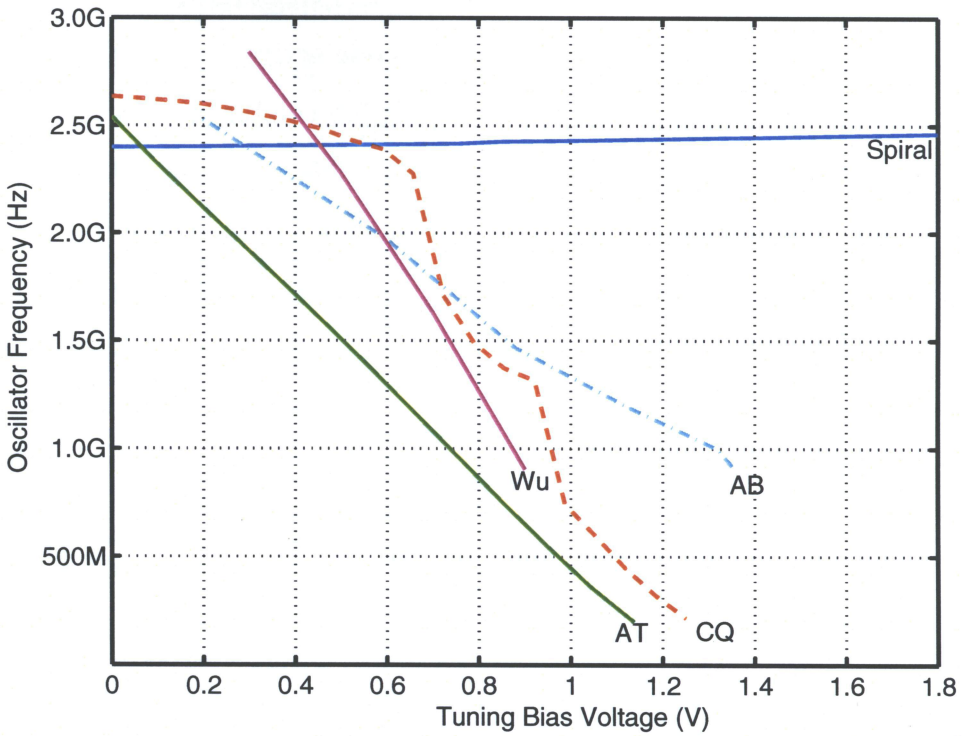


Figure 5.4: Tuning ranges of active inductor oscillators and spiral oscillator. AT Linear active transformer, CQ-Constant-$Q$, Wu-Wu active inductor, Spiral-Spiral Inductor, AB-Class AB active transformer.

## 5.2 2.4 GHz Current-Mode PLL

One of the main drawbacks of voltage-mode PLLs which employ LC oscillators is the need for large spiral inductors to provide low phase noise operation. Voltage mode PLLs also require large capacitors in the loop filter to effectively suppress high- frequency components present on the control line[23, 24]. This application of CMOS cascode active transformers and constant-Q active inductors proposes a new PLL which employs CMOS cascode active transformer current-mode loop filters with configuration shown in Fig.5.5 combined with the constant-Q CCO presented in chapter 3. The current-mode loop filter is constructed using an active transformer with multiple primary windings and a single secondary winding. The large tunable self-inductance of the primary windings of the active transformer enables the loop filter to have a low cut-off frequency while occupying only a small silicon area.

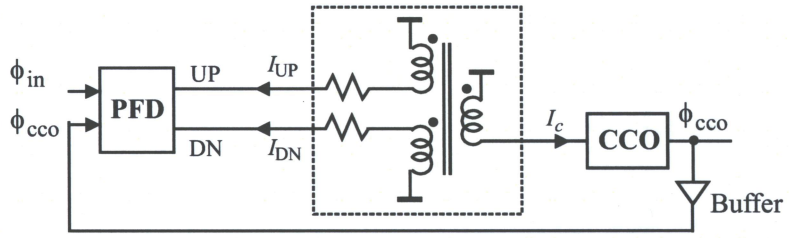


Figure 5.5: Current-Mode PLL with constant-$Q$ CCO and cascode active transformer loop filter.

### 5.2.1 Current-Controlled LC Oscillators with Constant-$Q$ Active Inductors

The constant-$Q$ active inductor is employed in the 2.4 GHz LC current-controlled oscillator as shown in Fig.5.6, and analyzed using SpectreRF from Cadence Design Systems with BSIM3V3 device models that account for device parasitics and high-order effects. Fig.5.7 plots the phase noise of the CCO at the four pro-

cess corners provided by TSMC, namely FF (Fast-nMOS/Fast- pMOS, FS (Fast-nMOS/Slow-pMOS), SF (Slow-nMOS/Fast-pMOS), and SS (Slow-nMOS/Slow-pMOS). Fig.5.8 plots the phase noise of the CCO at varying temperatures from 0 to 60 degrees Celsius and Fig.5.9 shows the phase noise of the oscillator with 10% VDD fluctuations. Note that at each temperature, process corner, and supply voltage, the CCO was re-tuned to 2.4 GHz by adjusting the input current. The phase noise of the oscillator with the proposed constant-$Q$ active inductor is -123.1 dBc/Hz with nominal VDD and process variation at room temperature.

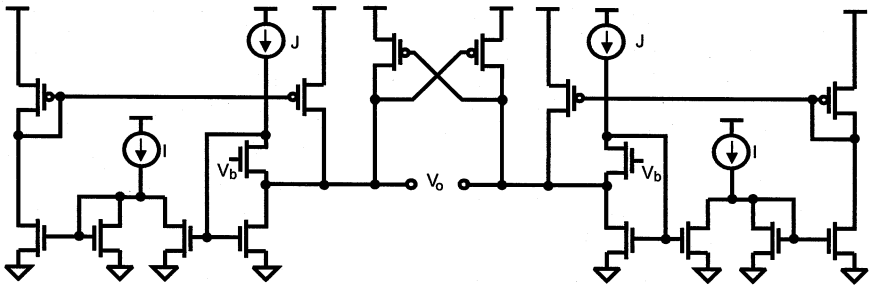


Figure 5.6: Constant-$Q$ Current-controlled oscillator. Switching transistor size: $W = 60\mu$m, $L = 0.18\mu$m

### 5.2.2 Current-Mode Cascode Active Transformer Loop Filter

Current-mode filtering is widely used in power electronics where a constant output current is required. This differs from voltage-mode filtering where sustaining a constant output voltage is the objective. A transformer-based current-mode low-pass filter can be constructed by connecting a resistor in series with the primary winding of a transformer, as shown in Fig.5.10. For current-mode circuits, the

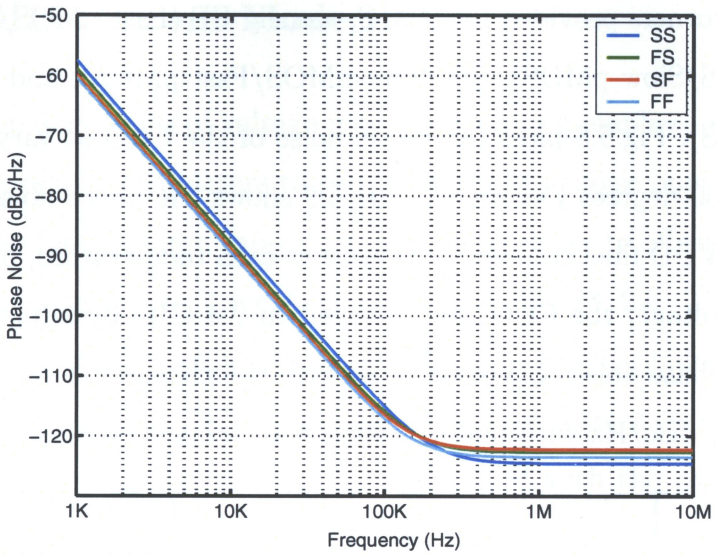


Figure 5.7: Phase noise of 2.4 GHz Constant-$Q$ oscillator at process corners. Note: The CCO was retuned to 2.4GHz at each corner.

load of the secondary winding $R_2$ is ideally zero, this leads to $V_2(s) = 0$. Because

$$\begin{aligned} V_{in}(s) &= R_1 I_1(s) + V_1(s), \\ V_1(s) &= sL_{11} I_1(s) + sM_{12} I_2(s), \\ V_2(s) &= sL_{22} I_2(s) + sM_{21} I_1(s), \end{aligned} \tag{5.1}$$

where $L_{11}$ and $L_{22}$ are the self-inductance of the primary and secondary windings, respectively, $M_{21}$ and $M_{12}$ are the mutual inductance from the primary winding to the secondary winding and that from the secondary winding to the primary winding, respectively, we arrive at

$$\frac{I_2(s)}{V_{in}(s)} = -\frac{M_{21}}{R_1 L_{22}} \frac{1}{s(\frac{L_{11}L_{22} - M_{12}M_{21}}{R_1 L_{22}}) + 1}. \tag{5.2}$$

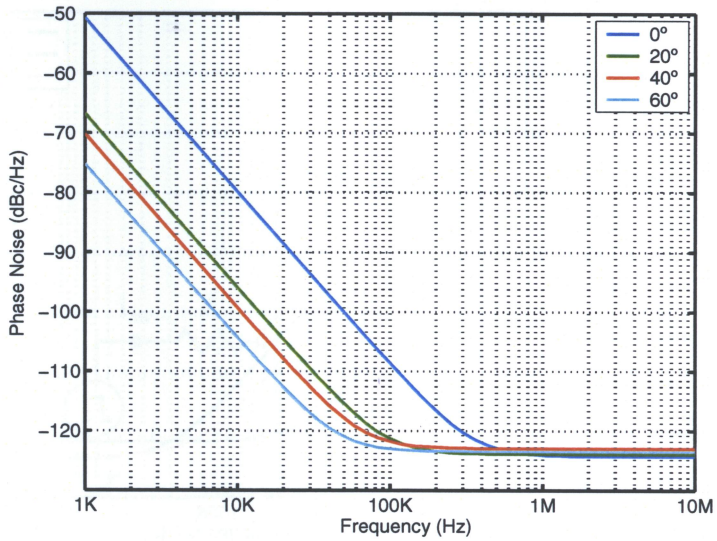


Figure 5.8: Phase noise of 2.4 GHz Constant-$Q$ oscillator with varying temperature. Note: The CCO was retuned to 2.4GHz at each temperature.

It is evident that the filter is a low-pass with its cutoff frequency

$$\omega_{-3dB} = \frac{R_1}{L_{11}} \frac{1}{\left(1 - \frac{M_{12}M_{21}}{L_{11}L_{22}}\right)}. \tag{5.3}$$

The schematic of the current-mode loop filter is shown in Fig.5.11. The bandwidth of the loop filter with 10% $V_{DD}$ fluctuations as the bias voltage $V_{BW}$ is tuned, is plotted in Fig.5.12. The bandwidth of the loop filter is also shown at process corners in Fig.5.13. As seen from the plots the bandwidth of the loop filter is configurable to values between 100 and 400 MHz at each process corner and $V_{DD}$ fluctuation. This allows the effects of VDD fluctuations and process variation on the loop filter bandwidth to be compensated for by manually adjusting the bias voltage $V_{BW}$ to set a desired filter bandwidth within this range.

The inductances of the cascode active transformer are inversely proportional to the transconductance of the gyrators constituting the active inductors. Nor-

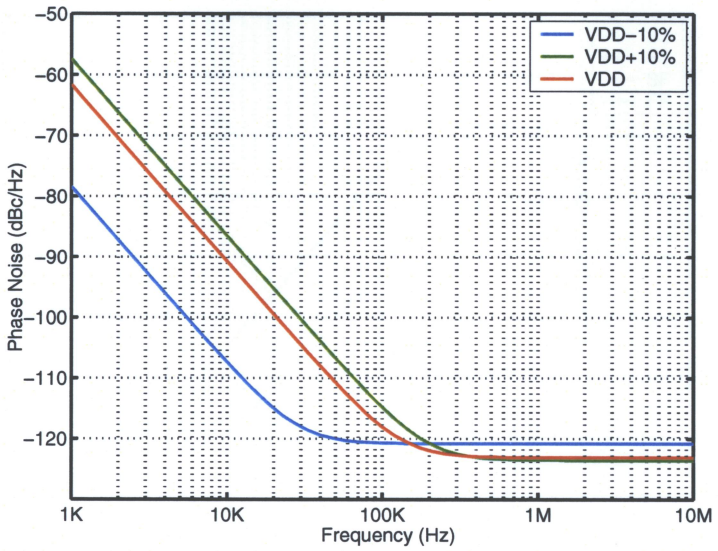


Figure 5.9: Phase noise of 2.4 GHz Constant-$Q$ oscillator with VDD supply fluctuations. Note: The CCO was retuned to 2.4GHz at each supply voltage.

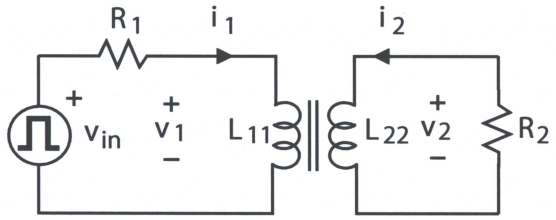


Figure 5.10: Current-mode transformer loop filter.

mally the transistors of the gyrators are biased in saturation. When the transistors are in the triode region, they behave as a transconductor with its transconductance $g_{ds} < g_m$. In this case, an inductive characteristic still exists, except with a larger inductance. It should be noted that although the output voltage of the preceding phase detector is near rail-to-rail, the resistor and the input capacitance of the primary winding of the active transformer limit the swing of the voltage at the input of the transformer to a rather small range, ensuring that the transistors connected to the primary winding node remain in saturation.

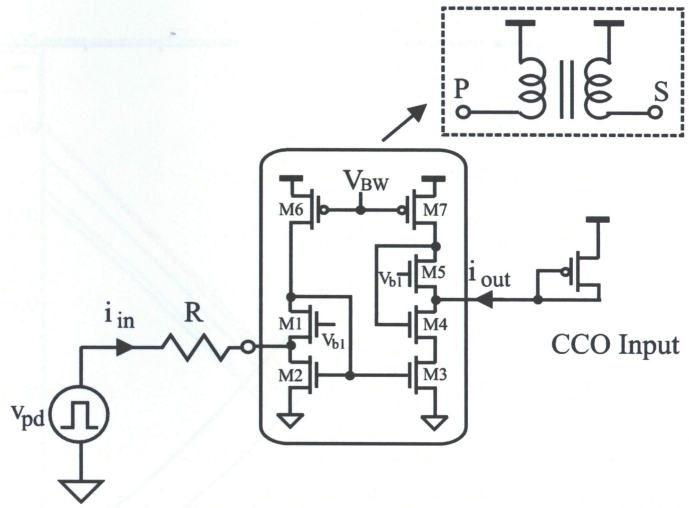


Figure 5.11: Current-mode loop filter. $V_{b1} = 0.8$V, $R = 7K\Omega$, $W_1 = 50\mu$m, $W_2 = 50\mu$m, $W_3 = 100\mu$m, $W_4 = 40\mu$m, $W_5 = 50\mu$m, $W_6 = 1\mu m$, $W_7 = 1\mu m$,$L_1 = 0.18\mu$m, $L_2 = 0.18\mu$m, $L_3 = 0.18\mu$m, $L_4 = 0.18\mu$m, $L_5 = 0.18\mu$m, $L_6 = 10\mu m$, $L_7 = 10\mu m$.

### 5.2.3 Phase/Frequency Detector

The phase/frequency detector is a standard D-flipflop phase/frequency detector shown in Fig.5.14 with true-single phase clocking-configured DFFs.

### 5.2.4 Loop Dynamics in Lock State

From Fig.5.15, we have

$$V_{pd}(s) = RI_1(s) + sL_{11}I_1(s) + sM_{12}I_2(s). \tag{5.4}$$

because the cascode active transformer is uni-directional, $M_{12} = 0$. For the secondary winding, $V_2(s) = sL_{22}I_2(s)+sM_{21}I_1(s)$, Because the load of the secondary winding is a CCO whose input impedance is zero ideally, we have $V_2(s) = 0$. Fur-

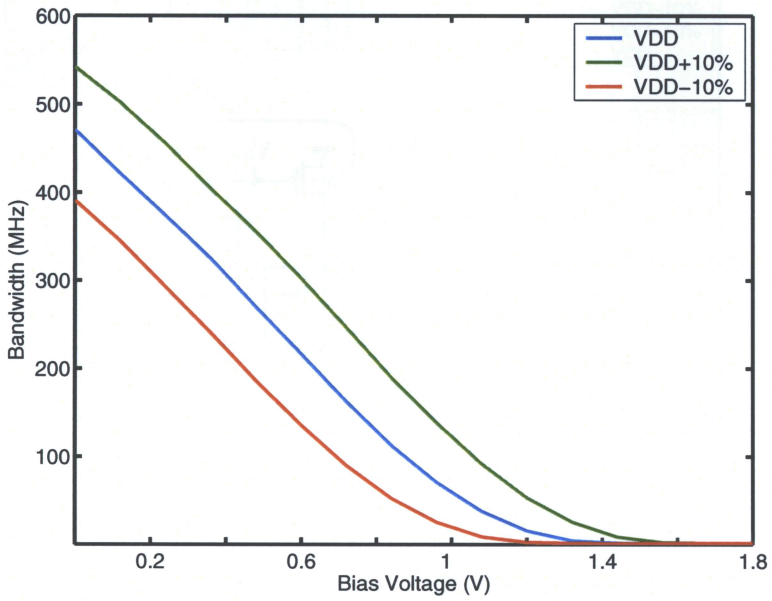


Figure 5.12: Simulated dependence of the loop filter bandwidth on VDD supply voltage.

ther noting $I_c(s) = -I_2(s)$, we arrive at

$$I_c(s) = \frac{M_{21}}{L_{22}(sL_{11} + R)} V_{pd}(s). \tag{5.5}$$

The phase transfer function of the PLL is given by

$$\frac{\Phi_o(s)}{\Phi_i(s)} = \frac{K_{pd}K_{cco}M_{21}}{\Delta}, \tag{5.6}$$

where $\Delta = s^2 L_{11}L_{22} + sRL_{22} + K_{pd}K_{cco}M_{21}$. The loop gain-bandwidth product $\omega_n$ and damping factor $\xi$ of the PLL are given by

$$\begin{aligned} \omega_n &= \sqrt{\frac{K_{pd}K_{cco}M_{21}}{L_{11}L_{22}}}, \\ \xi &= \frac{R}{2}\sqrt{\frac{L_{22}}{K_{pd}K_{cco}L_{11}M_{21}}}. \end{aligned} \tag{5.7}$$

The PLL is type I. and the damping factor $\xi$ can be tuned by varying $R$ with-

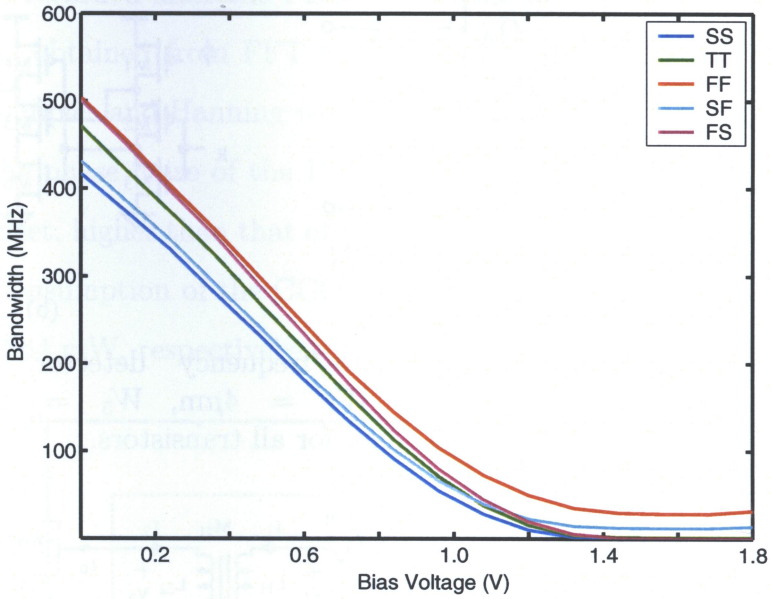


Figure 5.13: Simulated loop filter bandwidth at process corners.

out affecting the loop bandwidth. The higher the self inductances, the smaller the loop bandwidth, the better the suppression of transient disturbances encountered at the input. The larger the mutual inductance, the larger the loop bandwidth, the weaker the suppression of transient disturbances at the input because large $M_{21}$ will allow these disturbances to couple to the CCO more easily.

### 5.2.5 Simulation Results

The 2.4 GHz current-mode PLL with a constant-$Q$ CCO and cascode active transformer loop filter with its building blocks presented earlier was implemented in TSMC-0.18$\mu$m 1.8V 6-metal CMOS technology. Fig.5.16 plots the control current of the PLL. The PLL reaches the lock state in 80 ns approximately. The phase noise of the PLL was analyzed using the time-domain behavioral simulation techniques proposed in [25, 26, 27], specifically, (i) the phase noise of the CCO was analyzed using Cadence's SpectreRF with the consideration of the fold-over

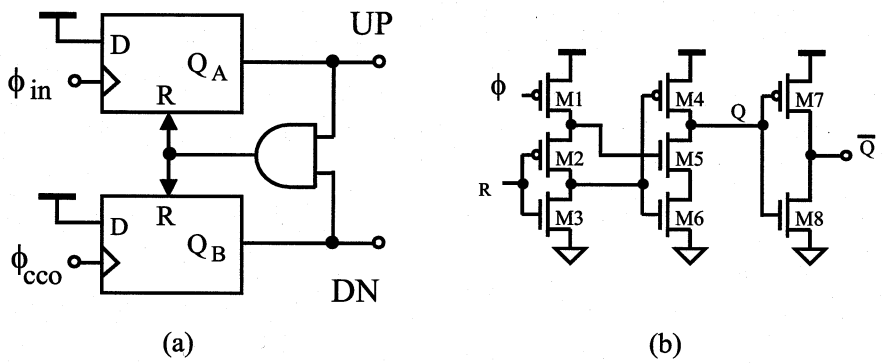


Figure 5.14: D-Flipflop phase/frequency detector. $W_1 = 1\mu$m, $W_2 = 4\mu$m, $W_3 = 4\mu$m, $W_4 = 4\mu$m, $W_5 = 1\mu$m, $W_6 = 8\mu m$, $W_7 = 2\mu m$,$W_8 = 1\mu m$,$L = 0.18\mu$m for all transistors.

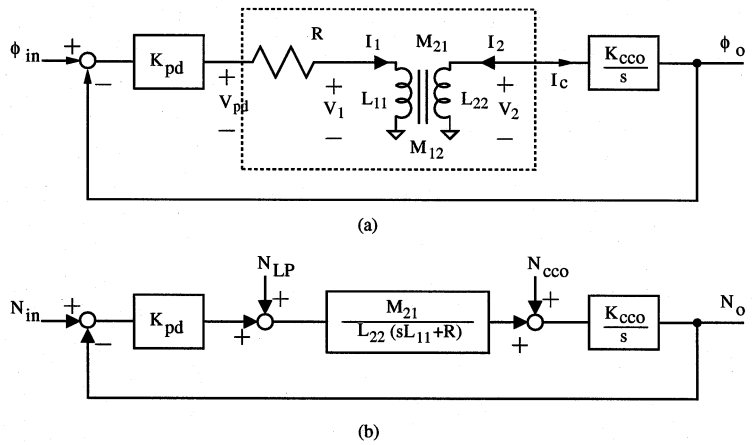


Figure 5.15: Block diagram with noise sources of the PLL in lock state.

of the broad-band noise sources. The amplitude of the timing jitter of the CCO was obtained from its phase noise. In Verilog-AMS time-domain simulation of the PLL, the oscillation period of the CCO was disturbed using the extracted timing jitter, together with a normally distributed random generator with zero mean and unity variance. (ii) The active transformer loop filter is modeled as a series RL network with the inductance, resistance and noise power extracted from its SpectreRF simulation results. (iii) The PFD was modeled using Verilog-AMS with delays extracted from its schematic-level SpectreRF simulation results. (iv) Time-domain analysis of the PLL was carried out and a large number of oscillation

periods were recorded after the PLL reached the lock state. The phase noise of the PLL was obtained from FFT analysis of the recorded periods of the CCO with 256K samples and Hanning window using *Matlab*. The results are shown in Fig.5.17. The phase noise of the PLL is approximately -116 dBc/Hz at 1 MHz frequency offset, higher than that of the CCO alone at the same frequency offset. The power consumption of the CCO, the filter, and the PFD is 24.1 mW, 0.138 mW, and 0.864 mW, respectively with a total silicon area of 4600 $\mu m^2$

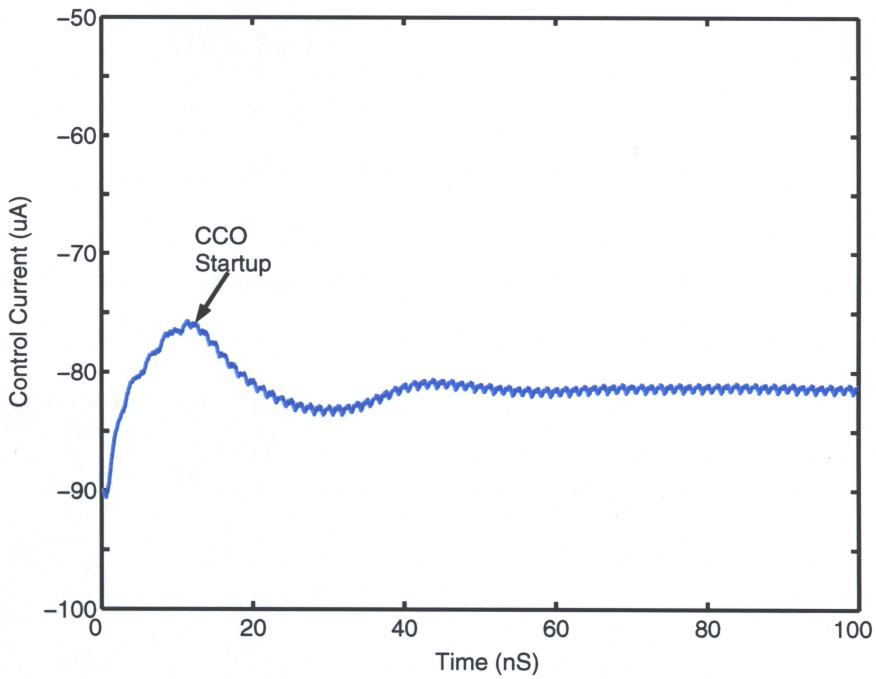


Figure 5.16: Simulated control current of the PLL.

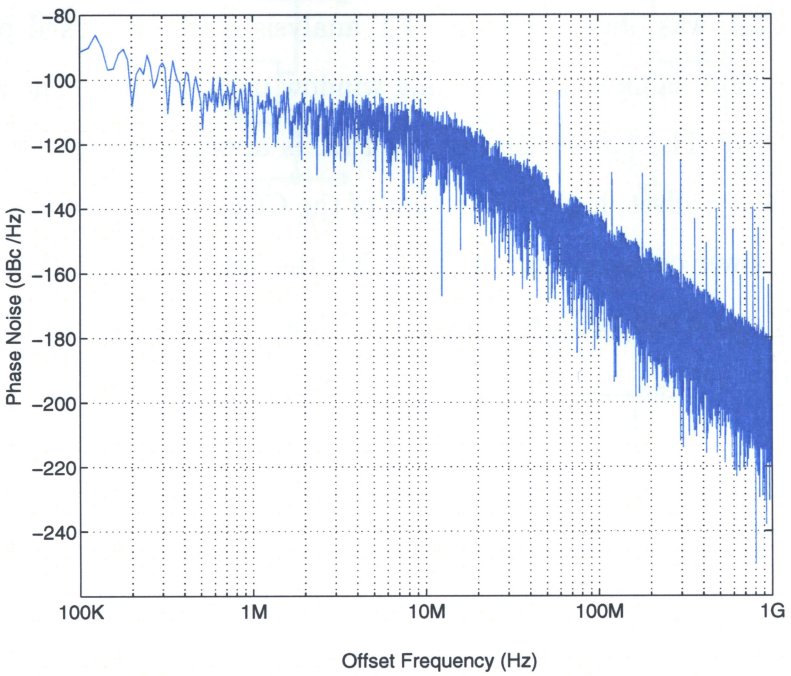


Figure 5.17: Simulated phase noise of the PLL.

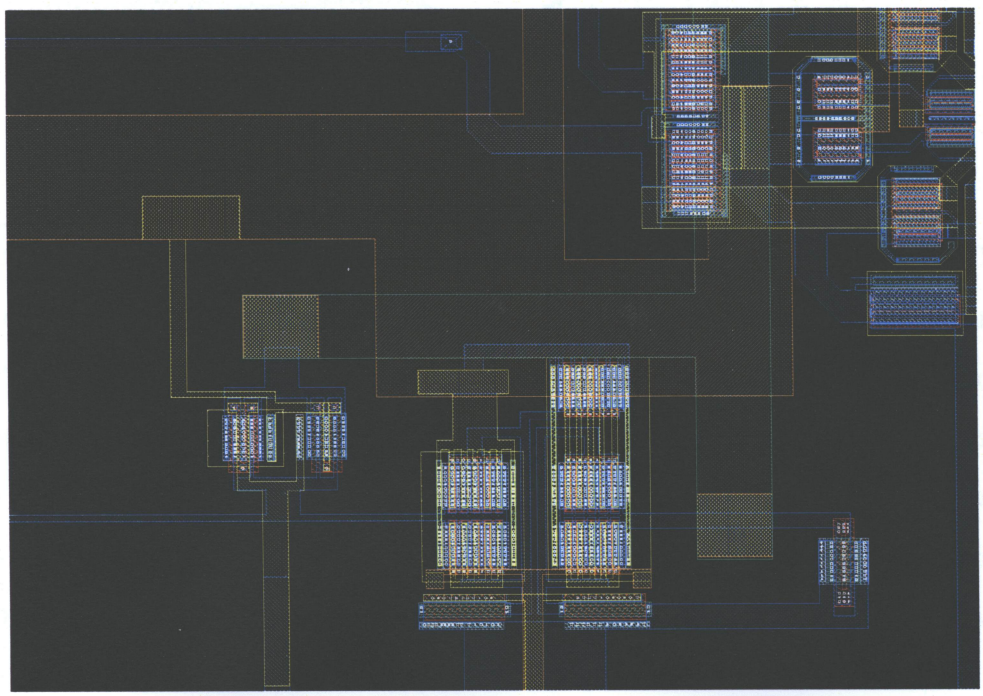

Figure 5.18: Layout of the proposed PLL.

## 5.3 Current-Mode Sigma Delta Modulator

This application of cascode CMOS active transformers presents a new current-mode sigma delta modulator with extremely small silicon area requirements for bluetooth applications. Oversampled sigma-delta modulators emerged recently in analog-to-digital (ADC) and digital-to-analog base-band applications in wireless transceivers. With the continuous increase in base-band data rates of wireless systems, the design of these modulators has become increasingly challenging. High resolution in ADCs for base-band applications is not of a critical concern as most wireless schemes have constant-envelope signals and only require phase and frequency tracking. Oversampled sigma-delta modulators employ either a band-pass or a low-pass filter to form a desired noise shaping characteristic [28, 29, 30, 31, 32, 33, 34]. These filters are usually constructed from passive or active RC networks employing large on-chip capacitors. These loop filters suffer from a number of drawbacks including a fixed bandwidth, a fixed and limited quality factor, and the need for a large silicon area.

This application of cascode CMOS active transformers proposes a new current-mode circuit implementation of an oversampled first order sigma-delta modulator for bluetooth baseband applications. Although a first order topology has limited noise-shaping ability it is selected to keep the required silicon area to a minimum. The proposed sigma-delta modulator is a standard 1st order configuration and replaces the passive RC filter with a cascode active transformer based loop filter. This allows the modulator to incorporate the advantages of CMOS active transformers including a large and tunable inductance, a large self-resonant frequency, and the need for a negligibly small silicon area. The tunability of the loop filter bandwidth and oscillation frequency of the VCO allow the proposed oversampled sigma-delta modulator to offer a variable noise-shaping characteristic. They also

enable the tunability of the performance of the entire modulator so that the effect temperature variation, supply voltage fluctuation, and process spread can be compensated effectively and so that it can be adjusted to suit a large range of applications. The exclusive use of active devices in the loop filter also allows the sigma-delta modulator to occupy an extremely small silicon area.

### 5.3.1 Current-Mode Oversampled Sigma Delta Modulator

The block diagram of the proposed current-mode sigma-delta modulator is shown in Fig.5.19. The topology is that of a standard 1st order sigma-delta modulator. The ADC and DAC in this design are a 4-level configuration, to provide 2 output bits. The ADC is clocked with a ring oscillator operating at 500 MHz to provide 100x oversampling operation.

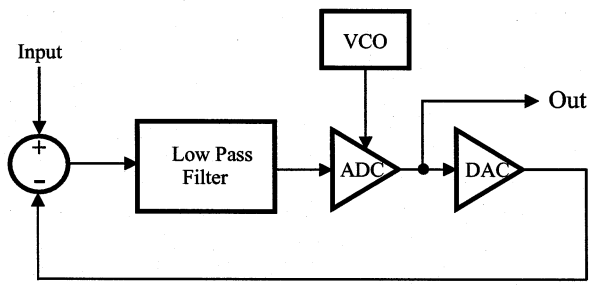


Figure 5.19: Block diagram of standard 1st order sigma-delta modulator.

The SNR for an ideal sigma delta modulator with n-bit quantizer can be calculated as

$$SNR = 10log[\frac{3\pi}{2}N^2(2K+1)(\frac{OSR}{\pi})^{(2K+1)}], \tag{5.8}$$

where K is the order of the loop filter, OSR is the oversampling ratio, and N is the number of quantizer bits. For a 4 bit quantizer with 100X oversampling the SNR is predicted to be in the 69 dB range. Note one advantage of current-mode

design is that implementation of a summer circuit is not required as unlike voltage mode circuits, the current contributions of the input and DAC are linearly added at the input node of the loop filter.

### 5.3.2 Comparator and Sample-and-Hold Circuit

The comparator with its schematic shown in Fig.5.20 is a cross-coupled static inverter pair consisting of M1-M4. The latch is first disabled by resetting transistors M7-M8 prior to a comparison operation. Once M7-M8 are off, the input transistors M5-M6 determine the direction in which the latch switches based on the current flowing into the drain of M9 and M10. The transmission gate performs the sample-and-hold operation on the output of the comparator and the second inverter restores the signal swing. The ADC consists of three comparators to provide a 4-level quantizer operation. The DC transfer of the quantizer with ADC and DAC connected in open loop configuration is shown in Fig. 5.22.

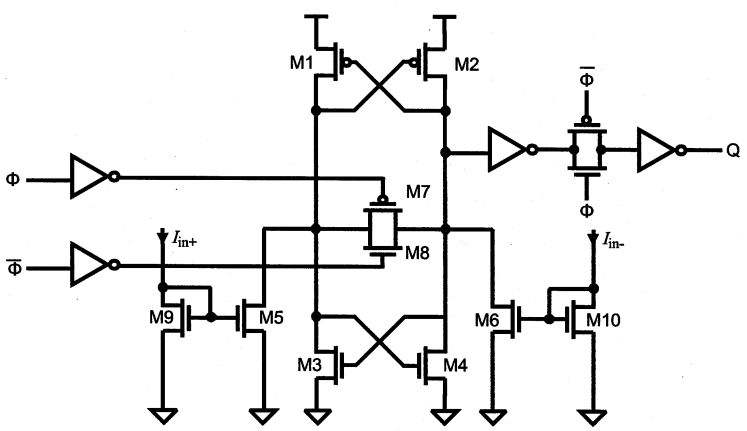


Figure 5.20: Current-mode comparator. Circuit parameters : $W_1 = 30\mu$m, $W_2 = 30\mu$m, $W_3 = 30\mu$m, $W_4 = 30\mu$m, $W_5 = 5\mu$m, $W_6 = 5\mu m$, $W_7 = 50\mu m$, $W_8 = 40\mu m$, $W_9 = 5\mu m$, $W_{10} = 5\mu m$, $L = 0.18\mu$m for all transistors.

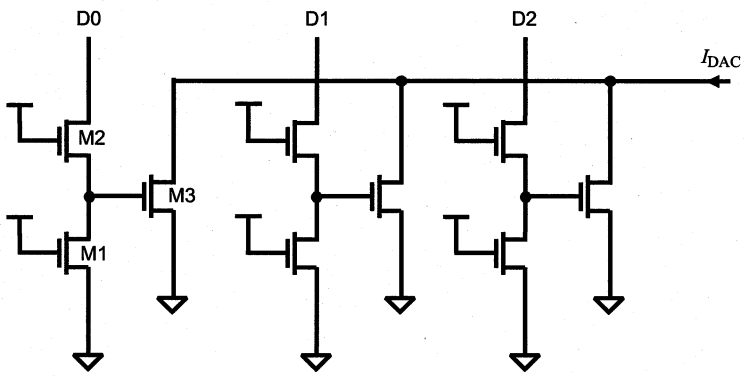


Figure 5.21: Current-mode DAC circuit. Circuit parameters : $W_1 = 0.5\mu$m, $W_2 = 2\mu$m, $W_3 = 8\mu$m, $L_1 = 0.3\mu$m, $L_2 = 0.18\mu$m, $L_3 = 1\mu$m, all 3 stages have the same dimensions.

### 5.3.3 Voltage Controlled Oscillator

The ADC comparators are clocked from a standard ring oscillator with 4 stages as shown in Fig.5.23a. The detailed design of each ring stage is shown in Fig.5.23b.

### 5.3.4 Current-Mode Loop Filter using Cascode Active Transformers

The simplified schematic of the current-mode loop filter is shown in Fig.5.24. As the active transformer is uni-directional, $M_{12} = 0$, and for the secondary winding $V_2(s) = sL_{22}I_2(s) + sM_{21}I_1(s)$. As the secondary winding is loaded with a current mirror which has an input impedance of 0 ideally, we have $V_2(s) = 0$, which provides the expression for output current,

$$I_{out} = \frac{M_{21}R}{L_{22}(R + sL_{11})}. \tag{5.9}$$

It is evident that the loop filter has a low pass characteristic with the cutoff frequency given by,

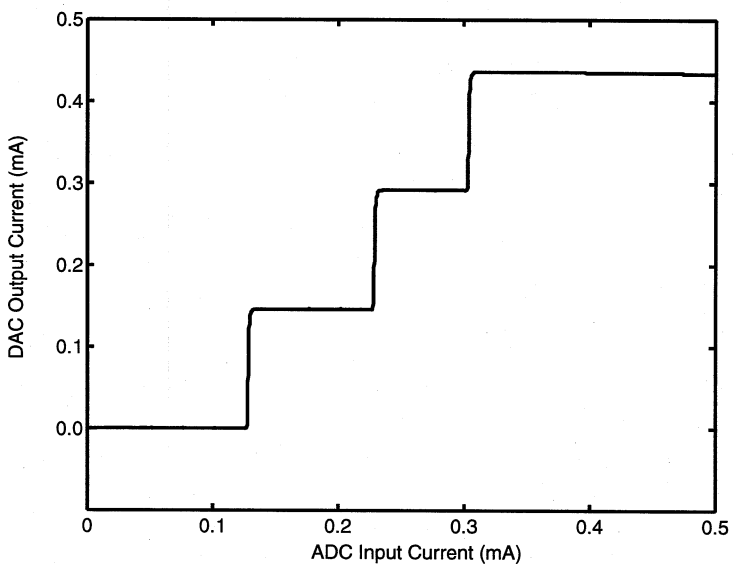


Figure 5.22: Input current of ADC vs. output current of DAC in open loop configuration.

$$\omega_{LF} = \frac{R}{L_{11}} \tag{5.10}$$

The detailed schematic of the loop filter is shown in Fig.5.25. M8 and M9 form a symmetrical load implementation of the resistor R. The primary and secondary bias current sources are replaced with DC biased NMOS current sources. The bandwidth of the loop filter with 10% $V_{DD}$ fluctuations as the bias voltage $V_{BW}$ is tuned, is plotted in Fig.5.26. The bandwidth of the loop filter is also shown at process corners in Fig.5.27 and at varying temperatures in Fig.5.28. As seen from the plots the bandwidth of the loop filter is configurable to values between 1 and 100 MHz at each process corner, temperature and $V_{DD}$ fluctuation. This allows the effects of VDD fluctuations and process variation on the loop filter bandwidth to be compensated for effectively by manually adjusting the bias voltage $V_{BW}$ to

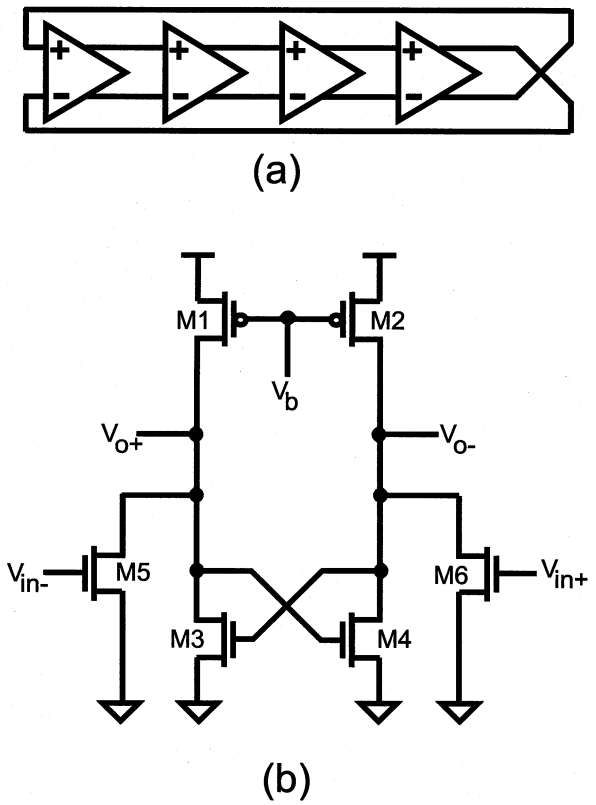


Figure 5.23: (a) 4 stage ring VCO. (b) VCO delay cell. Circuit parameters: $W_1 = 5\mu$m,$W_2 = 5\mu$m, $W_3 = 3\mu$m, $W_4 = 3\mu$m, $W_5 = 8\mu$m, $W_6 = 8\mu$m, $L_1 = 0.3\mu$m,$L_2 = 0.3\mu$m, $L_3 = 0.5\mu$m, $L_4 = 0.5\mu$m, $L_5 = 0.18\mu$m, $L_6 = 0.18\mu$m, all 4 stages have the same dimensions.

set a desired filter bandwidth within this range.

The inductances of the active transformer are inversely proportional to the transconductance of the gyrators constituting the active inductors. Normally the transistors of the gyrators are biased in saturation. When the transistors are in the triode region, they behave as a transconductor with its transconductance $g_{ds} < g_m$. In this case, an inductive characteristic still exists, except with a larger inductance.

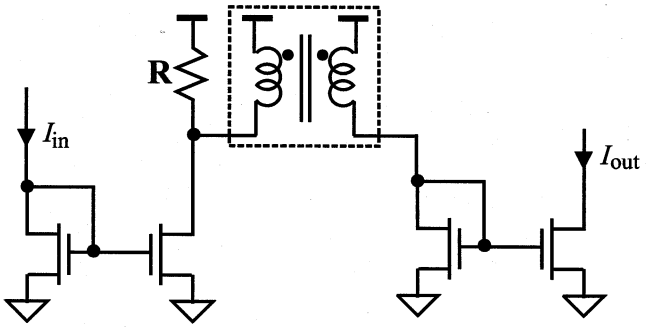


Figure 5.24: Current-mode loop filter.

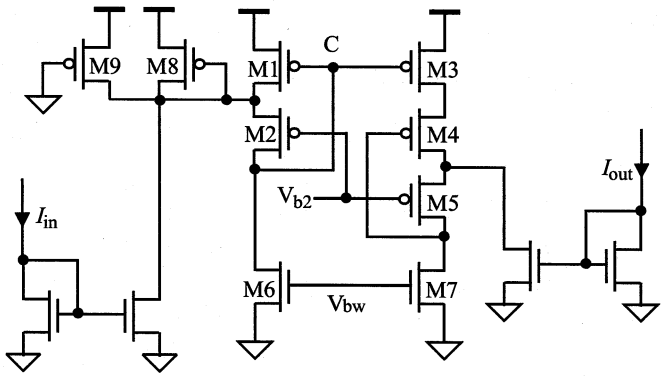


Figure 5.25: CMOS active transformer current-mode loop filter. Circuit Parameters: $V_{b2} = 0.8$V, $W_1 = 30\mu$m, $W_2 = 10\mu$m, $W_3 = 30\mu$m, $W_4 = 30\mu$m, $W_5 = 40\mu$m, $W_6 = 1\mu m$, $W_7 = 1\mu m$, $W_8 = 15\mu m$, $W_9 = 15\mu m$, $L_1 = 0.18\mu$m, $L_2 = 0.18\mu$m, $L_3 = 0.18\mu$m, $L_4 = 0.18\mu$m, $L_5 = 0.18\mu$m, $L_6 = 1\mu m$, $L_7 = 1\mu m$,$L_8 = 2\mu m$, $L_9 = 2\mu m$.

### 5.3.5 Simulation Results

The modulator was implemented in TSMC's 1.8V 0.18$\mu$m CMOS technology and analyzed using Cadence SpectreRF with BSIM3v3-RF device models. A 5 MHz sinusoidal input of amplitude 400 uA was applied to the modulator. Fig.5.29 shows the power spectral density of the output of the modulator. It was obtained from the FFT analysis of the transient response of the modulator over a 500$\mu$s period in the steady state. The FFT analysis was performed with 128k samples and a Hanning window. From the plot an SNR of 65 dB is obtained. Also observed from the plot is the noise corner frequency of 20 MHz. As the total

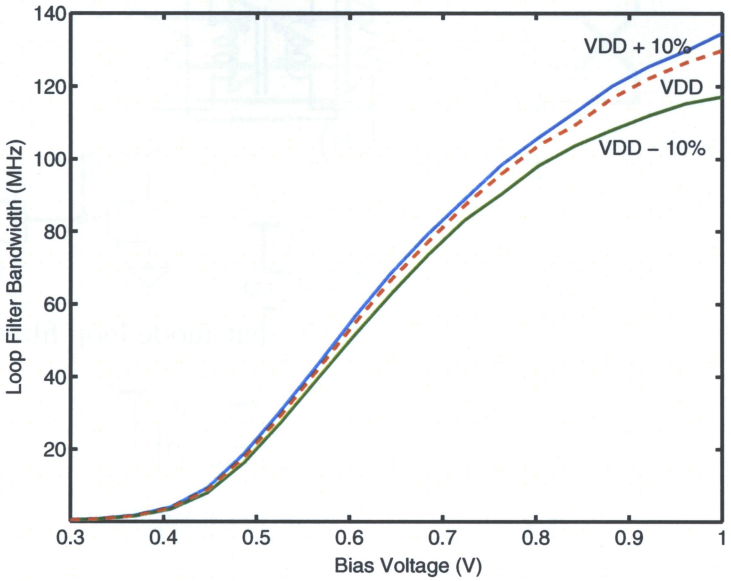


Figure 5.26: Simulated dependence of the loop filter bandwidth on VDD supply voltage.

time of the transient simulation is finite and limited by computational intensity and data size, the resolution is less detailed at lower frequencies. Table 5.2 summarizes the performance of the proposed modulator and Fig.5.30 shows the layout of the proposed modulator.

Table 5.2: Performance of the proposed sigma delta modulator.

| | |
|---|---|
| Technology | TSMC-0.18$\mu$m 1.8V CMOS |
| Sampling frequency | 500 MHz |
| Bandwidth | 5 MHz |
| Oversampling Ratio (OSR) | 100 |
| Total Layout Area | 7300 $\mu m^2$ |
| Dynamic Range (DR) | 50 dB |
| SNR | 65 dB |
| Power consumption | 28 mW |

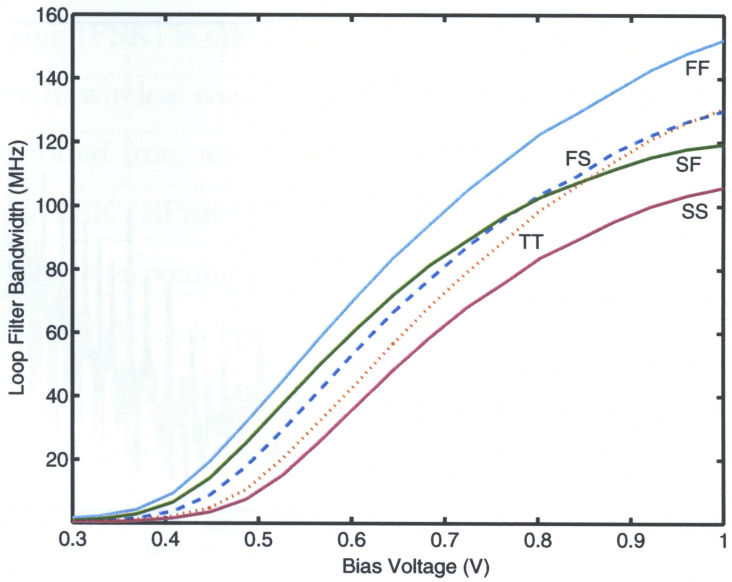


Figure 5.27: Simulated loop filter bandwidth at process corners.

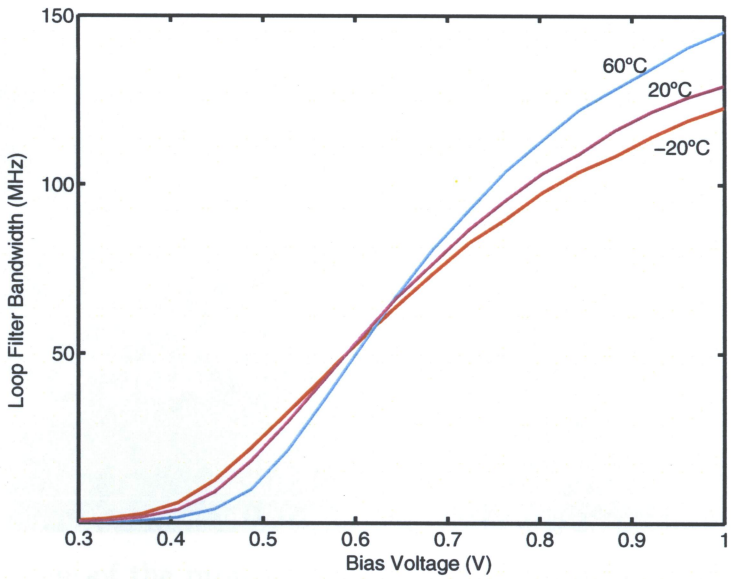


Figure 5.28: Simulated dependence of the loop filter bandwidth on temperature.

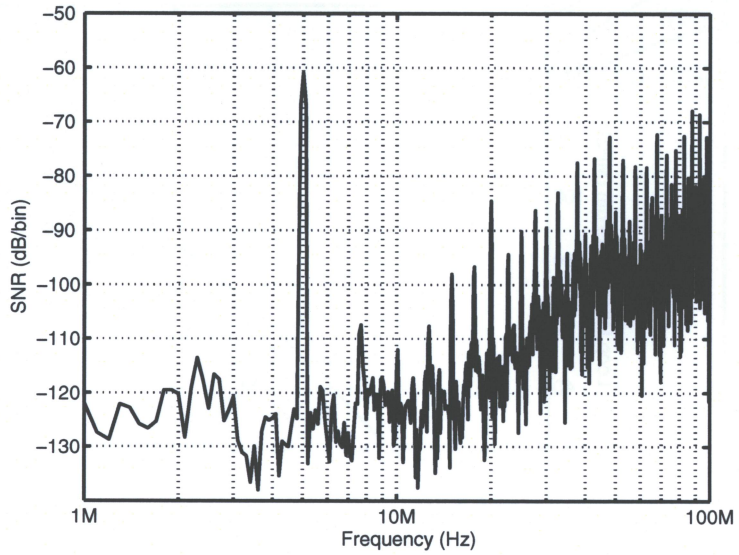


Figure 5.29: Power spectral density at the output of the modulator with a 5 MHz sinusoidal input.

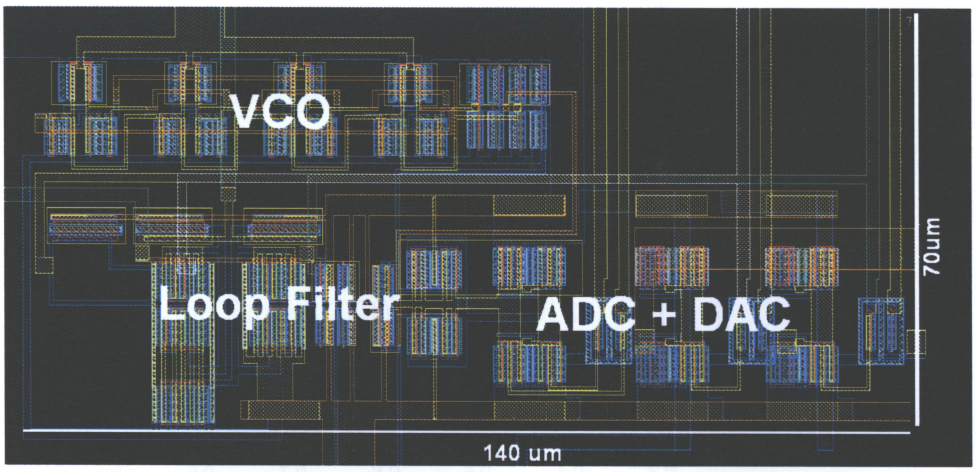


Figure 5.30: Layout of the proposed current-mode sigma-delta modulator.

## 5.4 1.6 GHz QPSK Phase Modulator

Phase shift keying (PSK) is one of the most widely used constant envelope modulation schemes in wireless communications. Quadrature PSK (QPSK) in which the carrier generated from an oscillator is shifted in 4 increments of 90 degree each and binary PSK (BPSK) where the carrier is shifted in two increments of 180 degree each are two common PSK schemes. In QPSK each symbol represents two bits while in BPSK each symbol represents 1 bit. The phase of the carrier is usually selected by a multiplexer driven by an incoming digital stream [35, 36]. While providing improved power performance and removing the need for a baseband with DAC, this approach suffers from the drawback that the modulation transactions of the carrier may occur at any phase of the carrier [37]. Due to the existence of sharp transactions in the modulated carrier, the bandwidth of the modulated carrier becomes excessive. This application of linear active transformers proposes a new QPSK modulator with an optimal transaction bandwidth control.

The proposed modulator minimizes the bandwidth of the modulated carrier by adjusting the modulation phase such that the sharpness of the transactions of the modulated carrier is minimized. The implementation of the modulator, specifically, the quadrature oscillator and multiplexer, is realized using CMOS linear active transformers to provide comparable phase noise performance without using area-greedy spiral inductors and transformers.

### 5.4.1 Architecture of QPSK Modulator

The block diagram of the proposed modulator is shown in Fig.5.31. A quadrature oscillator provides the carrier. For blue-tooth compatible operation the phase

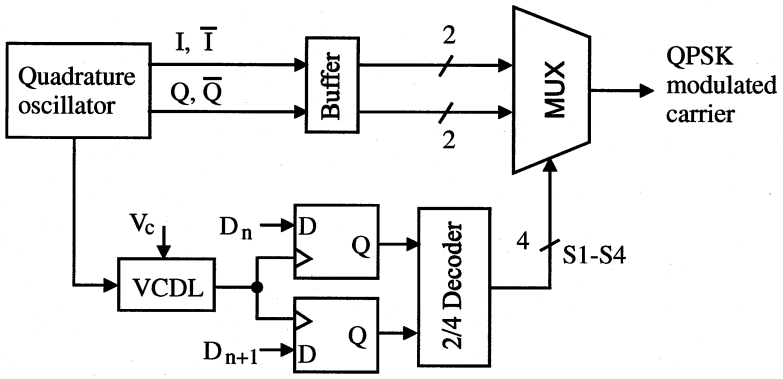


Figure 5.31: Block diagram of proposed QPSK phase modulator.

noise of this oscillator must be under -95dBc/Hz at 500 KHz offset. The multiplexer selects one of four oscillator outputs in accordance with the logic state of the incoming digital stream (2 bits per symbol). The multiplexer is controlled by a variable delay line whose input is the output of the oscillator. The sampling occurs at the optimal transaction points at which the bandwidth of the modulated carrier is minimal. The D flip-flops and multiplexer are only required to switch at the base-band frequency of up to 1 MHz. Linearity and distortion are not critical in this application as blue-tooth transceivers typically employ non-linear switching power amplifiers.

As frequency is the derivative of phase any phase discontinuity will result in a wider power spectral density. By lessening the discontinuity the modulated signal bandwidth can be minimized. To illustrate this, consider Fig.5.32 where the two extreme cases of QPSK modulation of a 1-Hz carrier are shown. $x_1(t)$ is obtained by modulating the carrier at its zero-crossings while $x_2(t)$ is obtained by modulating the carrier at its peaks. $x_1(t)$ can be written as

$$x_1(t) = -\sin(t)\mathrm{rect}\Big(\frac{t}{2\pi} + \pi\Big) + \sin(t)\mathrm{rect}\Big(\frac{t}{2\pi} - \pi\Big), \tag{5.11}$$

where $\mathrm{rect}(t)$ is the unit-pulse function. The power spectral density (PSD) of

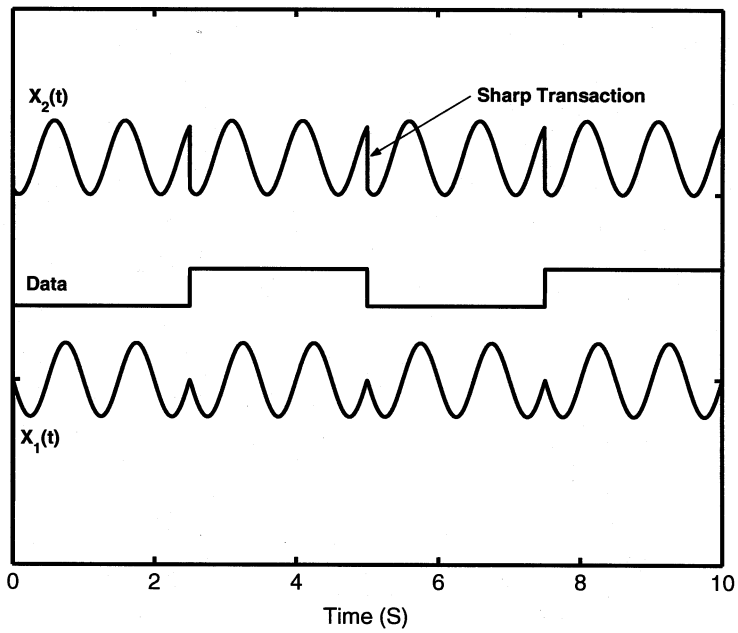


Figure 5.32: $x_1(t)$ (optimal) and $x_2(t)$ (worst-case) QPSK data transactions of a 1 Hz carrier.

$x_1(t)$, denoted by $S_{x_1}(\omega)$ is given by

$$S_{x_1}(\omega) = 4\pi^2\Big[\text{sinc}^2(\pi\omega - 1) + \text{sinc}^2(\pi\omega + 1)\Big]. \tag{5.12}$$

$x_2(t)$ can be represented by

$$x_2(t) = \cos(t)[2u(t) - 1], \tag{5.13}$$

where $u(t)$ is the unit-step function. The PSD of $x_2(t)$, denoted by $S_{x_2}(\omega)$, is given by

$$S_{x_2}(\omega) = 4\pi^2\left[\frac{1}{(\omega - 1)^2} + \frac{1}{(\omega + 1)^2}\right]. \tag{5.14}$$

$S_{x_1}(\omega)$ and $S_{x_2}(\omega)$ are plotted in Fig.5.33. It is seen that $S_{x_1}(\omega)$ has a smaller

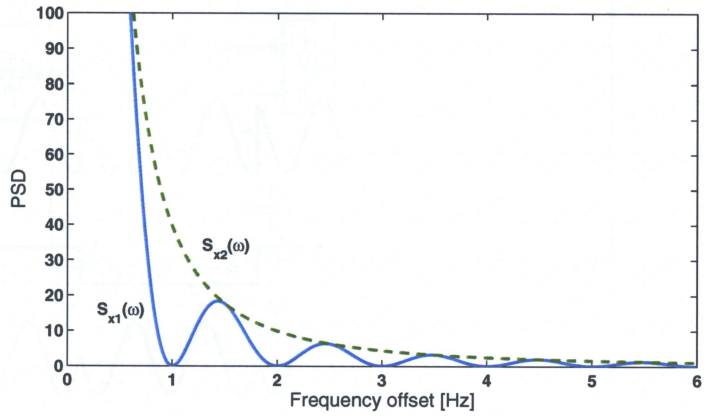


Figure 5.33: PSD of $x_1(t)$ and $x_2(t)$.

bandwidth as compared with $S_{x_2}(\omega)$. This observation reveals that the bandwidth of the modulated carrier can be minimized by varying the modulating point. The lower the degree of the sharpness of the modulated carrier waveform, the smaller its bandwidth. The delay of the delay line is adjusted such that the sampling of the output of the quadrature oscillator occurs at the optimal modulating points.

### 5.4.2 Voltage Controlled Delay Line.

The VCDL is a 40-stage current-starved CMOS inverter chain with a voltage-controlled variable delay. The schematic of the VCDL is shown in Fig.5.34. Two static CMOS inverters are employed with one before and one after the VCDL to improve signal swing. The linearity of the delay line is not critical as the control input will be a DC signal, resulting in no distortion. Fig.5.35 shows the waveform of the output voltage of the delay line with different control voltages.

### 5.4.3 Quadrature Oscillator

The schematic of the quadrature oscillator employing two bidirectional single-winding linear active transformers is shown in Fig.5.36. The connection between

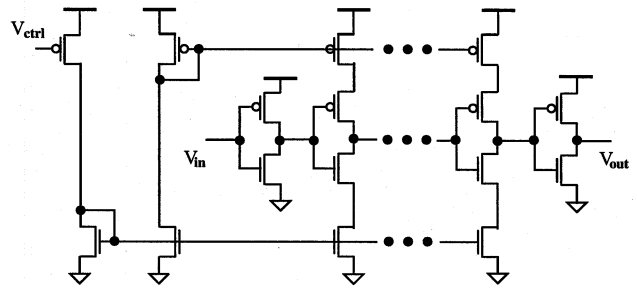


Figure 5.34: Schematic of delay line. Circuit parameters : Inverters : $W_n = 2\mu$m, $W_p = 1\mu$m. Current mirrors : $W_p = 40\mu$m, $W_n = 20\mu$m.

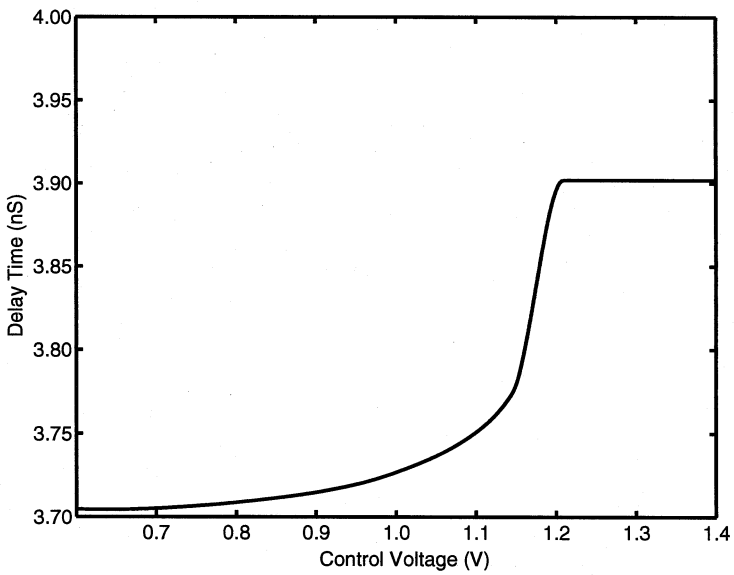


Figure 5.35: Delay time of the voltage controlled delay line.

stages is coupled using parallel transistors. To minimize the phase noise the inductance is made as large as possible at 1.6 GHz, improving the quality factor, $Q = \frac{L\omega}{R_s}$ [38].

### 5.4.4 Multiplexer

The multiplexer shown in Fig.5.37 is a linear active transformer with four primary windings and a single secondary winding. Four transmission gates select which primary winding is connected to the secondary winding.

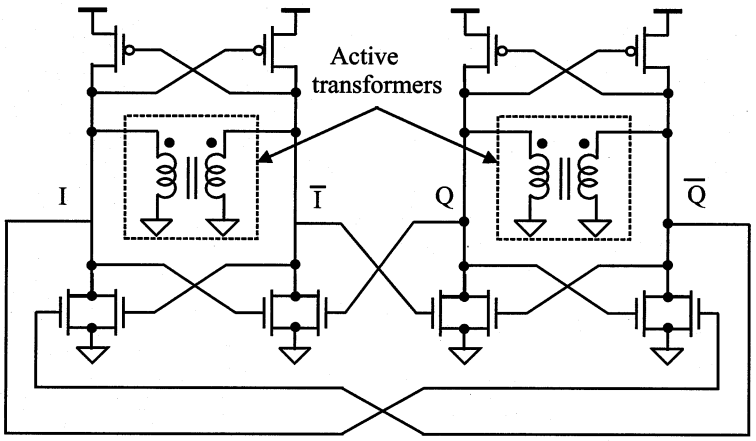


Figure 5.36: Quadrature oscillator using active transformers. Circuit Parameters: Switching transistors $W_n = 10\mu$m, $W_p = 20\mu$m; Stage input transistors : $W_n = 1\mu$m, $W_p = 1\mu$m .

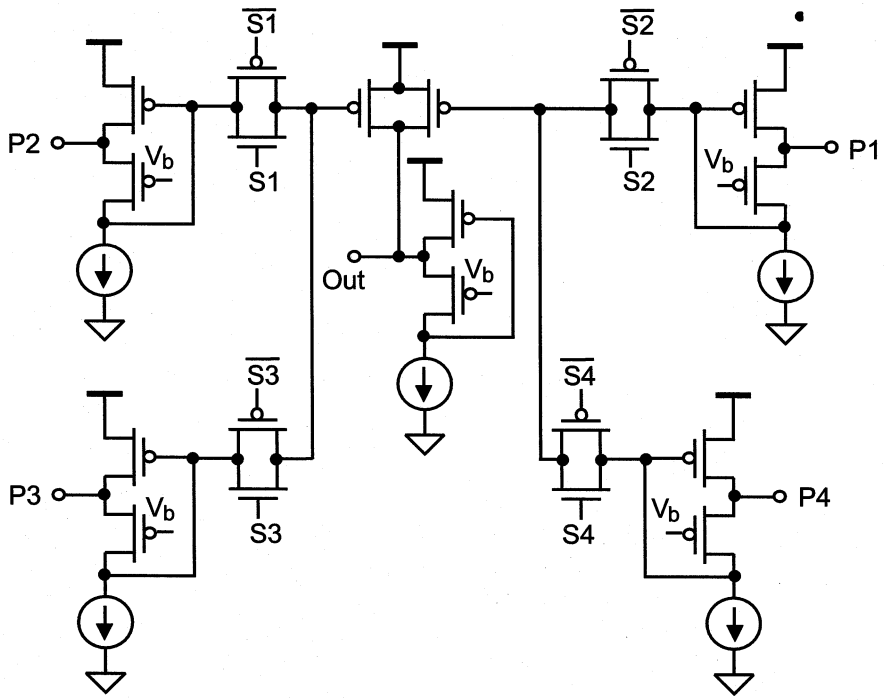


Figure 5.37: Multiplexer using active transformers. Circuit parameters : Transmission gates : $W_n = 1\mu$m, $W_p = 1\mu$m.

### 5.4.5 Simulation Results

The modulator was implemented in a TSMC's 1.8V 0.18$\mu$m CMOS technology and analyzed using Cadence SpectreRF with BSIM3v3 device models. A 400 MHz periodic data signal was applied to the input of the modulator. The oscillation frequency of the quadrature oscillator is 1.6 GHz. Fig.5.38 shows the phase noise of the quadrature oscillator at nominal supply voltage $V_{DD}$ = 1.8V and $\pm$10% $V_{DD}$ variations. Fig.5.38 also plots the phase noise of the oscillator at four process corners provided by TSMC, namely FF (Fast-nMOS/Fast-pMOS), FS (Fast-nMOS/Slow-pMOS), SF (Slow-nMOS/Fast-pMOS), and SS (Slow-nMOS/Slow-pMOS). The phase noise at the modulator output including contributions from the buffers, multiplexer and delay line is also shown in Fig.5.38. Most of the noise contribution comes from the multiplexer as the delay line and D flip-flops only operate at base-band frequencies (several MHz).

The PSD of the output voltage of the modulator with the optimal and worst-case modulation transactions is shown in Fig.5.39. Because the input data is periodic, the PSD of the modulated carrier only contains discrete inter-modulation components at 0.4GHz, 1.2GHz, 2.0GHz, ... within the envelope of the PSD. It is seen that the envelope of the optimal case has a smaller bandwidth as compared with that of the worst case. This agrees with our earlier results.

Fig.5.40 shows the simulated data transaction at the output of the modulator for three different delay line control voltages. The dependence of the modulating point of the incoming data on the delay line control voltage is evident. Table 5.3 summarizes the performance of the proposed modulator.

The die photo of the modulator is shown in Fig.5.41.

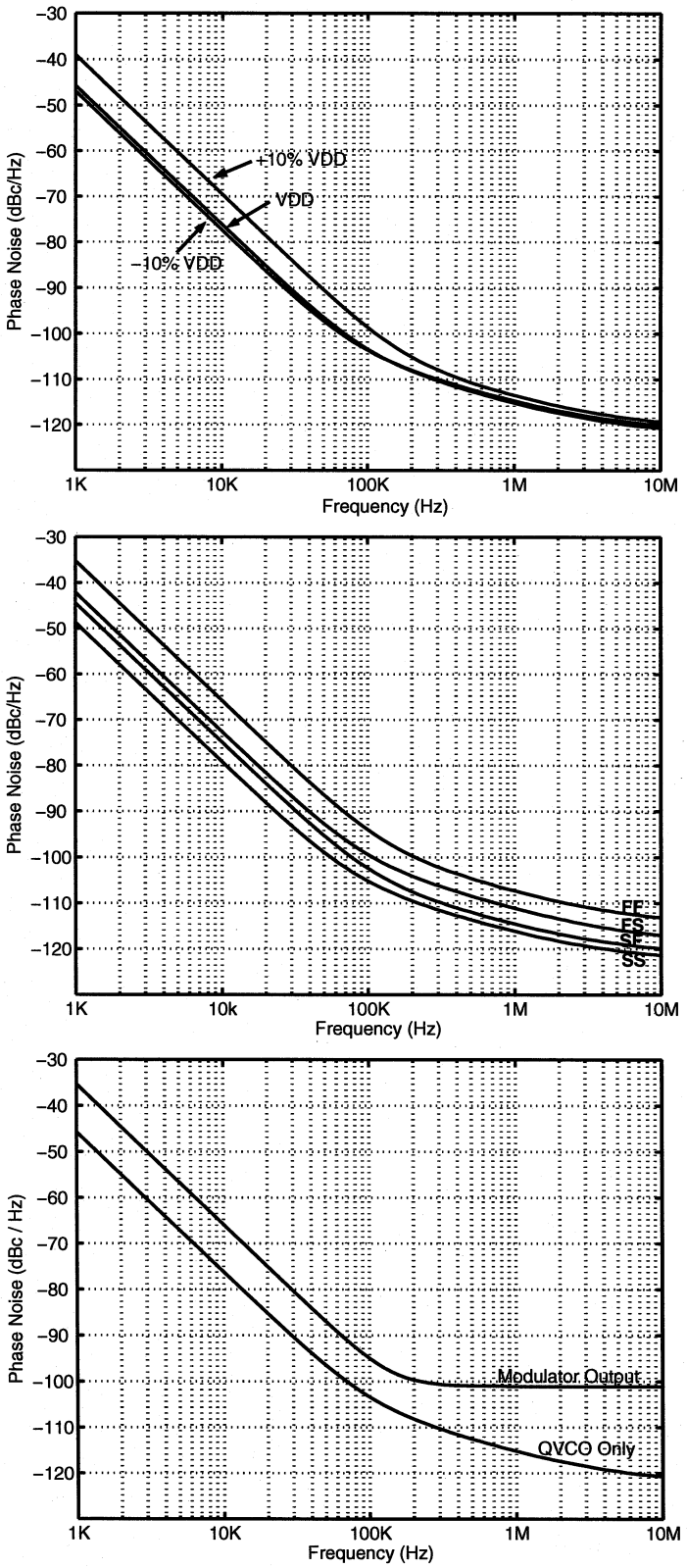


Figure 5.38: Simulated phase noise of quadrature oscillator with $\pm 10\%$ $V_{DD}$ variations (top), at process corners (middle) and total modulator phase noise (bottom).

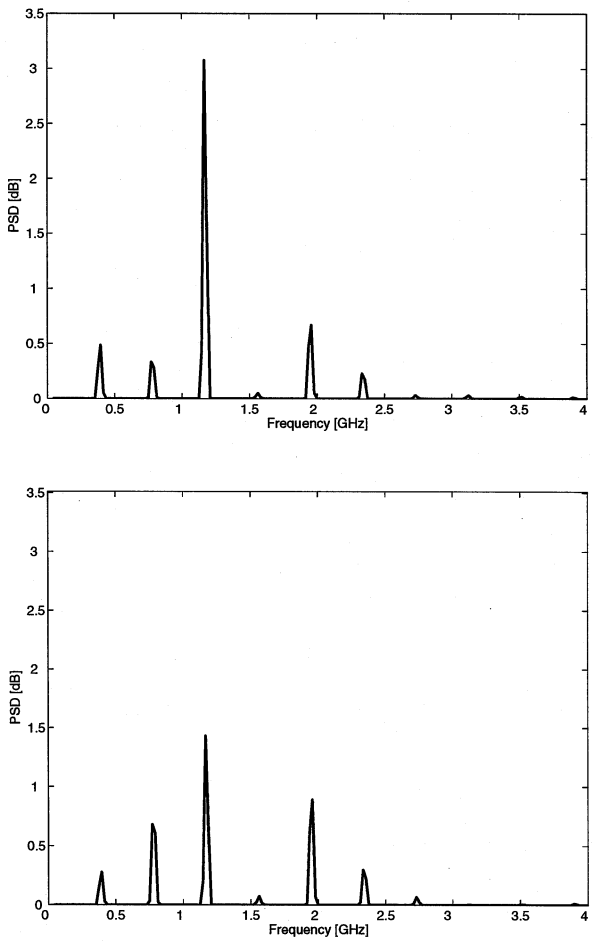


Figure 5.39: Simulated PSD of the output of modulator with the best (top) and worst (bottom) modulation transactions.

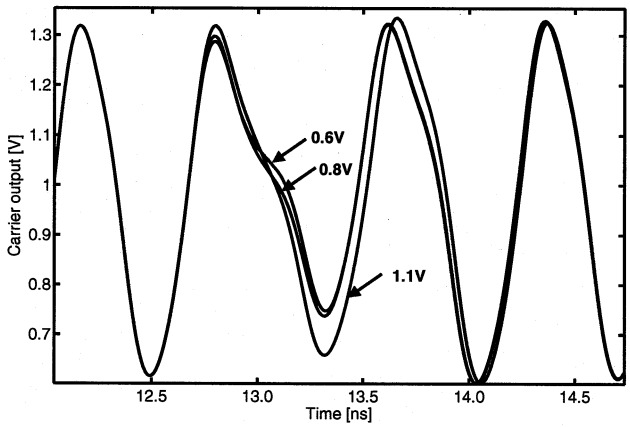


Figure 5.40: Dependence of the modulating transaction on the delay-line control voltage.

Table 5.3: Performance of phase modulator.

| | |
|---|---|
| Technology | TSMC-0.18$\mu$m 1.8V CMOS |
| Carrier frequency | 1.6 GHz |
| Total Area | 3340 $\mu m^2$ |
| Power consumption of delay line | 18 mW |
| Power consumption of oscillator | 10.8 mW |
| Power consumption of MUX | 2.1 mW |
| Phase noise of modulator | -101 dBc/Hz (at 500 KHz freq. offset) |
| Phase noise of oscillator | -110 dBc/Hz (at 500 KHz freq. offset) |

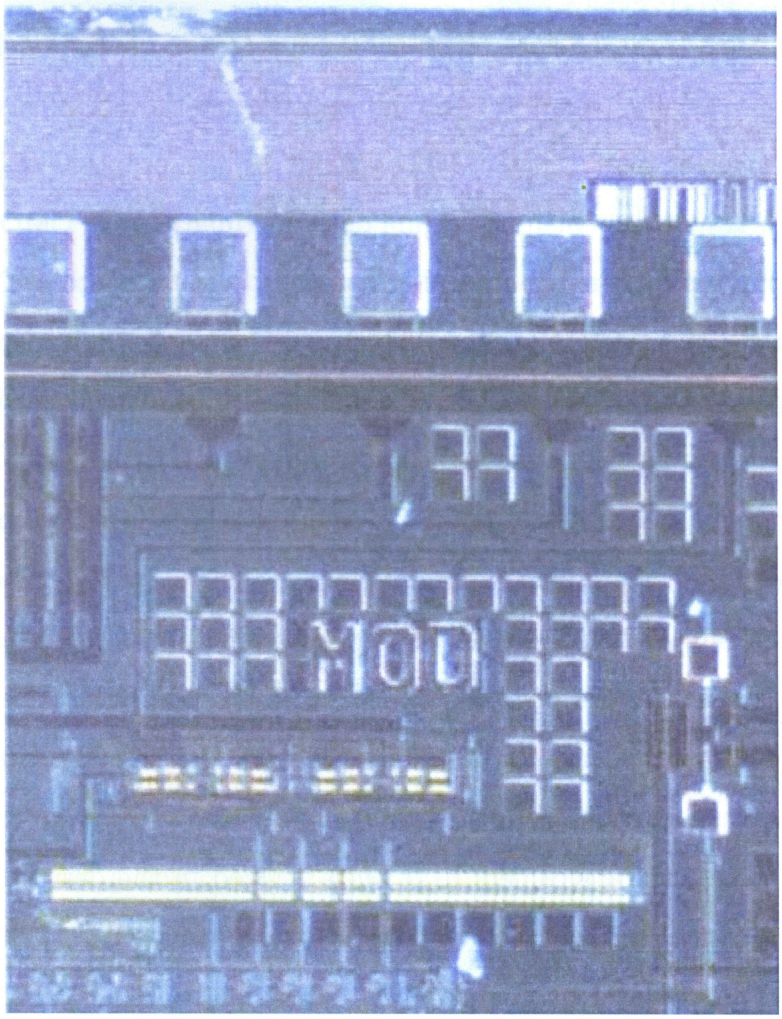


Figure 5.41: Die photo of QPSK modulator.

## 5.5 Summary

Four applications of constant-$Q$ active inductors and CMOS active transformers have been presented. The architecture and design of a current-mode phase-locked loop with a constant-$Q$ CCO and a CMOS cascode active transformer loop filter has been proposed that offers the advantages of an extremely small silicon area, low sensitivity to supply voltage and process variation, fast locking, and good phase noise performance. The layout of the proposed PLL is shown in Fig. 5.18. A new current-mode sigma delta modulator with CMOS active transformer loop filter for blue-tooth applications has been presented. The modulator uses a current mode DAC and ADC together with an active transformer based loop filter to provide tunable bandwidth while greatly reducing the silicon area required. Simulation results of the modulator implemented in TSMC's 0.18$\mu$m 1.8V CMOS technology show the SNR of the modulator is 65 dB with a dynamic range of 50 dB at a 100x oversampling ratio. The total silicon area of the modulator 0.0073 mm$^2$. A new QPSK modulator with optimal bandwidth control has also been presented. It has been shown both analytically and numerically that the proposed modulator reduces the bandwidth of the modulated carrier by minimizing the degree of sharpness of the waveform of the modulated carrier at transactions. CMOS linear active transformers have been utilized in the design of both the 1.6 GHz quadrature oscillator and the 4-to-1 multiplexer. The simulation results of the QPSK modulator implemented in a TSMC-0.18$\mu$m 1.8V CMOS technology have demonstrated that the proposed QPSK modulation scheme effectively minimizes the bandwidth of the modulated carrier.

# CHAPTER 6

# CONCLUSIONS

## 6.1 Active Inductors and Active Transformers.

This thesis has reviewed existing work in gyrator-C configured active inductors and two implementations, the Wu and differential floating CMOS active inductors. The thesis has also proposed a new method of quantifying the performance of active inductors with a figure-of-merit called "mean quality factor" that is better suited to the large signal behavior of active inductors. As the quality factor of active inductors depends on the biasing conditions the conventional quality factor cannot effectively quantify their large signal performance. New CMOS constant-Q active inductors[39] have been proposed which are an active inductor intended for applications where large signal operation is required. Constant-Q active inductors use current-mode feedback to keep the current flowing into the active inductor at a nearly constant level, allowing stabilization of the quality factor in the presence of large signal swings. The key advantages provided by CMOS constant-Q active inductors are:

- Constant-Q active inductors provide a tunable inductance.
- Constant-Q active inductors require a small amount of silicon area as compared to spiral inductors.

- Constant-Q active inductors unlike other active inductors are able to maintain a large quality factor even in large signal operation.
- Constant-Q active inductors are fully compatible with digitally oriented CMOS.

This thesis has also presented a new family of active inductors, CMOS active transformers[40, 41] which are the active circuit equivalent of two magnetically coupled coils. Active transformers use voltage controlled current links to provide the mutual inductance between two active inductors. CMOS active transformers come in both a linear configuration which provides a higher frequency limit, and cascode-configuration providing less sensitivity to the supply and a higher inductance. The key advantages provided by CMOS active transformers are:

- CMOS active transformers are the only active realization of passive coupled coils.
- CMOS active transformers provide a large and tunable self and mutual inductance.
- CMOS active transformers require a small silicon area as compared to spiral transformers.
- CMOS active transformers are fully compatible with digitally oriented CMOS.

This thesis has presented four applications of the proposed constant-$Q$ active inductors and CMOS active transformers. The first application presented is a 2.4 GHz voltage-controlled oscillator with -119.5dBc/Hz phase noise at 1 MHz offset and offers the following advantages:

- The proposed VCO offers a large tuning range.

- The proposed VCO requires a small silicon area.

In the second application a 2.4 GHz current-mode phase-lock loop with -116dBc/Hz phase noise at 1 MHz offset and 80ns lock time has been proposed using a CMOS constant-$Q$ active inductor CCO and a loop filter employing a CMOS cascode active transformer[42, 43]. The proposed PLL offers the following advantages:

- The proposed PLL has adjustable bandwidth to suit a variety of applications.
- The proposed PLL provides execellent phase noise performance.
- The proposed PLL has a much wider frequency range than is possible with passive spiral inductor based VCO or CCOs due to the wide tuning range of the constant-$Q$ CCO.
- The proposed PLL occupies a small silicon area.

The third application presented was a 5 MHz 100X oversampled current-mode sigma-delta modulator with 50dB dynamic range and 65dB SNR for bluetooth applications[39]. The proposed sigma-delta modulator uses a cascode active transformer based loop filter to provide the noise shaping filter and offers the following advantages:

- The tunability of the loop filter bandwidth offers a variable noise-shaping characteristic.
- The tunability of the loop filter bandwidth and the oscillation frequency allow the modulator to be adjusted to suit a large range of applications.

- The exclusive use of active devices in the loop filter allow the sigma delta modulator to occupy a small silicon area.

The final application presented was a 1.6 GHz QPSK phase modulator with -101dBc/Hz phase noise at 1 MHz offset which provided optimized phase transactions in the output carrier using a CMOS linear active transformer based quadrature-VCO and multiplexer[44, 45]. The proposed modulator offers the advantages of:

- The output of the modulator is a bandwidth optimized QPSK output carrier suitable for bluetooth applications.
- The exclusive use of active inductors in the QVCO and multiplexer allow the QPSK modulator to occupy a small silicon area.

## 6.2 Future Work in CMOS Active Inductors.

As seen in this thesis CMOS active inductors although greatly improved are still not capable of the same noise performance as their passive spiral inductor counterparts. Future work would be to investigate methods to further reduce the phase noise of active inductor oscillators to the levels achievable with passive spirals. Work in active inductors is also extremely important as CTM capacitors and spiral inductors occupy extremely large areas, limiting their use in applications where very large numbers of these devices are required such as multi-channel sigma-delta ADCs, and multiple standard radio. Finally active inductors provide much larger frequency ranges than is possible with spiral inductor or spiral transformer type circuits, making them a candidate for wireless schemes where a large tuning bandwidth is required such as ultra-wide-band and possibly even 60 GHz wireless applications.

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