ALL-DIGITAL ΔΣ TIME-TO-DIGITAL CONVERTER WITH BI-DIRECTIONAL GATED DELAY LINE TIME INTEGRATOR

by

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ABSTRACT

All-Digital ΔΣ Time-to-Digital Converter with Bi-Directional Gated Delay Line Time Integrator

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This report presents a low-power time integrator and its applications in an all-digital first-order ΔΣ time-to-digital converter (TDC). Time-to-Digital Converter (TDC) that map a time variable to a digital code is the most important building blocks of time-mode circuits. The time integrator is realized using a bi-directional gated delay line (BD-GDL) with time variable to be integrated as the gating signal. The integration of the time variable is obtained via the accumulation of the charge of the load capacitor and the logic state of gated delay stages. Issues affecting the performance of the time integrator and TDC are examined. The all-digital first-order ΔΣ TDC utilizing the time integrator was designed in using IBM 130 nm 1.2 V CMOS technology and analysed using Spectre ASP from Cadence Design Systems with BSIM4 models. A sinusoid time input of 333 ps amplitude and 231 kHz frequency with an oversampling ratio 68 was digitized by the modulator. The TDC provides first-order noise-shaping and a SNR of 34.64 dB over the signal band 48.27 ~ 231 kHz while consuming 293.8 μW.

Key words - Time-mode circuits, ΔΣ time-to-digital converters, Voltage-to-time converter (VTC), Bi-Directional gated delay line (BD-GDL), Bi-directional gated delay cell (BD-GDC)

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List of Abbreviations

ADC	Analog-to-Digital Converter
BD-GDC	Bi-directional gated delay cell
BD-GDL	Bi-directional gated delay line
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DFF	D Flip-Flop
DLL	Delay-Locked-Loop
DTC	Digital-to-time converter
FFT	Fast Fourier Transform
FIR	Finite-impulse-response
FOM	Figure-of-merit
GRO	Gated Ring Oscillator
IIR	Infinite-impulse-response
LSB	Least Significant Bit
MASH	Multi-stage Noise Shaping
OTA	Operational trans conductance amplifier

OSR	Over Sampling Ratio
PD	Phase Detector
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
PSD	Power Spectral Density
PVT	Process (supply-)Voltage Temperature
PWM	Pulse Width Modulation
SAR	Successive Approximation Register
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SQNR	Signal-to-Quantization-Noise Ratio
TDC	Time-to-Digital Converter
VCO	Voltage-Controlled Oscillator
VCDU	Voltage-controlled delay unit
VTC	Voltage-to-Time Converter
XOR	Exclusive OR
ΔΣ	Delta-sigma

1. Introduction

This chapter examines the motivation of this project by reviewing time-mode signal processing and important building blocks for time-mode signal processing. The key building blocks of time-mode circuits includes time-to-digital converters (TDCs), Digital-to-time converters (DTCs), time amplifiers and time quantizers. A detailed review on these building blocks and applications will also be discussed in this chapter.

1.1 Motivation

The rapid scaling of CMOS technology and improvement in the intrinsic delay of digital circuits has resulted in sharp increase of time resolution and the continuous reduction of voltage resolution. As a result, CMOS analog circuits are continuously losing the benefits of specialized and process-controlled components which are critical to the performance of these circuits. In addition, voltage-mode systems also cope with a rapidly decreasing voltage headroom, that is, the difference between the given supply voltage of a circuit and the minimum supply voltage of the circuit required for MOS transistors to operate in saturation region. The shrinking voltage headroom not only limits the maximum achievable signal-to-noise ratio (SNR), it also signifies that the effect of the nonlinear characteristics of MOS devices subsequently reduces the dynamic range of voltage-mode circuits. Further, technology scaling raises the thermal noise floor quantified by kT/C where k is Boltzmann's constant, T is temperature in Kelvin, and C is the minimum capacitance. As a result, the accuracy of voltage-mode circuits, loosely defined as the ration of the minimum detectable voltage, typically set by thermal noise floor, to the maximum available voltage headroom, scales poorly with technology. Furthermore, current-mode circuits achieve low voltage swing by lowering the impedance of the nodes. This low-impedance gives rise to large branch

currents. As a result, current-mode circuits typically consume more power. Hence, they are suitable for applications where speed rather than power consumption is most critical. Therefore, the performance of both circuits does not scale well with technology due to their limitations.

As a result, time-mode signal processing where information is represented by the time difference between occurrence of two digital events rather than the nodal voltages or branch currents of electric networks offer viable and technology friendly way to reduce scaling-induced performance degradation of mixed-mode systems.

1.2 Overview of time-mode signal processing

Time-mode approaches where information is represented by the difference between the time instants at which digital events take place rather than the nodal voltages or branch currents of electric networks. The time difference between the rising edges of the two digital signals is directly proportional to the amplitude of the analog signal. Since time-mode circuits perform analog signal processing in the digital domain, not only the performance of these circuits scales well with technology, but also offer several attractive characteristics including full programmability, low-power consumption and high-speed operation. The detrimental effect of technology scaling on the performance of voltage-mode and current -mode analog signal processing disappears in time-mode circuits. Time-mode circuits are less sensitive to interferences such as cross talk, switching noise and substrate coupling, which have a severe impact on the performance of voltage-mode and current-mode circuits. Although time-mode signal processing has a number of advantages over voltage-mode and current-mode counterparts, there are some challenges that need to be overcome in order for time-mode circuits to be deployed in broad range of applications. The intrinsic gated delay of the digital circuits benefits from technology scaling, device mismatch arises mainly from process spread deteriorates with technology scaling. In order to minimize the effect of device

mismatch, minimum sized unit delay cells should be avoided. This inevitably has a detrimental effect on the speed and subsequently on the resolution of time-mode circuits. Time-mode circuits mostly built upon delay cell, such as static CMOS inverters and current-starved CMOS inverters, the propagation delay of these delay cell is a strong function of supply voltage fluctuation. For time-mode circuits, delay-locked loops (DLLs) are widely used to minimize the effect of process, supply and temperature (PVT) variations on the delay of the delay lines. Although DLLs can be used to stabilize the delay of the delay lines, it is difficult to use them to minimize the effect of PVT on the delay of the logic gates that are often part of time-mode circuits and control the operation of time-mode circuits. Time-mode circuits have also been used in audio [12], medical imaging [13], instrumentations [14], infinite-impulse-response (IIR) filters [15], finite-impulse-response (FIR) filters [16], and anti-imaging filters [17], frequency synthesizers [18, 19]. Despite these developments, there are very few literatures that offer a comprehensive analysis of the principles and design techniques of CMOS time-mode circuits for mixed-signal processing. Therefore, the principles and design techniques of the building blocks for time-mode circuits are provided in the next few chapters as part of this report.

1.3 Current Literatures on Time-mode Circuits

Time-mode signal processing, where information is represented by the time difference between the occurrence of digital events, offer a viable and technology friendly means to combat scaling-induced difficulties encountered in mixed-mode systems. ΔΣ modulators are perhaps one of the most widely used mixed-mode systems. Li *et al.,* showed that an input voltage can be digitized using a voltage-to-time converter (VTC) followed by a time-to-digital converter (TDC) [1]. Itawa *et al.,* demonstrated that an input voltage can be digitized using a voltage-controlled oscillator (VCO). The number of the oscillation cycles of the oscillator recorded using a counter provides

the digital representation. The continuity of the phase of the oscillator yields the desired first-order noise-shaping of quantization noise [2]. Hovin *et al.,* showed that first-order noise-shaping can also be obtained from first-order phase differentiators [3]. Straayer *et al.*, showed that gated ring oscillators (GROs) also possess first order noise-shaping obtained by freezing the residual phase of one sampling phase and passing it over to the next phase [4]. Konishi *et al.,* demonstrated that the floating output state of GROs during the absence of the gating signal can be replaced with another oscillation state to minimize the detrimental effect of charge leakage and charge redistribution [5]. The main drawbacks of reported ΔΣ modulators with a GRO/SRO quantizer include poor scalability and excessive power consumption arising mainly from the use of operational trans conductance amplifier (OTA) loop filters for a large loop gain. Many efforts were made to replace OTA-based active filters with time-mode filters such that entire modulators are realized digitally. Taillefer and Roberts proposed a ring oscillator voltage-to-time integrator that performs both voltage-to- time conversion and time integration [6]. Ali-Bakhshian and Roberts introduced a time memory cell consisting of two switched delay units (SDUs) that can store a time variable indefinitely and reading out the stored time variable upon a read command so that time integration is possible [7]. The time-difference accumulator proposed by Hong *et al.*, consists of two back-to-back connected time adders realized using four gated delay cells [8], [9]. Kim *et al.,* showed that a gated delay line functions as a time register with the gating signal consisting of the time variable to be stored and a trigger signal [10], [11].

1.4 Outline

This report presents all-digital time-mode integrator realized using a bi-directional gated delay line with the time variable to be integrated as the gating signal. The integration of the time variable is obtained via the accumulation of the charge of the load capacitor and the logic state of the delay

stages. The report is organized as follows: Chapter 2: Building Blocks of Time-mode Circuits and Applications of Time-mode Signal Processing, Chapter 3: Proposed work: All-Digital ΔΣ TDC using Bi-Directional Gated Delay Line Time Integrator, Chapter 4: Discussion, Chapter 5: Design Consideration and Simulation Results, Chapter 6: Conclusion, Chapter 7: Future work.

2. Building Blocks of Time-mode Circuits and Applications

2.1 Building Blocks of Time-mode Circuits

A complex analog circuit is typically constructed from a set of building blocks such as common-source amplifiers, common-gate amplifiers, common-drain amplifiers, cascode amplifiers, and differentially configured amplifiers. Similarly, time-based signal processing systems are made of a set of building blocks that perform tasks such as interfacing with voltage-mode and current-mode circuits, time amplification, time quantization, time-to-digital and digital-to-time conversion.

2.1.1 Voltage-to-time Converters

One of the key building blocks of time-mode systems for processing analog signals is voltage-to-time converters (VTCs) that map a voltage to time variable with its value directly proportional to the amplitude of the voltage. A VTC serves as a gateway bridging between voltage-mode and time-mode domains. The most important performance indicators of VTCs are linearity, bandwidth and conversion gain. As time-mode circuits are digital circuits, the linearity of time-mode system is largely dominated by that of its VTC. A large and constant conversion gain over a large input voltage range is highly desirable. The bandwidth of VTC, on the other hand, determines the maximum frequency of the input that time-mode circuits can process. Since MOSFETs are highly nonlinear devices, the design of VTCs with a large conversion gain over a large input range, low power consumption, and a high conversion speed is rather challenging. VTCs are typically implemented using a voltage-controlled delay unit (VCDU) with a reference signal with which the

input signal is compared from a timing ring voltage-controlled oscillator (VCO) whose frequency is constant.

A voltage can be mapped to a time variable using the VCDU as shown in Fig. 2.1. The VCDU consists of a current-starved inverter, that is, a static inverter with its charging or discharging current controlled by a current source, a load capacitor, and a static inverter. The load capacitor should be linear and its capacitance should be much larger as compared with the capacitances of the transistors such that the effect of the nonlinearity of the device capacitances is negligible as compared with that of the load capacitor. The current-starved inverter is clocked by a periodic signal CLK that presets the VCDU prior to a conversion operation. In the pre-charge phase where CLK is low, the load capacitor charges to V_{DD} and the output of static inverter is set to logic-0. In the following discharge phase where CLK = 1, the load capacitor is discharged by the current of M3 whose value is set by the input voltage V_{in} at the end of the pre-charged phase.

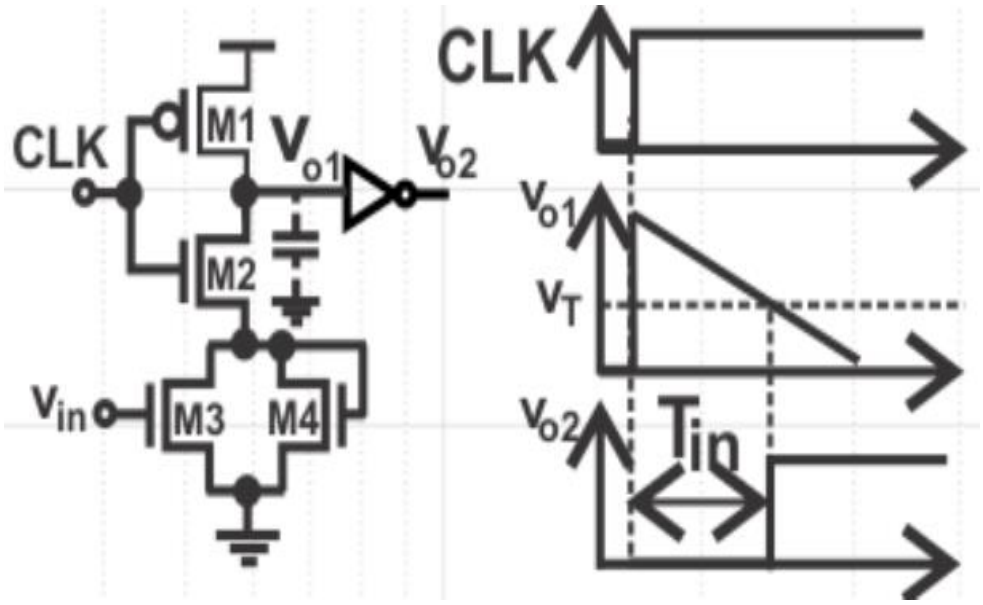

Fig. 2.1 Voltage-to-time converter using voltage controlled delay cell.

The voltage of the gate of M3 is kept unchanged during the discharge phase and so is the discharging current of the load capacitor. As a result, the voltage of capacitor *C* decreases linearly

with time. When V_{o1} drops below the threshold voltage V_T of the following static inverter, V_{o2} will be set to logic-1. The value of resultant time variable T_{in}, which measured from the time instant at which CLK = 1 to the time instant at which V_{o1} crosses the threshold voltage of the inverter. An additional transistor M4 is added in parallel with M3 to improve the linearity of time variable T_{in}. To further improve the linearity, a differentially configured VTC consisting of two identical VTCs can be used, which will be discussed in later chapters.

2.1.2 Time-to-Digital Converters

TDCs map a time variable to a digital code. TDCs are perhaps the most important building blocks of time-mode circuits. The deployment of TDCs in nuclear science research dates to 1970s [20,25]. The application of TDCs has extended well beyond nuclear science to digital storage oscillators [21,22], laser range finder [23], and digital frequency synthesizers [24]. Similar to analog-to-digital converters, the performance of TDCs is quantified by a number of parameters such as SNR and SNDR for noise shaping TDCs, and differential nonlinearity (DNL) and integral nonlinearity (INL) for sampling TDCs. To compare the performance of different architectures, the amount of power consumption per conversion step of TDCs is the most widely used figure-of-merit (FOM).

A. Direct-Counter TDC

A direct-counter TDC is basically a counter that quantizes a time-difference variable by counting the number of the cycles of a reference clock whose period T_c is much smaller as compared with the time-difference T_{in} to be measured, as shown in Fig. 2.2(a). These TDCs have a dynamic range upper-bounded by the size of the counter. In addition, they provide a superior linearity as the linearity is only affected by the stability of the frequency of the reference clock. The quantization errors Δ_1 and Δ_2 are due to the misalignment of the rising edges of START, STOP, and that of the reference clock. Clearly, $0 \leq \Delta_1, \Delta_2 \leq T_c$. The resolution of direct-counter TDCs is set by the period

of the reference clock. The higher the frequency of the reference clock, the better the resolution, and the smaller the quantization error. This, however, is at the cost of high power consumption and a deteriorating crosstalk. Direct-counter TDCs are therefore preferred only if T_{in} is large simply due to their ease of implementation. To minimize the quantization error of direct-counter TDCs, Chen *et al.* showed that the quantization errors Δ_1 and Δ_2 can be first stretched much larger than T_c and then digitized by the reference clock, yielding a significantly reduced quantization error, as shown in Fig. 2.2(b) [22]. Pulses T_1 and T_2 are generated at the rising edge of START and STOP, respectively with their falling edge aligned with the next rising edge of the reference clock. Pulse stretching starts with the assertion of a reset (RST) command that brings the voltage of C_1 and C_2 to V_{DD}. The discharge of C_1 and C_2 is controlled by J_1 and J_2, respectively. Since $J_1 = N J_2$ and $C_2 = M C_1$ with M, N > 1, the discharge of C_1 is much faster than that of C_2. The discharge process is initiated by T_1. V_o is set to HIGH and will remain HIGH until $V_{c2} = V_{c1}$. Since V_{c2} drops much slower, it will take k cycles of CLK before $V_{c1} = V_{c2}$ occurs. The number of cycles needed is recorded by the counter incremented by CLK. The content of the counter therefore provides the digital representation of the quantization errors Δ_1. The same process is followed when quantizing Δ_2. To determined k, from $\Delta V_{c1} = \Delta V_{c2}$ where ΔV_{c1} and ΔV_{c2} are the voltage drop of C_1 and C_2 from V_{DD}, respectively and noting $\Delta V_{c1} = (J_1=C_1) T_1$ and $\Delta V_{c2} = (J_2=C_2) T_c k$, we arrive at $k = M N (T1=Tc)$ or equivalent $T1= k T_c = M N T_1$. T_1 is the stretched version of T_1. It is evident that T_1 is stretched by $M N$ times. The dual-slope of the preceding pulse stretching approach makes it less sensitive to the effect of PVT. This approach, however, suffers from a speed penalty due to the slow discharge of C_2. The need for a voltage comparator and two constant current sources also makes it less attractive in digital-oriented designs.

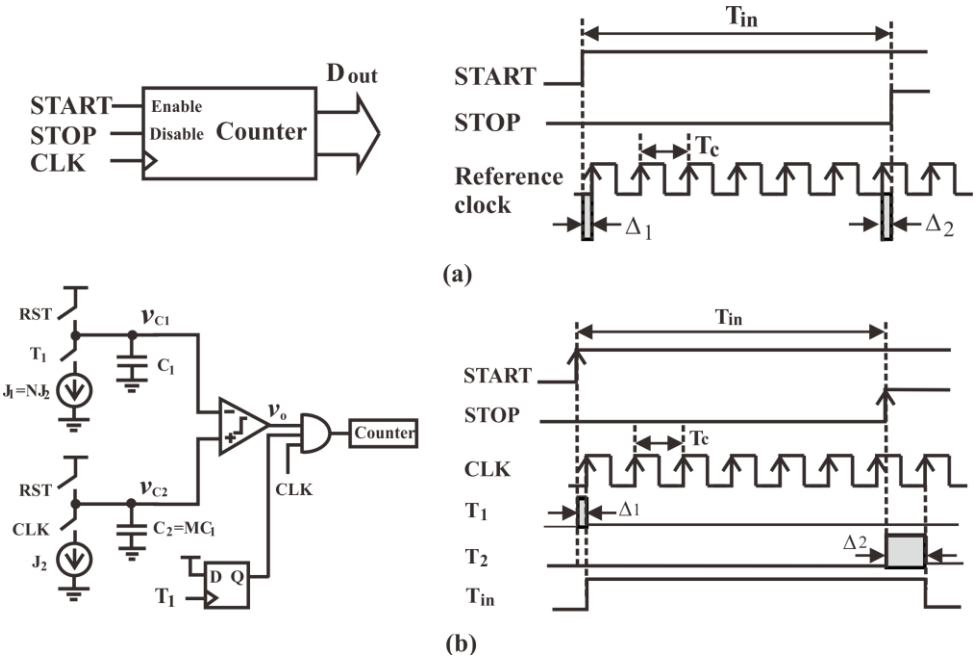

Fig. 2.2 (a) Direct-counter TDC. The counter starts at START=1 and stops at STOP=1. Δ_1 and Δ_2 are quantization errors with Δ_1; $\Delta_2 \leq T_c$. The input in the time domain is represented by: $T_{in} = nT_c + \Delta_1 + \Delta_1$. (b) Direct-counter TDC with pulse stretching.

B. Delay-Line based TDC

To reduce quantization error without sacrificing speed or deploying analog circuitry, the delay-line TDC shown in Fig. 2.3 (without the counter) with a START signal propagating through the delay line and a STOP signal disabling D Flip-Flops (DFFs) can be used. The dynamic range of delay-line TDCs is from 00…0 to 11…1, thermometer coded. Clearly, the upper bound of the dynamic range of delay-line TDCs is set by the length of the delay line while the lower bound is set by the delay of the delay stages. Since the resolution is limited by the delay of the delay cells, the performance of delay-line TDCs scales well with technology [26]. The linearity of delay-line TDCs is determined by the mismatch of the delay of the delay stages and worsens when the number of delay stages is large, simply due to the accumulation of delay mismatch-induced error. To minimize the effect of PVT on the delay of delay cells and error accumulation along the delay line, a delay-locked loop (DDL) is typically employed, as shown in Fig. 2.3 [27]. If the delay of each

delay stage is τ and the number of delay stages is *N*, then in the lock state, START and X_N are phase-aligned, i.e. X_N lags START by T_c where T_c is the period of START. Since START and X_N are phase-aligned, we have $\tau = T_c = N$ where τ is the delay of the delay stages. Clearly τ is only affected by T_c and *N*, and is not subject to the effect of PVT. Note that since the DLL locks to the input signal in this configuration, delay-line TDCs do not need a reference clock. It should also be noted that TDCs with DLLs locked to a reference rather than the input was also proposed [28]. In this approach, two identical delay lines, one locked to the reference and the other processes the input, are needed. The key advantage of this approach is that the delay of the dual delay lines is only determined by the reference clock and is independent of the input.

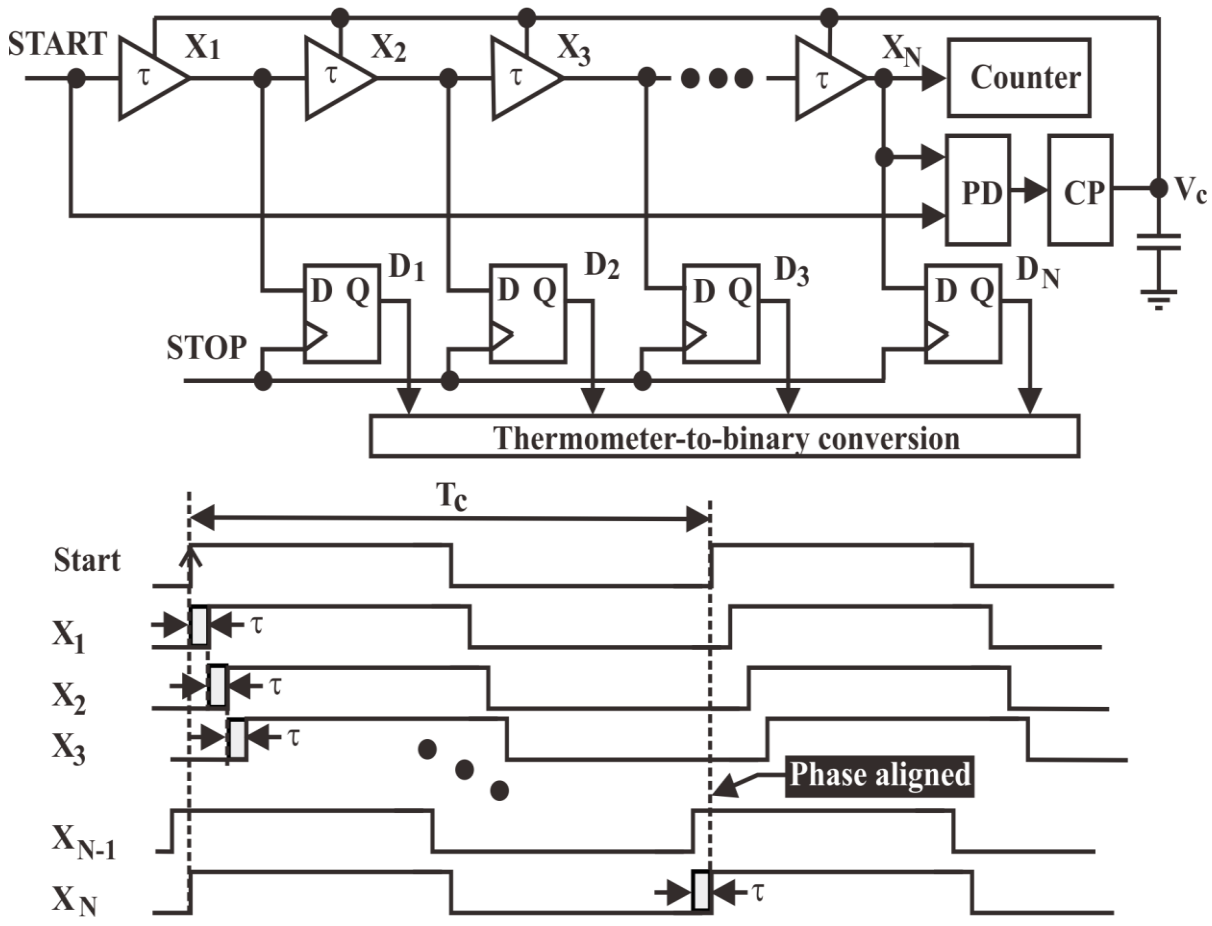

Fig. 2.3 Delay-line TDCs (w/o counter). The delay of *kth* delay cell is given by $\tau_k = \tau + \Delta\tau_k$ where τ is nominal value of the delay and $\Delta\tau_k$ is the random deviation of the delay from τ. When the counter is added, it becomes a direct-counter TDC with gate-delay interpolation.

C. Vernier Delay-Line TDC

High-resolution TDCs can be obtained using Vernier delay lines where START and STOP signals whose time difference is to be measured propagate in two separate delay lines of the same length but different delays, as shown in Fig. 2.4 [29, 30]. The delay line in which START propagates thereafter called START-line has a slightly longer delay as compared with that of STOP-line, i.e. $\tau_1 > \tau_2$. Since the delay of START-line is larger, STOP signal propagating in STOP-line will catch START signal in START-line if the lines are long enough and the time difference between START and STOP signals is not overly large. When this occurs, time-to-digital conversion is completed and the resultant digital code is given at the output of the DFFs. The time at which a catch-up occurs is determined from $T_{catch} = N\tau_1 = N\tau_2 + T_{in}$ where N is the number of the delay stages of the Vernier delay lines and T_{in} is the time difference between START and STOP. For a given T_{in}, the number of the delay stages is determined from $N = \Delta T = (\tau_1 - \tau_2)$. Clearly, the dynamic range of Vernier delay line TDCs is upper-bounded by the length of the lines and lower-bounded by $\tau_1 - \tau_2$. Although theoretically, if $\tau_1 - \tau_2$ is sufficiently small and Vernier delay lines are sufficiently long, the resolution of Vernier delay line TDCs can be made arbitrarily small. In reality, it is limited by the finite length of Vernier delay lines and the mismatch of the delay of the delay cells. Vernier delay line TDCs suffer from a large hardware cost due to the need for two long delay lines and a finite dynamic range upper-bounded by the length of the delay lines, especially when $\tau_1 - \tau_2$ is small. The performance of Vernier delay line TDCs can be improved using two-level Vernier lines with the coarse Vernier lines having a large delay difference $\Delta\tau_c$ and the fine Vernier lines having a small delay difference $\Delta\tau_f$ where the subscripts c and f signify “coarse” and “fine”, respectively [31]. Although the dynamic range is improved, the complexity of the TDC is also significantly increased. To minimize the effect of PVT on Vernier delay line TDCs, DLL-stabilized Vernier delay line TDCs shown in Fig. 2.4 (with dotted sections) can be utilized [30]. The transition edge

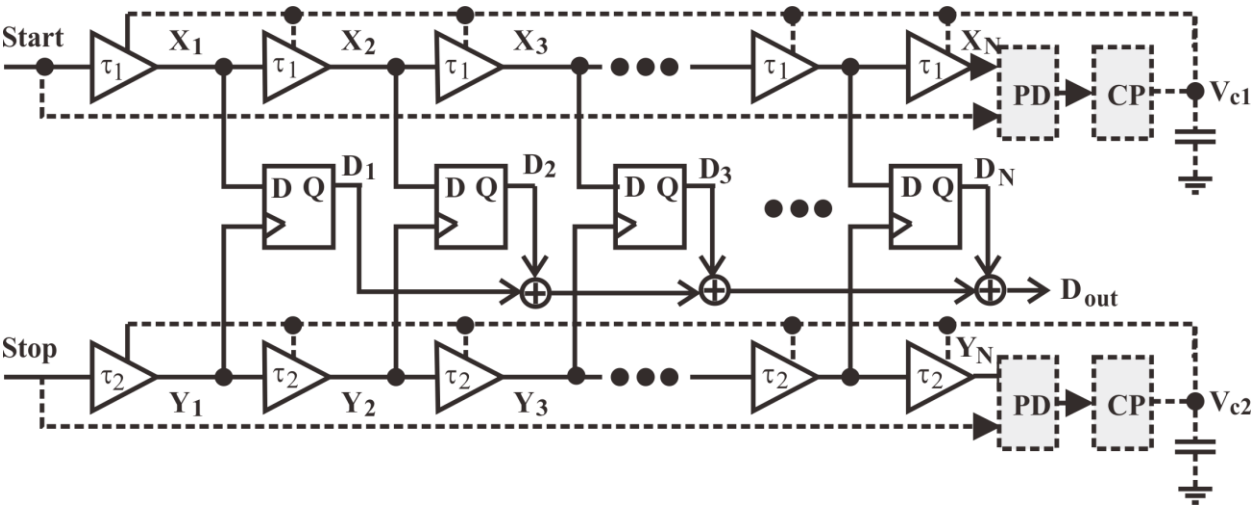

Fig. 2.4. Vernier delay line TDC.

of X_N is phase-aligned with START such that $N\tau_1 = T_1$ where T_1 is the period of START from which we have $\tau_1 = T_1 = N$. Clearly this configuration does nothing to minimize the effect of PVT on STOP-line. To minimize the effect of PVT on the delay of STOP-line, another DLL can be utilized, as shown in Fig. 2.4.

2.1.3 Digital-to-Time Converters

DTCs map a digital code to a time variable. A digital-to-time operation is needed in applications such as time-mode successive approximation TDCs. A DTC assumes a similar role as that to a digital-to-analog converter in voltage-mode successive approximation analog-to-digital converters (ADCs) or multibit ΔΣ modulators to establish negative feedback.

2.1.4 Time Amplifiers

Similar to a voltage amplifier that amplifies a voltage, a time amplifier amplifies a time variable. Time amplification is needed in application such as the precision measurement of the width of a narrow pulse where the pulse width is often too small to be quantized accurately. Time amplification can also be employed for accurately quantizing the output of TDC-based phase

detectors near the lock state to establish a precision phase lock. Time amplifiers play vital role in improving the resolution of time-mode circuits. For the high-speed time digitization, the bandwidth of time amplifiers is also a great of importance.

A. Regenerative Time Amplifier

Time amplifiers that are based on the metastability of SR-latches were proposed by Abas *et al.*, [32] and are shown in Fig. 2.5(a). These time amplifiers utilize the re-generative mechanism of the SR-latch to expend narrow pulses [34, 35]. A key advantage of RS-latch time amplifiers is their fast response and ability to amplify a small-time difference. The main drawback of these time amplifiers is that the gain of the amplifiers is set by the characteristics of the latch and is strongly subject to the effect of PVT. Another notable drawback of these time amplifiers is small input range due to the positive feedback mechanism and poor gain nonlinearity. The SR-latch time amplifier proposed by Lee and Abidi and shown in Fig. 2.5(b) improves the input range of the generic SR-latch time amplifiers by inserting two delay units with delay τ to generate an unbalanced re-generation mechanism. A drawback of Lee-Abidi time amplifier is that the time mismatch of the buffer delays might be significant once the input time difference to be amplified is small, introducing a negligible error. This drawback can be removed by using unbalanced active charge pump load proposed in [36].

B. DLL-based Time Amplifier

The DLL-based time amplifier proposed by Rashidzadeh *et al.*, and shown in Fig. 2.6 uses a closed-loop approach to amplify time while minimizing the effect of PVT on the delay [33, 37]. The two periodic inputs of identical period T are fed to two delay lines of the same number of delay stages N but different stage delays. The phase of the waveform at nodes A and B is aligned using the DLL that adjusts the delay of delay line 1 such that $\phi_{in1} + 2\pi\tau_1/T = \phi_{in2} + 2\pi\tau_2/T$ from

which we have $\tau_1 - \tau_2 = 2\pi/T = T(\tau_1 - \tau_2)$. The output of the time amplifier is given by $T_{out} = (N - 1)(\tau_1 - \tau_2)$.

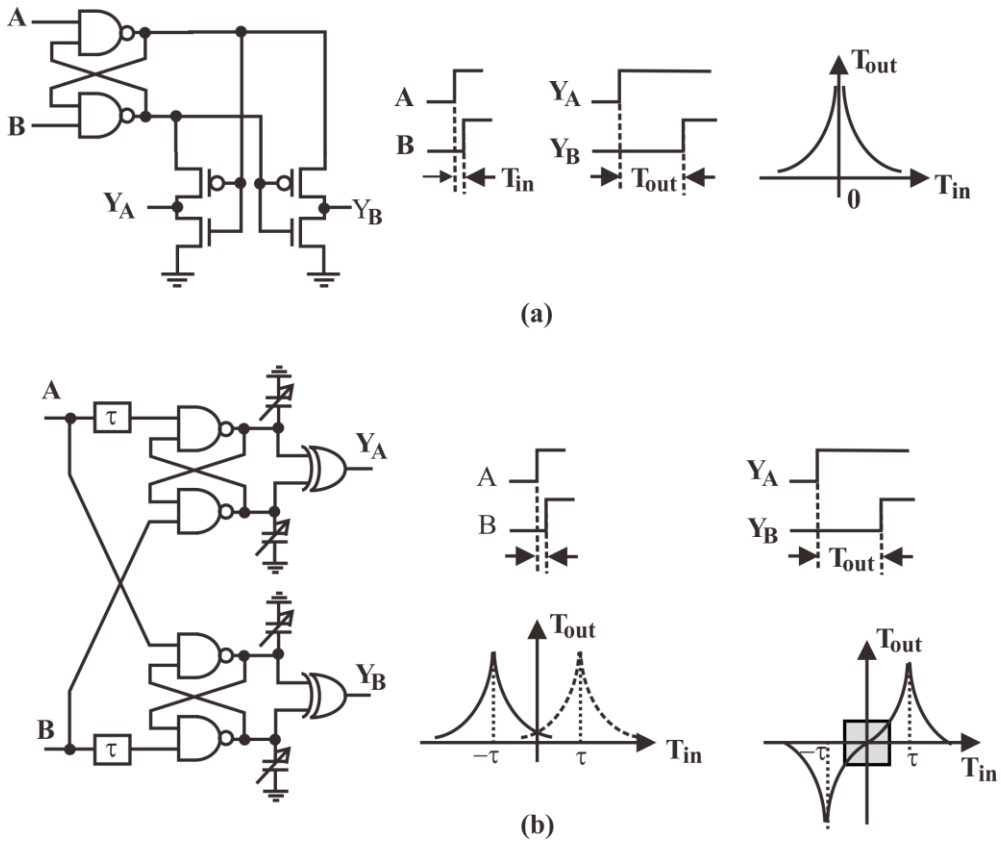

Fig. 2.5 (a) RS-latch time amplifier (b) RS-latch time amplifier with an improved input range.

Since the DDL must be settled in order to amplify the time difference, the deployment of this type of time amplifiers for high-speed applications is rather difficult. The mismatch of the delay of the delay stages, which is not corrected by the DLL, will also affect the accuracy of the amplifier especially when $\phi_{in1} - \phi_{in2}$ is small.

C. Charge-pump Time Amplifier

Time amplification can also be accomplished by first charging a pair of capacitors with two digital signals whose time difference is to be measured and then sensing the difference of the voltage of the capacitors [38, 39]. The need for constant current sources and voltage comparators of this

approach, however, undermines the very reason why time-mode approaches are wanted in the first place. The time amplifier proposed by Kim *et al.,* in [40] utilizes a primitive logic operation to achieve a 3.75 ps resolution in 65 nm CMOS. Since the implementation is completely open-loop, its performance is subject to the effect of PVT.

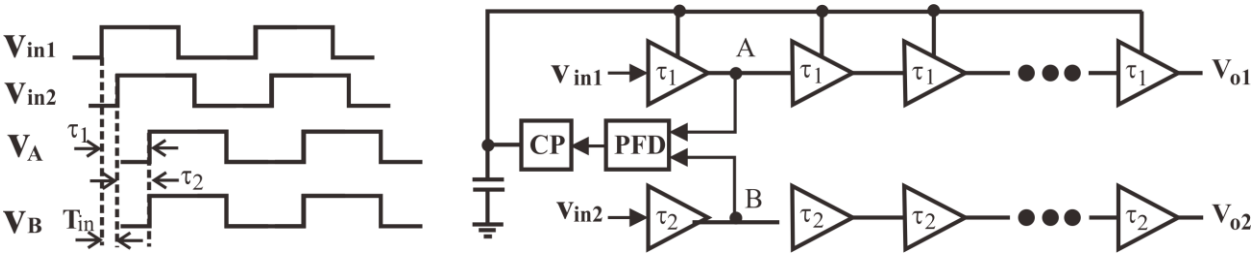

Fig. 2.6. DDL-based time amplifier proposed by Rashidzadeh *et al.* [33].

2.1.5 Time Quantizers

A single bit voltage quantizer maps a voltage to a Boolean variable by comparing it with a reference voltage. Similarly, a single bit time quantizer maps a time variable to a Boolean output by comparing it with a time reference. Time quantizers can be realized using a time comparator with the time reference with which the input compares coming from a voltage controlled oscillator (VCO) of a constant frequency. To conduct the multibit quantization of a time variable, the time variable can be used as a gating signal to activate or deactivate a multistage ring oscillator of a constant oscillation frequency, as known as gated ring oscillator (GRO). Since the number of the oscillation cycles of the oscillator and the output of each stage of the oscillator uniquely correspond to the duration of the gating signal, a multibit time quantizer can be constructed. GRO-based multibit time quantizers offer the intrinsic advantage of first-order noise shaping. In addition, as compared with voltage-mode multibit quantization, which requires a total of 2^N voltage comparators where N is the number of quantization bits, VCO based multibit time quantization

offers the advantage of low-power consumption, fast quantization resulting in a large over sampling ratio (OSR), good linearity, first -order noise-shaping and all-digital realization.

2.2 Applications

The key applications of time-based signal processing include analog-to-digital converters, all-digital phase locked loops (PLLs), all-digital frequency synthesizers, and time-based temperature sensors.

2.3 Summary

In this chapter, the key building block of time-mode circuits including VTCs, TDCs, DTCs, time amplifiers and time quantizers and applications of time-mode signal processing were briefly examined. It can be concluded that the current-starved VTC, regenerative time amplifier, GRO-based TDC can be used to realize all-digital time-mode circuits since they offer the advantage of low-power consumption, simple architecture and require small area.

3. Proposed work: All-Digital ΔΣ TDC using Bi-Directional Gated Delay Line Time Integrator

This chapter presents a new all-digital time-mode integrator realized using a bi-directional gated delay line with the time variable to be integrated as the gating signal. The integration of the time variable is obtained via the accumulation of the charge of the load capacitor and the logic state of the delay stages. The differential VTC implemented using two identical voltage controlled delay units (VCDUs) is discussed in Section 3.1. Section 3.2 examines the bi-directional gated delay cell (BD-GDC). The bi-directional gated delay line (BD-GDL) implemented using BD-GDCs is investigated in Section 3.3. Section 3.4 looks into how BD-GDL function as a time integrator. Other key building blocks required for all-digital ΔΣ TDC are analyzed in Section 3.5. The all-digital first order single-bit ΔΣ TDC is discussed in Section 3.6. The chapter is summarized in Section 3.7.

3.1 Differential Voltage-to-time converter

A differentially configured VTC consisting of two identical single-ended VTCs generates the gating signal which is a sinusoidal time signal from a sinusoidal voltage signal using a sampling clock, as shown in Fig. 3.1. Since the capacitor voltage V_c drops with time in a nonlinear fashion due to the dependence of the current following through the output resistor of transistors M1 and M2 on V_c, single-ended VTCs exhibit a high degree of nonlinearity. The differentially configuration of the VTC ensures that even-order harmonics are adequately suppressed. Fig. 3.2 plots the spectrum of the output of the differential VTC. Fig. 3.3 shows the comparison of the spectrum of single-ended VTC and differential VTC.

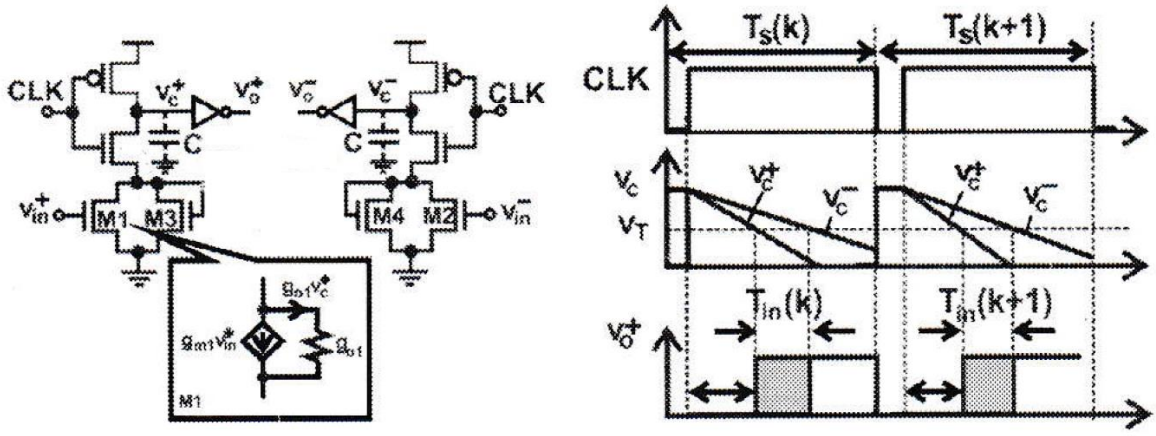

Fig. 3.1 Differential voltage-to-time converter. Diode-Connected M3 and M4 improve the linearity.

3.2 Bi-Directional Gate Delay Cell

Consider the bi-directional gated delay cell shown in Fig. 3.4. The rising edge of a digital signal propagates from node 1 to node 2 (forward) if gating signal T_{in} is positive or from node 2 to node 1 (backward) if T_{in} is negative. The per-stage delay in both directions is identical. Consider the case where the signal propagates from node 1 to node 2. Node 1 and node 2 are initialized to V_{DD} and 0 V, respectively. When T_{in} [j] > 0, the capacitor connected to node 2 will be charged and the variation of capacitor voltage denoted by ΔV_2 will be proportional to the duration of T_{in} [j]. Similarly, if T_{in} [j] < 0, the capacitor connected to node 1 will be discharged and the variation of capacitor voltage denoted by ΔV_1 will be proportional to the duration of T_{in} [j]. The gating signal T_{in} [j] can therefore be represented by the voltage variation of the load capacitors. Consider that T_{in} is a train of pulses T_{in} [j], k = 1, 2, …, K, that can be either positive or negative. If T_{in} [j] is positive, the load capacitor is charged and the resultant voltage increment is proportional T_{in} [j]. If T_{in} [j] is negative, the load capacitor is discharged and the resultant voltage decrement is also proportional T_{in} [j]. We therefore have $\Sigma_{j=1} T_{in,k} = \Sigma_{j=1} k_j \Delta V_{c,j}$. If V_c exceeds the threshold voltage

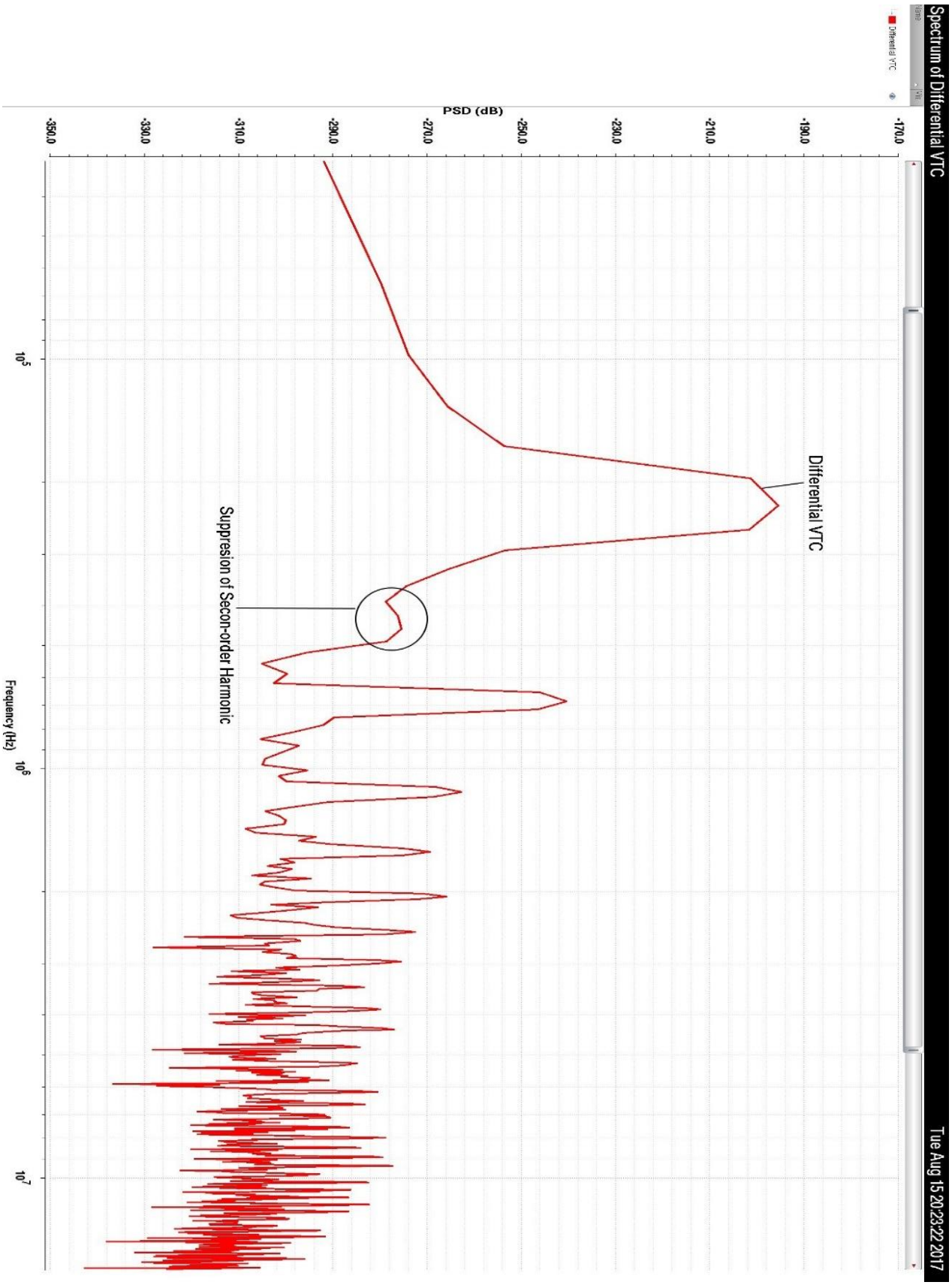

Fig. 3.2 Spectrum of Differential voltage-to-time converter

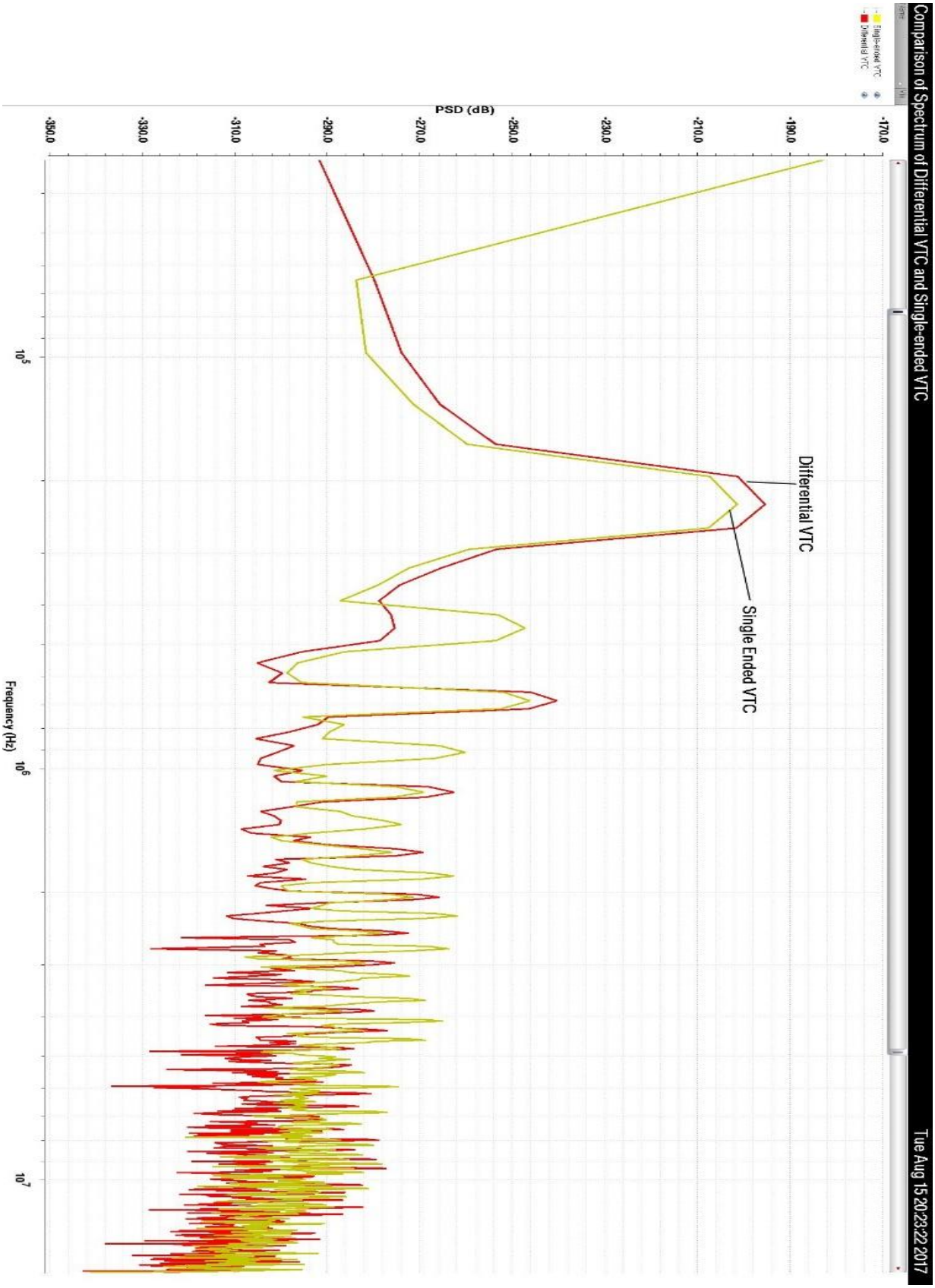

Fig. 3.3 Comparison of Spectrum of Differential VTC and Single-ended VTC

of the next delay stage, the signal will propagate to the next stage. The bi-directional gated delay cell thus performs the accumulation (integration) of T_{in} by means of charge accumulation and the change of the logic state of the delay stages.

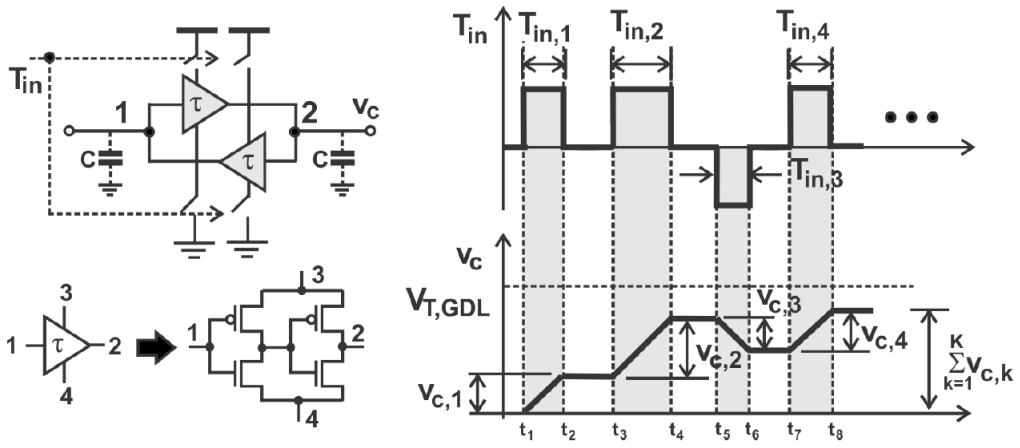

Fig. 3.4 Bi-Directional Gated Delay Cell.

3.3 Bi-Directional Gate Delay Line

A bi-directional gated delay line performs the same task as up-down counter does, but the key difference between them is that BD-GDL can do that withholding load capacitor residual voltage V_c. This is essential to noise-shaping when BD-GDL is used as an integrator. If the load of a BD-GDC is another identical BD-GDC whose threshold voltage is $V_{T,\,GDL} = V_{DD} / 2$, the voltage range of the load capacitor is only $0 \sim V_{T,\,GDL}$, limiting the number of T_{in} [j] pulses that can be summed up. Although one can use a large load capacitor to handle a long train of positive or negative pulses, like what a charge pump does, in order to quantify the voltage of the load capacitor so as to yield the output of the time integrator, a voltage-to-time converter is needed, contradicting our goal to perform time-mode integration in digital domain only. An alternative is to cascade multiple identical BD-GDCs to form a BD-GDL, as shown in Fig. 3.5. Load capacitance C_k is formed by device capacitances only such that no explicit capacitors are needed. When the voltage of the gated

delay stage exceeds $V_{T,\,GDL}$, the output of the driven gated delay stage will be toggled. The use of the gated delay line allows us to perform time accumulation over a large range set by the length of the delay line. The BD-GDL used in this work has 30 stages. In order to handle both positive and negative time variables encountered in time-mode ΔΣ modulators, the left-half-side nodes from node M in Fig. 3.5 are initialized to V_{DD} and those in the right-half side from node M are initialized to ground. It is important to note that the left-most gated delay cell is connected to V_{DD} while the right-most gated delay cell is grounded to ensure that ”1” always propagates rightwards when $T_{in} > 0$ and ”0” always propagates leftwards when $T_{in} < 0$.

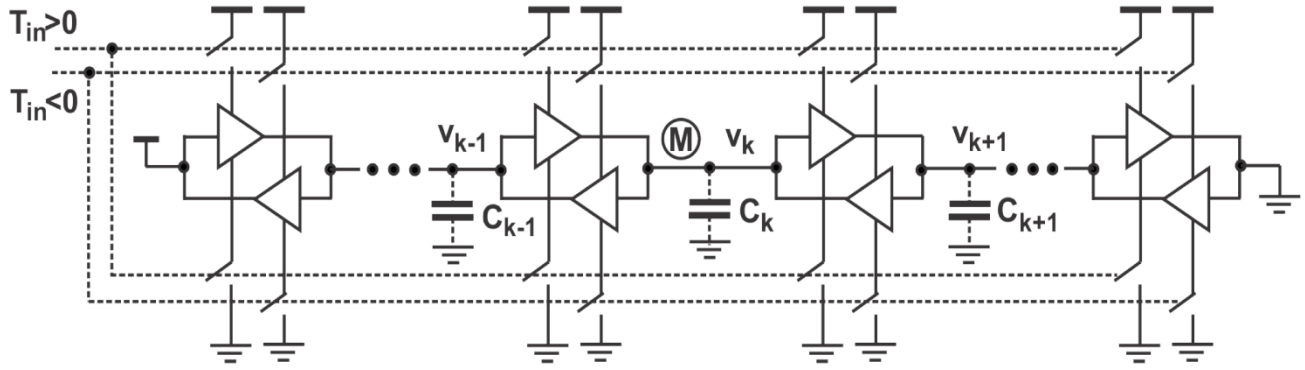

Fig. 3.5 Bi-directional gated delay line. When T_{in} is positive, the forward direction is enabled, and T_{in} is negative, the reverse direction is enabled.

3.4 Single-ended Bi-Directional Time Integrator

The single-ended bi-directional gated delay line (BD-GDL) can function as a time integrator if the time variable to be integrated is the gating signal. To demonstrate that, consider a 5-stage BD-GDL. As shown in Fig. 3.6, consider a train of 5 pulses, T_{in} [k] where k = 1, 2, …, 5 with T_{in} [1] = 1.2 τ, T_{in} [2] = 1.5 τ, T_{in} [3] = -1.1 τ, T_{in} [4] = 0.7 τ, and T_{in} [5] = -2.5 τ where τ is the per-stage delay. Assume $V_{1n} = V_{2n} = V_M = 1$ and $V_{1p} = V_{2p} = 0$ initially. Further assume if $T_{in} = \tau$, signal “1” will propagate through one delay stage, i.e., the averaged rate of change of the output voltage of

gated delay cells is $V_{T,\,GDL}$ / τ. With T_{in} [*1*] = 1.2 τ, logic-1 at node M propagates through one stage in the forward direction and charges C_{1p} to 0.2 $V_{T,\,GDL}$. Similarly, with T_{in} [*2*] = 1.5 τ, the signal continues to propagate through 2-stage and charges C_{2p} to 0.7 $V_{T,\,GDL}$. When T_{in} [*3*] = -1.1 τ

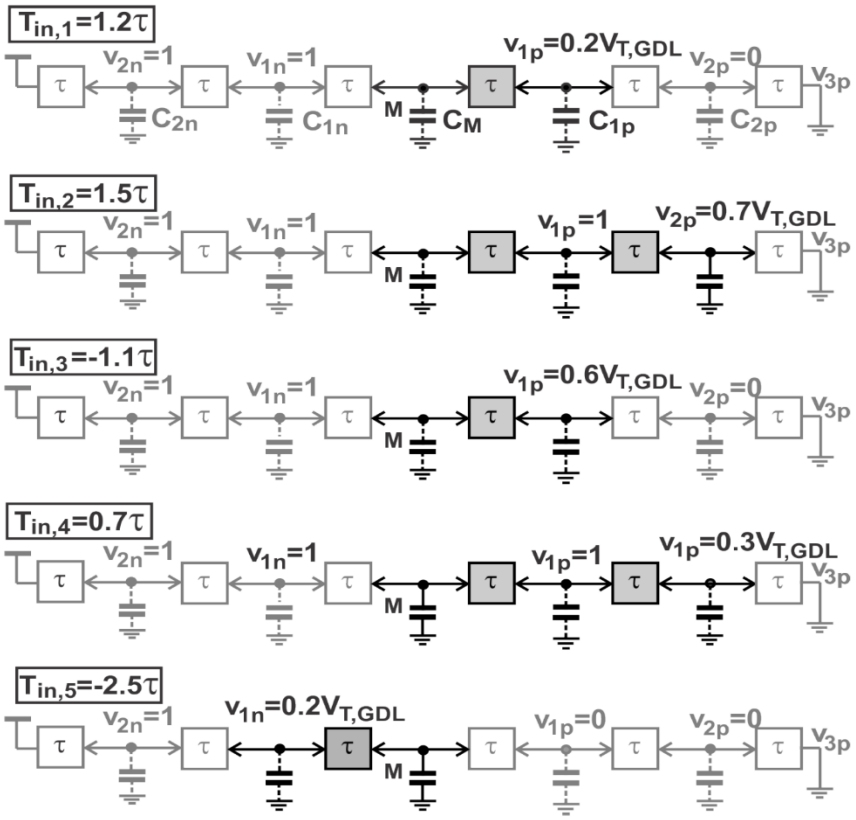

Fig. 3.6 Signal propagation in bi-directional gated delay line. The bold lines highlight the path that the signal propagates. Gating signals are not shown for brevity.

arrives, the forward gated delay line is disabled while the reverse gated delay line is activated. Since V_{3p} = 0, the charge of C_{2p} is discharged. The same for V_{1p}. It becomes evident that the bi-directional gated delay line performs the accumulation (integration) of T_{in} [*k*]. To digitize the result of the time integration, D-flip flops (DFFs) can be deployed at the output of each gated delay stage. The output of the time integrator is a thermometer code in the form 1...10...0 with the left-most 0 specifying the vanishing location of the node M. It becomes apparent that the maximum quantization error of the time integrator, denoted by Δ_{max}, is τ. The actual quantization error,

denoted by Δ_k, is preserved in the form of the voltage of the load capacitor $V_{c,k}$ of the stage whose right-adjacent stage has an output of 1. Utilizing the relation between $V_{T,GDL}$ and τ, we arrive at $\Delta_k = \frac{V_{c,k}}{V_{T,GDL}}\tau$.

3.5 All-digital first order single-bit ΔΣ TDC with single-ended BD-GDL time integrator

In this section, we utilize the preceding time integrator to construct an all-digital first-order ΔΣ TDC with a single-bit time quantizer. To construct the time quantizer, we notice that the output of the bi-directional gated delay line time integrator is a thermometer code. If the output of the time integrator is larger than τ, V_{1p} will be set to 1, otherwise, it will be set to 0. Note that $\Sigma\, T_{in}$ smaller than τ cannot be detected. It, however, is preserved by the residual voltage of the load capacitor and can be further processed using a MASH architecture. This observation reveals that the output of the delay stage that is right-connected to node M provides the single bit quantization of the output of the integrator. The minimum quantization noise is per-stage delay. The addition/subtraction of feedback time T_{fb}, approximately $1.2T_{in} \sim 1.5\, T_{in}$, to/from T_{in} are performed using a single-bit digital-to-time converter (DTC) and a time adder shown in Fig. 3.7(A). The multiplexers are controlled by the output of the time quantizer D_{out}. If $D_{out} > 0$, meaning $\sum_{j=1} T_{err}[j] > 0$, T_{fb} is subtracted from T_{in} aiming at generating $T_{err}[j+1] < 0$. Otherwise, it is added to T_{in} to generate $T_{err}[j+1] > 0$. The resultant T_{err} along with its polarity are connected to the $|\, T_{in}\, |$-block where the absolute value of T_{in} is obtained. Since T_{err} can be quite small, a time offset $T_{off} =$ 200 ps is added such that the duration of the gating signal exceeds per-stage delay. The polarity of T_{err} is determined using a DFF whose output is 1 if $T_{err} > 0$ and 0 otherwise, and determines the direction of propagation. Also, the deployment of the AND2 gate ensures that integration is carried out only during IN1 = 1. The de-multiplexer, controlled by "Sign" signal, following to the AND2

gate determines the right-propagation signal and left-propagation signal. The edge aligners, as shown in Fig. 3.7(B), ensure that the right-propagation signal RS and $\overline{RS}$ are completely out of phase. The same also goes for the left-propagation signal LS and $\overline{LS}$.

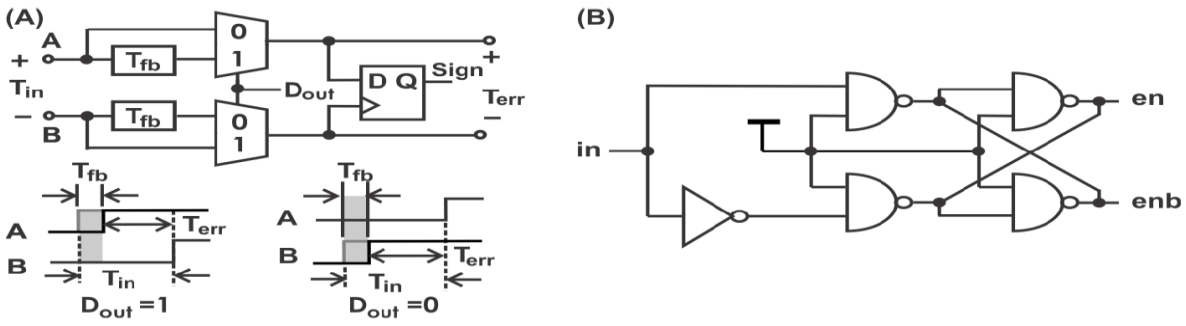

Fig. 3.7 (A) Digital-to-time converter [8], (B) Edge Alignment block [44].

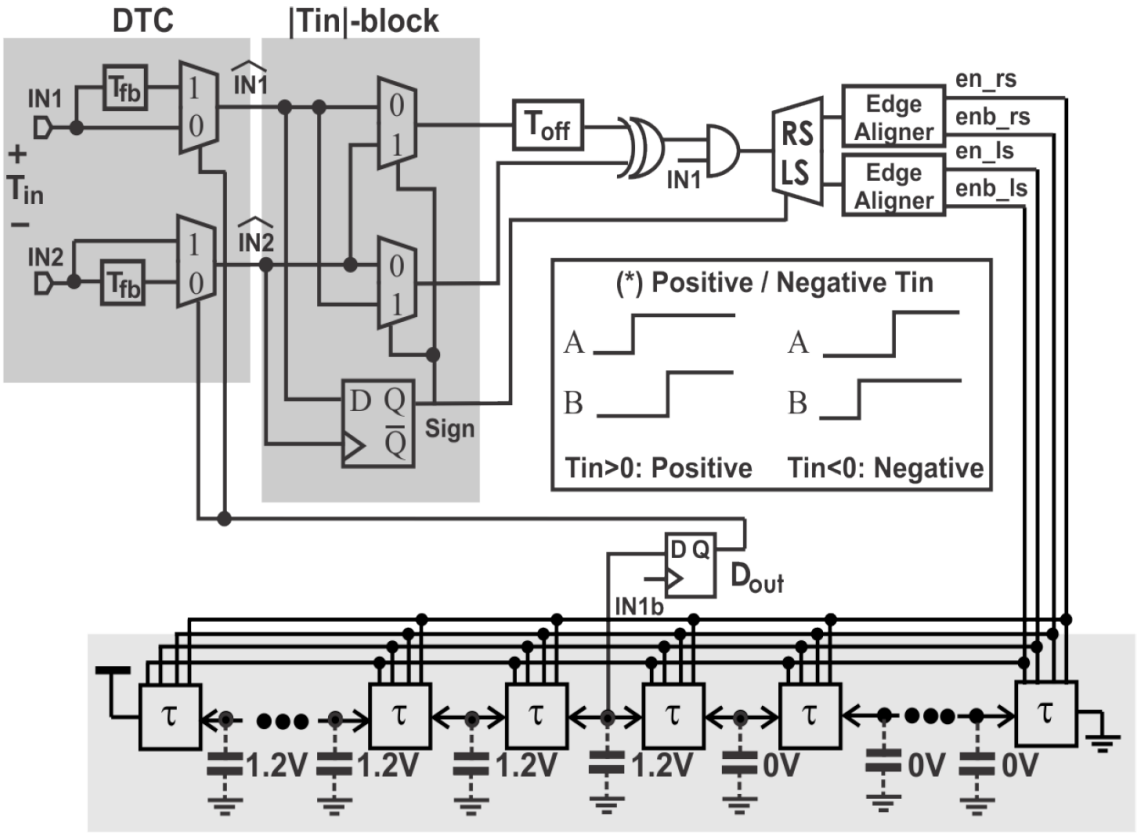

Fig. 3.8 All-digital first-order ΔΣ TDC with a single-bit time quantizer [43].

The right and left propagation signals generated by edge aligners are fed to single ended BD-GDL. The output of DFF connected to the node M of the BD-GDL provides a time-quantized feedback pulse. Furthermore, the input of the modulator is a sinusoidal time signal, generated using the differential VTC detailed earlier. The design specification and simulation results are attached in Chapter 5.

3.6 Summary

In this chapter, the function of all the key building blocks for all-digital ΔΣ TDC including differential VTC, bi-directional gated delay cell, bi-directional gated delay line, digital-to-time converter, $|T_{in}|$-block, edge aligner was briefly investigated. It can be concluded that the single-ended BD-GDL can function as a time integrator if the time variable to be integrated is the gating signal. Also, it is evident that single-ended VTC exhibits a high degree of nonlinearity as compared with differential VTC. The differential configuration of the VTC ensures that even-order harmonics are adequately suppressed. Furthermore, the output of DFF connected to the node M of the BD-GDL provides a time-quantized feedback pulse.

4. Design Consideration

In this chapter, some issues critical to the performance of the TDC are examined.

4.1 Nonlinearity

The integration of T_{in} is obtained by means of the accumulation of the charge of the load capacitor and the logic state of the delay stages. If we neglect the variation of per-stage delay caused by process spread, BD-GDLs will be linear over different stages. The relation between T_{in} and residual voltage V_c, however, is nonlinear. To illustrate this, let T_{in} [j] be identical for j = 1, 2, 3, …. Consider the charging process of the load capacitor and neglect the drain source voltage V_{DS} of the gated PMOS transistor. Using the pinch-off condition, one can show that the charging PMOS transistor will operate in saturation if $0 \leq V_c \leq V_T$ and triode if $V_T \leq V_c \leq V_{T,\,GDL}$. In both cases, the relation between Tin and V_c is nonlinear, as shown in Fig. 4(a). This is because for $0 \leq V_c \leq V_T$, the charging current is (V_{DD} - V_c)-dependent while for $V_T \leq V_c \leq V_{T,\,GDL,}$ V_c rises with time exponentially with time constant R_pC where R_p is the channel resistance of the charging PMOS transistor.

4.2 Inner-stage mismatch

Gated delay cells in both forward and reverse directions should be identical such that if $\Sigma\ T_{in} = 0$, $\Sigma\ V_c = 0$ will follow, as illustrated in Fig. 4(b). Should a mismatch between forward and reverse gated delay cells exists, $\Sigma\ V_c \neq 0$ even though $\Sigma\ T_{in} = 0$. Similar to delay-line TDCs, per-stage delay mismatch in either forward or reverse directions gives rise to the nonlinear characteristics of the time integrator.

4.3 Inter-stage mismatch

The range of the time integrator is set by both per-stage delay and the number of the delay stages. Inter-stage mismatch deteriorates once the number of the delay stages is exceedingly large. In order for the time integrator to have a large range without employing a large number of delay stages, the per-stage delay can be gradually increased when moving away from the middle node of the delay line. This is particularly true for ΔΣ TDCs as $\Sigma\ T_{err}$ is zero ideally in the steady state, the per-stage delay of stages distance away from the middle node can be made large without affecting the performance of the modulator.

4.4 PVT effect

Per-stage delay of BD-GDLs is subject to the effect of PVT (process, voltage, and temperature). If one wants to have a precision value of the gain of the time integrator, BD-GDLs need to be calibrated. The per-stage delay of BD-GDL can be calibrated using a delay-locked loop approach similar to those used for calibrating delay-line TDCs.

4.5 Threshold voltage mismatch

The threshold voltage of gated delay cells, denoted by $V_{T,\ GDL}$, and that of the quantizing DFF, denoted by $V_{T,\ DFF}$, should be identical. If $V_{T,\ GDL} < V_{T,\ DFF}$, V_{1p} will be set to 1 before $D_{out} = 1$. Otherwise, D_{out} will be set to 1 before $V_{1p} = 1$. The variation of the time instant at which $D_{out} = 1$ affects when time error signal $T_{err} = T_{in} - T_{fb}$ is generated subsequently the transient behaviour of the TDC.

4.6 Charge injection and clock feed-through

The load capacitor is isolated from gated MOS switching transistors by either a PMOS or a NMOS transistor. The effect of charge injection from the switching transistors and clock feed-through from the gating signal T_{in} to the load capacitor is therefore minimized.

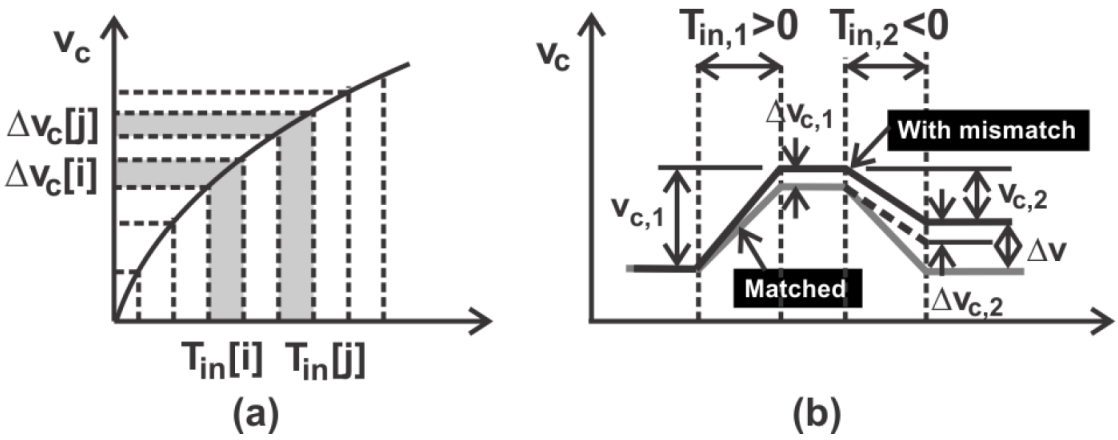

Fig. 4.1 (a) Residual voltage nonlinearity. (b) Inner-stage mismatch.

5. Design Specifications and Simulation Results

This chapter presents the design of time-mode all-digital ΔΣ modulator including all the building blocks used in the design. The all-digital first order single-bit ΔΣ TDC with single-ended BD-GDL time integrator is designed in an IBM 130 nm 1.2 V CMOS technology and analysed using Spectre ASP from Cadence Design Systems with BSIM4 device models. The BD-GDL has a total 30 stages with per-stage delay 60 ps. The outputs of the 15 stages on the left of node M are initialized to 1.2 V while and those on the right of node M to 0 V. A sinusoid time signal $T_{in}(t)$ of frequency 231kHz and amplitude 333 ps is fed to the TDC. $T_{in}(t)$ is generated from a 231kHz sinusoidal voltage signal of amplitude 100 mV fed to a clocked differential voltage-to-time converter with external load capacitors of 50 fF and clock frequency 33.33 MHz [42]. The minimum quantization noise is per-stage delay. The addition/subtraction of feedback time T_{fb}, is approximately $1.2T_{in}$ ~ $1.5\ T_{in}$, to/from $T_{in.}$ Fig 5.26 shows the transient response of the output of each block in ΔΣ TDC. The transient response shown in Fig. 5.27 depicts the change in the digital output "D_{out}" of ΔΣ TDC with respect to the analog input signal "V_{in}". Fig.5.28 shows the spectrum of the proposed ΔΣ TDC obtained using FFT analysis with 2048 samples and a Hanning window. First-order noise-shaping is evident. Furthermore, the large harmonics are present in the spectrum of the all-digital first-order single-bit ΔΣ TDC due to the nonlinear characteristics of the single-ended BD-GDL time integrator. The stage at which the output of the time integrator is quantized is stage 2 on right from the middle node. The ΔΣ TDC offers a SNR of 34.64 dB over frequency band 48.27~231 kHz with OSR of 68 and consumes 293.8 μW. In Table 5.1, the performance of recently published time-mode ΔΣ TDCs is compared with this work. In Table 5.2, breakdown of the power consumption of ΔΣ TDC.

Table 5.1 Performance Comparison of ΔΣ TDCs.

Ref.	Tech. (nm)	V_{DD} (V)	BW	OSR	Res. (ps)	PWR (mW)	Order
[4]	130	1.5	1 MHz	25	1	2.2-2.1	1st
[6]	180	1.8	400 kHz	348	8.7(*)	0.78	1st
[45]	130	1.2	100 kHz	250	11	1.7	3rd
[8]	32	1.0	100 kHz	50	4.4	0.25	1st
[43]	130	1.2	231 kHz	54	10.8	0.0046	1st
This	130	1.2	231 kHz	68	6.0595(*)	0.2938	1st

*This is the effective number of bits

Table 5.2

Breakdown of the power consumption of ΔΣ TDC with single-ended BD-GDL time integrator.

Block	Single-ended (μW)
DTC for quantization	137.6
Time integrator	45.52
Tin-Block	12.25
Differential VTC	85.65
Other blocks	12.78
Total	293.8

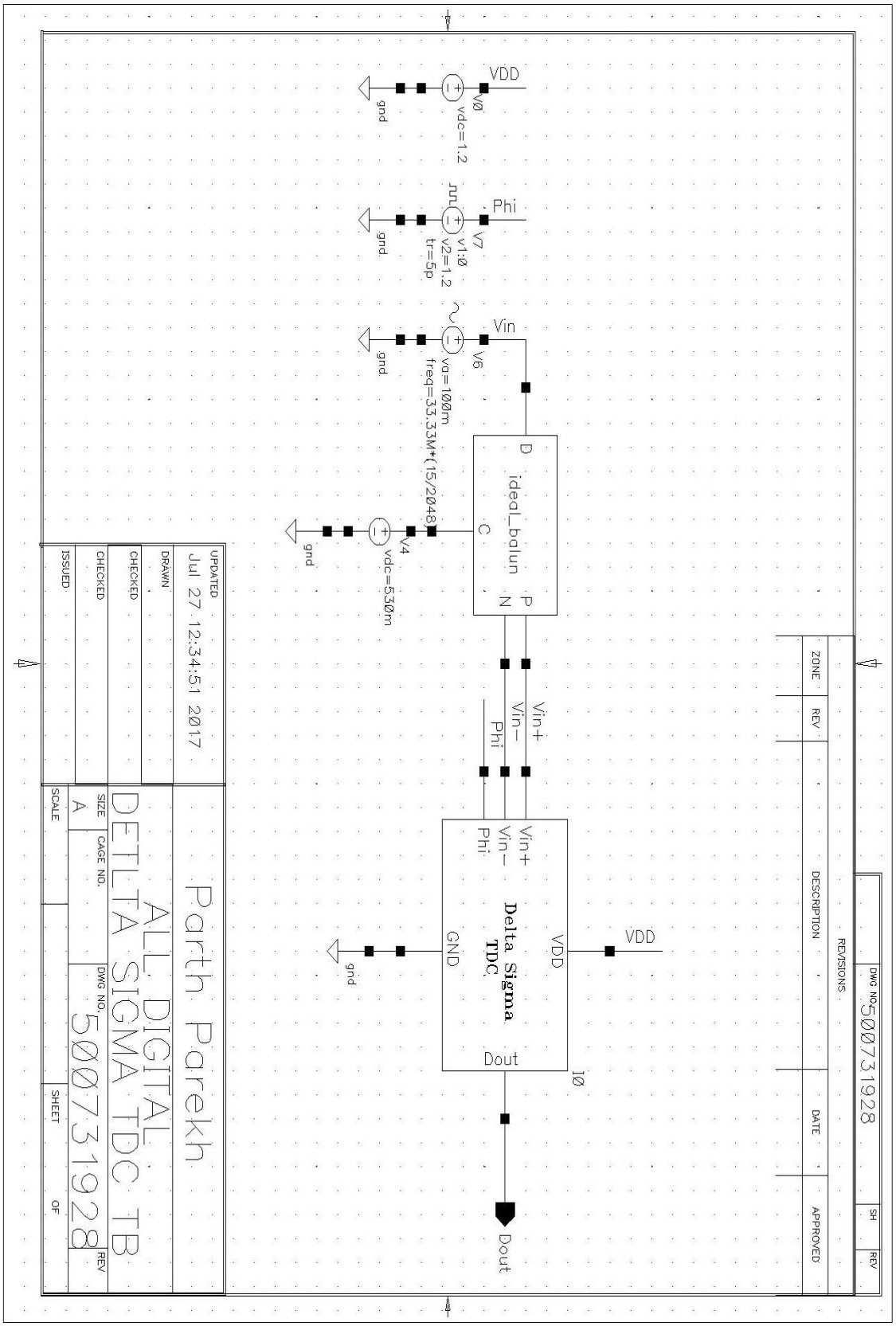

Fig. 5.1 All-Digital Delta-Sigma TDC test bench

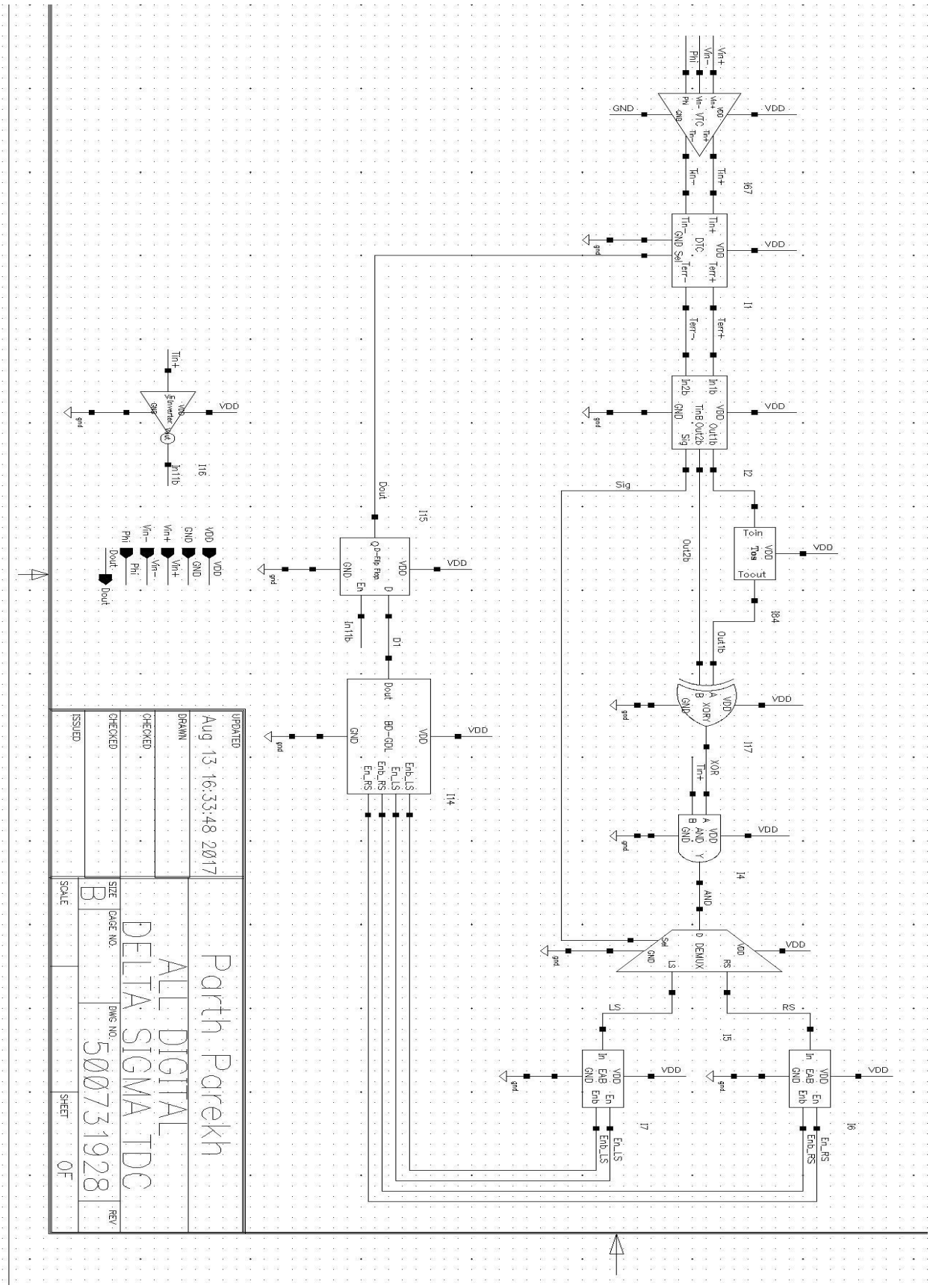

Fig. 5.2 All-Digital Delta-Sigma TDC

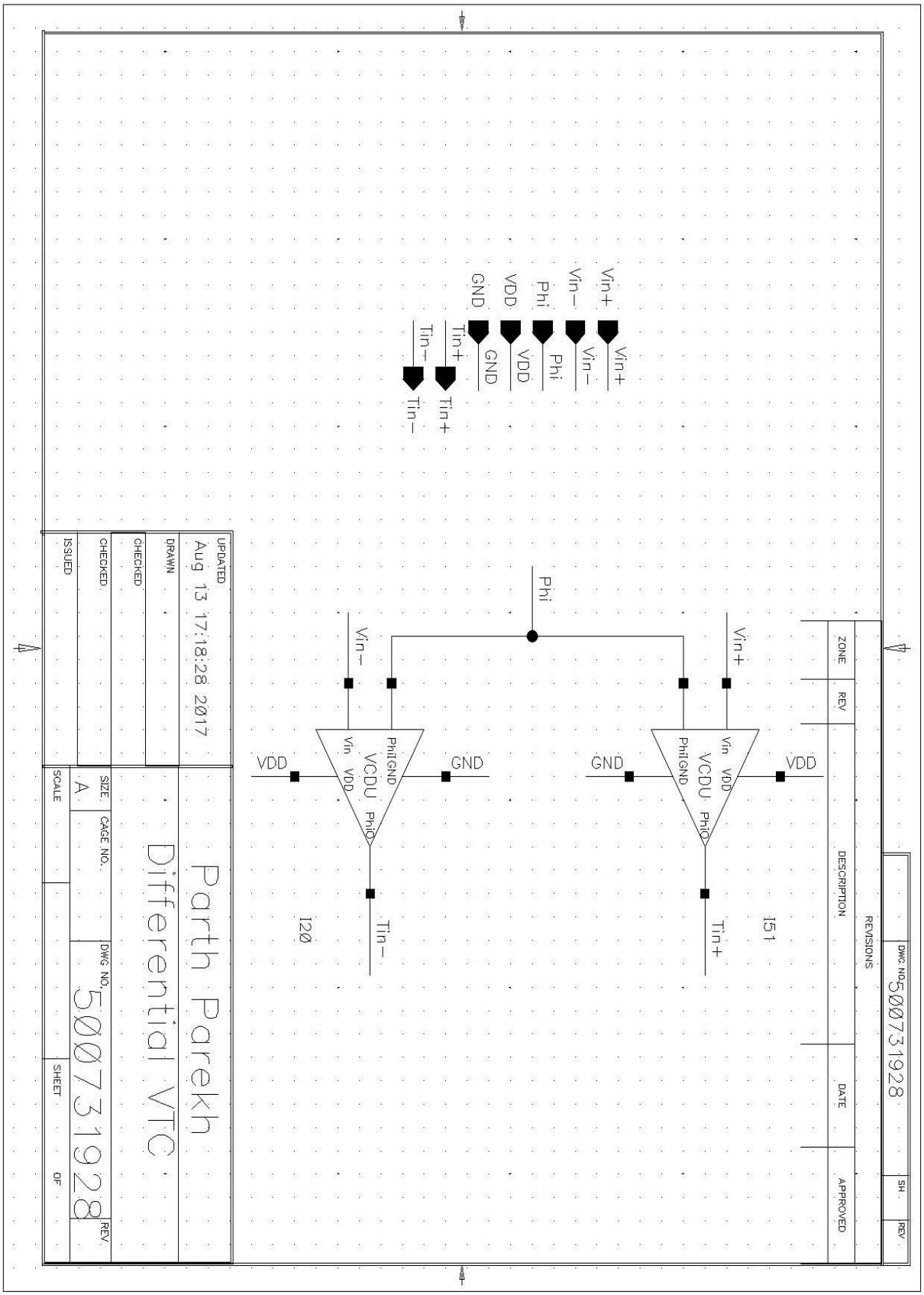

Fig. 5.3 Differential VTC

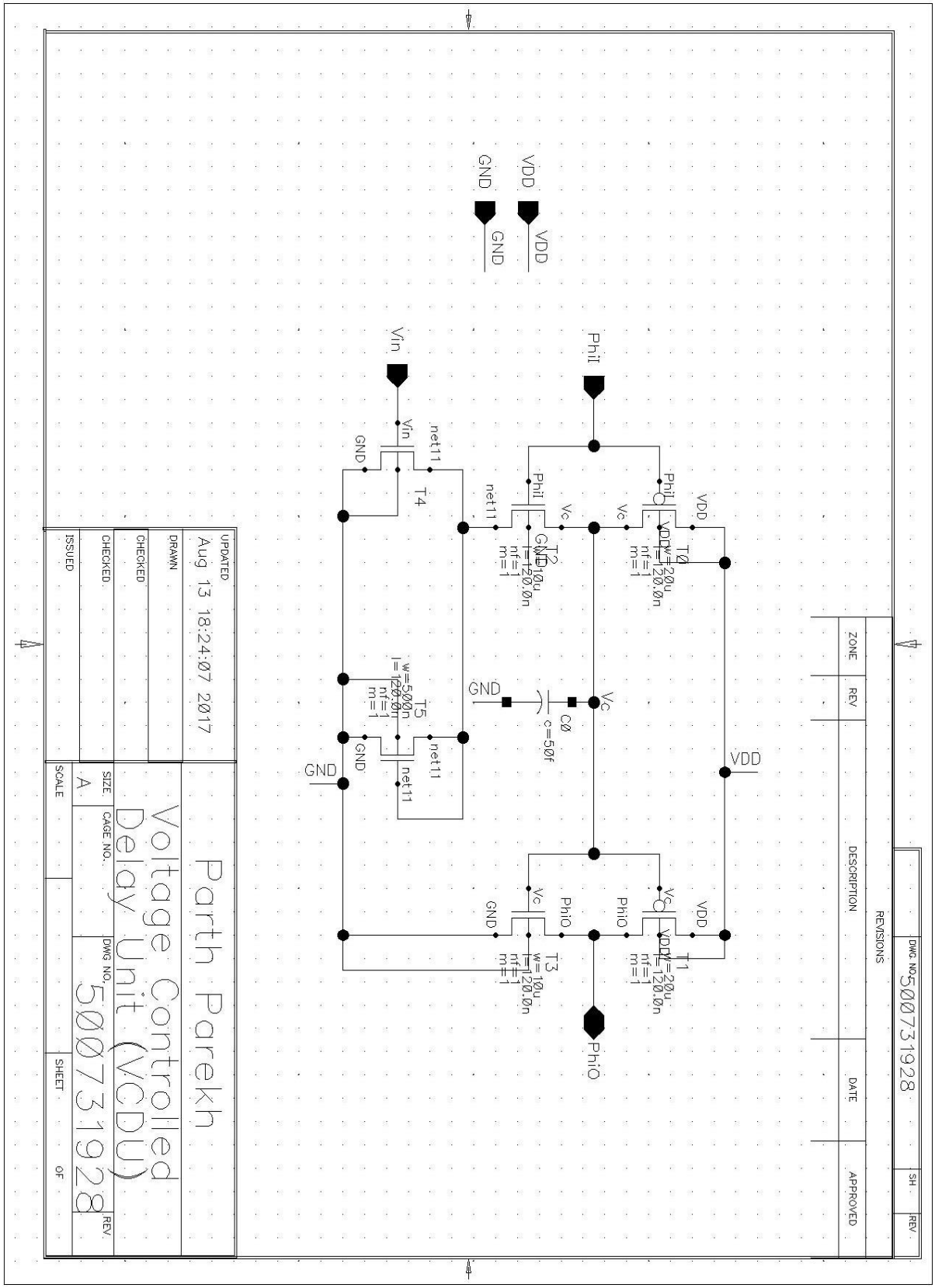

Fig. 5.4 Voltage Controlled Delay Unit (VCDU)

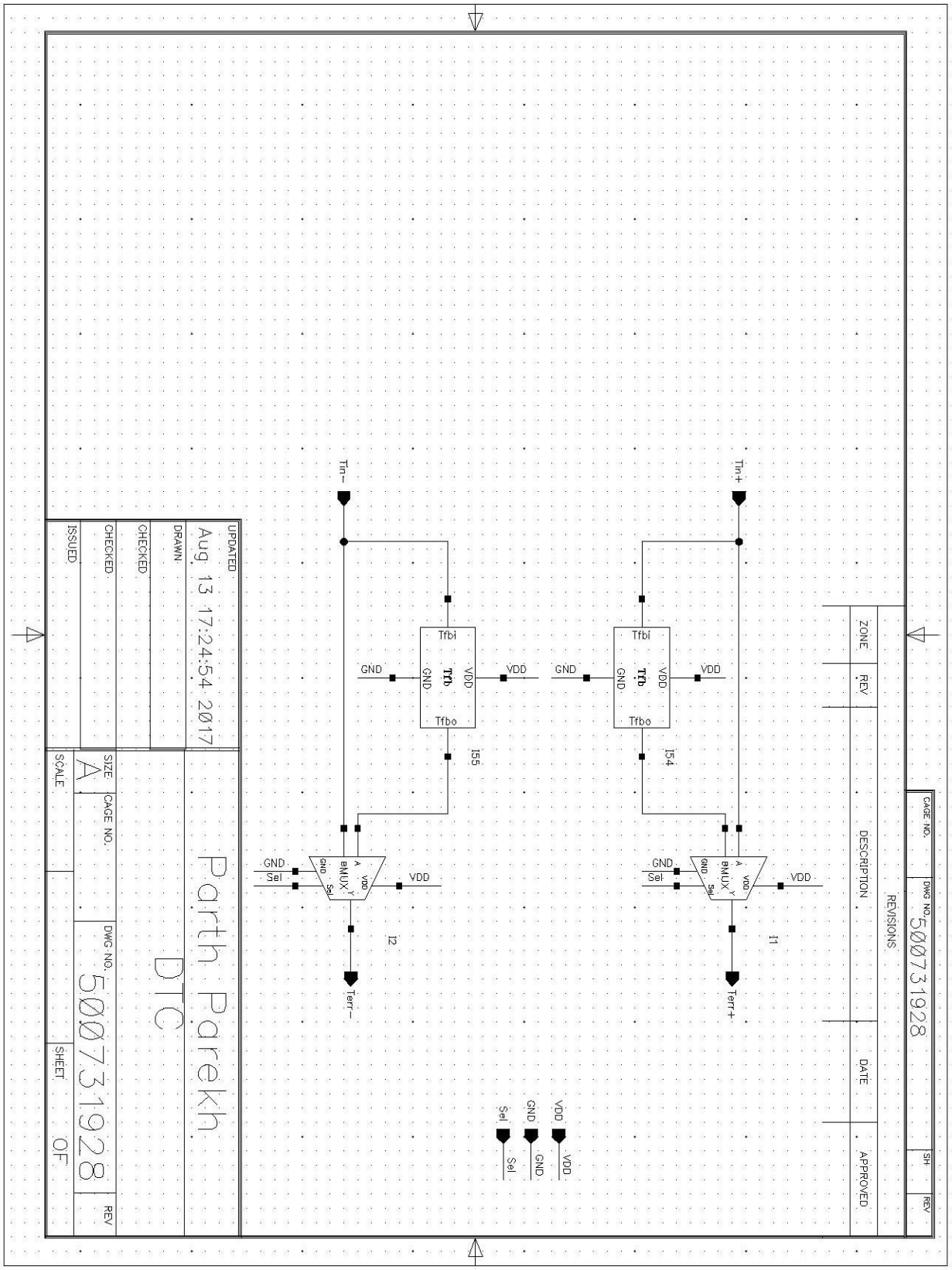

Fig. 5.5 Digital-to-time Converter (DTC)

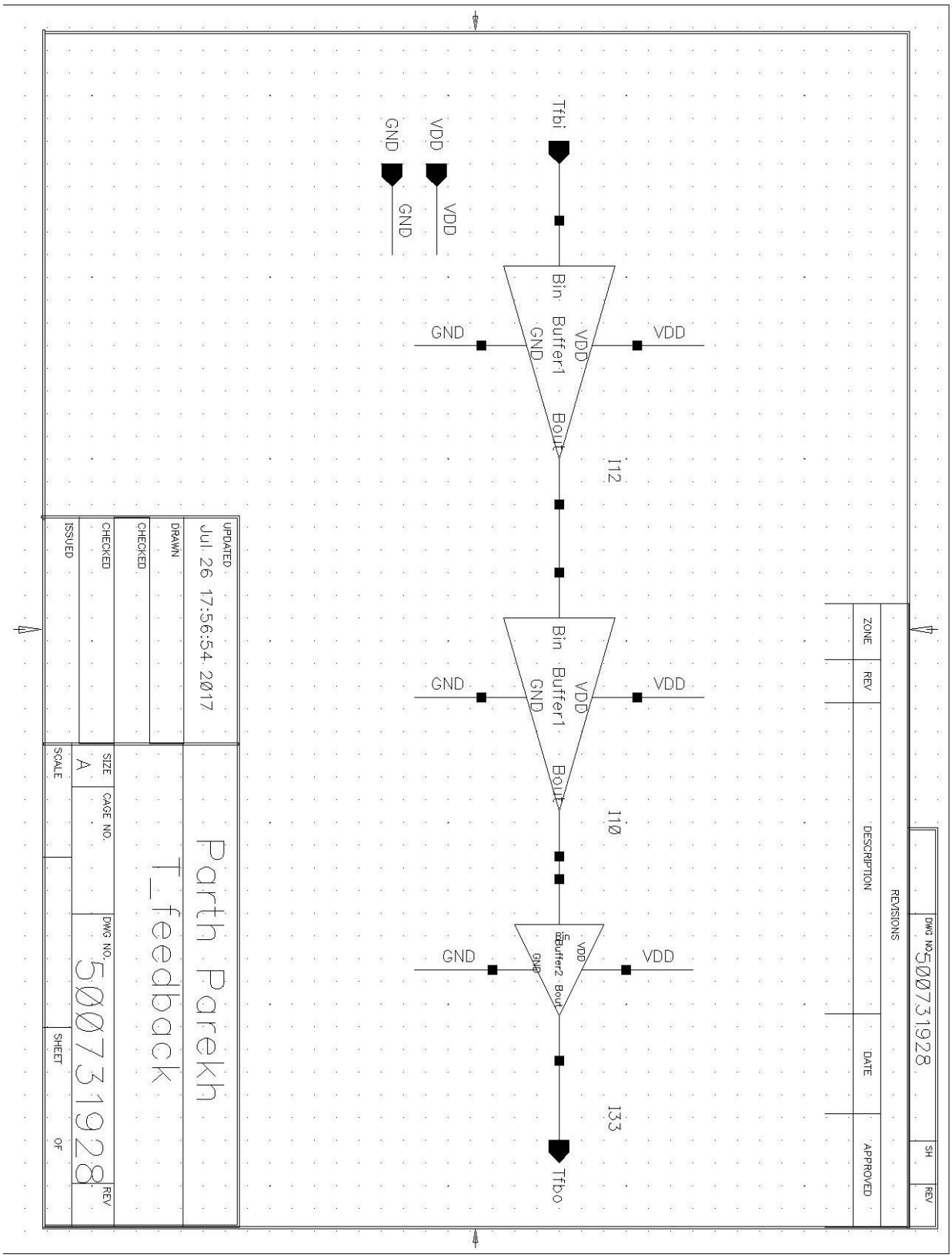

Fig. 5.6 T-Feedback

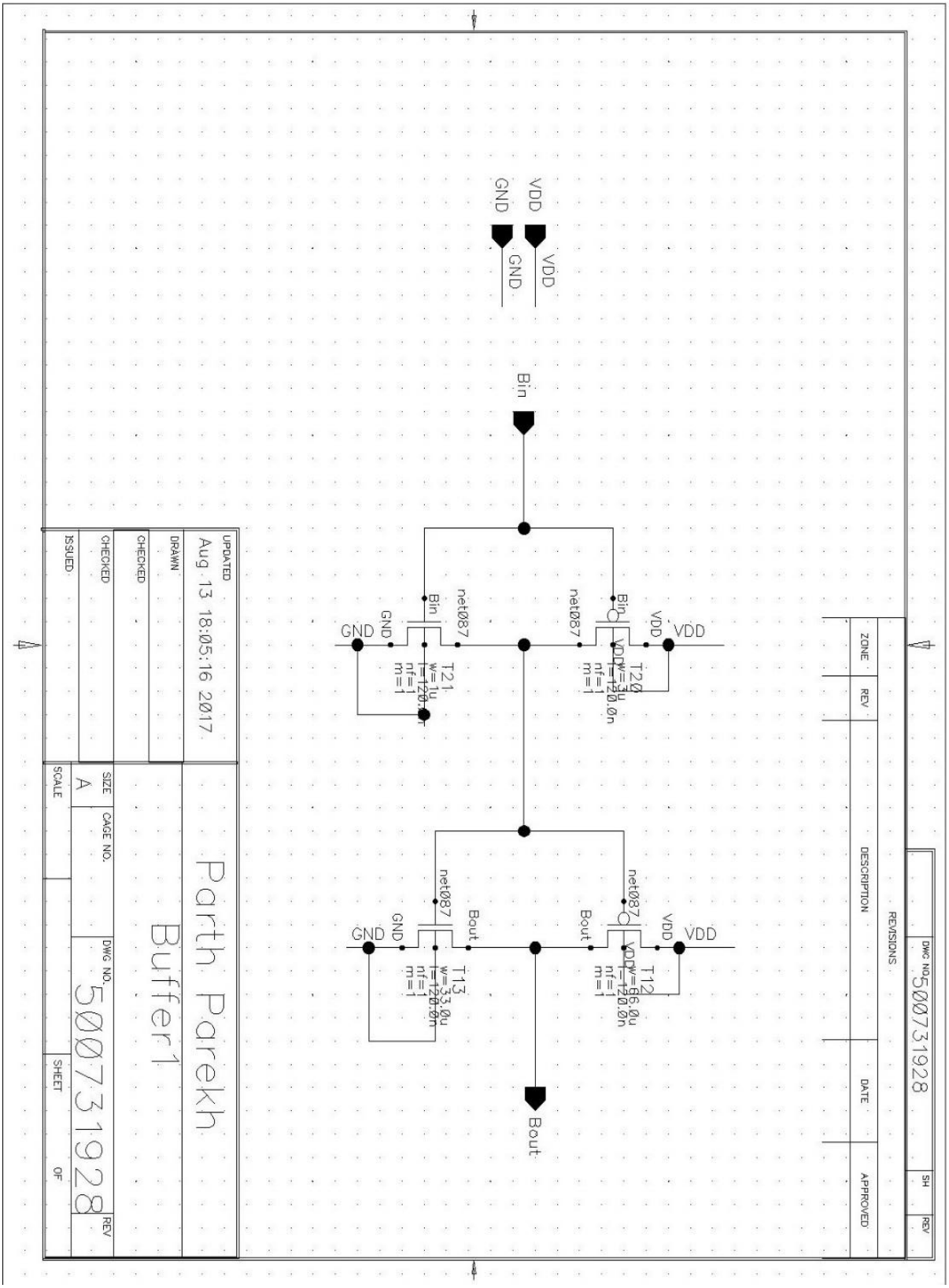

Fig. 5.7 Buffer1 for T-Feedback

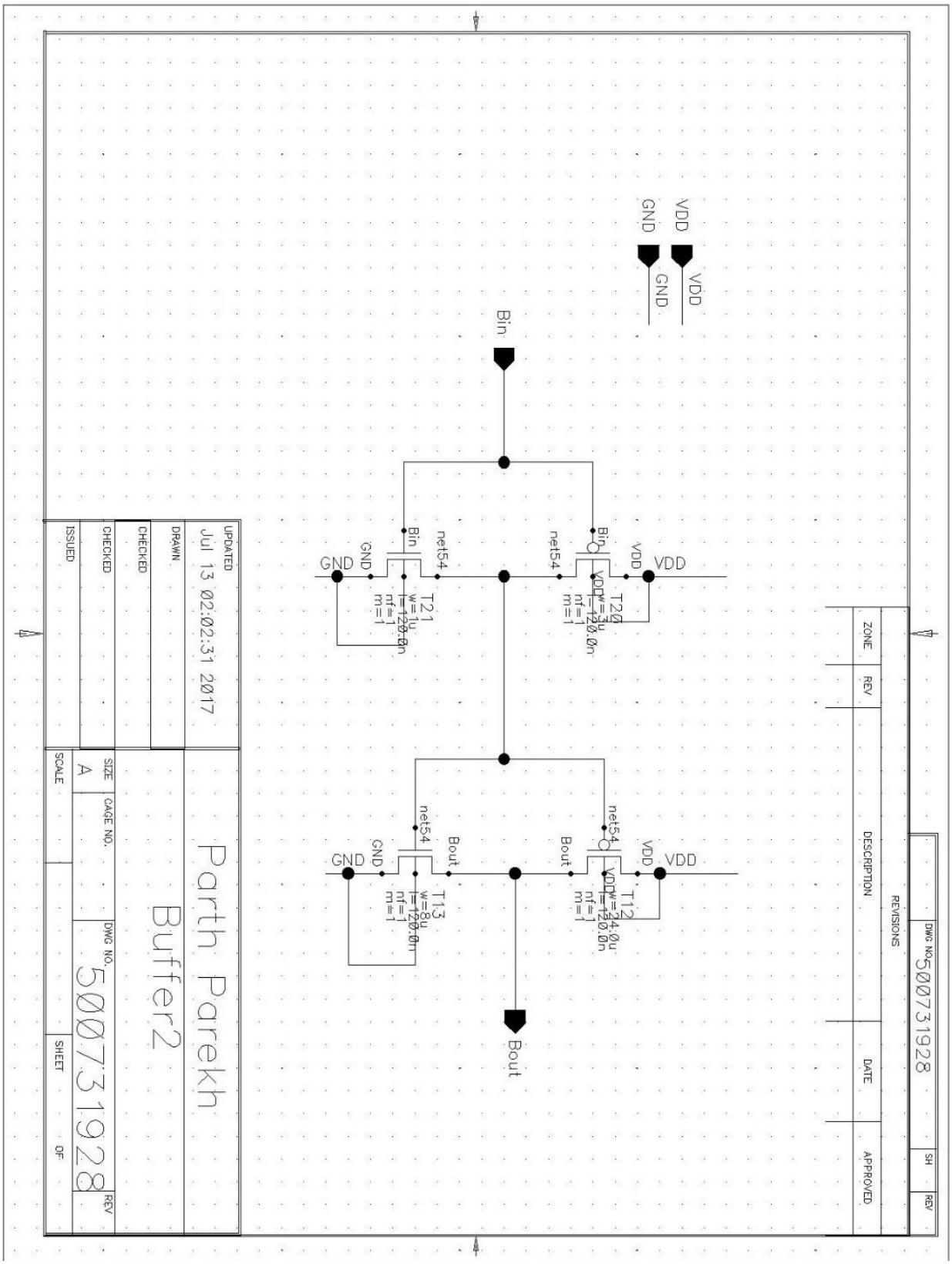

Fig. 5.8 Buffer2 for T-Feedback

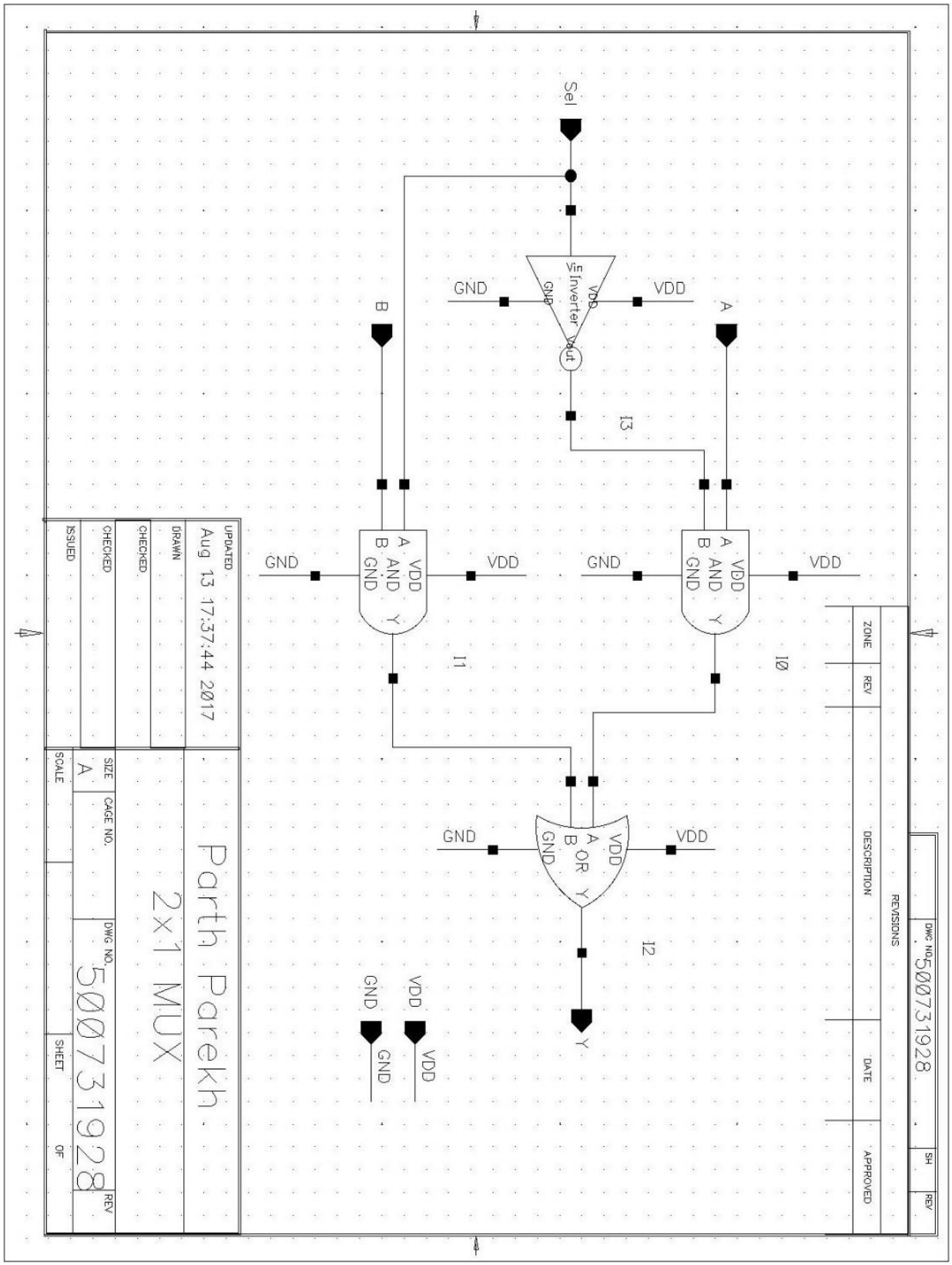

Fig. 5.9 2x1 MUX for DTC

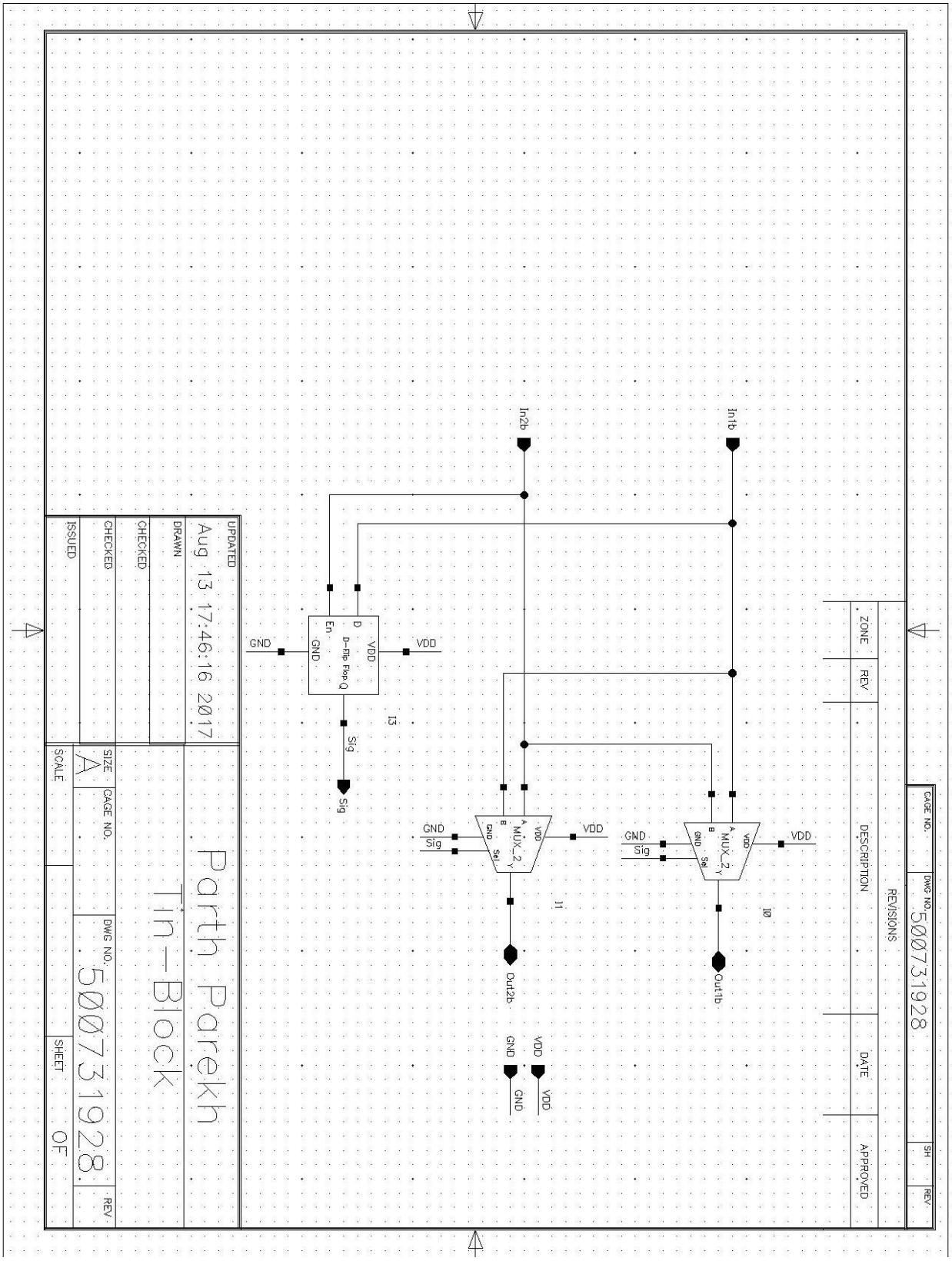

Fig. 5.10 Tin-Block

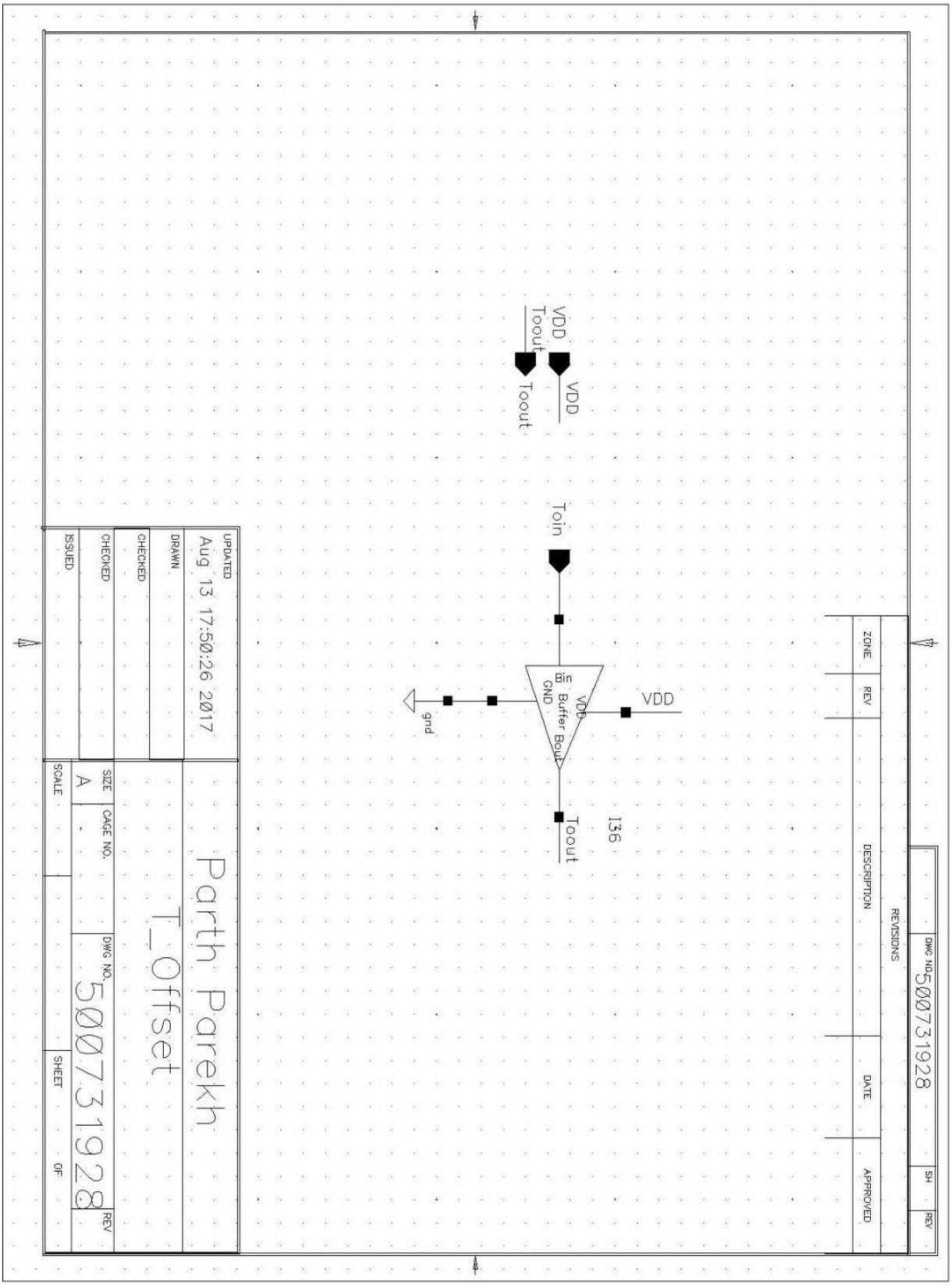

Fig. 5.11 T-offset

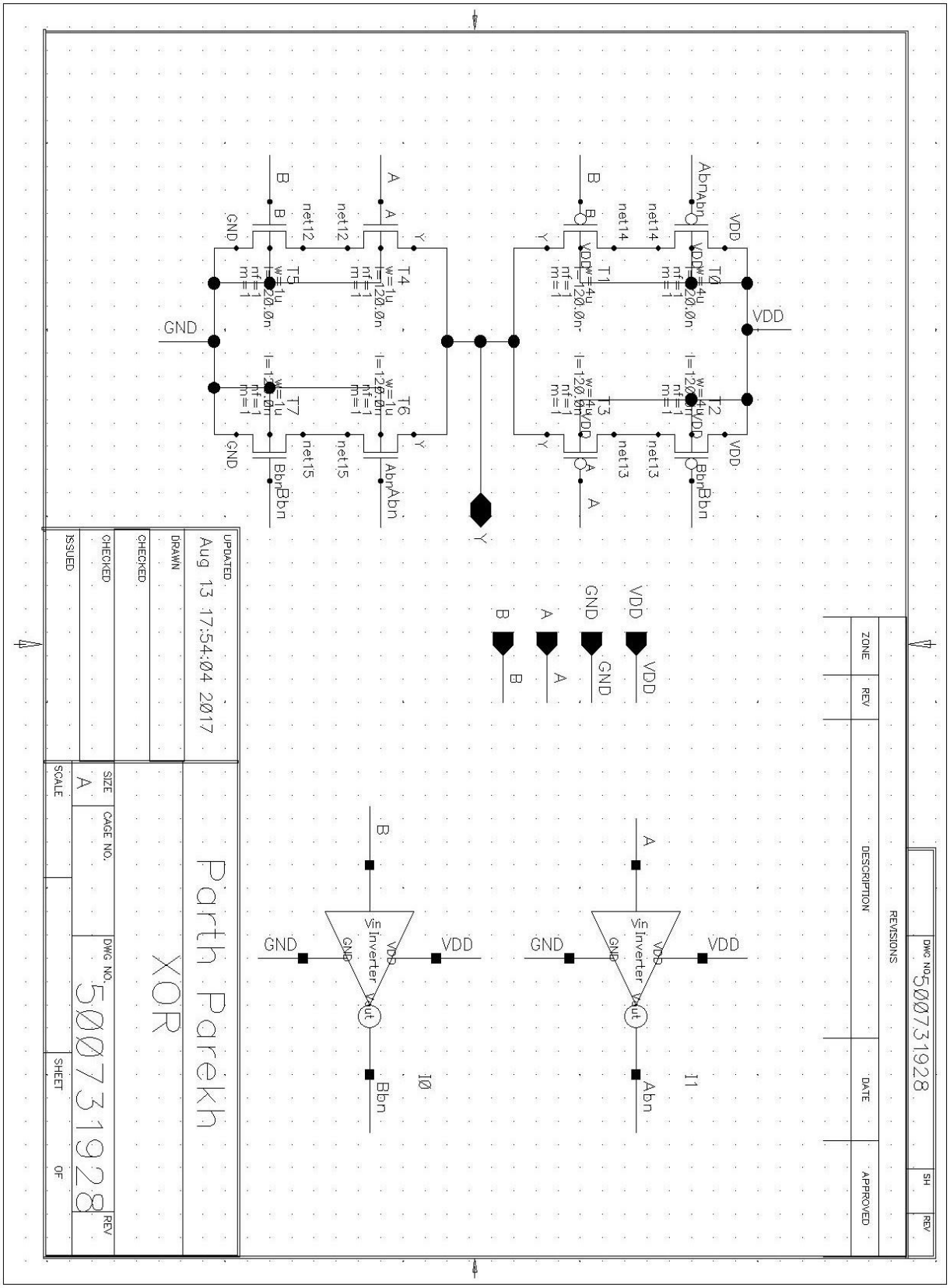

Fig. 5.12 XOR2 Gate

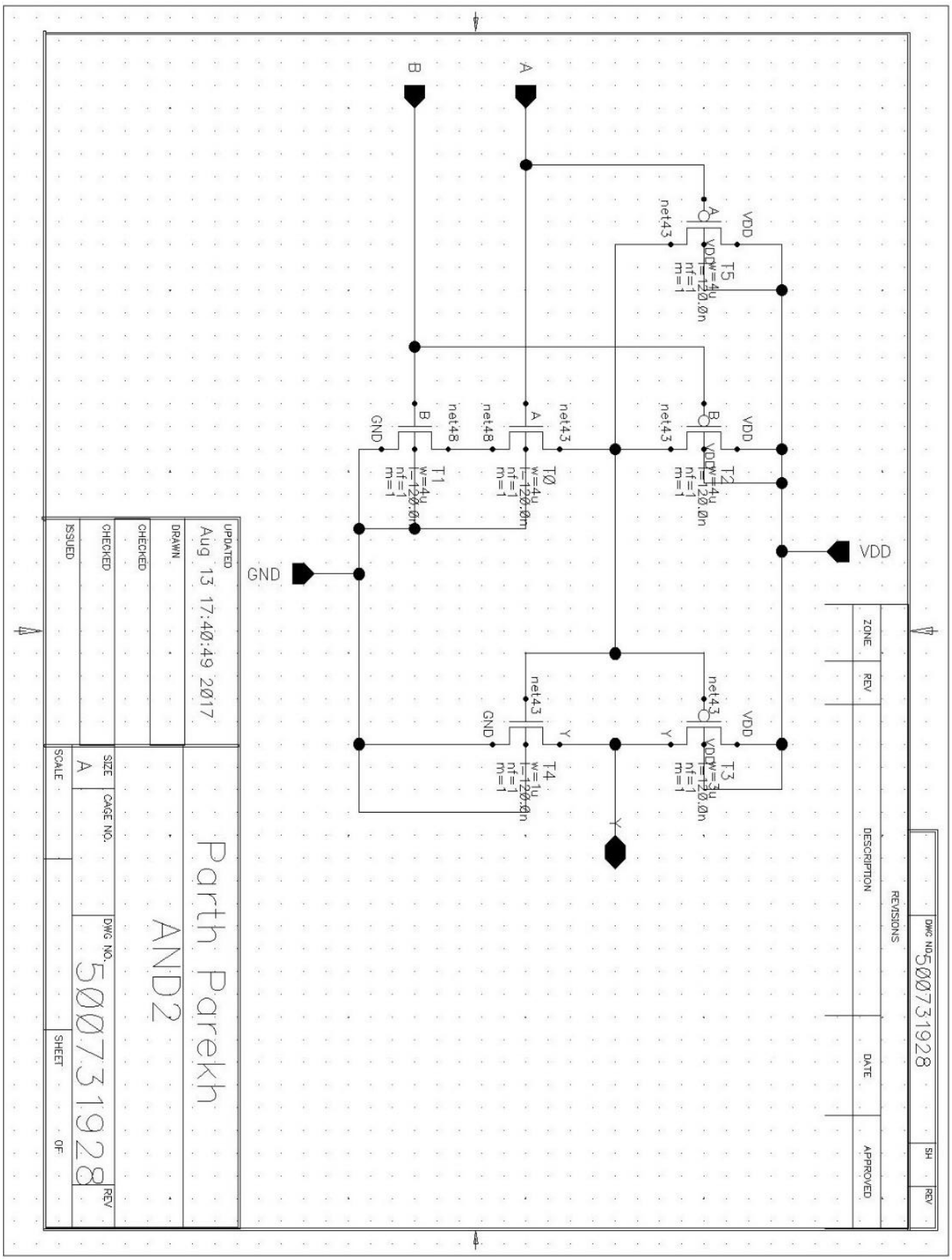

Fig. 5.13 AND2 Gate

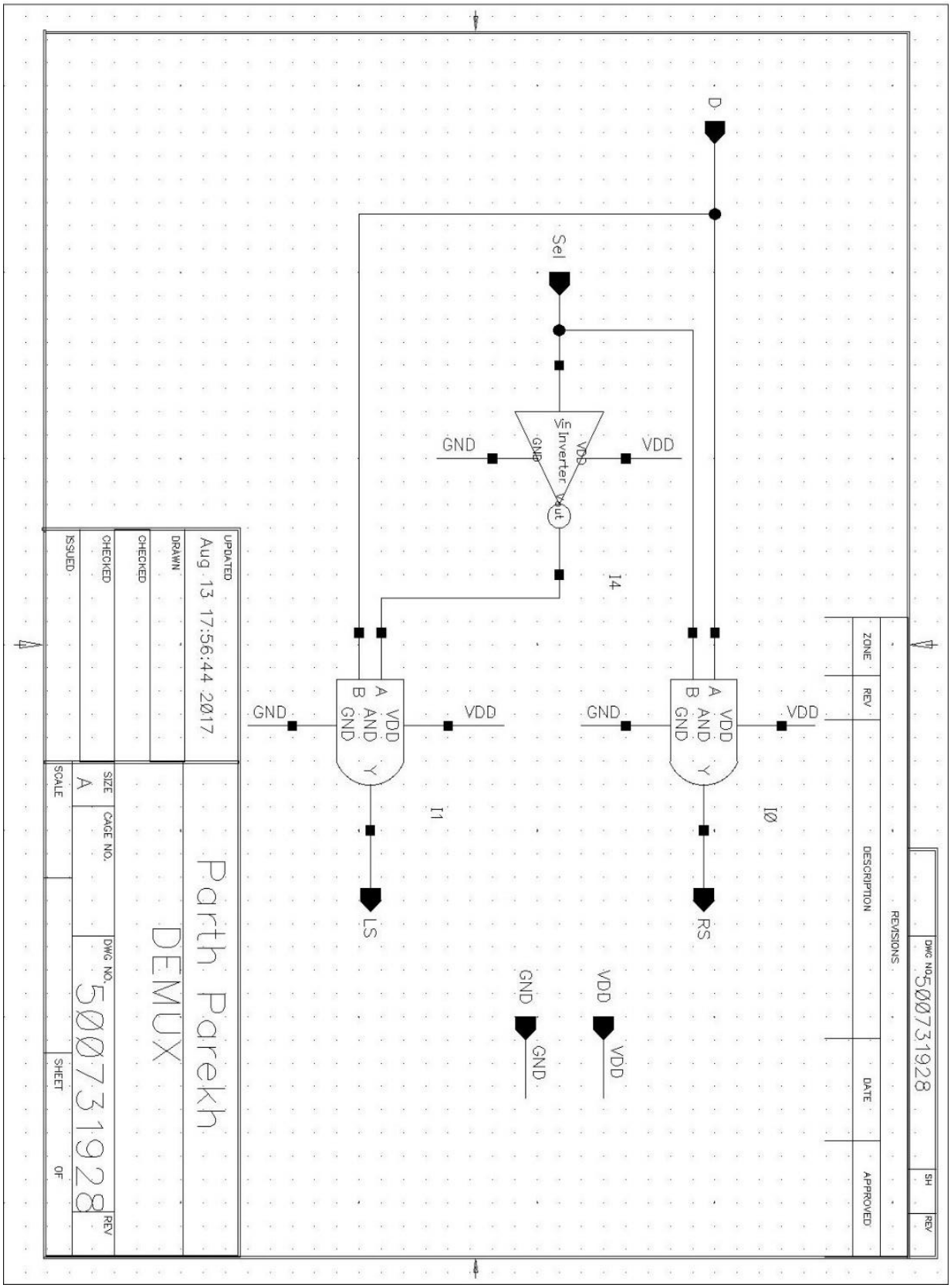

Fig. 5.14 DEMUX for RS and LS signals

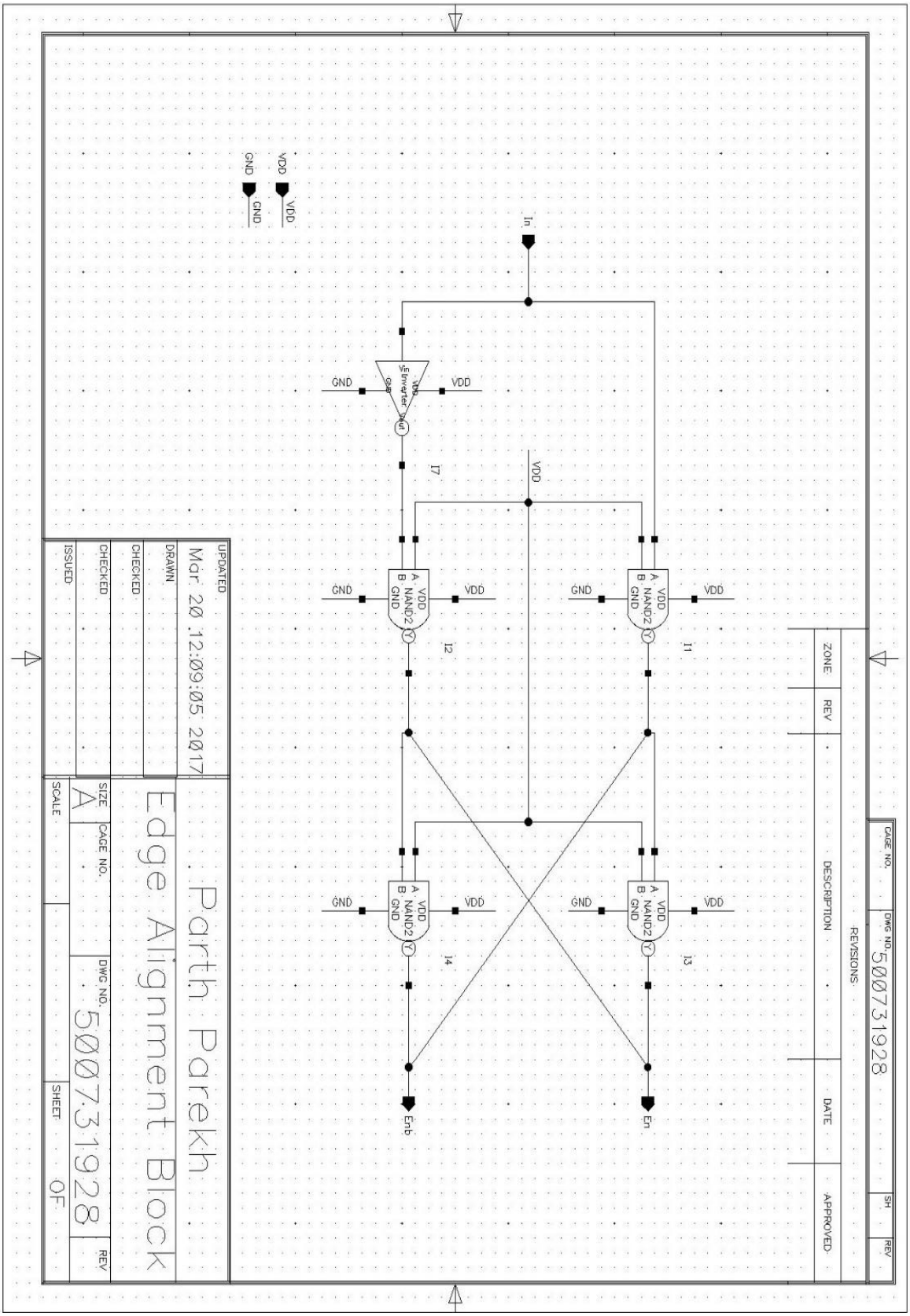

Fig. 5.15 Edge Alignment Block

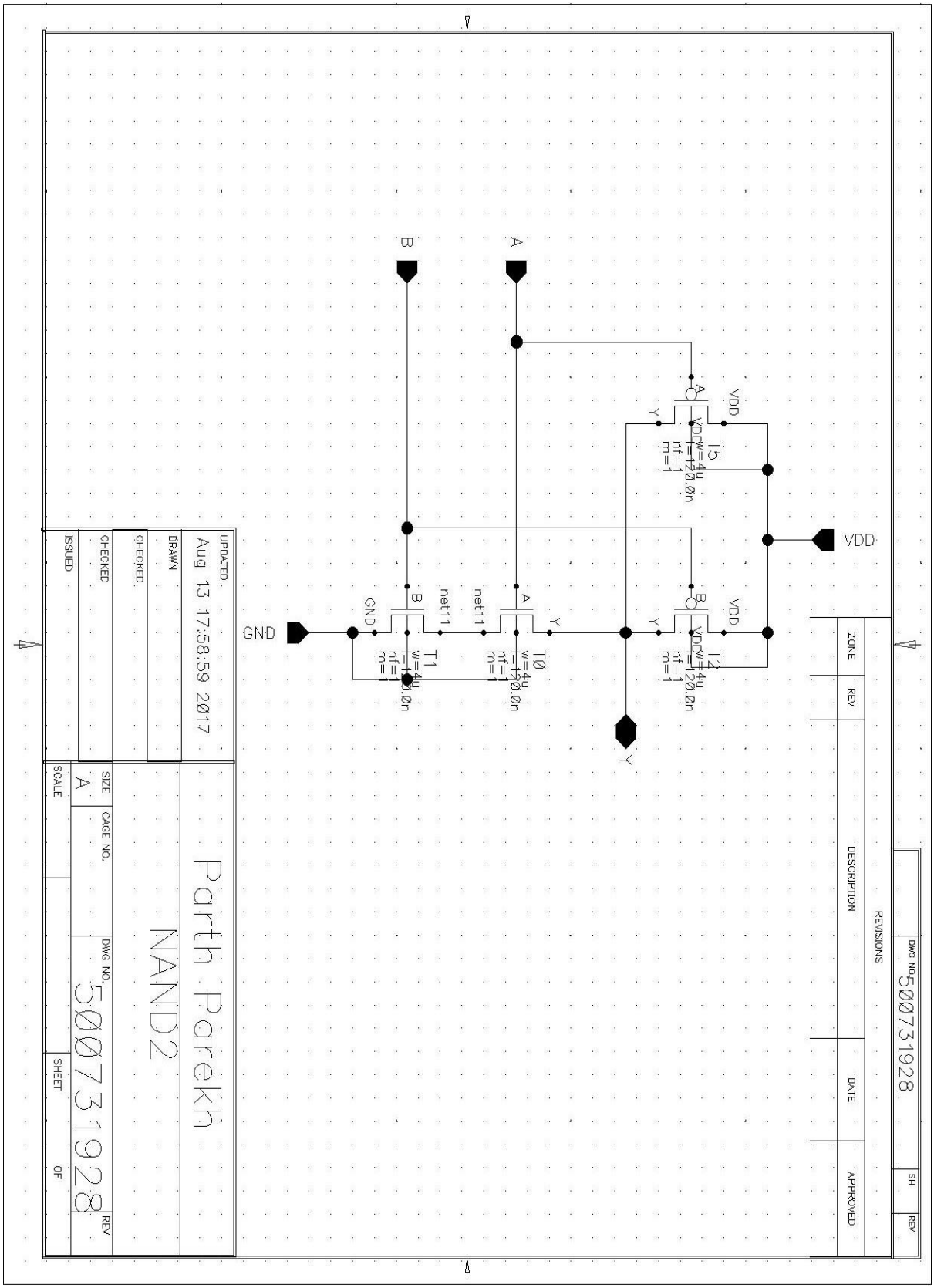

Fig. 5.16 NAND2 Gate

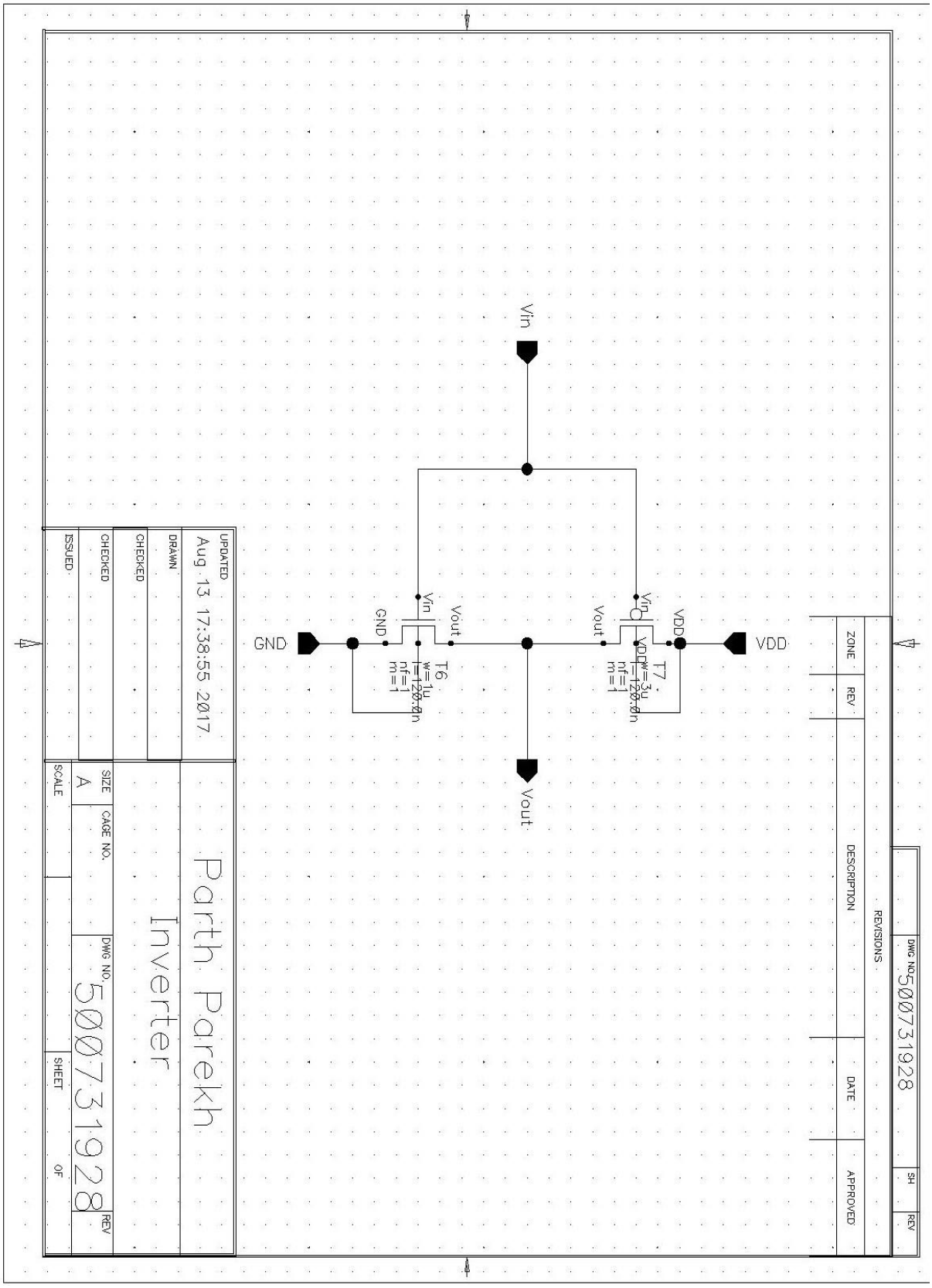

Fig. 5.17 Inverter

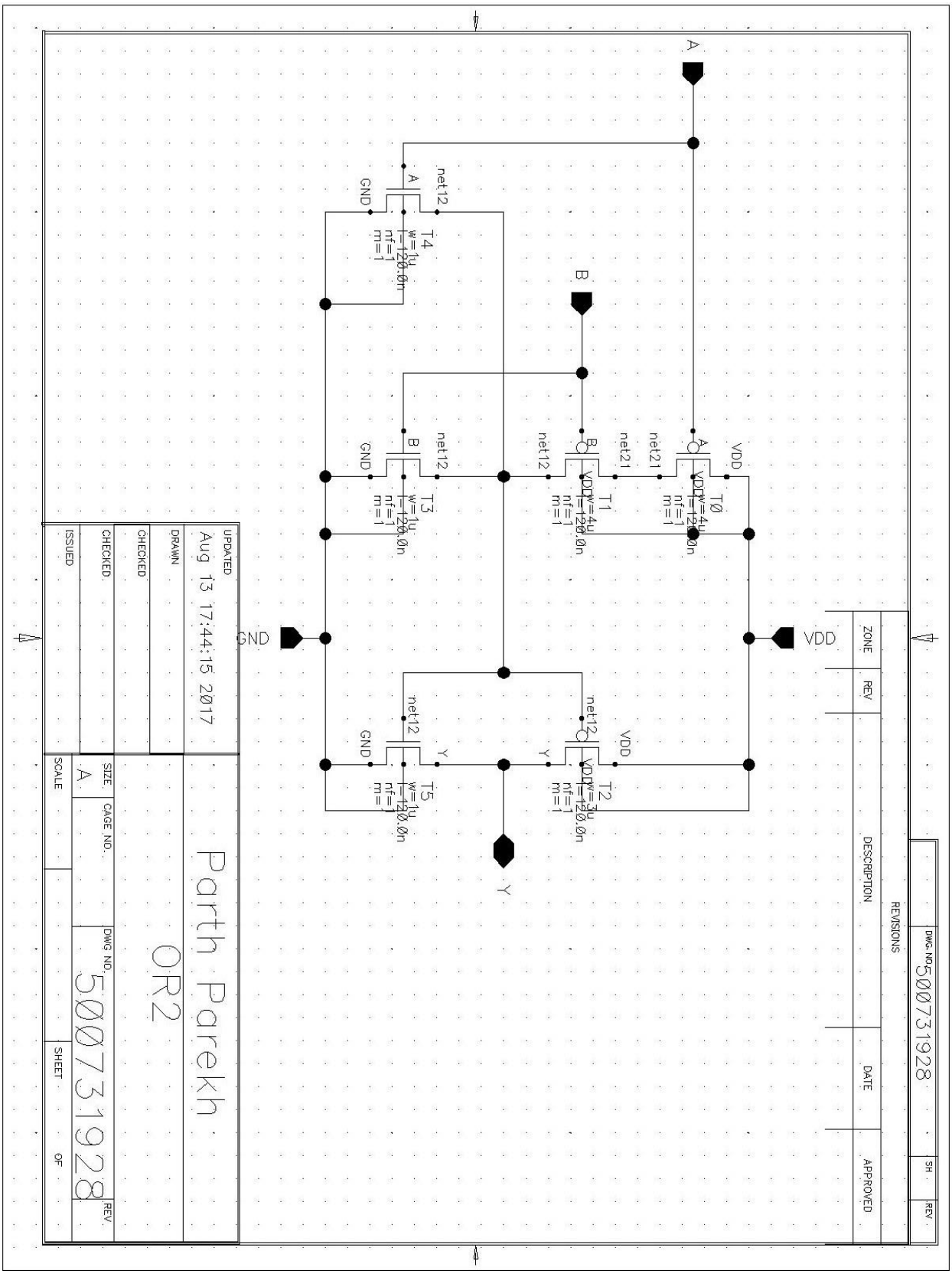

Fig. 5.18 OR2 Gate

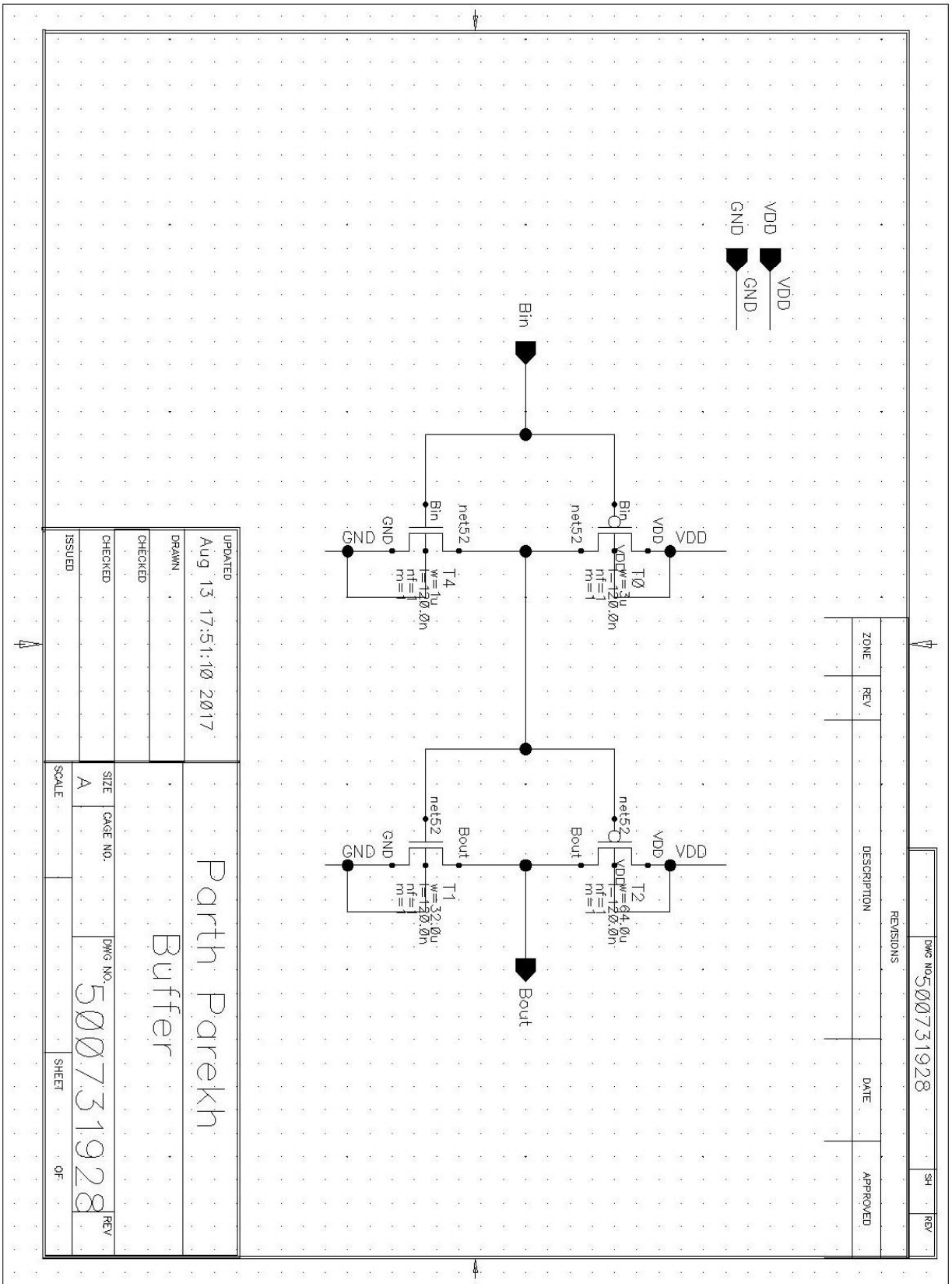

Fig. 5.19 Buffer for T-offset

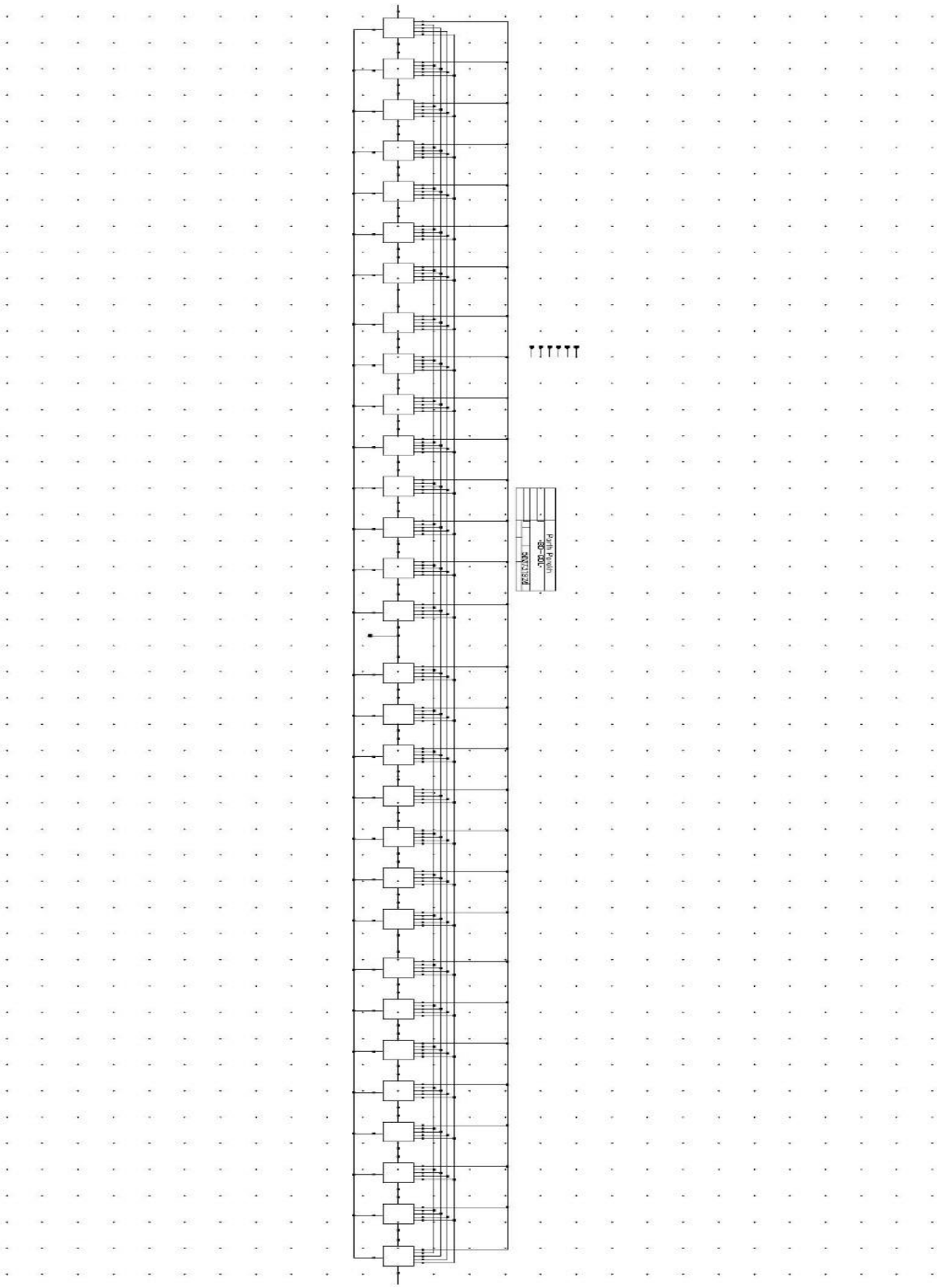

Fig. 5.20 30-stages Bi-Directional Gated Delay Line (BD-GDL)

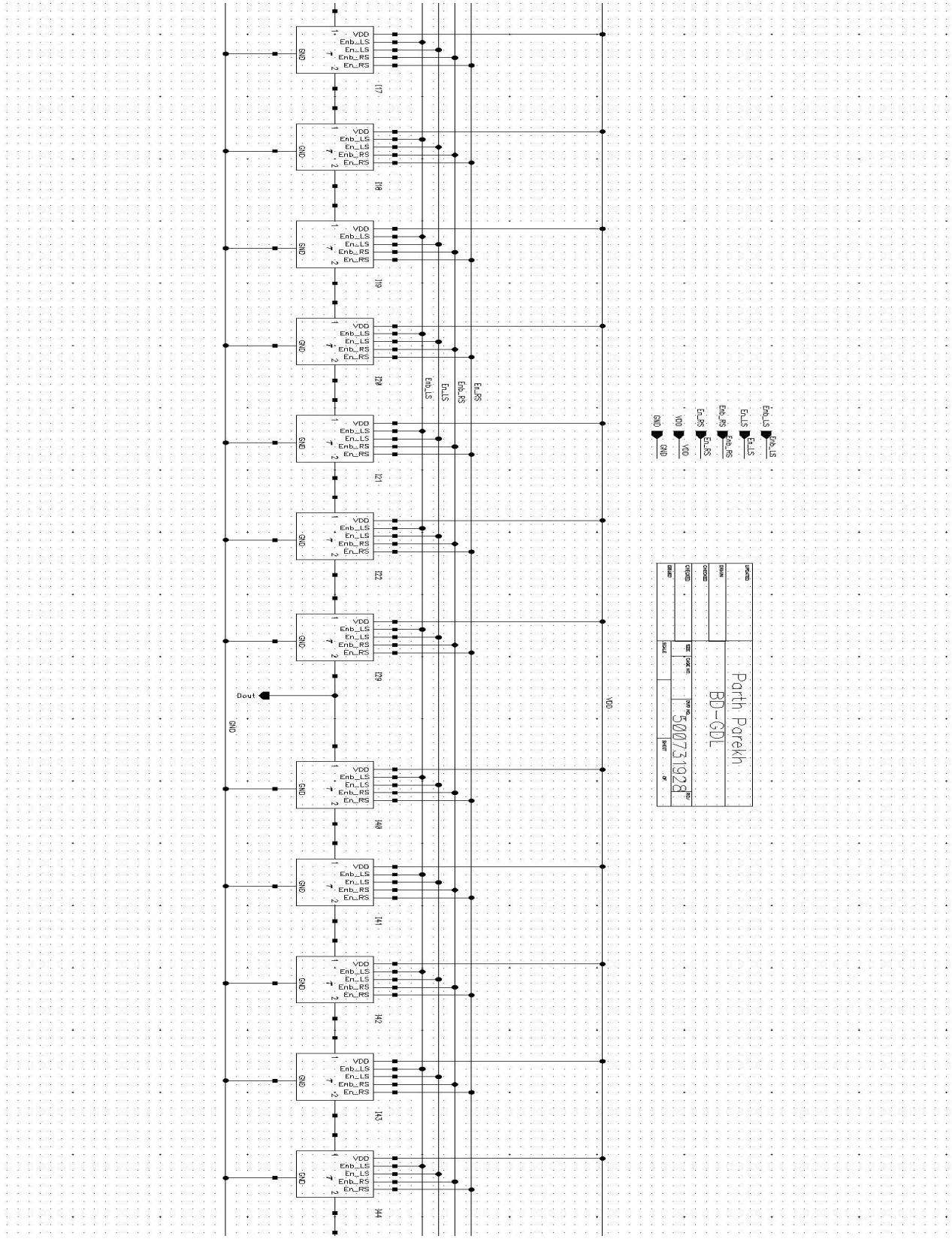

Fig. 5.21 Closer look of BD-GDL

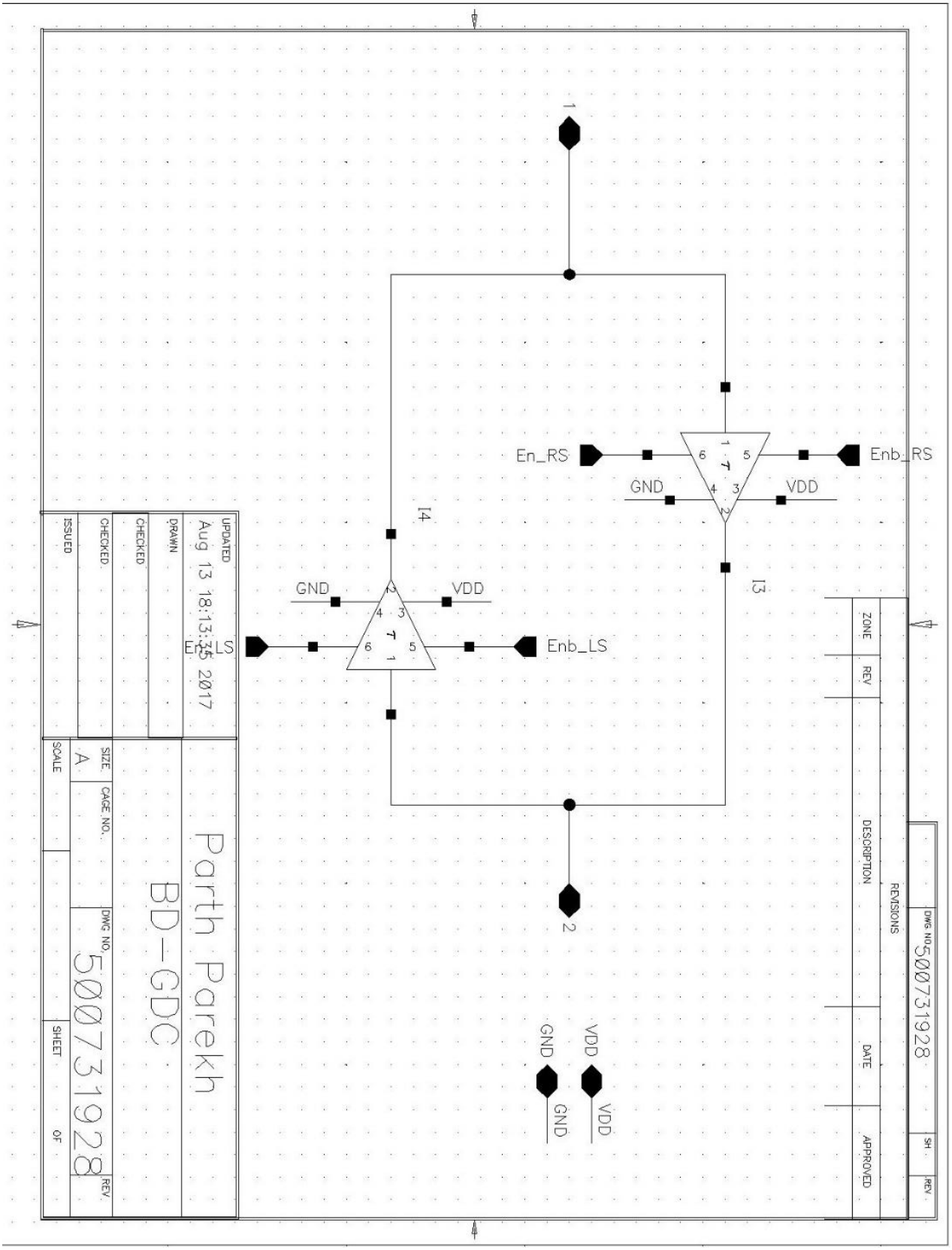

Fig. 5.22 Bi-Directional Gated Delay Cell (BD-GDC)

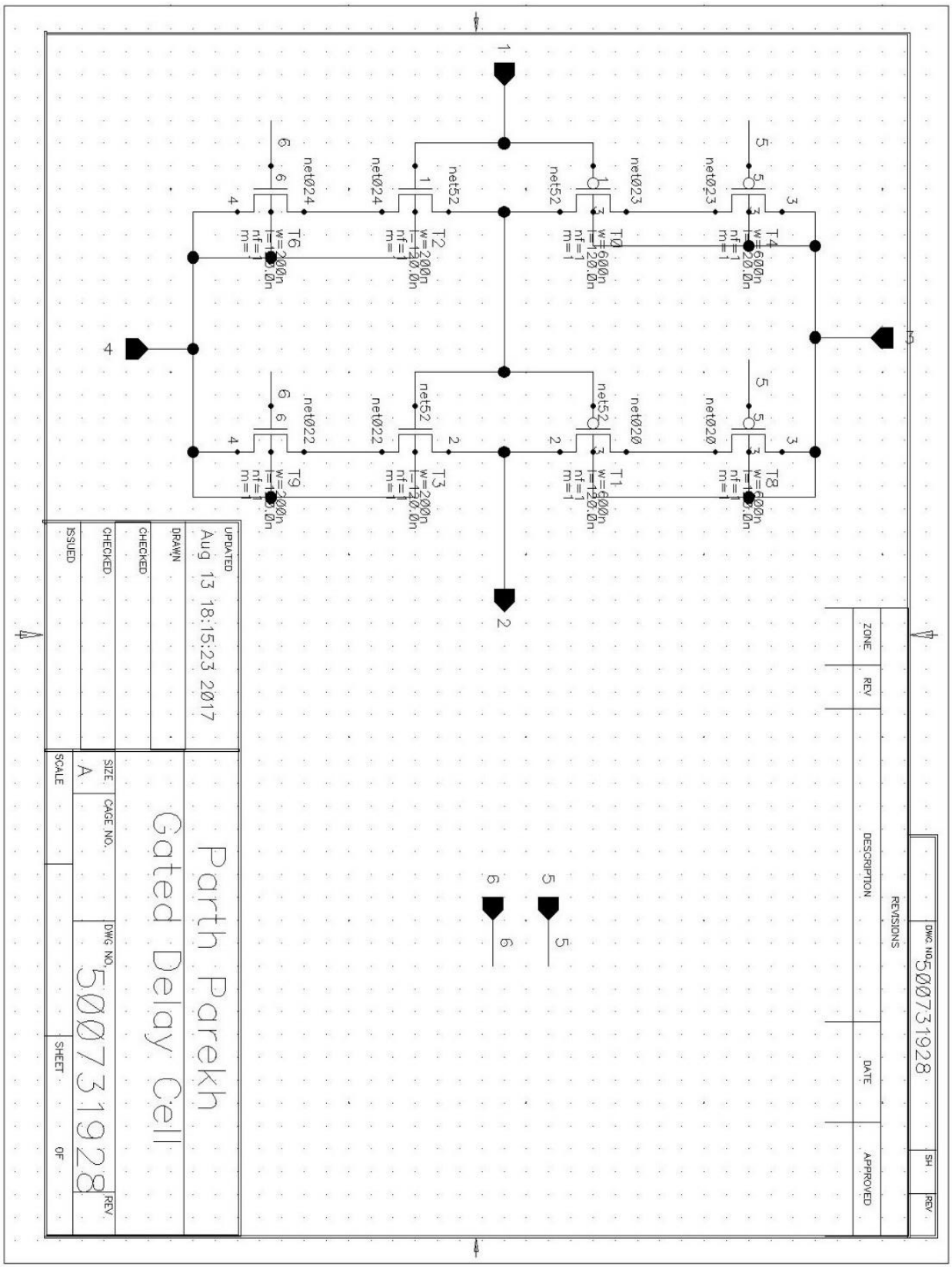

Fig. 5.23 Gated Delay Cell

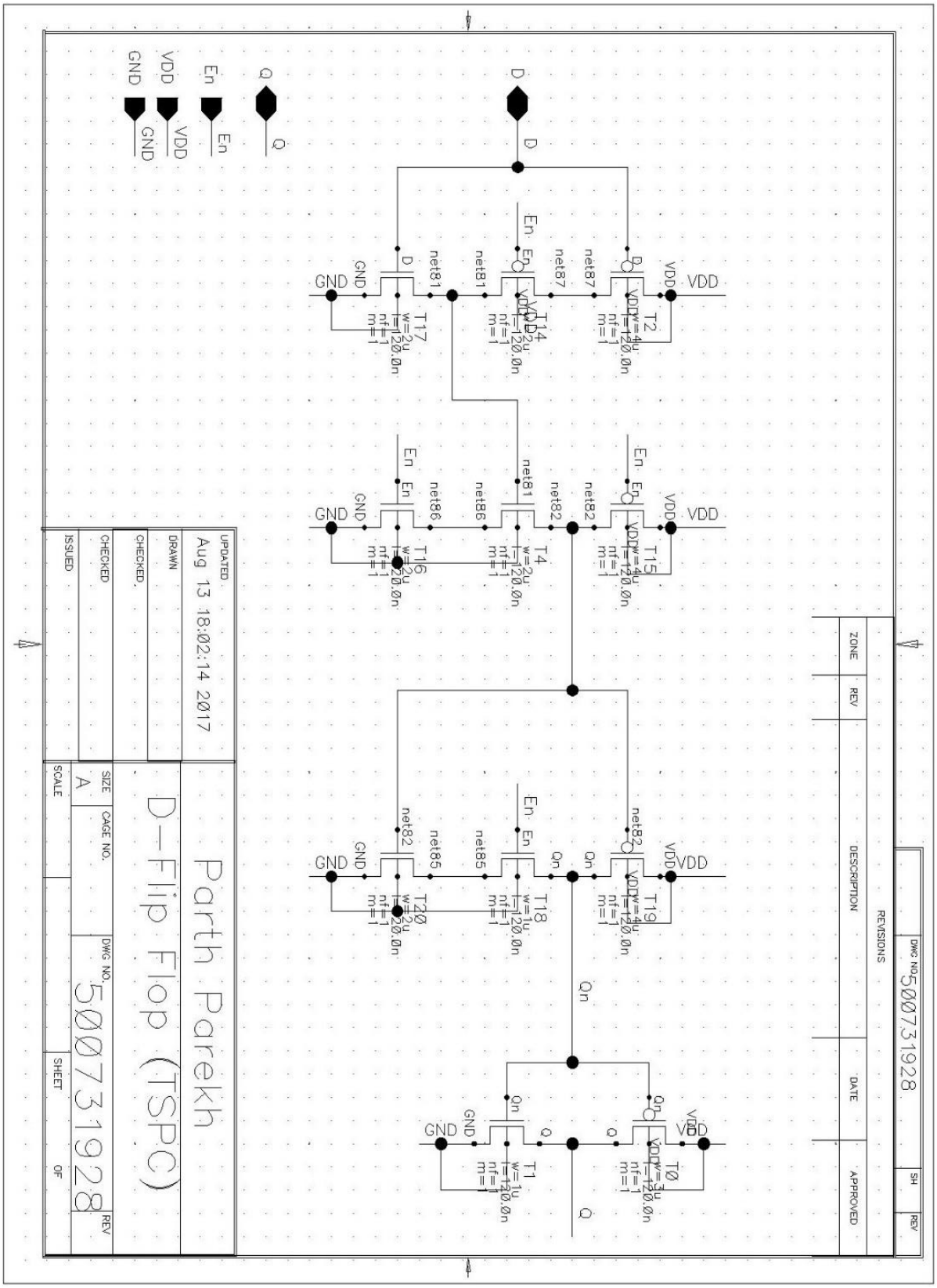

Fig. 5.24 D-Flip Flop

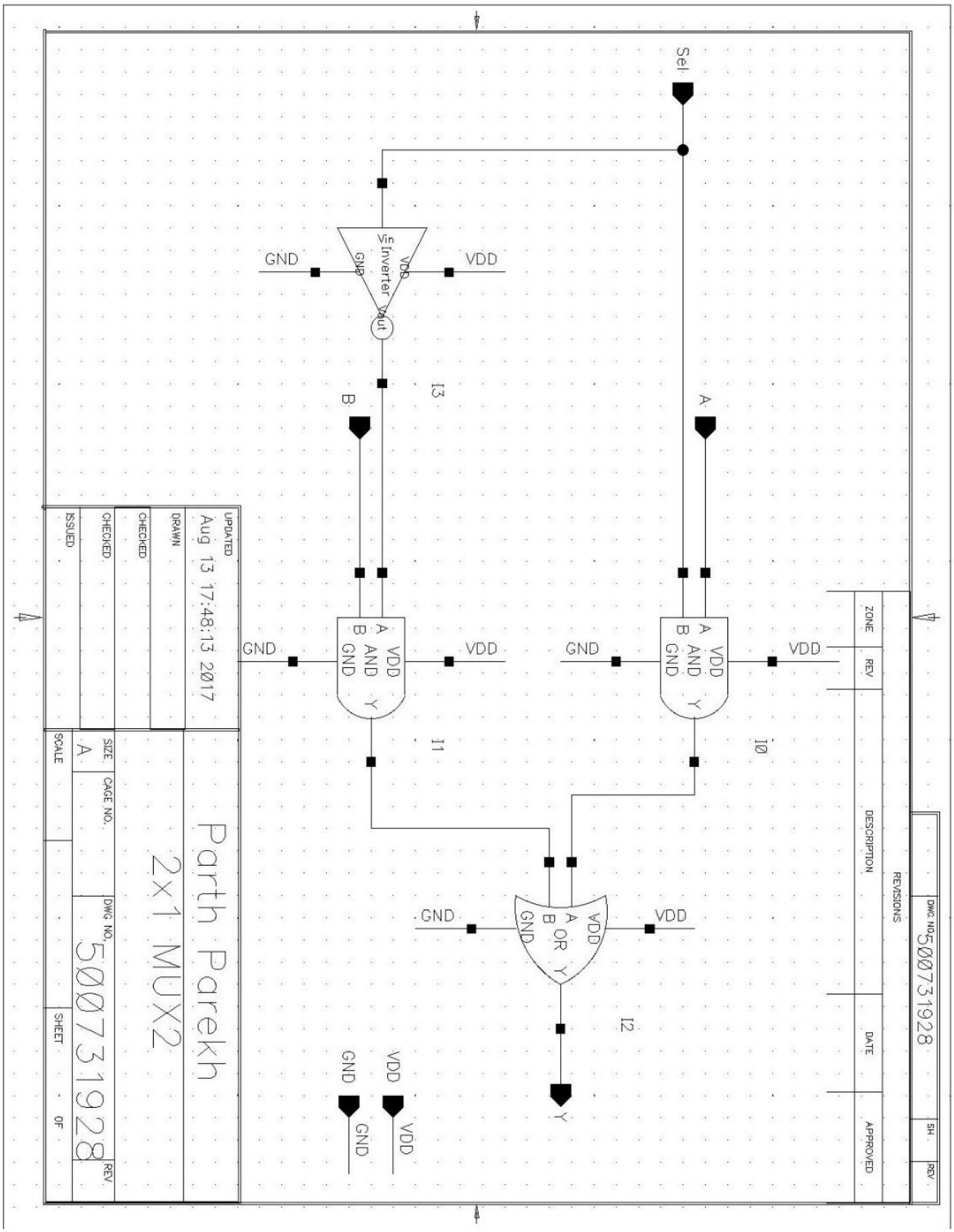

Fig. 5.25 2x1 MUX2 for Tin-Block

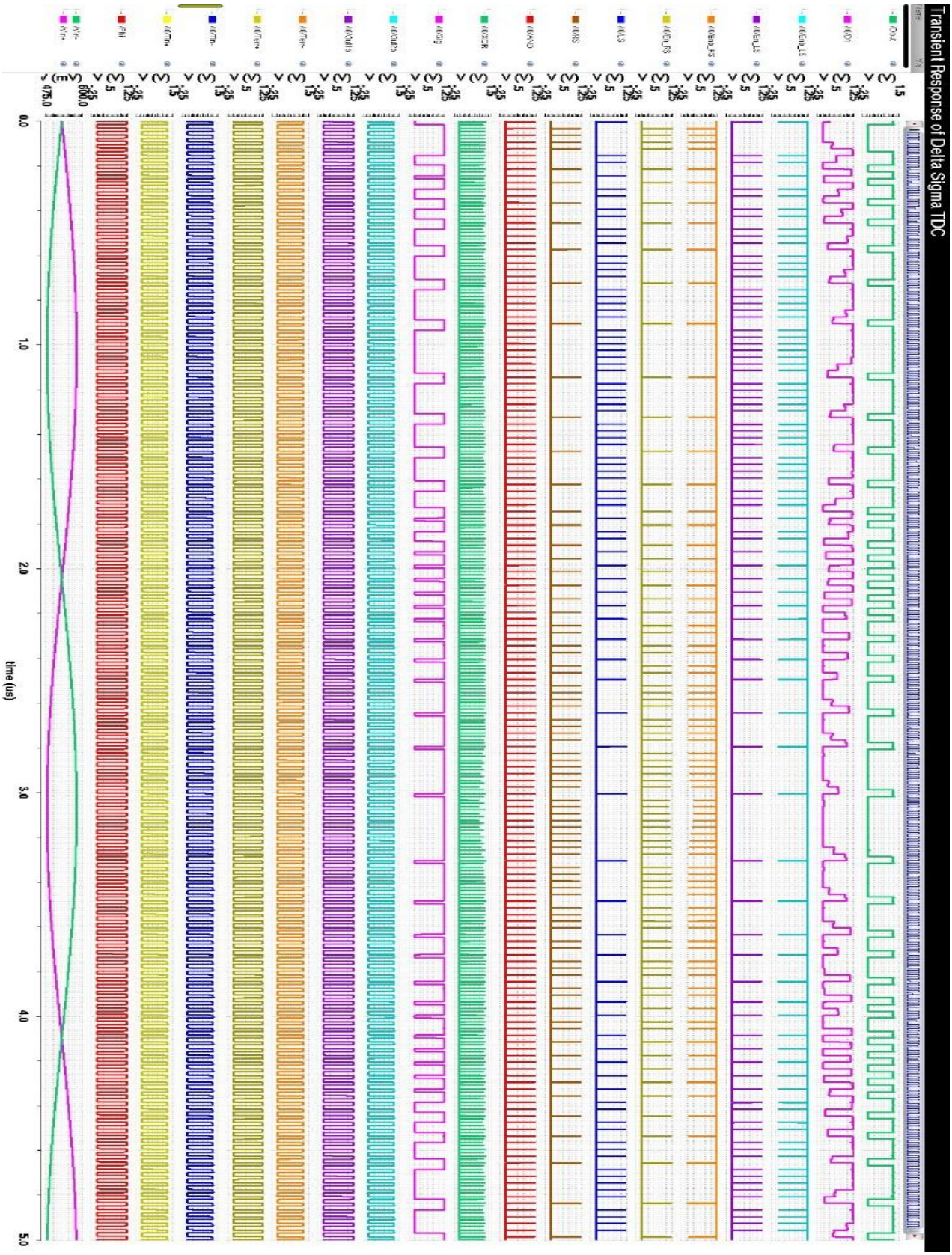

Fig. 5.26 Transient Response of Delta Sigma TDC

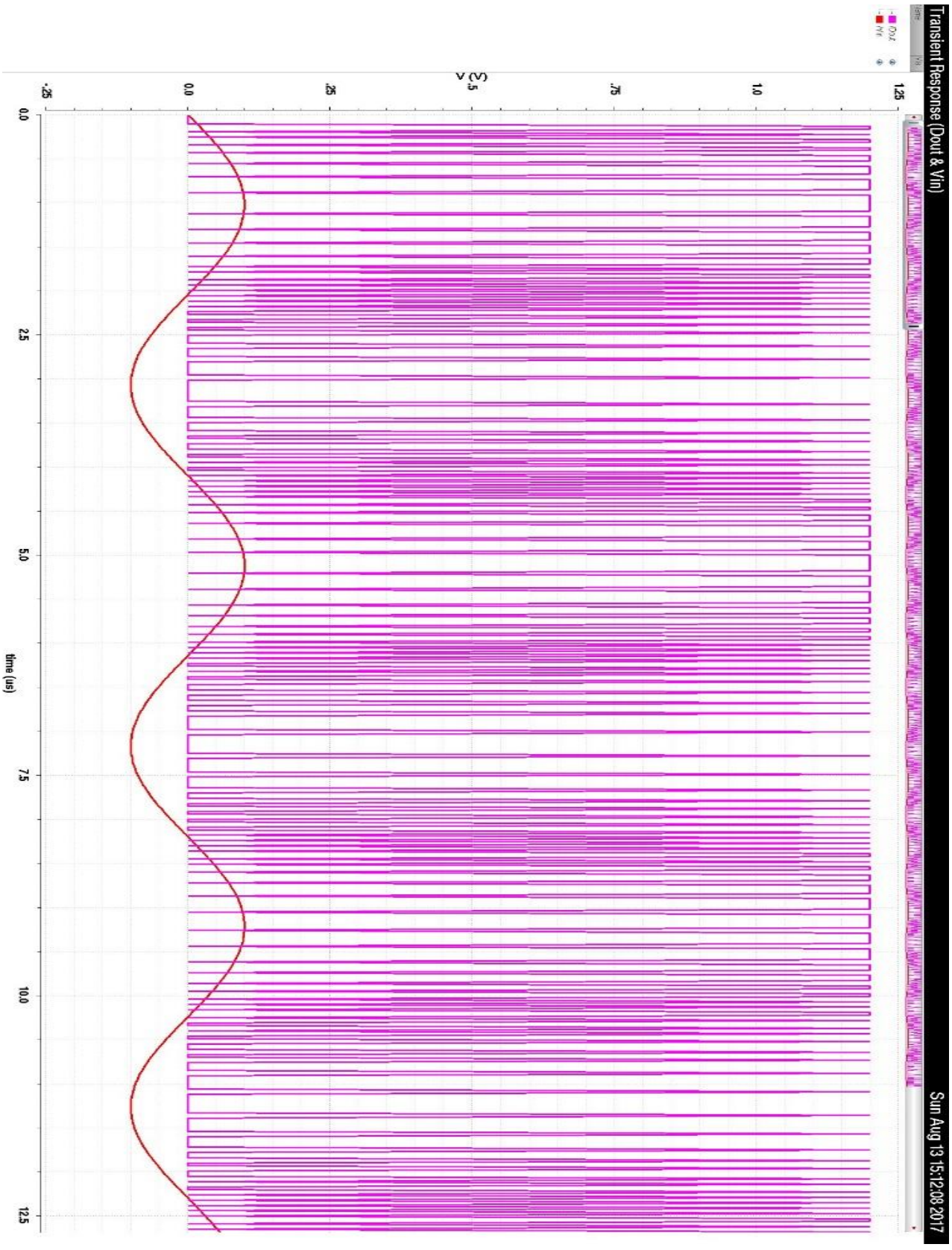

Fig. 5.27 Transient Response [Dout and Vin]

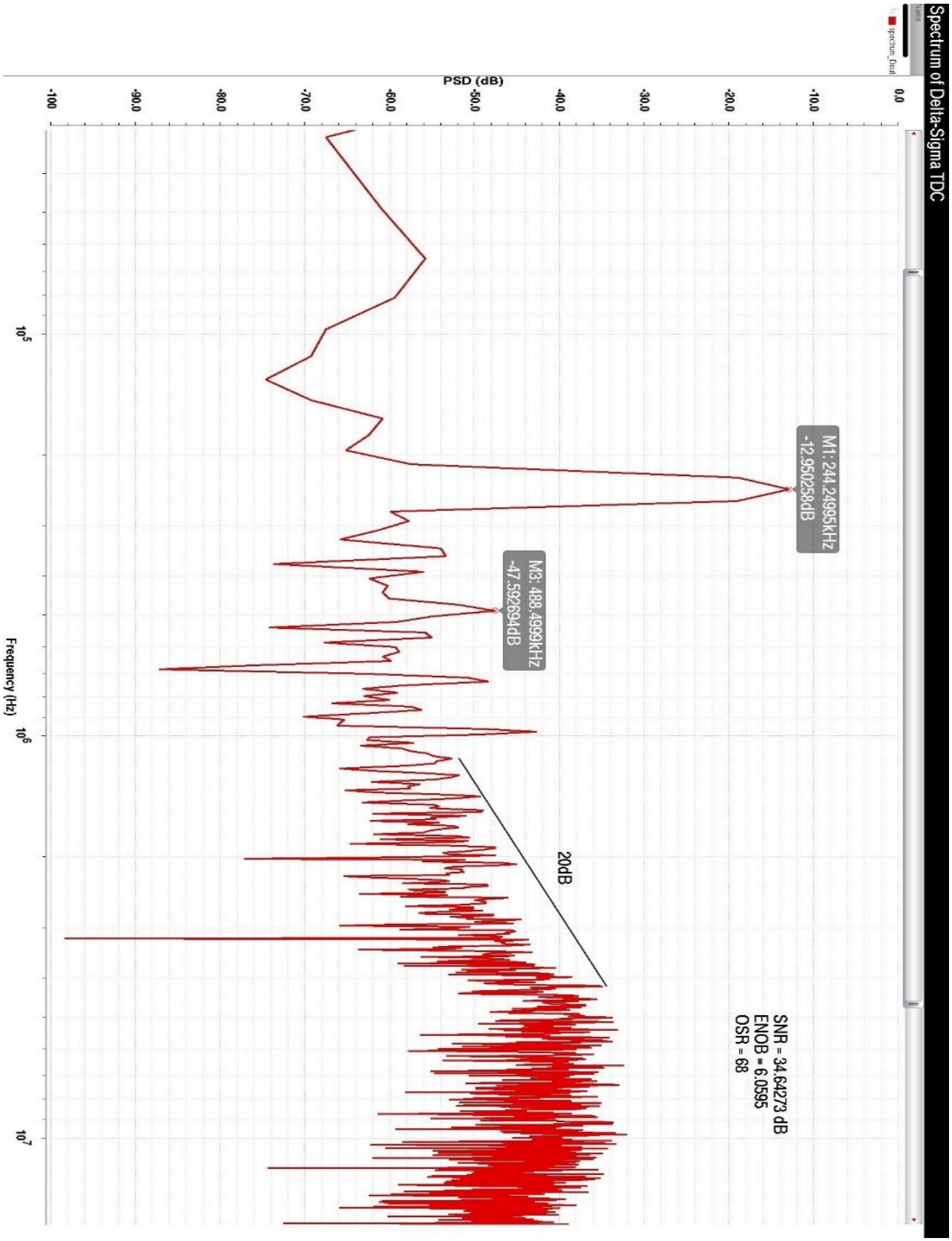

Fig. 5.28 Spectrum of all-digital delta sigma TDC

6. Conclusion

A BD-GDL time integrator with applications in an all-digital first-order single-bit ΔΣ TDC were presented. The time integrator consists of a bi-directional gated delay line with the time variable to be integrated as the gating signal. The accumulation of time variables is performed via the accumulation of the charge of the load capacitor and logic state of the gated delay stages. Issues critical to the performance of the time integrator and modulator were examined. The simulated spectrum of the TDC contains large harmonics arising from the nonlinear characteristics of the BD-GDL, signifying the need for differential BD-GDLs. A fully differential BD-GDL time integrator inspired by dual-slope ADCs is currently being developed, aiming at suppressing the detrimental effect of the nonlinearities of the BD-GDL. The proposed ΔΣ TDC features all-digital realization, ultra low power consumption, and the preservation of quantization noise while possessing first-order noise-shaping. The preservation of quantization noise in the residual voltage of load capacitors is critical as it opens the door for the deployment of MASH architectures to achieve high-order noise-shaping. With a sinusoid time input of frequency 231kHz with OSR 68 and amplitude 333 ps, the ΔΣ TDC exhibits first-order noise-shaping and provides a SNR of 34.64 dB over frequency band 48.27~231 kHz while consuming 293.8 μW. First order noise shaping is also achieved.

7. Future Work

As examined earlier, the large harmonics, both even and odd-order, are present in the spectrum of the all digital first-order single-bit ΔΣ TDC with single-ended BD-GDL time integrator. These harmonics arise due to the nonlinear characteristics of the single-ended BD-GDL time integrator. In order to suppress even-order harmonic tones within the signal band and further improve SNR without sacrificing the benefit of all-digital implementation, it is appealing to design a differential bi-directional time integrator and replace it with single-ended BD-GDL time integrator. Furthermore, the output of the single-ended BD-GDL is a thermometer code 1…10…0 with the left most “0” specifying the node at which propagating “1” vanishes. The BD-GDL is therefore not only a time integrator but also a multi-bit quantizer. Therefore, using that as a motivation, an architecture for all-digital first order multi-bit ΔΣ TDC with single-ended BDL time integrator can be developed which help us to reduce the noise floor.

Appendix A

The MATLAB code required to plot the FFT spectrum and calculate important parameter of ΔΣ TDC is attached as following:

```
%*********************************************************%
% Project: All-Digital Delta Sigma TDC using              %
%          Bi-Directional Gated Delay Line Time           %
%          Integrator                                     %
% Author: Parth Parekh                                    %
% Date: August 15, 2017                                   %
%*********************************************************%
clear all;

close all;

clc;

data = csvread('Dout.csv',1,0); %Loading the raw data saved from the cadence

Time = data (:, 1);

Wave = data (:, 2);

Wave = Wave-mean(Wave); % remove DC offset

order = 1;

nLev = 2; % since I'm using 1 bit slice

Nfft = 2^11; % Total number of samples

fs = 33.33E6; % sampling frequency

bin = 15; % Number of FFT bins

fin = ((bin)/Nfft) *fs % fin should be linked to fs.

OSR = round(fs/(2*fin))

t = [0: Nfft-1];
```

```
n =1:2048;

spec2 = fft (Wave (1: end-0). *hann (length (Wave (1: end-0))))/(Nfft*(nLev-1)/4); %spec2 should have 2048 values. Therefore, if the recorded data is longer than 2048, user should be specifying the range which has 2048 samples.

fftout2 = abs(spec2);

fftout2dbv = 20*log10(fftout2);

Sig_Power2 = fftout2(bin+1);

s2 = norm (fftout2(bin: bin+2)); % Since Hanning window is used, the effective bin number should be bin +/- 1.

Harm_Power2 = sum (fftout2(1: bin-1));

n2 = norm (fftout2(1: bin-1));

SNR2 = 20*log10(s2/n2) % Signal-to-Noise Ratio

ENOB = (SNR2-1.76)/6.02 % Effective number of bits

f = 0:(fin/fs)/Nfft:(fin/fs)/2; % Normalized frequency f/fs)

plot (f (1: Nfft/2+1), fftout2dbv (1: Nfft/2+1), 'r') % Plotting the FFT

grid on;
```

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