Modelling and Current-Mode Control of a Modular Multilevel DC-DC Converter

by

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Abstract

The visions of multi-terminal direct-current (MTDC) grids, DC distribution systems for densely populated urban areas, and DC microgrids for more straightforward integration of distributed energy resources (including renewable energies, electric vehicles, and energy storage devices) have sparked a great deal of research and development in the recent past. An enabling technology towards the fulfilment of these visions is efficient, highly-controllable, and fault-tolerant AC-DC and DC-DC electronic power converters capable of interfacing networks that operate at different voltage levels. This thesis thus presents the results of an in-depth investigation into the operation and control of a particular class of DC-DC converters. The DC-DC converter studied in this thesis is based upon the so-called modular multi-level converter (MMC) configuration, employing half-bridge submodules and with no galvanic isolation. The thesis first presents the governing dynamic and steady-state equations for the converter. Then, based on the developed mathematical model, it identifies suitable variables, strategies, and feedback loops for the regulation of the submodule DC voltages as well as converter power throughput. In particular, two current-control loops are proposed that, in coordination with one another, not only enable the control of the power flow within the converter, but also promise protection against overloads and terminal shorts. The validity of the mathematical model and effectiveness of the proposed control are verified through off-line simulation of a detailed circuit model as well as experiments conducted on a 1-kW experimental setup.

The results of this exercise motivate the extension of the proposed control method to more compact designs with galvanic isolation and enhanced power handing capabilities.

Acknowledgments

I would like to take this opportunity to thank Prof. Amirnaser Yazdani for being the best supervisor, mentor, and friend that I could have ever asked for. The amount of support, knowledge, and the number of opportunities that I have received because of him have truly been a blessing.

To my parents

For all that they have done,

and all that they still do.

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Convention for Notations

For clarity and consistency, the following is used in this thesis.

- Variables that are constant are represented using upper case characters (e.g., P_{max} and V_{cn}.

- Variables that are varying are represented lower upper case characters (e.g., v_1 and i_c.

- Constant and time varying components of composite variables are denoted with the superscripts dc and ac respectively (e.g., v_Δ^{ac} and v_t^{ac}).

- The average value of a time varying component is denoted by an overline (e.g., $\overline{v_1 i_1}$).

List of Abbreviations

DIN	Deutsches Institut fr Normung
EMI	Electromagnetic Interference
F2F	Front-to-Front
HV	High Voltage
HVDC	High Voltage Direct Current
LV	Low Voltage
MMC	Modular Multilevel Converter
MV	Medium Voltage
NI-cRIO	National Instruments CompactRIO
PI	Proportional Integral
PSCAD	Power System Computer-Aided Design
PWM	Pulse-Width Modulation
SM	Submodule
VSC	Voltage-Sourced Converter

Nomenclature

α Phase shift between upper and lower arm voltages

δ_k Reference offset for local voltage regulation

ω Angular frequency of converter AC component

ω_b Bandwidth of system

ω_c Crossover frequency of compensator

ω_m Angular frequency of the modulating waveform

ϕ Phase shift between adjacent PWM carriers

τ_i Integral time constant

d Conversion ratio of the converter

e_{ck} Error associated with the kth submodule capacitor voltage

f_{sw} Switching frequency of submodules

i_m Amplitude of the AC component of i_c

i_1 Current of the upper arm

i_2 Current of the lower arm

i_c Common mode current of the converter

i_t Output current of the converter

k Index of submodule

K_1 Compensator function for the output current

K_2 Compensator function for the input current

K_{cap} Proportional gain of local voltage regulation

K_i Integral gain of compensator function

K_p	Proportional gain of compensator function
L	Arm inductance
L_e	Effective arm inductance seen by the converter output
L_f	Output filter inductor
M	Number of submodules in an arm
m	Modulation index
m_k	Modulation index of the kth submodule
p_1	Power of the upper arm
p_2	Power of the lower arm
P_{dc_1}	DC power of the high voltage side
P_{dc_2}	DC power of the low voltage side
P_{max}	Maximum power transferable by the converter
R	Arm resistance
R_e	Effective arm resistance seen by the converter output
R_f	Output filter resistance
v_Δ	Difference of the arm voltages
v_Σ	Sum of the arm voltages
v_m	Amplitude of the AC component of v_t
v_t	Output voltage with respect to DC side midpoint
v_1	Voltage of the upper arm
v_2	Voltage of the lower arm
v_{c_k}	Voltage of the kth submodule capacitor
V_{c_n}	Nominal submodule capacitor voltage
v_c	Voltage of the submodule capacitor
v_{dc_1}	Voltage of the high voltage side
v_{dc_2}	Voltage of the low voltage side
v_{dc}	DC voltage
v_{SM_k}	Output voltage of the kth submodule
v_{SM}	Output voltage of a submodule

Chapter 1

Introduction

1.1 Background and Motivation

In recent years, there has been an increased demand for a switch to renewable energy sources from the traditional fossil fuel sources. Moreover, an increase in carbon emissions over the past few decades has resulted in a global effort to curb the impact of fossil fuels on the environment. In 2014, it was estimated that around 77% of the energy used in the world was generated from fossil fuels, a percentage that is too large to sustain in the future [1].

Studies have shown that 30% of the fossil fuels extracted annually around the world are used for electric power generation, and that 40% of all energy related carbon emissions originate from fossil fuels used to generate electricity. Also, considering that 80% of the energy harvested from these fossil fuels is lost in the chain from the energy harvesting stage, to the end consumer use [1] means that there is a need for the harvesting and efficient transmission of cleaner energy sources. The need for higher efficiency in the harvesting and transmission of energy has become a primary focus for scientists and engineers across the world, and as a result the use of renewable energy sources has become a hot topic in recent years. In fact, the US Department of Energy estimates that 35% of the energy generated in the US will be done solely by wind energy in the year 2050 [2].

Still, a shift in the current paradigm is required in order to achieve the aforementioned goals of harvesting and transmission, and thus the state of the art must continue to be pushed forward. In order to do so, changes must be made to the framework that is in place at the moment. One of the main changes is the integration of the renewable energy sources into the already existing power grid. However, such an integration can be made much more effective and efficient if HVDC grids are used rather than the existing AC grids [3], [4], due to the nature of the energy sources such as off-shore wind farms.

In an off-shore wind farm, the wind turbines are set up in large bodies of water, and the energy that is generated by the turbines is transmitted to a power station via cables that are submerged in water. In this case, the use of a DC grid as opposed to an AC one is a much better option, as DC transmission lines are not susceptible to reactive power losses the same way that AC lines are, an effect which is amplified when the wires are

submerged in water [1], [2], [5]. Furthermore, when compared to AC transmission lines, DC lines have lower costs and lower power losses when compared to their AC counterparts for a comparable power capacity [5]. Lastly, another great benefit of the DC grid is that the frequencies of the sending and receiving ends are independent of one another which offers a great deal of versatility to the system [2].

Traditionally, HVDC grids have been developed for point-to-point bulk energy transmission. However, as the grids become more and more elaborate, the interconnection of different grids is necessary. There are two prominent cases where the interconnection of DC grids takes place: the interconnection of two HVDC transmission grids are, or the connection of a medium voltage (MV) DC generation system (such as a wind farm) to an HVDC transmission grid [6], [7]. In both cases, one of the biggest challenges is to provide an interface between the two grids, as they will generally be operating at different voltage and/or power levels.

Based on the discussion thus far, it is clear that there is a need to interface either medium voltages to high voltages, or high voltages to other high voltages. To address this need, the DC grids make use of DC-DC converters when converting between different voltage or power levels. However, when operating at medium to high voltages, the conventional two-level voltage-sourced converter (VSC) proves to be insufficient [1], [5], [8]. For efficient operation at MV and HV levels, mulitlevel converters are often used as they offer benefits that the conventional two-level VSC cannot.

One class of mulitlevel converter that is often used for the aforementioned types of HVDC applications is the Modular Multilevel Converter (MMC) [7], [9]–[21]. In essence, the MMC is similar to the two-level VSC, but instead of using a semiconductor switch in each arm, the arms are made up of numerous cells of semiconductor switches. Thus, the MMC allows the larger voltage levels to be divided among multiple smaller switches and capacitors which introduces a number of benefits. First, the requirements of the ratings on all of the components can be relaxed as each submodule will see a reasonably small voltage. Second, the fact that each submodule switches between smaller voltage levels means that the voltages will have much less harmonic distortion, and that the converter will be much less susceptible to stray capacitances and generate less EMI [1]. Next, the fact that the DC storage element is in each individual cell of the MMC, the converter does not require a large DC link capacitor [8]. And finally, the redundancy of the submodules makes the MMC much easier to maintain and makes it more convenient to deal with in the event of a fault, as faulty or damaged submodules can be bypassed as desired [22].

Before getting into the details of this thesis, it is important to understand what the state of the art is in regards to this particular area. Hence, the following section will present a literature review of the concepts and topics that are relevant to this thesis.

1.2   Literature Review Pertinent to Thesis Objectives

In this section, a review of the work that has been done thus far in the literature will be presented. The main focus of this review will be the different topologies and control

strategies used in MMCs implemented as DC-DC converters. Furthermore, the fault handling capabilities of the DC-MMC is also of interest.

In general, the DC-MMC has been reported in two main configurations: the two stage DC-DC converter, and the direct DC-DC converter. In the conventional two stage DC-DC converter, two DC-AC MMCs are connected in a front-to-front (F2F) configuration through an intermediate transformer [7], [20], [23], [24]. Of course, the introduction of an intermediate stage results in increased weight, cost, and losses in the converter, and so the directly connected DC-DC converter has been discussed in [14], [15], [21], [25]–[28] where the intermediate stage is removed altogether. In order to successfully remove the intermediate stage while retaining the desired DC-DC power conversion, an AC circulating current must be present in the upper and lower arms of every phase in the converter to maintain the necessary energy balance between the arms of the DC-MMC [29]–[33].

To have a feasible and economical converter, the MMC must be able to handle faults and have some fault tolerance. As such, a great deal of work has been done on the fault handling capabilities of the MMC, both from a topological aspect, and through the use of elaborate control strategies. First, in [34] a fault blocking control technique is presented for the F2F topology where the converter continues to operate while connected to the faulty side with reactive current absorption. This technique is reported to achieve a greater DC fault current declining rate, while also ensuring maximum power transfer between the interconnected DC grids. However, as mentioned before the F2F topology includes an intermediate transformer which increases the weight, cost, and most importantly losses in the system. Therefore, the remainder of this review and thesis will focus on the direct DC-DC converter topologies which eliminate the intermediate stage altogether.

In order to eliminate the need for an intermediate transformer, several different converter topologies have been presented. In [27], a transformerless topology is discussed which implements crossly connected upper and lower arms of the MMC using capacitors. The resulting AC and DC power loops formed by the capacitors allow for power balance between the primary and secondary sides. Next, in [35], a topology has been presented which replaces the intermediate transformer using an LCL-based DC-DC converter. Additional converter topologies including the thyristor-based high-ratio converter, rotating capacitor converter, switching-module converter, and resonant step down converter are presented in [36]–[39] which all allow for the elimination of the intermediate transformer. However, as discussed in [27], each topology comes with its own drawbacks. For instance, the rotating capacitor converter and switching-module converter have a discontinuous DC current at the primary and secondary side, while the resonant step-down converter loses its bidirectional power transmission capability when trying to achieve a high voltage ratio between the primary and secondary sides.

From the control point of view, the direct implementation of the DC-DC MMC requires the injection of an AC circulating current in order to implement a closed loop control of the converter. However, the introduction of this circulating current into the converter can result in a degradation of the converter's efficiency [30]. In order to preserve the efficiency of the converter, the AC current needs to be minimized. In [40], a

control strategy is presented which regulates the DC-link currents, ensures that the submodule capacitor voltages are balanced, and most importantly that the magnitude of the AC current is minimized. Next, in [41], an enhanced closed-loop control strategy which increases power transfer capabilities while also reducing the ac circulating current of the converter is presented. Furthermore, the harmonic content of the AC circulating current is also of interest, as in [42] where the second harmonic component of the circulating current is controlled in order to reduce power losses and balance the submodule capacitor voltages. Additional control techniques such as in [43] have also been presented, but the approach is more complicated as it makes use of modelling the converter in the d-q frame.

Finally, the topological solutions for increasing the fault handling abilities of the converter have also been a focus in the literature. In [29], a transformerless hybrid MMC is presented which uses a combination of half-bridge and full-bridge submodule arms. The lower and shunt arms of the MMC are made up of half-bridge submodules, whereas the upper arm is made up of full-bridge submodules. By introducing a shunt arm of half-bridge submodules, this configuration is capable of eliminating the output filter entirely. At the same time, this topology provides bidirectional fault ride through capabilities as a result of the full-bridge submodules used in the system, but still uses a lower number of switches than if the system was made up of full-bridge submodules entirely. The concept of bidirectional fault handling is further explored and considered for the application of an HVDC interconnect in [44] where a topology is introduced that features bidirectional power flow, step-up and step-down operation, and most importantly, bidirectional fault blocking similar to that of a dc circuit breaker, without actually using a circuit breaker, using multiple interleaved strings of submodules in order to perform the power conversion. In [45], a fault protection scheme for MMCs using half-bridge submodules is introduced which replaces the typical bypass thyristors found in the submodules with an independent modular rectifier bridge. Then, a switch with negligible losses is introduced to isolate the MMC in the event of a fault while the rectifier bridge suppresses the fault current by introducing a reverse DC voltage. Finally, [46] examines the different DC protection design choices and their impacts on the DC fault recovery of the MMC with half-bridge submodules. Also, a DC circuit breaker controller is developed along with a blocking scheme to limit the DC side fault current.

Having illustrated a clear picture of the work done thus far, the following section will introduce the objectives of this thesis.

1.3   Thesis Objectives

Based on a review of the literature, it is clear that there is a need for a DC-DC MMC that can provide DC fault handling capabilities. Thus, the objective of thesis is to present a DC-DC converter that can meet this requirement. In particular, a modular multilevel converter implemented as a DC-DC converter will be explored in detail along with the closed loop control of the converter. The objective of the control technique will be to control the current of the converter such that DC faults on the input or output side can be handled safely by limiting the input or output current.

In order for the MMC to operate as intended, the submodule capacitors in the arms of the MMC must act as a string of voltage sources. To ensure that this is indeed the case, there is a need for a closed loop control of the MMC such that it exhibits the desired characteristics. Moreover, since the input and output powers of any converter must also be controllable in some manner, the challenge of controlling the MMC can be broken into three main parts: the capacitor control, input power control, and output power control.

Therefore, the main objective of this thesis can be further broken down to consider control techniques by which all of the powers associated with the MMC can be completely regulated. As such, three main control loops are required which are dedicated to the input power, output power, and capacitor voltages. Moreover, it is expected that the concepts presented in this thesis should be verifiable by a practical system, and so a secondary objective is to present a fully functional converter that operates based on the theory presented in this thesis.

1.4 Thesis Structure

This thesis is categorized into five unique chapters, including this one. Here, an introduction of the converter and its relevance to the state of the art were presented along with some objectives for this thesis. In Chapter 2, the theoretical background of the MMC will be presented. First, the principles of operation will be discussed in detail to provide a fundamental understanding of how the MMC operates. Next, the mathematical modelling of the entire converter will be done considering a general system. Then, the steady state characteristics of the converter will be examined followed by a control methodology that can be used to guarantee that the steady state characteristics are realized. Furthermore, the synthesis of the arm voltages in a multilevel topology require some explanation. Finally, a numerical case study will be presented which will serve as a foundation for the simulation and experimental sections.

In the third chapter, the system presented at the end of Chapter 2 will be simulated using the PSCAD software. The simulation will subject the converter to several different cases in order to test and validate the proposed theory of Chapter 2.

Next, Chapter 4 will discuss the details of the physical implementation of the converter, along with experimental results from the hardware setup. The experimental results will be compared directly with the simulation results and the expected theory so as to further validate the theoretical concepts discussed in Chapter 2.

Finally, Chapter 5 will summarize the contributions and findings of the thesis, while also discussing potential future works to elaborate upon in related areas. Furthermore, the main body of the thesis will be followed by some appendices which will present details relating to the experimental setup including the hardware used, and details related to the control platform.

The main body of the thesis will be followed by a series of appendices which contain details related to the physical implementation of the converter.

Chapter 2

Theoretical Operation of the MMC Based DC-DC Converter

To fully understand the operation of the MMC, the theoretical basis of the converter must be discussed in detail. In this chapter, the principles of operation of the MMC will be introduced based on the two-level VSC. Then, the mathematical model of the converter along with its steady state characteristics will be presented along with some control techniques for the output and input power. Finally, a numerical case study will be presented in order to set the stage for the following chapters.

2.1 Principles of Operation

Before delving into the details of the MMC, a good starting point is the simple two-level voltage source converter. In this section, the principles of operation of the MMC will be presented based on the simple two-level VSC. Once the operation of the VSC is understood, the discussion will shift to the broader concept of the MMC.

2.1.1 The Two-Level VSC as a Building Block

While the MMC consists of a large number of submodules in general, it is a much simpler task to begin with the fundamental building block of the converter: the two-level voltage source converter. Since the MMC is essentially a number of strings of two level VSCs connected in series, by understanding how the two level VSC operates one can quite easily understand how the MMC operates. The simplest topology of the two level VSC is the half bridge configuration. In this configuration, the two semiconductor devices form a complementary pair, meaning that when one is active or conducting, the other is turned off and not conducting. Like any VSC, there is an energy storage element, which is often referred to as the DC link capacitor. The purpose of this capacitor is to maintain the DC side voltage at a fairly constant level for a reasonable portion of a fundamental cycle. The operation of the two-level VSC requires that the gates of the two semiconductor devices be fed with gating pulses. These gating pulses are used to control when the semiconductor device is in the on state (conducting) or off state (cut
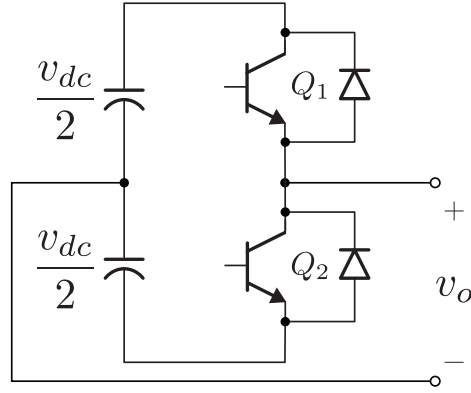
Figure 2.1: Basic two level voltage-sourced converter.

off). When the upper device is fed with a high pulse, the output of the VSC will have a value equal to the positive rail voltage of $v_{dc}/2$ which is the voltage of the DC side capacitor. Conversely, when the lower device is active, the output of the VSC is $-v_{dc}/2$. As such, by generating the desired patterns of the gating pulses, it is possible to control the output voltage of the VSC. To describe the output of a two-level VSC, the variable s, which denotes the state of the devices, can be introduced. Simply put, when s assumes a value of 1, the output is connected to the positive DC rail, and when s is -1, it is connected to the negative DC rail. Mathematically,

$$v_o = s \frac{v_{dc}}{2} \tag{2.1}$$

Having understood how the VSC operates physically, it is important to discuss how the switching instances of the devices can be determined in order to control the output voltage of the converter. The most common way to determine when the devices should be turned on or off is by employing pulse-width modulation (PWM). PWM is an operation in which two waveforms, referred to as the modulating wave and carrier wave are compared to one another, and at the intersection points of these two waveforms the devices switch states. A key quantity that is used in PWM is referred to as the modulation index, m. The modulation index is used to relate the DC side voltage to the fundamental component of the modulated voltage as follows:

$$\hat{v}_o = m \frac{v_{dc}}{2} \tag{2.2}$$

Therefore, the modulated voltage can be expressed as

$$v_s = \frac{m v_{dc}}{2} cos(\omega_m t) \tag{2.3}$$

where ω_m is the frequency of the modulating or reference waveform. It should be noted that (2.3) is only the fundamental component of the modulated voltage. In reality, the modulated voltage consists of a large number of harmonics since it is generated by the switching of semiconductor devices. Still, by ensuring that the carrier frequency

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is much larger than the modulating signal, the modulated voltage will more accurately represent an analog signal instead of a digital signal. Also, while the sharp changes in voltage levels will create higher-order harmonic content, these harmonics do not create significant currents in the system and can therefore be ignored in most cases [1], [8].

In this section, the two-level VSC was introduced in order to serve as a building block for the MMC. In the following section, the general concept of the MMC will be introduced and discussed.

2.1.2 The Modular Multilevel Converter (MMC)

Having explored the basic VSC topology, the discussion can be expanded to consider the MMC. Simply put, the MMC is a multilevel converter that consists of a string of two-level VSCs. In the general case, each VSC is usually referred to as a submodule (or sometimes referred to as a cell or chain link), and a string of submodules is referred to as an arm [9]. Typically, there are two types of submodules; half-bridge submodules, and full-bridge submodules, which as the names suggest, are made up of semiconductor switches configured as a half-bridge and full-bridge, respectively. While there are more sophisticated submodule configurations, the typical MMC makes use of either half or full bridge submodules [30].

As seen in Fig. 2.2, two arms, two DC terminals (a high voltage and low voltage side), and a relatively small inductor in each arm. In the two-level VSC, the inductors are required to allow fast current changes during the commutation of phase legs. However, in an MMC the inductors serve a different purpose since the commutation takes place in the submodules, meaning that the rapid change which takes place in the two-level VSC does not exist in the MMC arms [1], [8]. Instead, in the MMC the inductors are required to prevent direct parallel connection of voltage sources (which is implemented by the submodule strings). In Fig. 2.2, the arm voltages are represented by two voltage sources. However, in reality these two voltage sources will be replaced with strings of submodules. Later in this section, it will be shown that under certain conditions, the submodules can be simplified to be modelled as voltage sources.

As seen in Fig. 2.3, a half-bridge submodule consists of one two-level VSC, that is, two series connected semiconductor switches connected across a DC capacitor which is used to maintain a constant voltage. In order to create a chain of such submodules, the two external terminals of the submodule (the node labelled v_o in Fig. 2.3, and one of the DC capacitor terminals) are connected in series with other submodules. Based on the conduction states of Q_1 and Q_2, there are two possible switching states for the submodule: bypass or insertion. When the submodule is in the bypass state, the Q_2 is active. As a result, the submodule acts as a short circuit and exhibits a negligible voltage drop. On the other hand, when the submodule is inserted, Q_1 is active, meaning the submodule exhibits a voltage equal to the DC capacitor voltage [9]. Thus, the output voltage v_o of each submodule can be expressed as in terms of a switching function s as seen in (2.4).

$$v_o = sV_c \tag{2.4}$$

where s is 0 for the bypass state, and 1 for the insertion state. Furthermore, using a
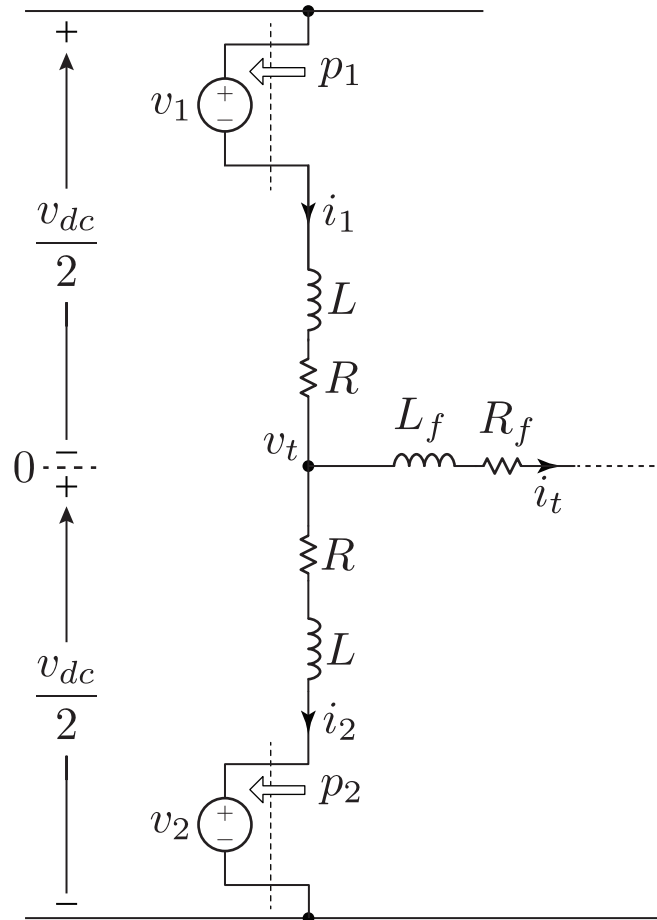
Figure 2.2: Generic MMC circuit configuration considering the two arm voltages to be voltage sources.
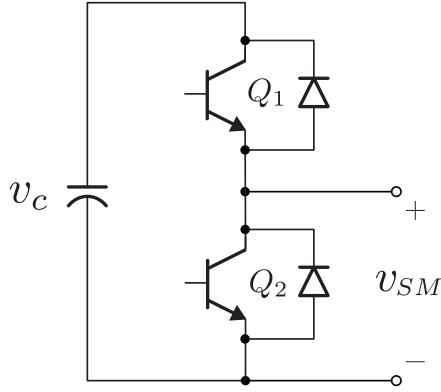
Figure 2.3: Half-bridge submodule used in the modular multilevel converter.

string of M half-bridge submodules with equal capacitor voltages, a voltage waveform such similar to that of Fig. 2.4 can be generated. Of course, the submodules can also be in the full-bridge configuration which would allow the MMC to operate at a higher power level [2], but they will not be considered for the purpose of this thesis.

In order for a submodule or string of submodules to operate correctly, the power flow of the submodule (or string) must be balanced over time [30], [32]. That is, a net power of zero must be ensured. In the event that this condition is violated, the capacitor energy and therefore capacitor voltage will increase or decrease uncontrollably. This problem of power balancing in multilevel converters can be addressed conveniently by splitting it into two parts: one for the overall energy exchange between strings of submodules, and one for the balancing of individual capacitor voltages [47]. Since all of the submodules will not be switched with the same duty cycle (in general), they will typically have varying voltage levels, and will require some type of individual regulation. It should be noted that regardless of the submodule configuration, the submodule capacitor should be chosen to be fairly large such that its voltage is fairly constant while carrying significant currents at a low harmonic order (typically first and second order) [1].

First, the issue of the energy exchange of each arm can be addressed by ensuring that the sum of the capacitor voltage in a given arm is maintained at a constant value. Since there will be low-frequency AC currents injected into the capacitors, there will generally be some variation in this sum during a fundamental cycle [1]. So, the objective here is to regulate the average voltage over a cycle. Second, the individual submodule regulation is local to each submodule. As long as the DC capacitor voltage can be held at a reasonable constant level, the converter submodules can be modelled as voltage sources [5], [30], [48]. This means that an entire string of submodules can be modelled as a single voltage source by combining the series connected voltage sources, and by doing so the overall analysis and operation of the MMC can be simplified substantially. Since the converter only requires that two voltages v_1 and v_2 be generated according to all of the specifications of the system, the means by which the two voltages are created are entirely arbitrary. Simply put, the converter doesn't care whether v_1 and v_2 are generated by
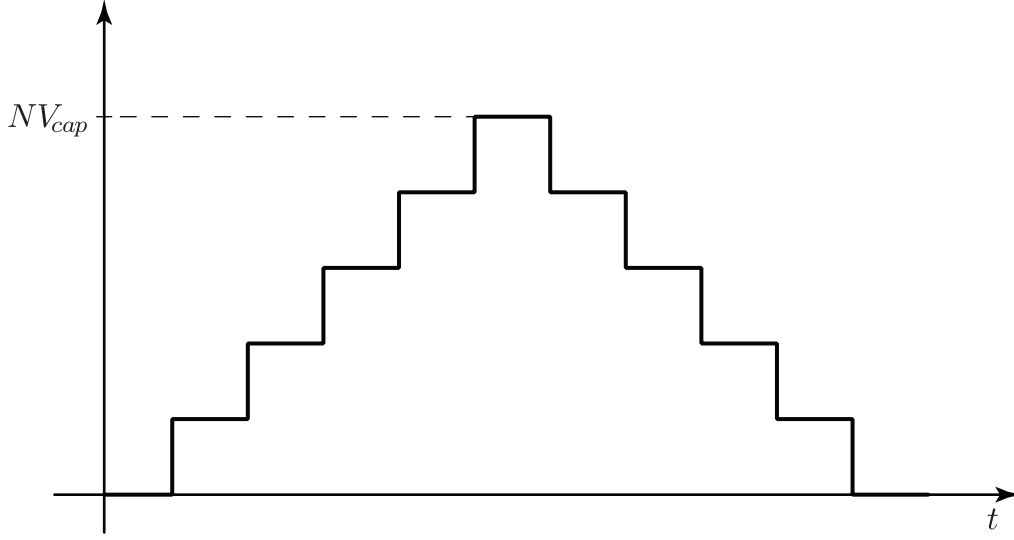
Figure 2.4: General arm voltage waveform using half-bridge submodules.

a single two-level VSC, or a string of 10 submodules, or even 100. All that it requires is that the voltages v_1 and v_2 take on the desired form: a very important characteristic that will be exploited in the mathematical modelling of the MMC.

Next, assuming that the arm powers and individual capacitor voltages are balanced, a submodule string of M submodules will produce a voltage waveform as seen in Fig. 2.4. As expected, the number of levels in the arm voltage and the maximum achievable magnitude of the voltage both increase with M. In general, a string of M half-bridge submodules that have capacitors being regulated at a voltage V_{cap} can take on values between zero and NV_{cap}, for a total of $M+1$ levels in the arm voltage. As the number of submodules increases, the waveform seen in Fig. 2.4 will approach a continuous waveform, since the magntiude of the voltage on the individual submodules will be much smaller than that of the maximum arm voltage resulting in a smaller discrete step. This is considered to be one of the greatest advantages of the MMC since the result is a much lower $\frac{dv}{dt}$, meaning stray capacitances have a much smaller impact, and the requirements on any equipment connected to the converter (such as transformers) can be relaxed. Also, the topology of the MMC removes the need for a large DC link capacitor as the submodule capacitors store the energy, and offers additional benefits such as modularity, and lower power ratings on the components used in the system which can significantly reduce the cost of the converter overall [1], [2], [5], [8].

Based on the discussions of this section, it is clear that the main challenges associated with the implementation of the MMC are the zero net power balance, and the individual capacitor voltage regulation. In order to better understand how these challenges can be addressed, the following sections will present a mathematical model of the MMC, along with some control techniques for the output and input power, as well as shed light on the zero net power balance and individual submodule regulation. For the majority of this analysis, the arm voltages will be treated as voltage sources since the conditions of power

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balance and capacitor voltage regulation will be assumed. Then, after the analysis has been carried out, the synthesis of these arm voltages using submodules will be discussed in order to bridge the gap between the theoretical analysis, and the practical converter.

2.2 Mathematical Modelling of the MMC

In the previous section, the fundamentals of the MMC were introduced. In this section, the MMC will be analyzed in order to obtain a mathematical model for the different quantities that are required in order to control the input and output power while ensuring that the zero net power balance and individual capacitor regulation are maintained. To begin the analysis, the arms of the MMC will be modelled as voltage sources v_1 and v_2. It should be noted that by considering these two arms to be voltage sources, this analysis assumes that the arms are operating under zero net power, and the capacitors are perfectly regulated. Then, based on Fig. 2.2 it is possible to define the following voltages:

$$v_\Sigma \triangleq v_1 + v_2 \tag{2.5}$$

$$v_\Delta \triangleq -v_1 + v_2 \tag{2.6}$$

where v_Σ and v_Δ are referred to as the common mode and differential mode voltages, respectively. Next, the following current can be defined as the common mode current:

$$i_c \triangleq \frac{i_1 + i_2}{2} \tag{2.7}$$

Next, it is possible to manipulate v_Σ and v_Δ in order to define voltages v_1 and v_2 as follows in terms of the common mode and differential mode voltages:

$$v_1 = \frac{v_\Sigma - v_\Delta}{2} \tag{2.8}$$

$$v_2 = \frac{v_\Sigma + v_\Delta}{2} \tag{2.9}$$

Similarly, it is possible to write a KCL at the node where the two arms of the MMC meet the output terminal, and using the definition of the common mode current, the currents i_1 and i_2 can be expressed in terms of the common mode current i_c and output current i_t:

$$i_1 = i_c + \frac{i_t}{2} \tag{2.10}$$

$$i_2 = i_c - \frac{i_t}{2} \tag{2.11}$$

Therefore, the upper and lower arm powers p_1 and p_2 can be determined by taking the products of v_1, i_1 and v_2, i_2, respectively.

$$p_1 = \overline{v_1 i_1} = \overline{\left(\frac{v_\Sigma - v_\Delta}{2}\right)\left(i_c + \frac{i_t}{2}\right)} \tag{2.12}$$

$$p_2 = \overline{v_2 i_2} = \overline{\left(\frac{v_\Sigma + v_\Delta}{2}\right)\left(i_c - \frac{i_t}{2}\right)} \tag{2.13}$$

Note, that the arm powers p_1 and p_2 are defined as the average power going into submodule strings in the upper and lower arm, respectively as seen in Fig. 2.2. Also, as mentioned in the previous section, the submodule capacitors will certainly have some ripple, and therefore the average voltage (and therefore average power) are of importance here. Next, it is possible to take the sum and difference of these two expressions in order to obtain two equations for $p_1 + p_2$ and $-p_1 + p_2$.

$$p_1 + p_2 = \overline{v_\Sigma i_c} - \frac{1}{2}\overline{v_\Delta i_t} \tag{2.14}$$

$$-p_1 + p_2 = \overline{v_\Delta i_c} - \frac{1}{2}\overline{v_\Sigma i_t} \tag{2.15}$$

Equations (2.14) and (2.15) are an important intermediate result and will be revisited later as they govern the power distribution between the upper and lower arms of the converter leg. The control of the upper and lower arm powers will be carried out through their sum and difference as will be seen in later sections. The next step in the mathematical modelling is to obtain equations for the dynamics of i_c and i_t so that they can be controlled. In order to understand the dynamics of the common mode and terminal currents i_c and i_t, it is possible to use KVL on the upper and lower arms. Doing so yields the following equations for the upper and lower arms respectively.

$$\frac{v_{dc_1}}{2} - v_1 - L\frac{di_1}{dt} - Ri_1 = v_t \tag{2.16}$$

$$v_t - L\frac{di_2}{dt} - Ri_2 - v_2 = -\frac{v_{dc_1}}{2} \tag{2.17}$$

These two equations can then be rearranged as follows:

$$L\frac{di_1}{dt} + Ri_1 = \frac{v_{dc_1}}{2} - v_1 - v_t \tag{2.18}$$

$$L\frac{di_2}{dt} + Ri_2 = \frac{v_{dc_1}}{2} - v_2 + v_t \tag{2.19}$$

Next, if (2.19) is subtracted from (2.18), and $-v_1 + v_2$ is replaced with v_Δ, the result is the following first order differential equation.

$$\left(\frac{L}{2}\right)\frac{di_t}{dt} + \left(\frac{R}{2}\right)i_t = \frac{1}{2}v_\Delta - v_t \tag{2.20}$$

Similarly, if (2.18) and (2.19) are added together, and $v_1 + v_2$ is replaced with v_Σ, the result is another first order differential equation.

$$L\frac{di_c}{dt} + Ri_c = -\frac{1}{2}v_\Sigma + \frac{1}{2}v_{dc_1} \tag{2.21}$$

Next, based on Fig. 2.2 and the fact that L_f behaves as a short circuit for DC, v_t can be expressed as:

$$v_t = \left(-\frac{v_{dc_1}}{2} + v_{dc_2}\right) + R_f i_t + L_f\frac{di_t}{dt} \tag{2.22}$$

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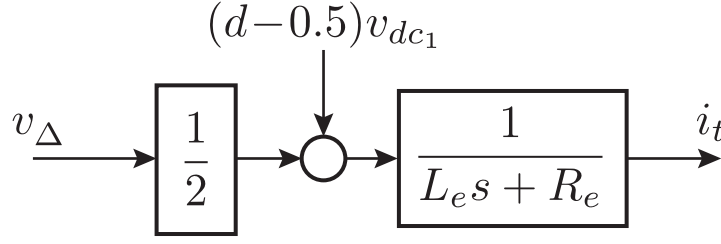
Figure 2.5: Block diagram representation of (2.20).
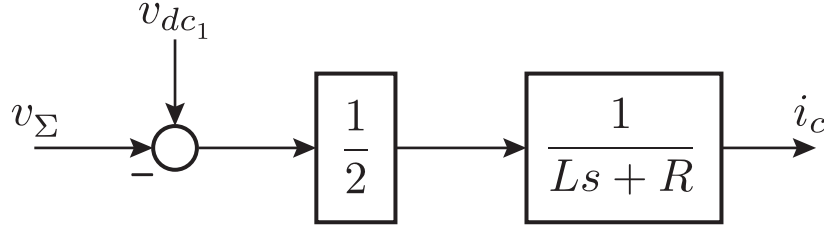
Figure 2.6: Block diagram representation of (2.21).

Now, if (2.22) is substituted into (2.20) and the equation is rearranged to collect like terms

$$L_e \frac{di_t}{dt} + R_e i_t = \frac{1}{2} v_\Delta - (d - 0.5) v_{dc_1} \tag{2.23}$$

where $L_e \triangleq \frac{L}{2} + L_f$ and $R_e \triangleq \frac{R}{2} + R_f$. The two equations (2.20) and (2.21) can be shown in a block diagram format as seen in Fig. 2.5 and Fig. 2.6. It is clear that i_c and i_t can be controlled through v_Σ and v_Δ respectively based on strictly proper first-order plants. According to (2.21) and (2.20), i_c and i_t will determine the required v_Σ and v_Δ, and through their initial definitions directly determine the desired v_1 and v_2 for the required operating point. At the same time, the required magnitudes of $p_1 + p_2$ and $-p_1 + p_2$ can be determined by regulation schemes for the submodule DC voltages. These control loops will be further elaborated upon at a later time. In this section, the basic mathematical model of the MMC was presented. Then, the dynamics of the system were presented in order to formulate expressions that will later be used for the purpose of controlling the MMC. In the next section, the steady state characteristics of the MMC will be discussed, such that the operation of the system under stable conditions can be better understood.

2.3   Steady State Characteristics of the MMC

Having laid the foundation for the mathematical model of the MMC in the previous section, this section will present the steady state characteristics of the MMC. In essence, the mathematical model must be used in order to develop a set of expressions that can be used to predict how the MMC should behave if all of the assumptions made previously hold true. Consider the circuit seen in Fig. 2.7. To begin, it is worth mentioning that in
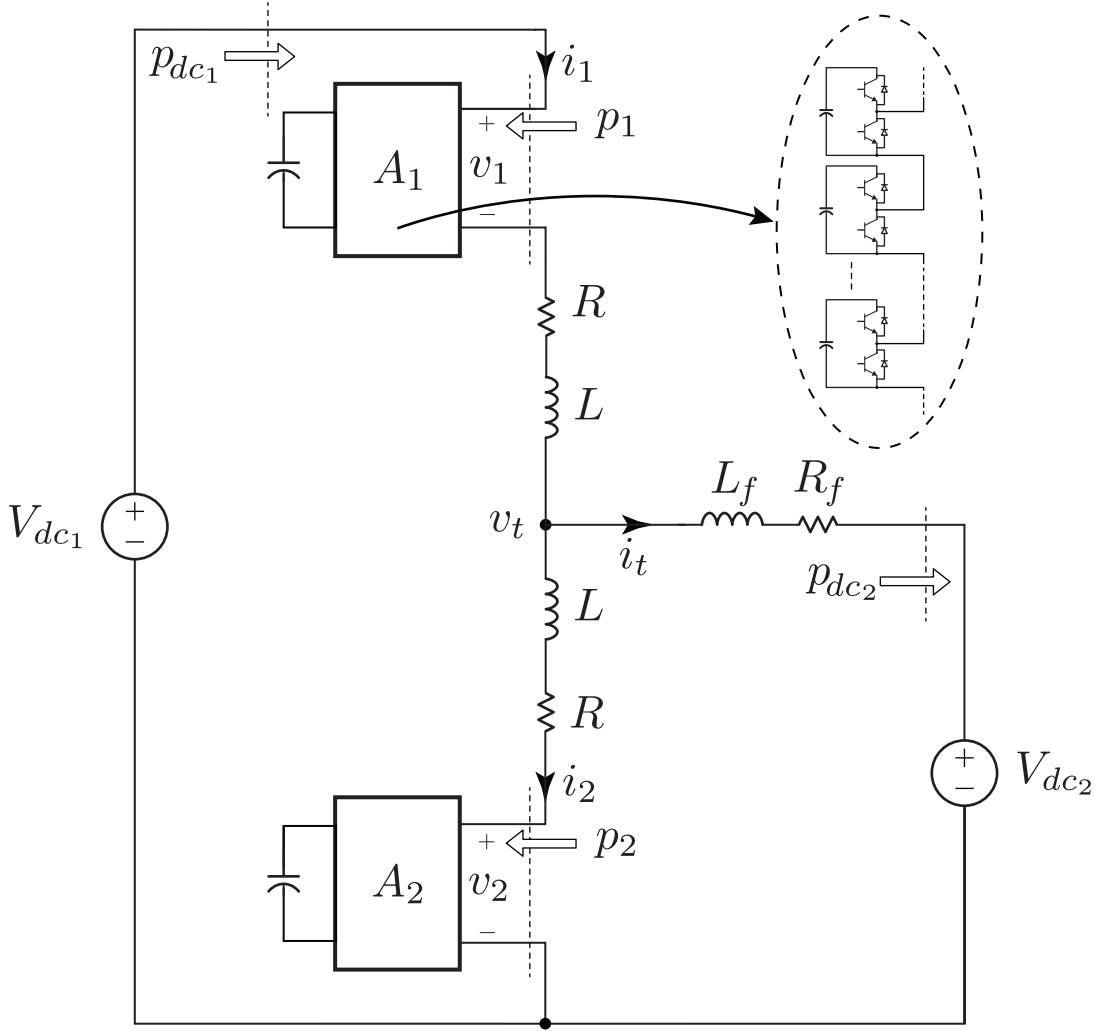
Figure 2.7: General MMC circuit considered for the analysis of Section 2.3. Note that A_1 and A_2 represent the strings of submodules in the upper and lower arm respectively.

general i_c and i_t can be AC, DC, or composite in nature depending on the application, and requirements for p_1+p_2 and $-p_1+p_2$. Therefore, in general the currents and voltages can be expressed as:

$$i_c = i_c^{dc} + i_c^{ac} \tag{2.24}$$

$$i_t = i_t^{dc} + i_t^{ac} \tag{2.25}$$

$$v_\Sigma = v_\Sigma^{dc} + v_\Sigma^{ac} \tag{2.26}$$

$$v_\Delta = v_\Delta^{dc} + v_\Delta^{ac} \tag{2.27}$$

Hence, (2.21) can be split into two equations; one for the AC components and the other for the DC components by substituting (2.24) into (2.21).

$$L\frac{di_c^{dc}}{dt} + Ri_c^{dc} = -\frac{1}{2}v_\Sigma^{dc} + \frac{1}{2}v_{dc_1} \tag{2.28}$$

$$L\frac{di_c^{ac}}{dt} + Ri_c^{ac} = -\frac{1}{2}v_\Sigma^{ac} \tag{2.29}$$

However, assuming that the converter operates in the quasi steady-state regime, and that the resistance R is small, the two terms on the left of (2.28), and the second term on the left in (2.29) can be neglected. So,

$$v_\Sigma^{dc} \approx v_{dc_1} \tag{2.30}$$

$$L\frac{di_c^{ac}}{dt} \approx -\frac{1}{2}v_\Sigma^{ac} \tag{2.31}$$

If L_f is chosen to be very large, it is fair to assume that i_t has a negligible AC component. The purpose of choosing L_f to be very large is to ensure that the current delivered to v_{dc_2} is approximately DC, since the MMC is to operate as a DC-DC converter. Therefore, the $\frac{di_t}{dt}$ term in (2.23) can be considered to be negligible, and since the resistance R is small, the entire left hand side of that equation can be neglected, and can be rewritten as:

$$0 \approx \frac{1}{2}v_\Delta^{dc} - \left(v_{dc_2} - \frac{v_{dc_1}}{2}\right) \tag{2.32}$$

$$v_\Delta^{dc} \approx 2v_{dc_2} - v_{dc_1} = (2d - 1)v_{dc_1} \tag{2.33}$$

where $d \triangleq \frac{v_{dc_2}}{v_{dc_1}}$ and is referred to as the voltage conversion ratio. Next, considering only the AC components of (2.20), it is clear that:

$$v_\Delta^{ac} = 2v_t^{ac} \tag{2.34}$$

since L_f suppresses the AC component of i_t. Having obtained expressions for the DC and AC components of the previously defined voltages and currents, it is possible to revisit (2.14) and (2.15) in order to obtain an expression that can relate the upper and lower arm powers to the voltages and currents. Based on (2.14),

$$\begin{aligned}
p_1 + p_2 &= \overline{v_\Sigma i_c} - \frac{1}{2}\overline{v_\Delta i_t} \\
&= v_\Sigma^{dc}i_c^{dc} + \overline{v_\Sigma^{ac}i_c^{ac}} - \frac{1}{2}v_\Delta^{dc}i_t \\
&= v_{dc_1}i_c^{dc} + \overline{v_\Sigma^{ac}i_c^{ac}} - \frac{1}{2}\left(2d - 1\right)v_{dc_1}i_t \\
&= v_{dc_1}i_c^{dc} - (d - 0.5)v_{dc_1}i_t + \overline{v_\Sigma^{ac}i_c^{ac}} \tag{2.35}
\end{aligned}$$

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Using the same procedure on (2.15),

$$
\begin{aligned}
-p_1 + p_2 &= \overline{v_\Delta i_c} - \frac{1}{2}\overline{v_\Sigma i_t} \\
&= v_\Delta^{dc} i_c^{dc} + v_\Delta^{ac} i_c^{ac} - \frac{1}{2}v_\Sigma^{dc} i_t \\
&= (2d-1)v_{dc_1} i_c^{dc} + \overline{v_\Delta^{ac} i_c^{ac}} - \frac{1}{2}v_{dc_1} i_t
\end{aligned}
\tag{2.36}
$$

Next, according to (2.31), it is clear that v_Σ^{ac} and i_c^{ac} are phased shifted by $90°$. Hence, the product $\overline{v_\Sigma^{ac} i_c^{ac}}$ in (2.35) will be equal to zero, and (2.35) can be reduced to

$$
p_1 + p_2 = v_{dc_1} i_c^{dc} - (d-0.5)v_{dc_1} i_t
\tag{2.37}
$$

Based on (2.37), if i_t is dedicated to controlling the output power (along with v_{dc_2}), then i_c^{dc} is the only variable that remains which can be used to control the sum of the upper and lower arm powers, $p_1 + p_2$. Since i_c^{dc} and i_t are both dedicated to controlling certain aspects of the converter, this means that the difference of the upper and lower arm powers, $-p_1 + p_2$, can only be controlled by the product of $\overline{v_\Delta^{ac} i_c^{ac}}$ as seen in (2.36). In order to make the control as effective as possible, it is necessary to ensure that v_Δ^{ac} and i_c^{ac} are cophasal, such that i_c^{ac} takes on the smallest possible value that it can so as to improve the efficiency of the converter [40]. Therefore, if

$$
\begin{aligned}
v_\Delta^{ac} &= 2v_m \cos(\omega t) \tag{2.38} \\
i_c^{ac} &= i_m \cos(\omega t) \tag{2.39}
\end{aligned}
$$

where v_m is the amplitude of the ac component of v_Δ, i_m is the amplitude of the ac component of i_c, and ω is the frequency of the two components, then

$$
\overline{v_\Delta^{ac} i_c^{ac}} = v_m i_m
\tag{2.40}
$$

and based on (2.34) this means that,

$$
v_t^{ac} = v_m \cos(\omega t)
\tag{2.41}
$$

With this expression, (2.33), (2.34), and (2.41) can be combined in order to obtain a complete expression for v_Δ as follows

$$
\begin{aligned}
v_\Delta &= v_\Delta^{dc} + v_\Delta^{ac} \\
v_\Delta &= (2d-1)v_{dc_1} + 2v_m \cos(\omega t)
\end{aligned}
\tag{2.42}
$$

Similarly, using (2.30), (2.31), and the fact that $i_c^{ac} = i_m \cos(\omega t)$, it is possible to obtain the following expression for v_Σ.

$$
v_\Sigma = v_{dc_1} + 2L\omega i_m \sin(\omega t)
\tag{2.43}
$$

Now, having obtained expressions for v_Σ an v_Δ in terms of the physical circuit elements from Fig. 2.7, the definitions of v_1 and v_2 can be revisited to be expressed as follows:

$$
\begin{aligned}
v_1 &= \frac{v_\Sigma - v_\Delta}{2} \\
&= \frac{v_{dc_1} - (2d-1)v_{dc_1}}{2} + L\omega i_m \sin(\omega t) - v_m \cos(\omega t) \\
&= (1-d)v_{dc_1} + L\omega i_m \sin(\omega t) - v_m \cos(\omega t)
\end{aligned}
\tag{2.44}
$$

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and employing a similar process for v_2

$$v_2 = dv_{dc_1} + L\omega i_m \sin(\omega t) + v_m \cos(\omega t) \tag{2.45}$$

Finally, by applying trigonometric identities v_1 and v_2 can be rewritten as

$$
\begin{aligned}
v_1 &= (1-d)v_{dc_1} - \sqrt{v_m^2 + (L\omega i_m)^2} \cos(\omega t - \alpha) \tag{2.46} \\
v_2 &= dv_{dc_1} + \sqrt{v_m^2 + (L\omega i_m)^2} \cos(\omega t + \alpha) \tag{2.47}
\end{aligned}
$$

where $\alpha = \tan^{-1}\left(\frac{L\omega i_m}{v_m}\right)$. Then, based on (2.46) and (2.47), it is clear that in general v_1 and v_2 both consist of an AC and DC component as explained in the beginning of this section. Hence, it can be said that the entire control of the MMC boils down to generating the correct values of v_1 and v_2, and therefore (2.46) and (2.47) are very important equations as they clearly show the behavior of the arm voltages. Therefore, by controlling v_1 and v_2, the currents i_c and i_t, the input and output power of the converter can also be controlled. Next, having dealt with the generation of the arm voltages, it is also important to understand how the zero net power balance condition ties into the operation of the system. Assuming that the net power in each arm is zero,

$$p_1 = p_2 = 0 \tag{2.48}$$

and as a result

$$
\begin{aligned}
p_1 + p_2 &= 0 \tag{2.49} \\
-p_1 + p_2 &= 0 \tag{2.50}
\end{aligned}
$$

Hence, applying the condition of (2.49) on (2.37),

$$
\begin{aligned}
0 &= v_{dc_1} i_c^{dc} - (d - 0.5)v_{dc_1} i_t \\
i_c^{dc} &= (d - 0.5)i_t \tag{2.51}
\end{aligned}
$$

Next, substituting (2.40) into (2.36) with the condition from (2.50) yields,

$$
\begin{aligned}
0 &= (2d-1)v_{dc_1} i_c^{dc} - \frac{1}{2}v_{dc_1} i_t + v_m i_m \\
-v_m i_m &= \left[(2d-1)i_c^{dc} - \frac{1}{2}i_t\right]v_{dc_1} \tag{2.52}
\end{aligned}
$$

And now substituting (2.51) into (2.52) and simplifying the result,

$$
\begin{aligned}
-v_m i_m &= \left[(2d-1)(d-0.5)i_t - 0.5i_t\right]v_{dc_1} \\
&= \left[2d^2 - d - d + 0.5 - 0.5\right]i_t v_{dc_1} \\
&= 2(d-1)i_t dv_{dc_1} \tag{2.53}
\end{aligned}
$$

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Finally, since $v_{dc_2} = dv_{dc_1}$ and $p_{dc_1} = p_{dc_2} = p_{dc}$,

$$
\begin{aligned}
-v_m i_m &= 2(d-1)p_{dc_2} \\
v_m i_m &= 2(1-d)p_{dc_2} \\
v_m i_m &= 2(1-d)p_{dc_1} \\
v_m i_m &= 2(1-d)p_{dc}
\end{aligned}
\tag{2.54}
$$

Since the polarity of the voltage is limited by the type of submodules used in the MMC, further restrictions can be imposed on v_1 and v_2. In this model, assuming that the submodules are composed of half-bridges means that v_1 or v_2 cannot be negative. Therefore, from (2.46) and (2.47) respectively,

$$
(1-d)v_{dc_1} \geq \sqrt{v_m^2 + (L\omega i_m)^2} \tag{2.55}
$$
$$
dv_{dc_1} \geq \sqrt{v_m^2 + (L\omega i_m)^2} \tag{2.56}
$$

By ensuring that $v_m = L\omega i_m$ one can alleviate the limitations imposed by these two expressions. As a result $\sqrt{v_m^2 + (L\omega i_m)^2} = \sqrt{2}v_m$ and,

$$
dv_{dc_1} \geq \sqrt{2}v_m \tag{2.57}
$$
$$
(1-d)v_{dc_1} \geq \sqrt{2}v_m \tag{2.58}
$$

Based on the conversion ratio, one of the two aforementioned constraints will become the bottleneck. For $d < 0.5$, (2.57) is the more restricting equation and when $d > 0.5$, (2.58) is more restrictive. Moving on, based on (2.54) and $v_m = L\omega i_m$,

$$
i_m = \sqrt{\frac{2(1-d)p_{dc}}{L\omega}} \tag{2.59}
$$

$$
v_m = \sqrt{(2L\omega)(1-d)p_{dc}}
$$

Next, it is possible to determine the upper limits placed on p_{dc} as a result of the previously derived restrictions for v_1 and v_2. Equations (2.57) and (2.60) will be used to determine the limit on the region where $d < 0.5$, while (2.58) and (2.60) will determine the limit on the power in the region where $d > 0.5$. For $d < 0.5$,

$$
\begin{aligned}
dv_{dc_1} &\geq 2\sqrt{L\omega(1-d)p_{dc}} \\
p_{dc} &\leq \frac{v_{dc_1}^2}{4L\omega}\frac{d^2}{1-d}
\end{aligned}
\tag{2.60}
$$

Similarly for $d > 0.5$,

$$
\begin{aligned}
(1-d)v_{dc_1} &\geq 2\sqrt{L\omega(1-d)p_{dc}} \\
p_{dc} &\leq \frac{v_{dc_1}^2}{4L\omega}(1-d)
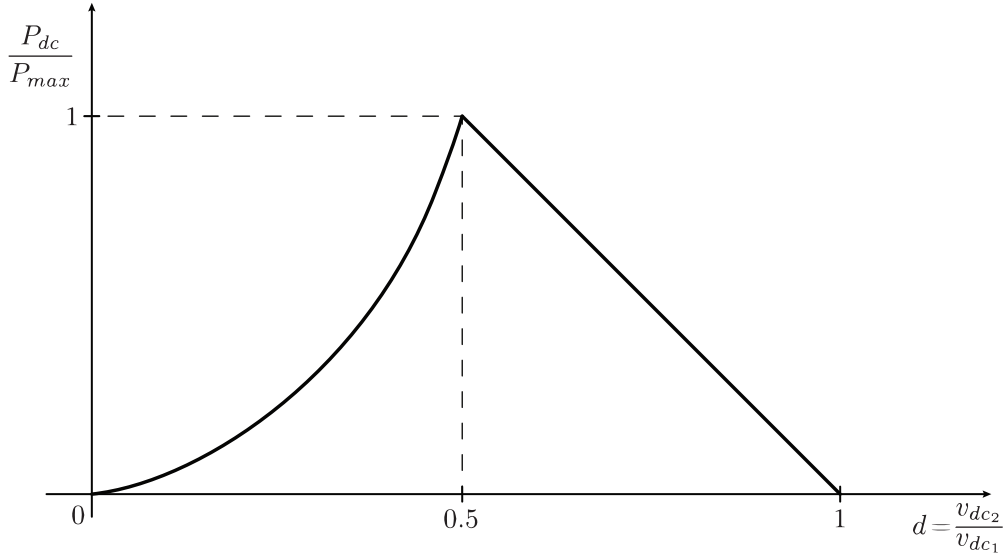\end{aligned}
\tag{2.61}
$$

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Figure 2.8: Variation of maximum achievable output power versus conversion ratio of the MMC.

Finally, at the boundary of these two regions, where $d = 0.5$, the power will be a maximum as seen in Fig. 2.8. Using either (2.60) or (2.61), and setting $d = 0.5$, the following expression for the maximum dc power can be obtained.

$$P_{max} = \frac{v_{dc_1}^2}{8L\omega} \tag{2.62}$$

A simple analysis of (2.60), (2.61), and (2.62) shows that the variation of the DC power with respect to the maximum achievable power varies as a quadratic for $d < 0.5$, and has a linear drop in the region with $d > 0.5$ after achieving a maximum at $d = 0.5$. This relationship can be seen in Fig. 2.8. In this section, the steady state characteristics of the MMC were developed using the mathematical model of the previous section. Having obtained expressions for the arm voltages, arm powers, input, and output powers, it is possible to utilize the dynamics of the system in order to put together a control scheme such that the parameters of interest can be controlled with precision. In the next section, the control of the different currents and powers will be presented.

2.4 Control

Since the fundamental behaviour of the MMC has been established with the set of equations produced in the previous sections, it is possible to present a process by which the converter can be controlled to abide by the zero net power balance and individual capacitor voltage regulation conditions. In this section, the control techniques utilized to ensure that the powers and currents can be controlled. In particular, the currents i_t, i_c will allow for the input and output power to be controlled, while the powers p_1 and p_2 will ensure that the arm power can be regulated. As a result, the powers internal and

external to the MMC can be controlled. The entire control flow for the converter can be seen in Fig. 2.9.

2.4.1 Output Current Control

If the output power that is delivered to the load is to be controllable, it must be ensured that the output current can be controlled. Based on the previous section, it was shown that the output power can be controlled through i_t. Therefore, the control of i_t is a good starting point when considering the various control loops that will be present in this converter. It was shown in Section 2.3 that the current i_t would have a negligible AC component due to the addition of L_f into the circuit. Thus, sticking with the assumption that i_t will have a purely DC component (or a negligible AC component) then the design of the controller for the current i_t becomes quite simple, as a PI controller is sufficient for this task. In general, the PI controller can be expressed as

$$K(s) = \frac{K_p s + K_i}{s} \tag{2.63}$$

where K_p is the proportional gain, and K_i is the integral gain. Since the plant is a single pole function, it is possible to use the pole-zero cancellation technique when designing the controller for i_t [49]. Therefore, if the control coefficients are chosen appropriately, the zero of the PI controller will cancel the pole of the plant, leaving behind an integrator with some constant gain.

In particular, the PI controller gains should be selected according to the following equations

$$\frac{K_p}{L} = \frac{1}{\tau_i} \tag{2.64}$$

$$\frac{K_i}{K_p} = \frac{R_e}{L_e + L_f} \tag{2.65}$$

where τ_i is the desired time constant of the closed loop system. Thus, the total inductance $L_e + L_f$ and resistance R_e must be known, along with the desired time constant of the response in order to accurately control the output current i_t. In a later section, the system parameters along with the final control parameters will be presented in detail.

2.4.2 Arm Power Control

Having presented techniques required to control the output power, the next step is to discuss the control of the arm powers. In Section 2.1, the zero net power balance concept was introduced and it was stated that in order to ensure that the MMC operates properly, the net power in the arms of the MMC must be equal to zero. To maintain regulation over the arm powers, the sum and difference of the powers p_1 and p_2 will be regulated according to (2.35) and (2.36). Since the MMC is to operate as a DC-DC converter, the powers that are of interest will be DC in nature. Therefore, the compensators used to control the arm powers can be quite simple in nature. The control becomes even simpler
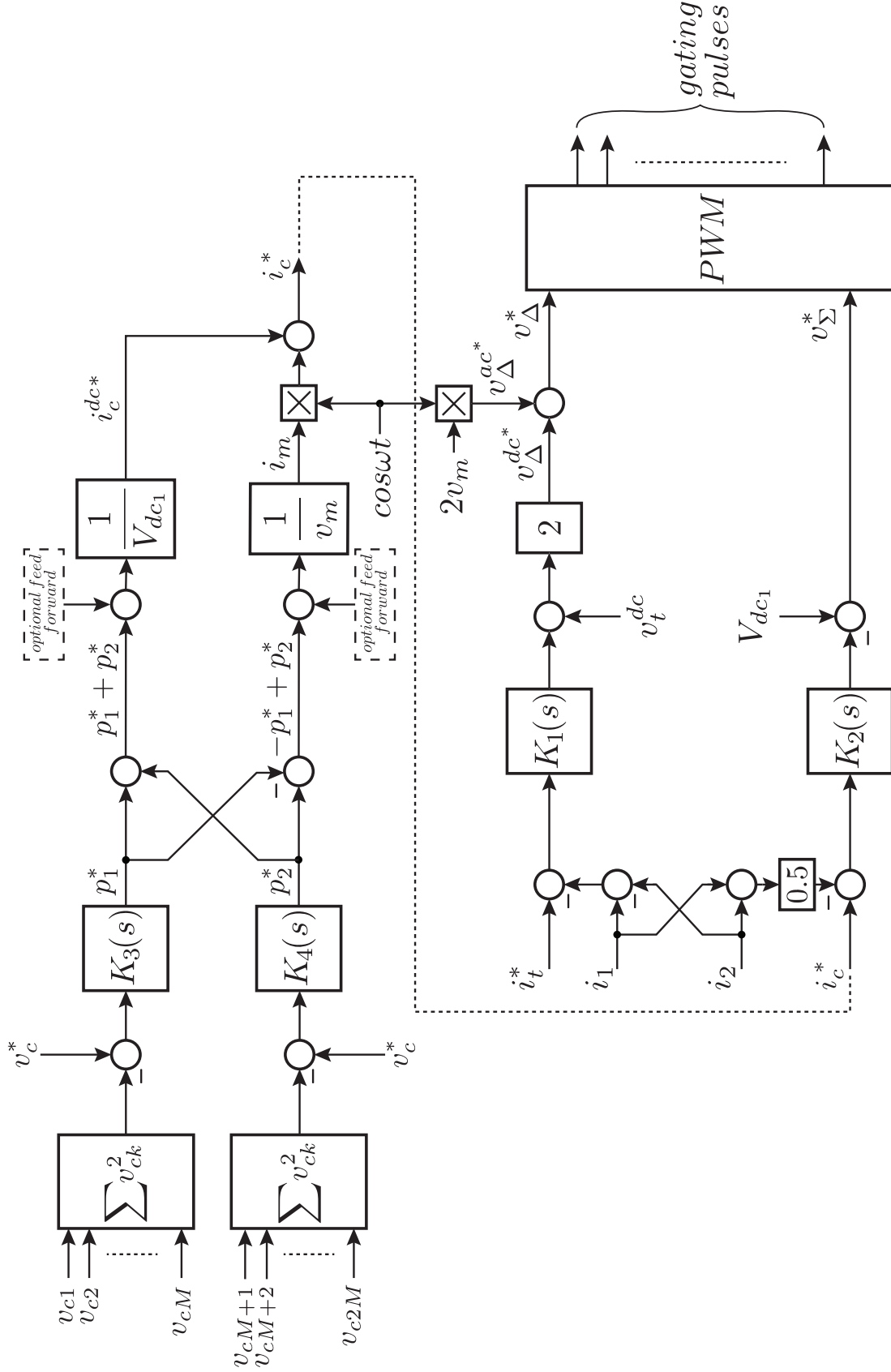
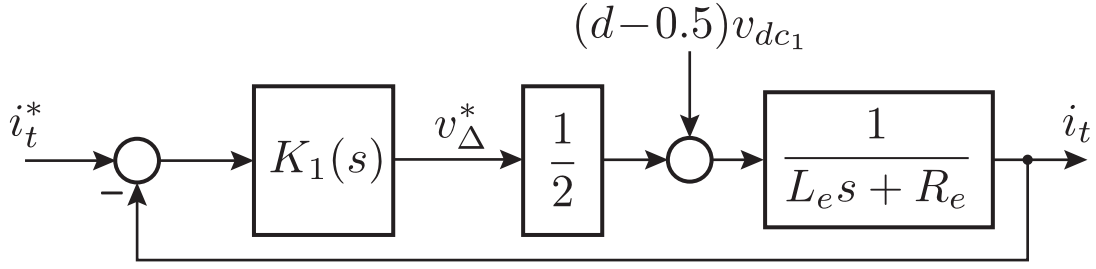Figure 2.9: Complete block diagram of the control flow for the MMC.

Figure 2.10: Block diagram representation of the closed loop system for i_t.

when one takes into account that the arm power is directly related to the energy of the capacitors, and that capacitors are inherently integrators. As such, the references for the arm powers can be generated using proportional compensators, since the integrator action can be applied by the capacitor. The control loop used to regulate the arm powers can be seen in Fig. 2.11. It is also worth mentioning that this control does not need to be very fast or accurate, as the PWM will also assist in adjusting the arm voltages such that the arm power is zero. So, since this dynamic of the converter is difficult to model, and does not need to be very accurate, it can be determined experimentally by trial and error.

As discussed in Section 2.3, (2.35) and (2.36) clearly show that the control of $p_1 + p_2$ and $-p_1 + p_2$ can be achieved by the DC and AC components of i_c respectively. Moreover, to achieve control of the input power, it is necessary to control the input current. Therefore, the next step in the converter control methodology is to control the current i_c such that the currents in the two arms, and therefore input current, can also be controlled. The theoretical approach to do so will be presented in the next section.

2.4.3 Input Current Control

In the previous section, the proposed method used to control the output power through the input power was presented. Since the input power must also be controlled, it is necessary to have a control loop for the input current. Rather than control the input current directly, it is possible to control the common mode current i_c, such that the two arm currents can also be controlled. The result of this is that the input current is also controlled. Thus, based on the definitions of the mathematical model, it is possible to control all of the currents present in the converter by controlling i_t and i_c.

As defined previously, i_c is defined as the average of the arm currents i_1 and i_2. It is also known that in general, the arm voltages can be DC, AC, or some composite of the two. Therefore, it is fair to conclude that the arm currents will also in general be DC, AC, or some composite form based on the arm voltages. As such, the control of i_c will be a little more complicated than i_t, since the arm currents will not be purely DC. Again, using the approach in [49], it is possible to design a control transfer function that will be capable of tracking a step and/or sinusoidal command. According to [49], a compensator that is capable of performing these tasks will require the following:
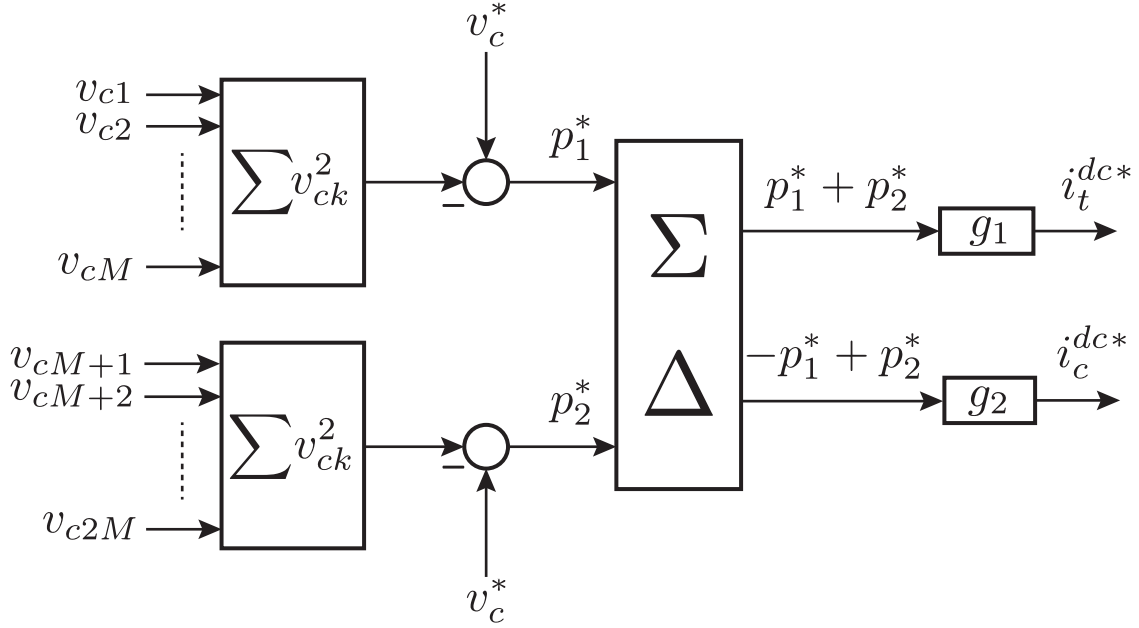
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Figure 2.11: Block diagram representation of the control path used to regulate the arm powers p_1 and p_2.

- A closed loop bandwidth that is much larger than (ie. 10 times larger than) the frequency of the sinusoid to be tracked.

- A large loop gain at the frequencies to be tracked. In this case, DC and the frequency of the sinusoid.

- A reasonably large phase margin at the crossover frequency. Crossover frequency should be chosen such that $\omega_c < \omega_b < 2\omega_c$, where ω_c and ω_b are the crossover frequency and closed-loop bandwidth, respectively in rad/s.

- A unity closed-loop gain at the frequency of the sinusoid to be tracked.

As long as these requirements are met the compensator will be able to track a step command, and/or a sinusoidal command without any issues. In order to design a compensator, the plant seen in Fig. 2.6 will be used based on the modelling of the Section 2.2 in one of the following sections. Fig. 2.12 illustrates the closed loop control diagram for the input current. In this section the requirements of the input current controller were presented. The next control loop to be discussed is that of the arm powers to ensure that both p_1 and p_2 can be regulated to maintain the zero net power balance. In the following section, all of these concepts will be tied together in order to present an in-depth design procedure for each controller in the form of a specific numerical case study.
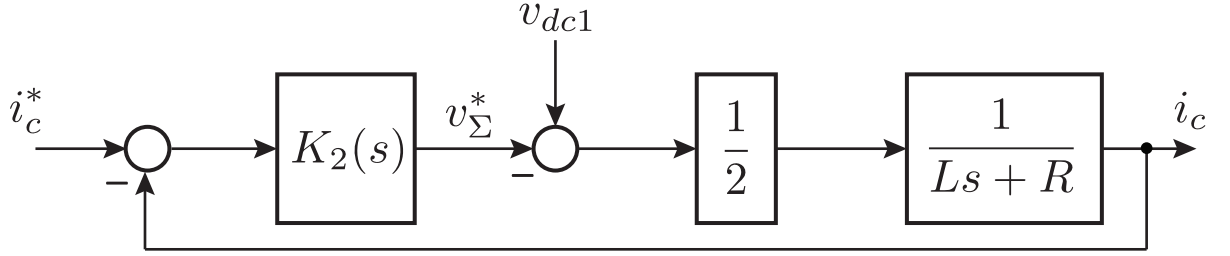
24

Figure 2.12: Block diagram representation of the closed loop system for i_c.

2.5 Multilevel Synthesis of Arm Voltages

So far the entirety of the discussion on modelling and control has been carried out with the assumption that each arm voltage is a single controllable voltage source, and at no point during the analysis was there any restriction on how the arm voltages were generated. It was mentioned that the controllable voltage source was an accurate model to use, so long as the zero net power balance could be achieved along with regulation on the individual submodule capacitor voltages. In essence, the converter is indifferent to how the arm voltages are generated. All that is required is that they are generated and have the characteristics described by (2.46) and (2.47). Now, since the converter is of a multilevel topology, it is necessary now to transition from the simplified discussion of two voltage sources, to two strings of submodules. That is, this section will discuss how the analysis and modelling carried out previously can be realized using a multilevel converter. In order to carry out a successful translation from the simple two level case to the multilevel system, the generation of the gating pulses through a modulation scheme, as well as the regulation of the individual capacitor voltages are two points that must be discussed. But first, it should be noted that the submodules will be half-bridge submodules and the implications of the half-bridge submodule on the generation of the gating pulses will be explored in the following section where the PWM technique is discussed in detail.

2.5.1 Phase-Shifted Pulse Width Modulation (PS-PWM)

In Section 2.1, it was discussed that the semiconductor devices must be switched according to specific timings in order to produce the desired output voltages. A typical method to generate these timings is PWM. In the simplest class of PWM, a single carrier is compared with a reference and the instances in time where the two intersect correspond to rising edges (or falling edges depending on the polarity of the comparison) of the gating pulses. These pulses are then applied to the semiconductor devices, causing the devices to change states. However, in the case of a multilevel converter the number of carriers must be increased, as there are multiple cells of semiconductor devices that must be switched. Such PWM techniques are classified as multicarrier PWM techniques.

One such technique is referred to as the Phase-Shifted Pulse Width Modulation, where instead of a single carrier with a single reference, there are multiple phase shifted carriers being compared with a single reference. The phase shift between adjacent carriers ϕ is set such that

$$\phi = \frac{2\pi}{M} \tag{2.66}$$

where M is the number of submodules in a converter arm. The main benefit of using this method in a multilevel converter is that each carrier can be assigned to a specific submodule. Hence, the gating pulses for every submodule will all have the same shape, but will be phase shifted depending on the phase shift of the carrier that generated said gating pulses. This means that the output voltage of a string of M submodules being driven by a PS-PWM scheme is a pulse train with M times the frequency of the individual carriers in the case of a DC reference. If the reference is not purely DC, then the resulting waveform may be more elaborate depending on the modulation index.

In general, M submodules will require M carriers all phase shifted by $\frac{2\pi}{M}$. But first, it is important to understand how the modulating signal interacts with these carriers when considering half-bridge submodules. Since the submodules are half-bridges, then the output voltage of the submodule (and thus string of submodules) can never be negative. Therefore, it is logical to assume that the carriers will run from 0 to 1, meaning that the modulating signal must also be normalized such that it runs from 0 to 1. Such a normalization requires that

$$m = \frac{v_{SM}^*}{V_{c_n}} \tag{2.67}$$

where m is the modulation index, v_{SM}^* is the voltage command to be generated by the PWM, and V_{c_n} is the voltage on the capacitor of a given submodule. As seen in (2.51) and (2.54), v_1 and v_2 have both a DC and AC component. This means that the resulting modulating signal can also have a DC and AC component. Hence, the modulation index can be represented more accurately as a time varying function $m(t)$ as follows,

$$m(t) = m^{dc}(t) + m^{ac}(t) \tag{2.68}$$

where $m^{ac}(t) = \hat{m}cos(\omega t)$. Furthermore, one must take into account that this voltage command will actually be some fraction of the overall arm voltage since the command is being given to a fraction of the arm. Therefore the kth submodule must be given a setpoint such that,

$$v_{SM_k}^* = \frac{v_j^*}{M} \tag{2.69}$$

where $j(= 1 \text{ or } 2)$, corresponds to the upper and lower arms respectively, and $k(= 1, 2, ..., 2M)$ corresponds to the index of the submodule in question. The result is that the desired arm voltages v_1 and v_2 will be scaled down according to the number of submodules and voltages on the submodule capacitors and generated at the submodule level, thus achieving the desired multilevel synthesis. The main benefit of the PS-PWM technique over other multi-carrier techniques such as level-shifted PWM and nearest level modulation techniques is the fact that each submodule will be switched equally. Since every carrier will coincide with the reference (with a phase shift) in the same fashion

regardless of the magnitude of the reference, there is no need to implement additional sorting algorithms for the selection of submodules. The fact that each carrier can be assigned directly to a submodule eliminates the need for additional selection algorithms [50].

For instance, if the nearest level modulation technique is to be used to generate a 200-V voltage, using a string of five capacitors whose voltages are regulated at 50 V, then only four capacitors need to be inserted. However, the selection of which capacitors need to be inserted at any given time requires an additional layer of complexity. On the other hand, if using the PS-PWM technique, all five capacitors can be inserted all the time, but the modulation index can be adjusted to $200/250 = 0.8$, and every submodule will be given a command of $40V$. Hence, there is no need for a selection algorithm. Still, it should be noted that as the number of levels increases, the PS-PWM technique becomes uneconomical as the number of required carriers increases as well, thus increasing the computational complexity of the modulation scheme. Despite the benefits of the PS-PWM technique, the individual capacitor voltages still need to be regulated, as equal switching does not guarantee that the capacitor voltages will be held at an equal magnitude. While the means by which the gating pulses are generated was discussed in this section, the regulation of individual capacitor voltages will be discussed in the following section.

2.5.2   Capacitor Voltage Balancing

In order to maintain and ensure stable operation of the MMC, the individual submodule capcitor voltages as well as the overall capacitor energy in each arm must be regulated. In this section, the methodology used to regulate the individual submodule voltages will be explored. While there are a number of different techniques including the Tolerance Band Method and Predictive Sorting Method [1], the individual submodule voltages can be regulated in a much simpler fashion if the PS-PWM technique is used [51]. Since PS-PWM allows for individual submodules to be assigned carriers directly regardless of their voltage, the submodule voltages can be regulated directly using a simple proportional control. It should be noted that integral action is not required since the capacitors themselves are integrators. When it comes to the regulation scheme, first consider the submodule of Fig. 2.13. For individual regulation of the capacitor voltages, the capacitor voltage is first compared with its setpoint to determine the error associated with the capacitor voltage.

$$e_{ck} = v_c^* - v_{c_k} \tag{2.70}$$

Next, this error is multiplied with a proportional gain K_{cap} and further multipled by the sign of the arm current (to distinguish whether the capacitor is charging or discharging) that flows through the submodule. This product will result in what will be referred to herein as the reference offset, δ_k. Mathematically,

$$\delta_k = e_{ck} K_{cap} sgn(i_k) \tag{2.71}$$

where e_{ck}, K_{cap}, and i_k are the error between the setpoint and measured capacitor voltage, proportional gain of the local regulation scheme, and current entering the kth submodule,
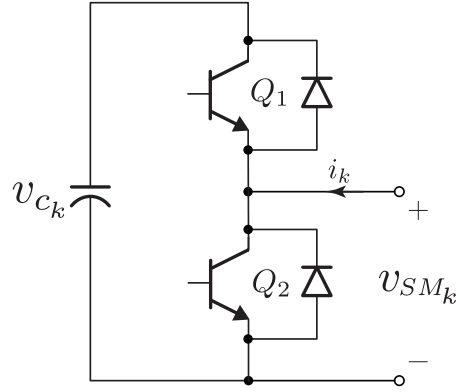
Figure 2.13: The kth submodule considered for the purpose of submodule capacitor voltage regulation.

respectively. The reference offset is then added to the previously generated reference voltage v_{SM}^* from the command given for the arm voltage,

$$v_{SM_k}^{*'} = v_{SM}^* + \delta_k \tag{2.72}$$

Finally, the modulation index m_k is generated by dividing this new submodule reference by the nominal capacitor voltage V_{c_n}

$$m_k = \frac{v_{SM_k}^{*'}}{V_{c_n}} \tag{2.73}$$

Graphically, this procedure can be seen in Fig. 2.14. The net effect is that the offset created by the local capacitor regulation will adjust the duty cycle of the PWM, such that the capacitor charges or discharges to maintain a fairly constant voltage with some small amount of ripple.

Having provided a means by which the arm voltages can be generated using a multi-level topology, along with the control technique used to regulate the capacitor voltages, the following section will present a numerical case study which will tie all of the concepts discussed thus far into a practical example.

2.6 A Numerical Case Study

So far all of the analysis and modelling has been done by in an algebraic form considering a generic system. This section will present an in-depth look at the selection of the various components, such as supply voltages and arm inductances, involved in the MMC. Then, based on these components the required compensator functions for the input, output, and arm powers will be developed based on analytical approaches. Finally, a summary of the system will be presented.
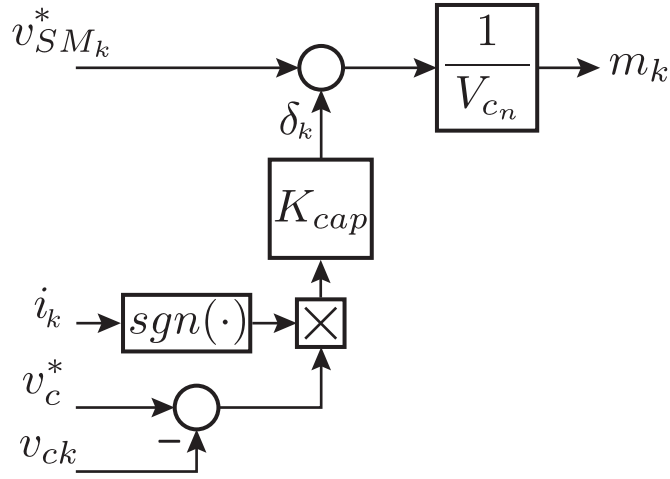
Figure 2.14: Block diagram representation of the control path used to regulate the arm powers p_1 and p_2.

In order to prototype the converter, the equipment that was available in the lab was considered. In order to ensure the maximum amount of power was transferred, the voltage conversion ratio was set to 0.5 according to Fig. 2.8. The maximum stable voltages in the lab that were achievable were 240 V for v_{dc_1} and 120 V for v_{dc_2}. Then, supposing that a maximum power of 1 kW is to be transferred, the inductance of the output filter L_f can be calculated based on the desired operating conditions. First, it is important to note that regardless of the inductance, there will always be some ripple on the output current. The calculation of L_f should therefore aim to minimize this ripple, while also bearing in mind that there is a trade-off between minimizing the current and the size of the output filter. That is, decreasing the ripple requires that L_f is increased. If $v_{dc_2} = 120$ V and the maximum power that will be transferred by this converter is 1 kW, then the maximum output current will be 8.33 A. Next, suppose that a ripple of 5% is acceptable on the output current, that is, a peak ripple of about 0.4 A. Then, based on (2.41), and the fact that $v_m = L\omega i_m$,

$$v_t^{ac} = i_t^{ac}(L_e + L_f)\omega \tag{2.74}$$

But since it is expected that L_f will be much larger than L_e, then L_e is negligible for this calculation and L_f can be calculated directly using (2.74) if L_e is set to 0. Before doing so, the selection of ω is worth commenting upon as the frequency at which the converter operates is a key characteristic. It was desired that the frequency not be too low so as to avoid low frequency disturbances in the system. At the same time, increasing the frequency substantially would increase the losses in the converter and could also potentially create unwanted noise in the system, while also increasing the required AC component of the arm voltages as seen in (2.46) and (2.47). Hence, 400 Hz was chosen as a suitable frequency for all of these requirements. Choosing ω to correspond to a frequency of 400 Hz meant that L could be calculated based on (2.62). Doing so results

in $L = 2.5mH$. Next, (2.60) can be used along with the newly determined parameters in order to calculate the expected AC component of v_t under the operating conditions.

$$
\begin{aligned}
v_t^{ac} &= \sqrt{2(1-d)P_{dc}L\omega} \\
&= \sqrt{2(1-0.5)(1200)(2.5 \times 10^-3)(2513)} \\
&= 86.8 \ V
\end{aligned}
$$

Therefore, the AC component of v_t will have an amplitude of 86.8 V. Finally, using the fact that a ripple of 5% is acceptable on i_t, (2.74) can be used along with $v_t = 86.8 \ V$ to calculate the inductance of the filter L_f,

$$
\begin{aligned}
L_f &= \frac{v_t^{ac}}{i_t^{ac}\omega} \\
&= \frac{86.8}{0.4 \times 2513} \\
&= 86 \ mH
\end{aligned}
$$

Due to the availability of components in the lab, L_f was chosen to be 85 mH instead. Finally, the switching frequency f_{sw} can be chosen in order to ensure that the Nyquist rate condition is satisfied by some reasonable amount. For a 400 Hz sinusoid, a switching frequency, f_{sw}, of 16 kHz is more than sufficient, as it is 40 times larger than the modulating signal. Moreover, the switching frequency of 16 kHz was chosen to ensure that there would not be any issues with the hardware when it came to sampling. The resulting system has been summarized in Table 2.1.

Table 2.1: Summary of converter parameters used in the PSCAD simulation.

Parameter	Value
v_{dc_1}	240 V
v_{dc_2}	120 V
L	2.5 mH
L_f	85 mH
R	0.06 Ω
ω	2513 rad/s
f_{sw}	16 kHz

Given this set of parameters, the control techniques described in Section 2.4 can be employed for the output, input, and arm powers of the MMC. The following sections will outline the procedure as well as show the relevant step and frequency responses of the designed compensators.

2.6.1   Output Current Controller Design

As discussed in Section 2.4.1, the output current can be controlled with a PI compensator in which the pole of the plant will be made to cancel the zero of the compensator. By
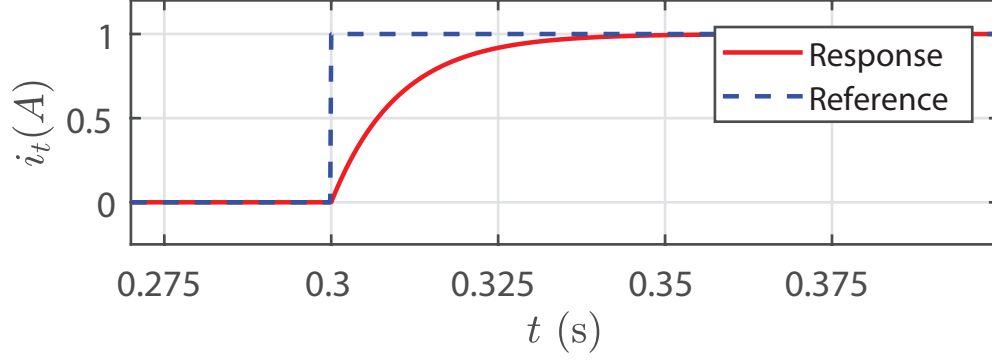
Figure 2.15: Step response of i_t using the gain parameters $K_p = 8.625$ and $K_i = 6.25$

choosing the appropriate gains K_p and K_i, it is possible to create a compensator that will respond in a reasonable amount of time, with minimal error. Using the parameters chosen for the system above, along with a desired time constant of 10 ms, and approximating the value of R_e to be 62.5 $m\Omega$ (based on datasheets and simple lab measurements), (2.64) and (2.65) can be used to determine the PI gains. In doing so, it can be found that $K_p = 8.625$ and $K_i = 6.25$, meaning that the resulting compensator function is

$$K_1(s) = \frac{8.625s + 6.25}{s} \tag{2.75}$$

In order to validate the choice of these parameters, a simple MATLAB simulation was put together to observe the behaviour of the step response of the closed loop system seen in Fig. 2.10. The resulting step response can be seen in Fig. 2.15.

As seen in Fig. 2.15, the step response follows the first order characteristics that are expected, as well as the desired time constant of 10 ms. Next, the design of the input current controller will be elaborated upon.

2.6.2 Input Current Controller Design

In Section 2.4.3, the requirements of a compensator that can track both a step and sinusoidal command were discussed. In this section, a compensator which fulfills all of the requirements presented in Section 2.4.3 will be presented based on the procedure in [49]. The first parameter to be designed for is the closed-loop bandwidth of the system. Since the frequency of the sinusoid that is to be tracked is 400 Hz, the closed-loop bandwidth of the system should be much greater than 2500 rad/s. Then, it is required that the open loop gain at the frequency to be tracked (in this case 2500 rad/s) is very large. Theoretically, the frequency of the signal is 400 Hz. However, if this system is to be practically implemented at some point, then the frequency may deviate slightly from the desired value and as a result the overall system may become unstable. In order to prevent such issues, the compensator can be damped around 2500 rad/s. Thus, following the process in [49], a compensator with the following transfer function can be created to meet these requirements.

$$K_2(s) = \frac{13.21s^4 + 1.77 \times 10^7 s^3 + 1.20 \times 10^{11} s^2 + 1.21 \times 10^{13} s + 1.12 \times 10^{16}}{s^4 + 4.74 \times 10^4 s^3 + 1.12 \times 10^7 s^2 + 2.89 \times 10^{11} s + 3.66 \times 10^{14}} \tag{2.76}$$
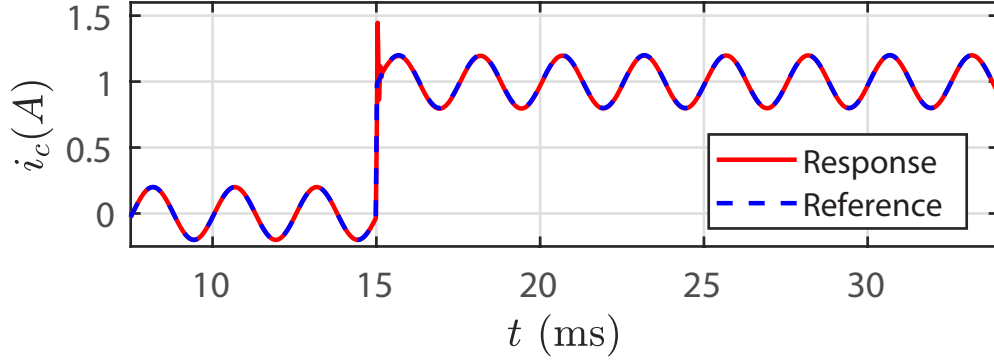
31

Figure 2.16: Step response of the compensator expressed by (2.76)

It should be noted that although the compensator was determined based on the process in [49], the result was slightly tailored in MATLAB in order to obtain a better response. The corresponding frequency response for this compensator can be seen in Fig. 2.17, and the frequency response of the closed loop system can be seen in Fig. 2.18. Furthermore, Fig. 2.16 shows the step response of i_c for the closed loop system of Fig. 2.12 from a MATLAB simulation. Clearly, the system is able to track both the sinusoidal and DC component without any issues.

According to the frequency response of the closed loop system, the system has a bandwidth of 1.225×10^5 rad/s corresponding to approximately 19.5 kHz, which is more than sufficient to be able to track the 400 Hz signal. Based on these frequency responses, it is clear that the requirements of the input current controller listed in Section 2.4.3 have all been met.

2.6.3 Arm Power Control

Having designed the controllers for the input and output powers, the last controller to be designed is the arm power controllers. Based on the discussion in Section 2.4.2, these controllers are simple proportional gains due to the fact that the arm power does not need to be controlled precisely, and that the capacitors are inherently integrators. Thus the gain parameters are determined experimentally since the development of the model for the arm powers is cumbersome and unnecessary.

2.6.4 Discretization of Control Parameters

Finally, since the control algorithm will be implemented using an FPGA, the converter model must be discretized along with the compensator functions. Since the frequency of

the sinusoidal component in the converter will be $400\ Hz$, a switching frequency of $16\ kHz$ was selected. Thus, the sampling rate of the discretization was chosen to be twice that of the switching frequency, that is, $32\ kHz$, and the assumption is that the effects of aliasing do not exist under these conditions. In order to simplify the process, the compensators designed in the previous section were simply converted to their discrete counterparts using the Tustin method in MATLAB as opposed to designing discrete compensators from scratch using discrete plants. The resulting discretized compensators for i_t and i_c can be seen in (2.77) and (2.78) respectively.

$$K_1(z) = \frac{8.625z - 8.625}{z - 1} \tag{2.77}$$

$$K_2(z) = \frac{182.6z^4 - 346.6z^3 + 11.82z^2 + 286.1z - 133.8}{z^4 - 3.141z^3 - 3.436z^2 - 1.445z + 0.149} \tag{2.78}$$

Hence, these two control functions will be implemented in the experimental setup as part of the digital control scheme in the experimental setup.

In this chapter, the principles of operation, mathematical modelling, steady state characteristics, control techniques, and multilevel synthesis of the MMC were all explored in detail, along with a numerical study of the parameters to be used in the practical system. This chapter will serve as the foundation on which the remainder of this thesis rests, as it provides insight into the operation and behaviour of the overall circuit, while also providing the details of the parameters for a practical converter. In the following sections, the system will be implemented first in a simulation, and then in a practical system where all of the concepts discussed in this chapter will be put to the test in a fully functional converter.
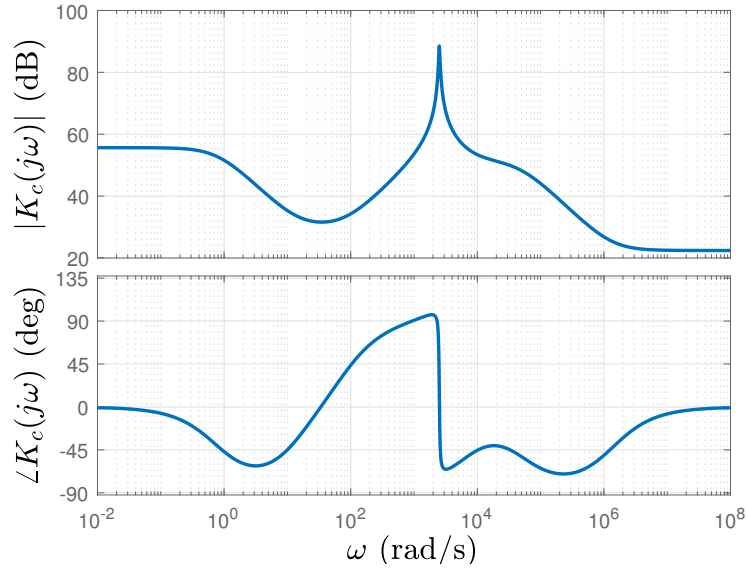
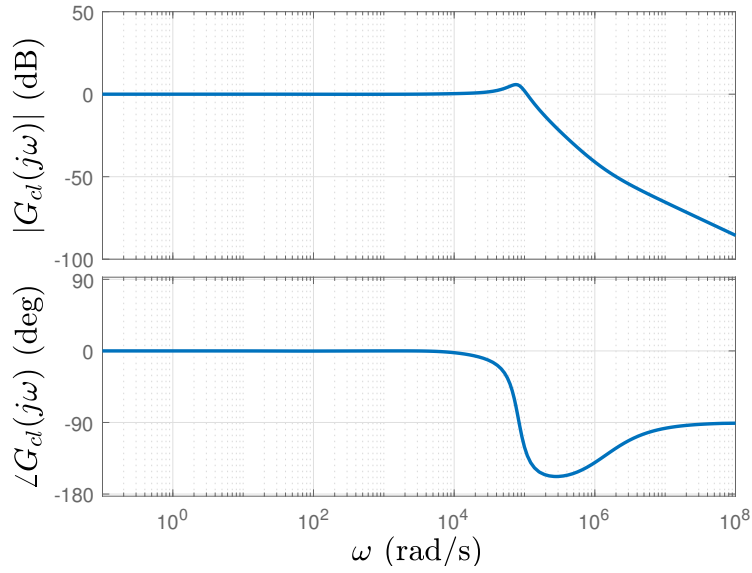Figure 2.17: Frequency response of the compensator expressed by (2.76)

Figure 2.18: Frequency response of the closed loop system using the compensator from Figure (2.17).

Chapter 3

Software Simulation of MMC

In the previous chapter, the theoretical foundation of the MMC was introduced along with a numerical case study based on a practically realizable system. In this chapter, the system designed in Section 2.6 will be simulated using PSCAD. Since the switching frequency of the system is 16 kHz, the solution time step used in this simulation was 0.25 μs while the plot step was 1 μs in order to maintain a fine resolution. The details of the physical system used in this simulation were presented in Table 2.1.

First, it is necessary to outline a set of test conditions such that the simulation can be thorough and insightful. In Section 2.1, it was stated that the MMC requires the net power in the arms to be zero, as well as the individual capacitor voltages to be regulated in order to operate correctly. Therefore, throughout all of the tests, the arm powers p_1 and p_2, as well as the capacitor voltages will be a main focus. Moreover, the regulation of these powers and capacitors requires regulation on the currents i_t and i_c, therefore the responses of these two currents are also of importance. Hence, the simulation process will consist of the following steps:

1. Selection of the desired output power level, P_{dc_2}.

2. Adjustment of v_m, if necessary, to ensure that the condition of (2.54) is satisfied.

3. Setting of the output current i_t to the required current to achieve the desired output power according to (2.62).

4. Observation of the desired quantities and their waveforms.

This process can be repeated as many times so long as the desired output power abides by the restriction of (2.62). In order to test the complete functionality of the MMC, the test process carried out in this section will observe the MMC under five different test cases. In particular, the MMC will first operate with an output current command of 0, corresponding to zero output power. Then, a step input will be applied to the output current which corresponds to approximately 480 W of power (ie. approximately 50% maximum power) and the transient response will be observed. Next, the steady-state characteristic of the MMC will be observed at 480 W. Then, the output current will be increased by a step input to the ultimate target of 1 kW, while the transient and following steady-state characteristics will be observed. A summary of the simulation test

cases can be seen in Table (3.1). The results for each of these cases will be presented in the remainder of this chapter. Before any simulation tests took place, a start-up procedure

Table 3.1: Summary of cases according to operating conditions.

Case	$i_t(A)$	$P_{dc_2}(W)$	$v_m(V)$
1	0	0	55
2	0 to 4	0 to 480	55
3	4	480	55
4	4 to 8.33	480 to 1000	55 to 80
5	8.33	1000	80

took place in which all of the submodule capacitors were pre-charged to the desired operating point of 55 V. This was done by connecting a voltage source in parallel with the capacitors through a breaker. After a small fraction of a second, the breakers were opened one by one until eventually the system was allowed to regulate itself entirely. The submodule capacitor voltage was selected as a result of (2.46) and (2.47). In essence, when all of the submodules are active, they are connected in series, which means their voltages will be added together. Thus, it is required that the submodule capacitor voltages should be able to achieve a level larger than the maximum values of v_1 and v_2. Using (2.46) and (2.47), the maximum value of the arm voltage v_2 can be determined as follows by assuming $v_{dc_1} = 240V, d = 0.5, v_m = 86.6V, i_m = 11.52A, L\omega = 2\pi$:

$$v_2 = dv_{dc_1} + \sqrt{(v_m)^2 + (L\omega i_m)^2} \tag{3.1}$$
$$= (0.5)(240) + \sqrt{86.8^2 + (2\pi \times 11.52)^2} \tag{3.2}$$
$$= 233.01V \tag{3.3}$$

Since v_1 and v_2 are practically identical (except for a phase shift) for the case when $d = 0.5$, then it is expected that v_1 will also have the same maximum value. Thus, by choosing the capacitor voltage to be 55 V, a string of 5 submodules can provide a maximum voltage of 275 V, which is sufficient to generate 233 V using PWM. Furthermore, it should be noted that only the waveforms of the output current have been included since the output power will have the exact same shape, but will be scaled by a factor of v_{dc_2}.

3.1 Case 1: Steady state with $i_t = 0$

In this case, the MMC has undergone the start-up procedure and is running with a current setpoint of 0. The capacitors have been pre-charged to 55 V. Since the output current is zero, the arm powers are also zero. As seen in Fig. 3.1, the currents are both practically zero corresponding to the desired steady-state condition. Next, in this region it is important to observe the arm powers to ensure that p_1 and p_2 are indeed zero. The arm power waveforms can be seen in Fig. 3.2. While the regulation requires that both of these powers be zero, this waveform does not show such a characteristic. Still, if the simulation is allowed to run for an extended amount of time, it can be seen that the
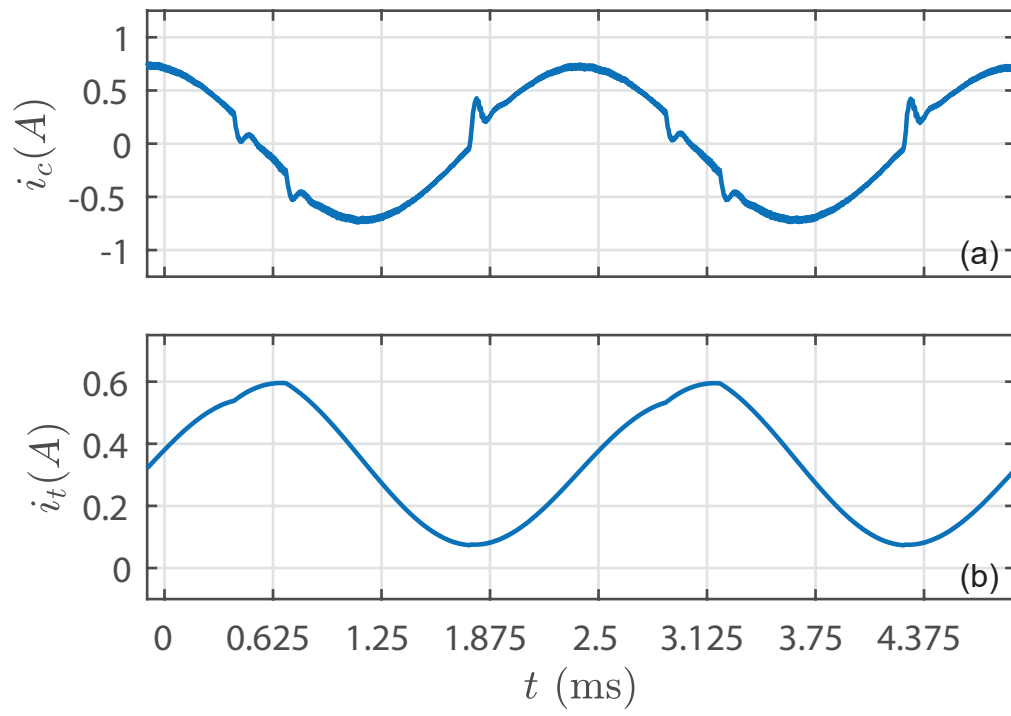
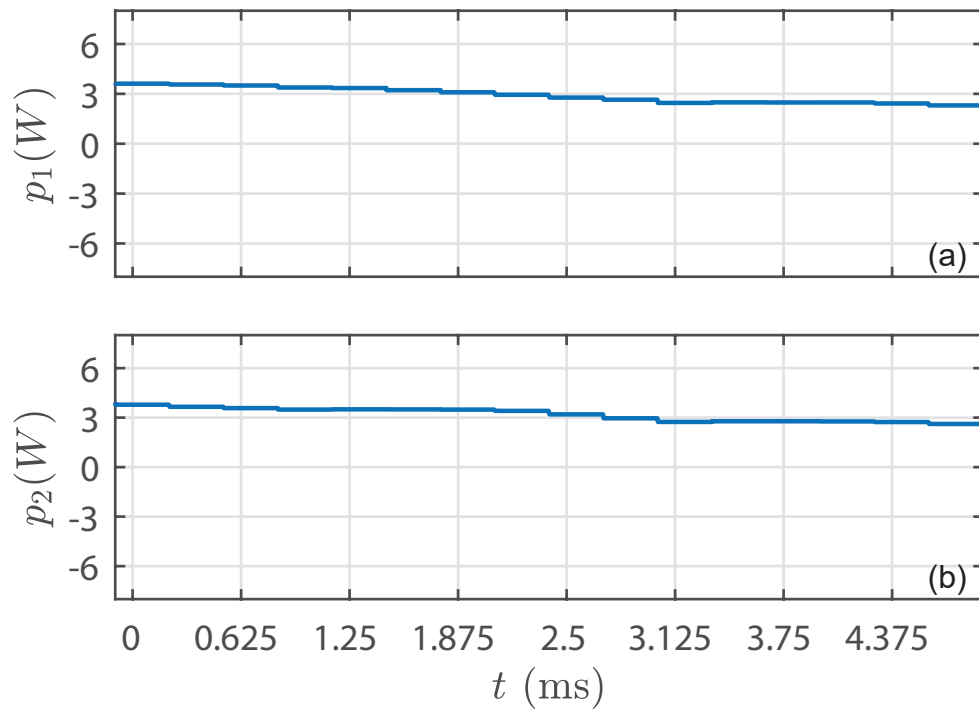Figure 3.1: Steady-state current waveforms: (a) i_c and (b)i_t for Case 1.

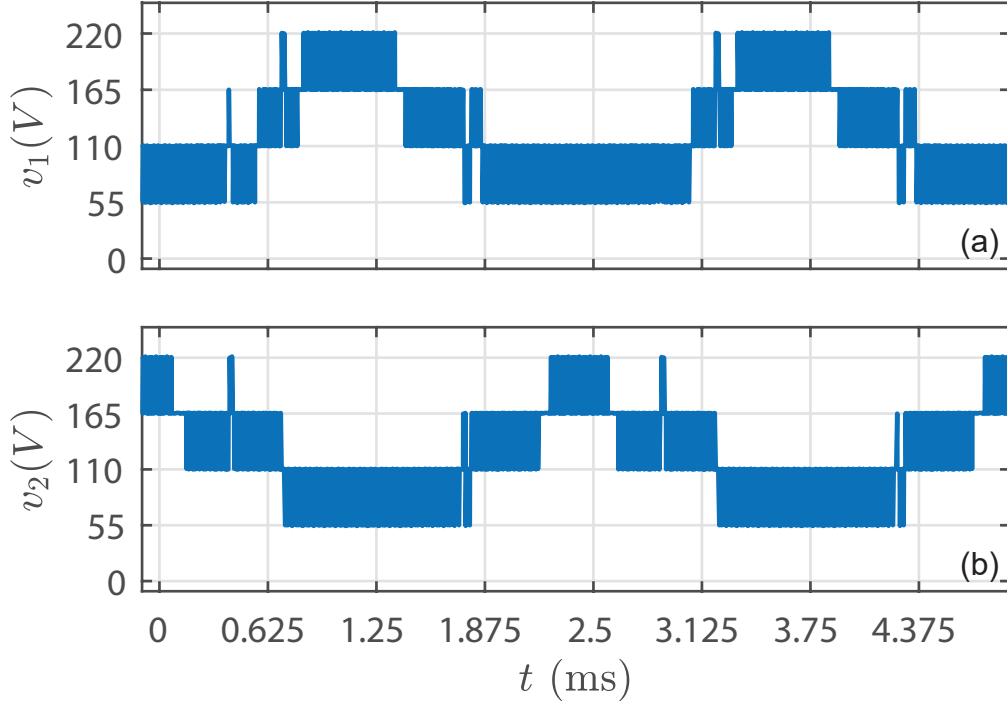Figure 3.2: Steady-state arm power waveforms: (a)p_1 and (b)p_2 for Case 1

Figure 3.3: Steady-state arm voltage waveforms: (a) v_1 and (b) v_2 for Case 1.

powers do indeed settle at 0 as expected. However, due to the start up procedure outlined above, the system was still settling to a state of zero power when this data was captured, and increasing the duration of the simulation resulted in memory errors. Next, the arm voltages can be seen in Fig. 3.3. The voltage waveforms show the expected discrete steps equal to the capacitor voltages, and the desired frequency of $400\ Hz$, corresponding to a period of $2.5\ ms$. At this point, v_m was set to $55\ V$ according to (2.62) and so the amplitude of the AC component on both arm voltages is small since i_t is zero, and therefore i_m is very small.

Finally, the individual capacitor voltages should be regulated at their setpoint of 55 V. It is expected that there will be some fluctuations in this voltage due to the regulation scheme, but it is expected that they will be minimal and the nominal value should be $55\ V$. In order to avoid a convoluted group of waveforms, only two waveforms for the capacitors have been presented herein. v_{c_1} corresponds to the voltage of an arbitrarily chosen capacitor from the upper arm, while v_{c_2} corresponds to a capacitor voltage in the lower arm. The waveform of the capacitor voltage can be seen in Fig. 3.4. Based on all of the figures presented in this section, it is clear that for Case 1, when the output current is 0, the arm powers are regulated, as well as the output current. In the following section, the transient responses of the converter to a step input will be examined.
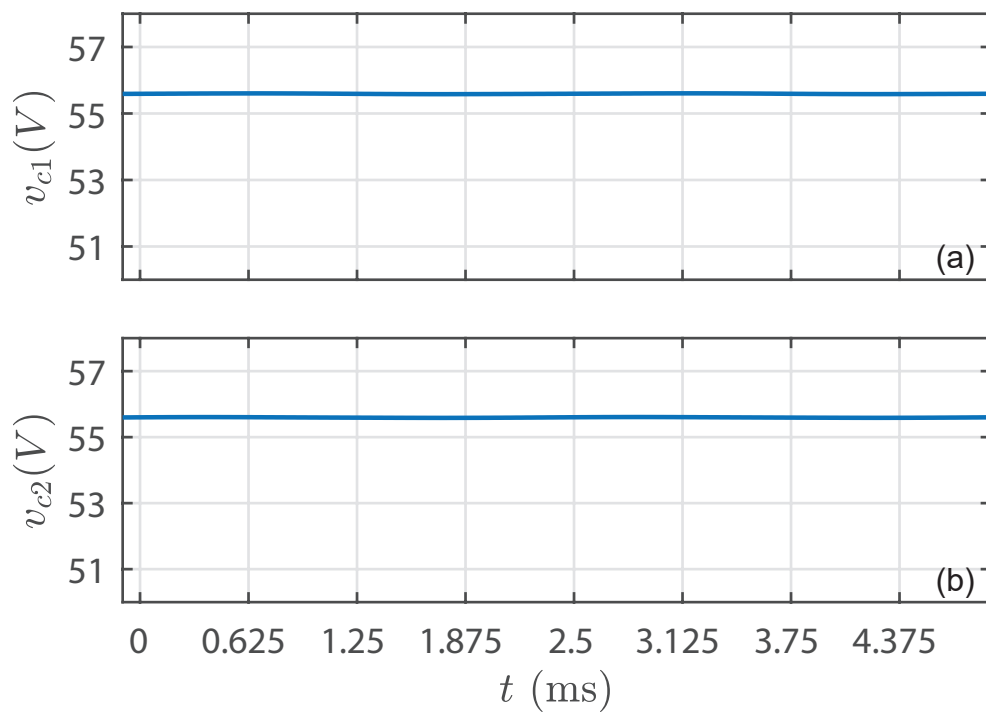
Figure 3.4: Steady-state capacitor voltage waveforms: (a) upper arm capacitor voltage v_{c_1} and (b) lower arm capacitor voltage v_{c_2} for Case 1.
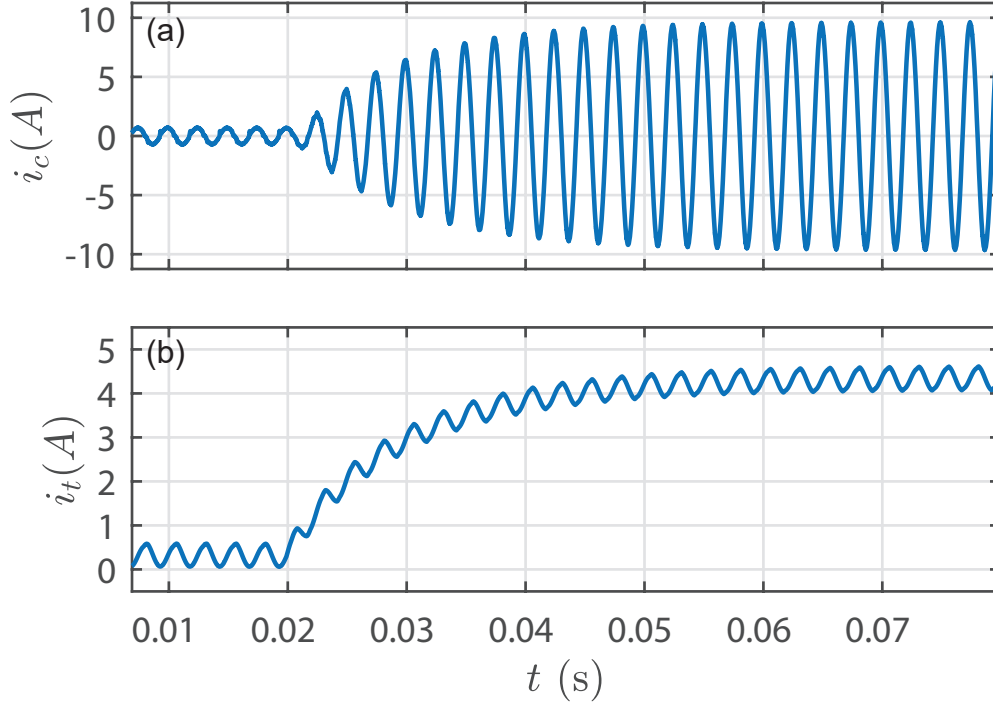
Figure 3.5: Transient step response of i_t and i_c for a step change from $i_t = 0$ to $i_t = 4\ A$

3.2   Case 2: Transient with $i_t = 0$ to $i_t = 4\ A$

In the second case, the output current was set to $4\ A$ in order to push the converter to 50% of the rated power. The response of the system to a step change from $i_t = 0$ to $i_t = 4\ A$ can be seen in Fig. 3.5, along with the change in i_c. Since the time constant of the PI controller was set to be $10\ ms$ in Section 2.6, the response of the current i_t should reach approximately 63% of its setpoint within one time constant. The step change takes place at $t = 0.02s$ and the current reaches about $2.5\ A$ (ie. 63% of $4\ A$) within the required $10\ ms$, and settles to its setpoint within 4 time constants as expected. [52].

The response of i_c is one that is not as obvious to observe as i_t, since it is not a simple step response. In order to maintain the zero net power requirement, (2.62) must hold true. In order to do so, the value of v_m must be adjusted accordingly. However, in this case since the initial condition was zero for the output current and power i_c was very small, and therefore both of the arm currents were small as well. As such, the value of v_m was fixed to the one that would be required to operate at $500\ W$ (i.e., $55\ V$) beforehand. So, there was no need to change v_m in order to adjust i_m to ensure that the power could be regulated. This means that if v_m was fixed to $55\ V$ during the transient, the change in amplitude of i_c is due entirely to the change in i_m based on (2.54). Moving on, the arm powers can be seen in Fig. 3.6.

The waveforms of Fig. 3.6 show precisely the type of behaviour that is expected of
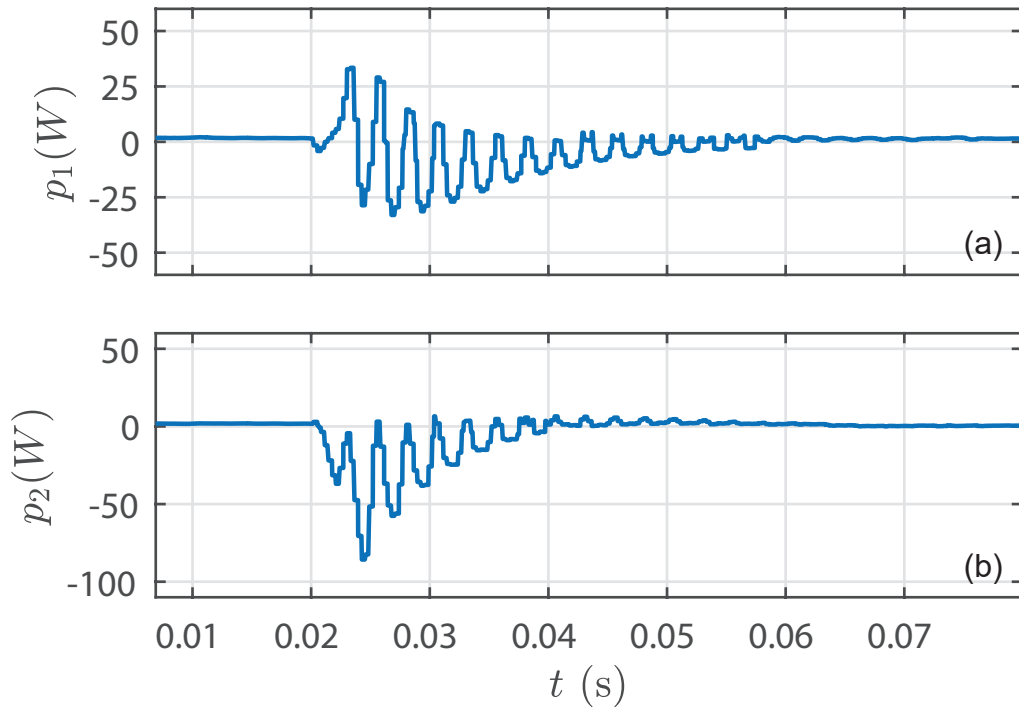
41

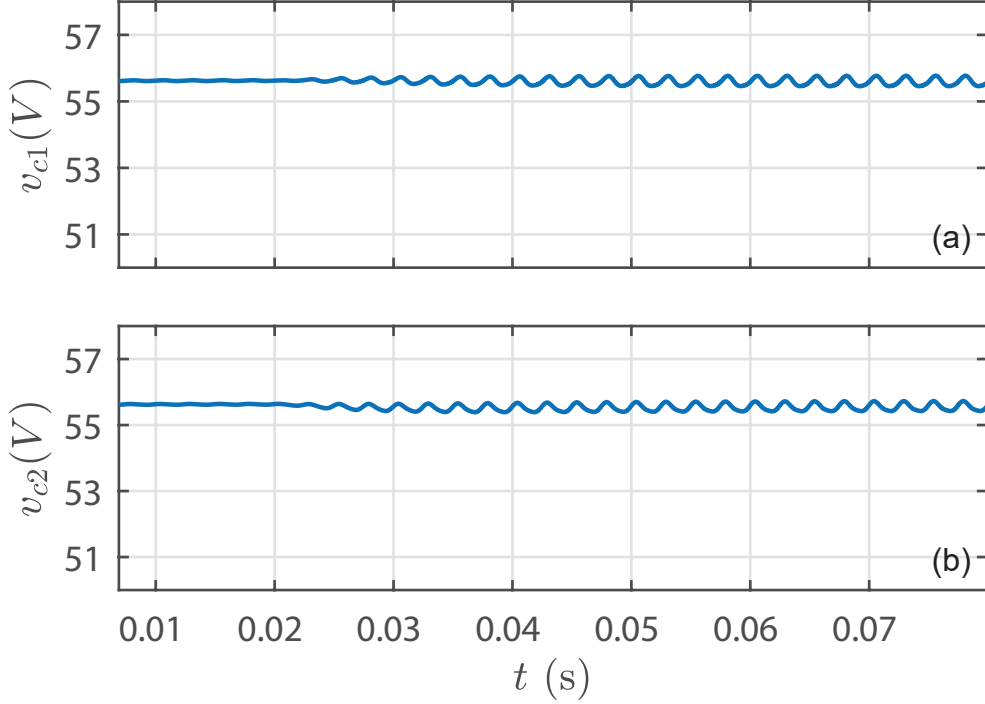Figure 3.6: Transient responses of arm powers: (a) p_1 and (b) p_2 for Case 2

Figure 3.7: Transient capacitor voltage waveforms for (a) v_{c_1} and (b) v_{c_2} for a step change from $i_t = 0$ to $i_t = 4\ A$

the MMC under the appropriate control techniques. That is, the step change in i_t causes an imbalance in the power but the controller is able to bring both arm powers back down to zero, thus ensuring that the zero net arm power condition is satisfied. If this were not the case, the step change would cause the system to become unstable, and regulation could never be achieved, causing the arm powers to increase or decrease uncontrollably. Next, the capacitor voltages during this transient period are of interest and can be seen in Fig. 3.7.

The waveforms clearly show that there is no disturbance in the capacitor voltages at the time of the step change. However, upon closer inspection a small ripple can be seen once the current settles to its setpoint. Such a small ripple is negligible as it was expected that the capacitor voltages would have some fluctuations due to the local regulation scheme. Therefore based on the waveforms presented in this section, it can be concluded that the transient response of the system is within a reasonable agreement with what is expected from the theory. As such, the following section will explore the steady-state behaviour of the system when $i_t = 4\ A$ to ensure that the waveforms follow their expected characteristics.
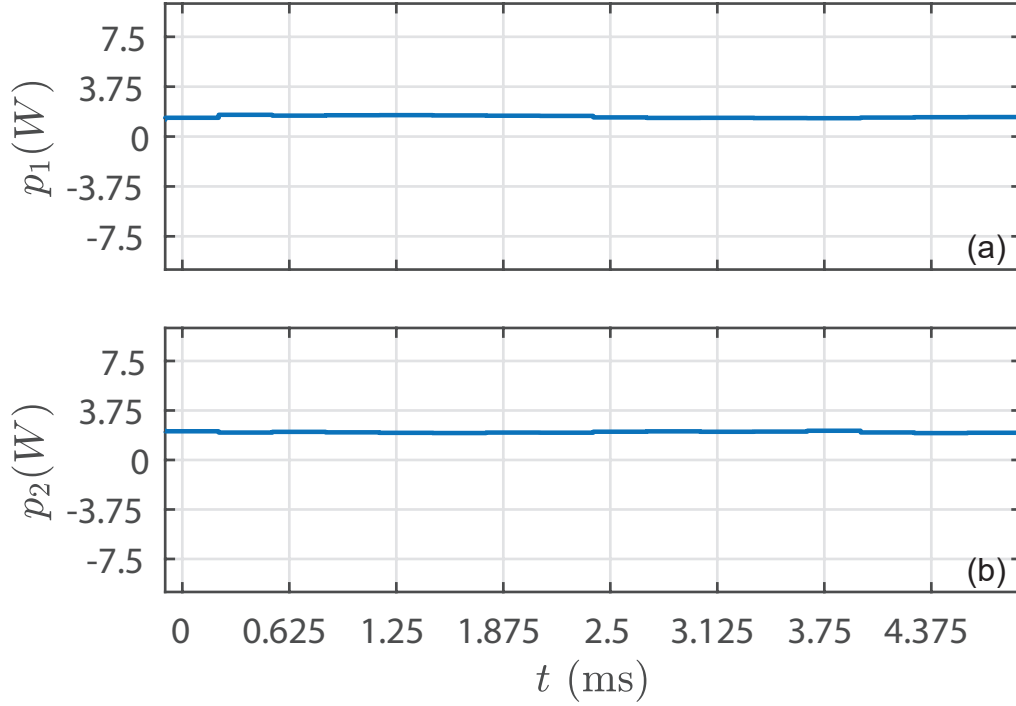
Figure 3.8: Steady-state waveforms of arm powers: (a) p_1 and (b) p_2 in Case 3

3.3 Case 3: Steady State with $i_t = 4\,A$

Once the current has settled to its setpoint of $4\,A$, the system should maintain stability similar to the initial steady-state condition. That is, the arm powers should be regulated at zero, and the individual capacitor voltages should also be maintained at their setpoint of $55\,V$, with the expected minor fluctuations as seen previously. First, the arm powers can be seen in Fig. 3.8. As in Case 1, the arm powers can both be seen clearly at some negligible amount with some minor fluctuation. Therefore, it can be concluded that the arm power condition is being satisfied. Next, the output current waveform should be maintained at the setpoint of $4\,A$ with some small ripple, while the waveform for i_c is expected to have a negligble DC component as predicted by (2.51), and have an AC component equal to i_m. Given the set of parameters and operating point for this region, the AC component of i_c can be calculated using (2.59) to be have a peak of approximately $9\,A$. Both of the aforementioned characteristics can be seen quite clearly in Fig. 3.9 which reinforces the expected behaviour of the MMC in Case 3. Still, the capacitor voltages must be maintained at $55\,V$, which the waveforms in Fig. 3.10 show quite clearly. Finally, the arm voltages can be examined in order to understand how the shape of the voltage changes depending on the output power. Since the output power is essentially controlled by controlling the arm voltages v_1 and v_2, then it is safe to assume that the waveforms will change shape as the product of $v_m i_m$ must change with the output power according to (2.62). As seen in Fig. 3.10, the amplitude of the
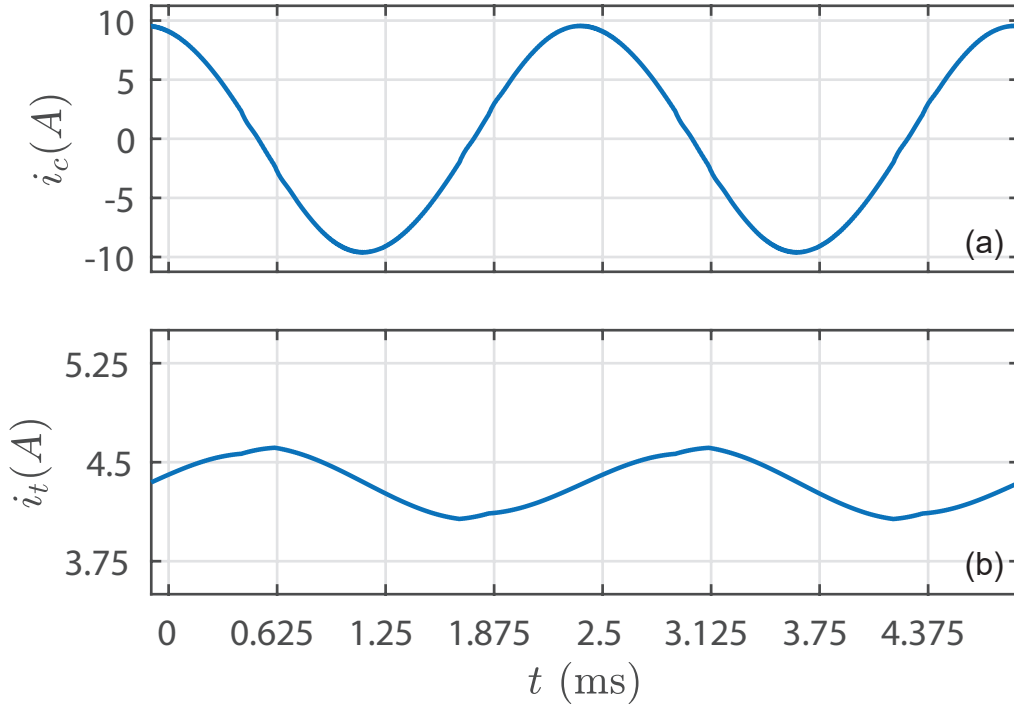
44

Figure 3.9: Steady-state waveforms of currents: (a) i_t and (b) i_c for Case 3

arm voltages has increased compared to Fig. 3.3 since the output power has increased. Hence, the waveforms contain a higher number of levels than the waveform from Case 1. This is expected due to the fact that the PWM scheme adjusts the duty cycle in order to achieve a larger voltage in each string of submodules.

Since the currents are being regulated their setpoints, the arm powers are practically zero, and the capacitor voltages are being regulated at 55 V, it can be concluded that the MMC is operating in a stable condition in Case 3. Next, the behaviour of the system as it approaches its upper limit must be explored in order to say with certainty that it is practically realizable. In the next section, the output current setpoint will be increased such that $i_t = 8.33$ A which will correspond to 1 kW of output power.

3.4 Case 4: Transient with $i_t = 4$ A to $i_t = 8.33$ A

In this section, the MMC will be set to approach its upper limit of operation by increasing the setpoint to $i_t = 8.33$ A. By doing so, 1 kW of output power will be transferred whereas the upper limit is approximately 1.1 kW. First, increasing the setpoint yields the step response seen in Fig. 3.12. One important aspect to note in Fig. 3.12 is the change in the amplitude of i_c. Since the output power P_{dc_2} was increased through i_t, v_m also had to be increased in order to be able to ensure that the net power in the arms of the MMC remains at zero. Therefore, when i_t was increased from 4 A to 8.33 A, P_{dc_2}
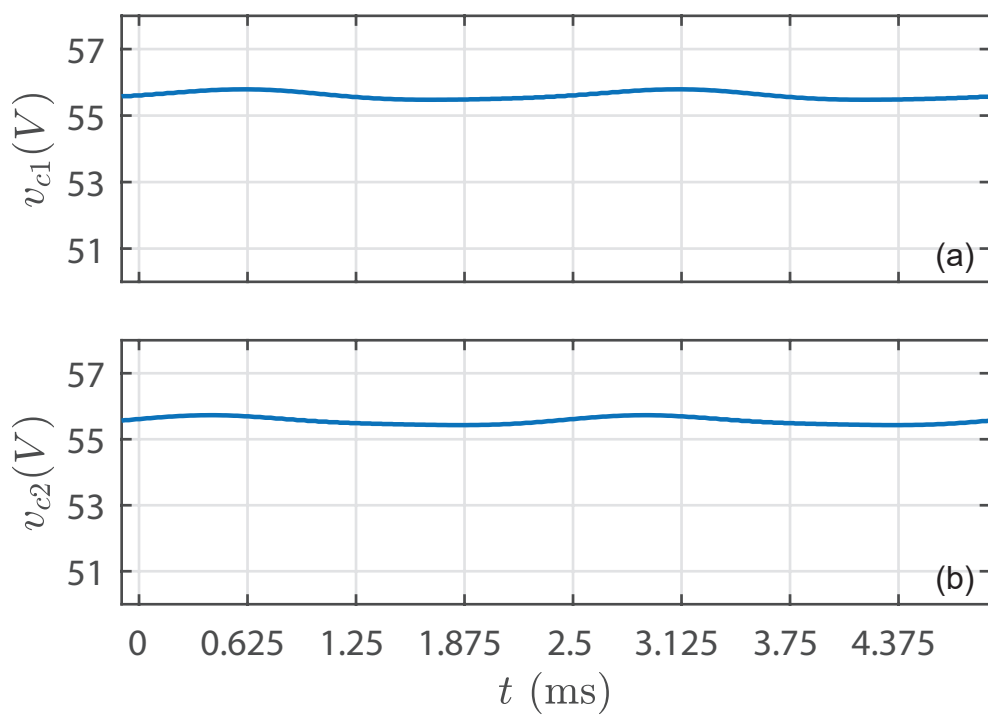
Figure 3.10: Steady-state waveforms of capacitor voltages: (a) v_{c_1} and (b) v_{c_2} for Case 3
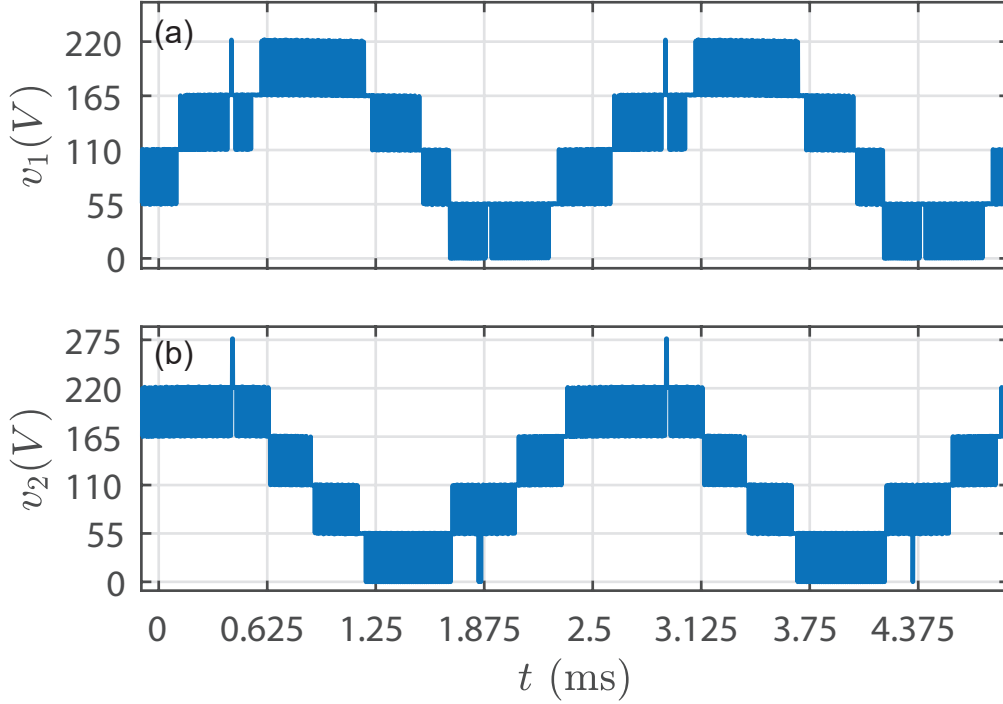
Figure 3.11: Steady-state waveforms of arm voltages: (a) v_1 and (b) v_2 for Case 3

was increased from 480 W to 1 kW, and so v_m had to be increased from 55 V to 80 V. At the same time i_m is increased in order to maintain (2.54). According to (2.59), i_c^{ac} (and therefore the amplitude of i_c) should increase to approximately 13 A which is consistent with Fig. 3.12. Furthermore, the response seen in i_t follows all of the expected characteristics, as it did in the previous case.

Next, the change in current setpoint should not disturb the regulation on the arm powers. Fig. 3.13 shows that the arm powers are indeed disturbed by the change in output power as expected. However as in Case 2, the controller is able to bring both of the powers back down to zero as required. Furthermore, the regulation on the individual capacitors is also maintained which can be seen in Fig. 3.14. Based on all of the waveforms presented in this section, it is clear that the system is stable even as it approaches its upper limit. Still, in order to ensure that it is fully functional in such close proximity to its maximum, the steady-state characteristics of the system must be explored in detail at the output power of 1 kW, which will be done in the following section.

3.5 Case 5: Steady State with $i_t = 8.33\,A$

The final region to examine is the steady-state operation at $i_t = 8.33\,A$, which corresponds to $P_{dc_2} = 1\,kW$. Under these conditions, the system can be considered to be operating at its theoretical maximum. First, it is important to observe the arm powers to
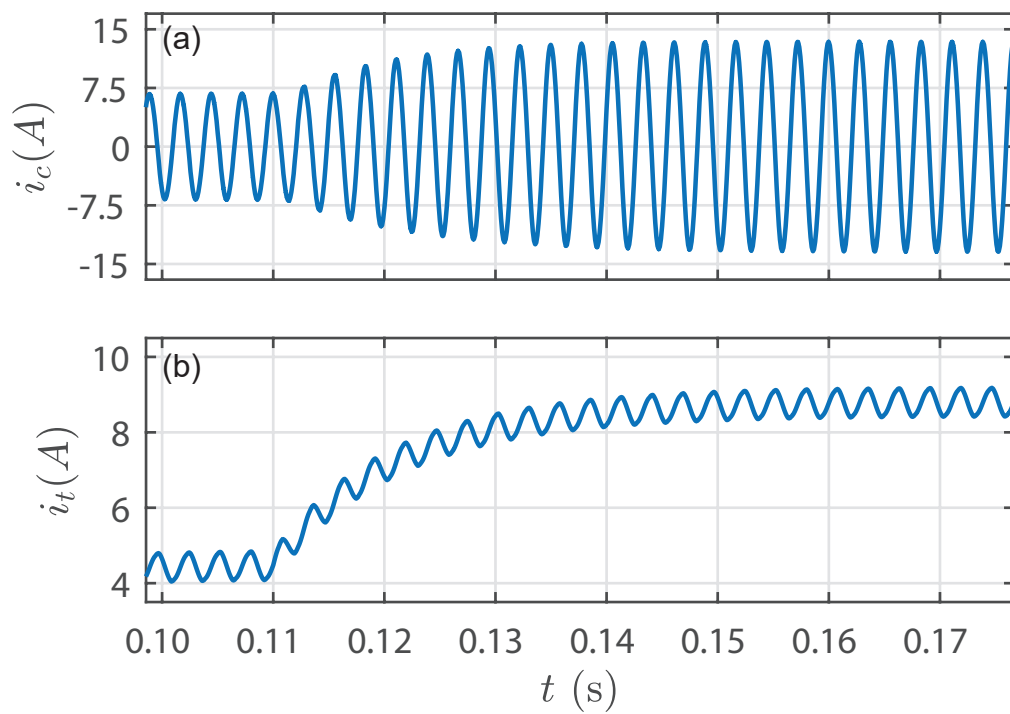
Figure 3.12: Transient responses of currents (a) i_t and (b) i_c for a step change from $i_t = 4\ A$ to $i_t = 8.33\ A$
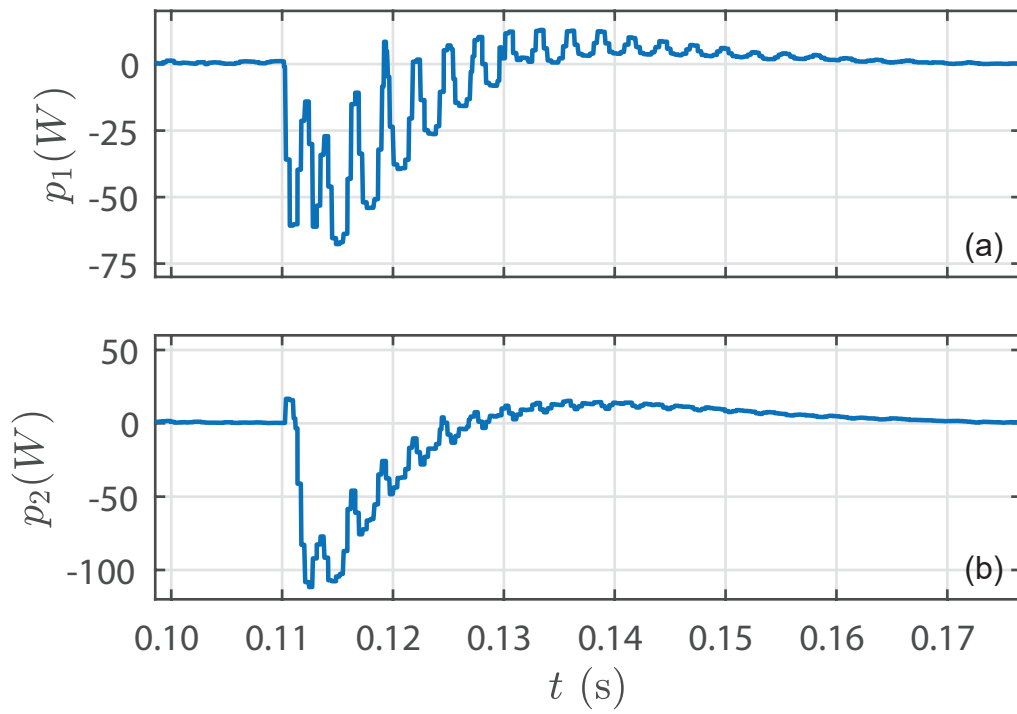
Figure 3.13: Transient response of arm powers (a) p_1 and (b) p_2 for a step change from $i_t = 4$ A to $i_t = 8.33$ A
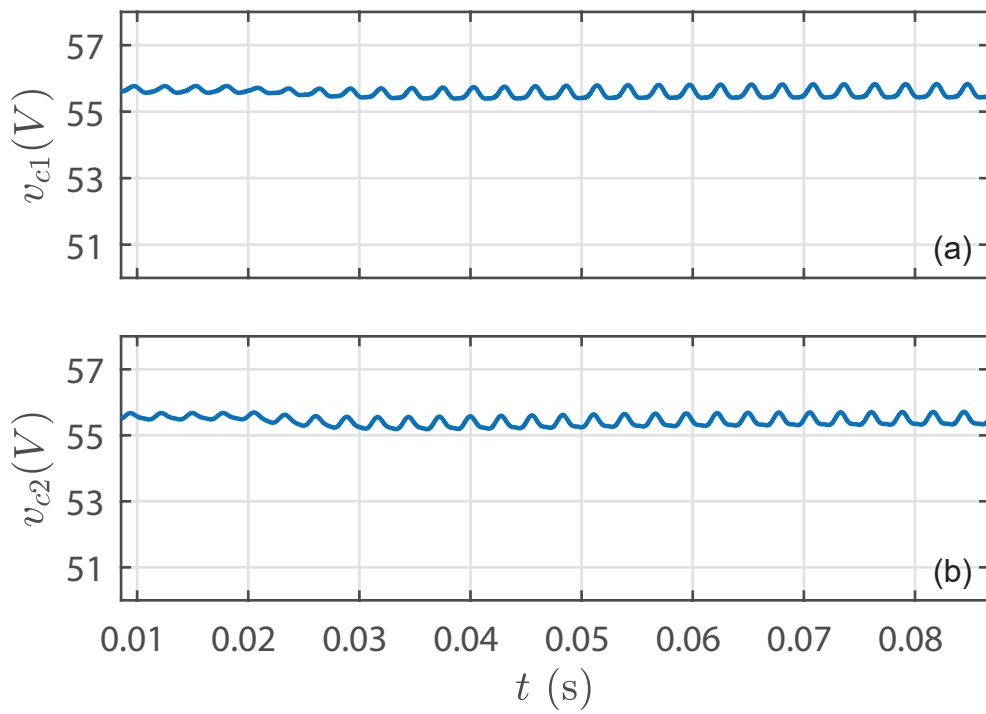
Figure 3.14: Capacitor voltage waveforms (a)v_{c_1} and (b) v_{c_2} during the transient period of Case 4.
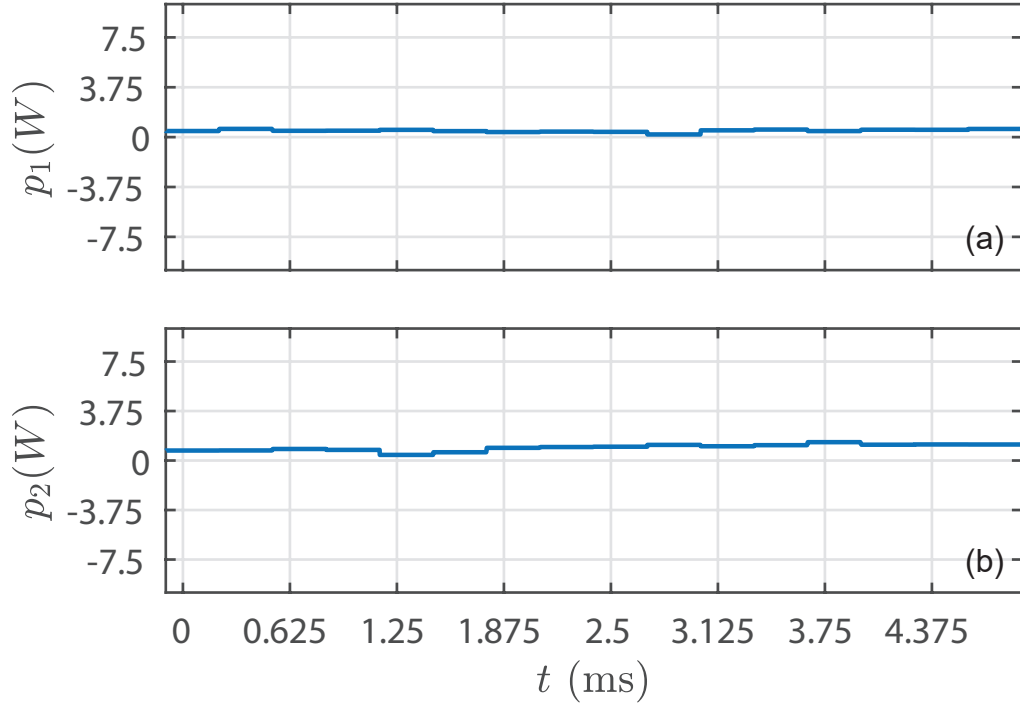
Figure 3.15: Steady-state waveforms of the arm powers p_1 and p_2 for $i_t = 8.33\ A$.

ensure that regulation has been maintained. The waveforms of Fig. 3.15 show that both arm powers are being regulated to ensure that the arm power is negligible. Next, the two currents i_t and i_c must also maintain regulation at their setpoints as they have in the previous regions. The steady-state waveforms of these currents can be seen in Fig. 3.16. The two current waveforms show that the system is stable in this region of operation with the expected magnitudes. The next requirement for the MMC to be stable is the regulation of the submodule capacitor voltages. The waveforms in Fig. 3.17 show quite clearly that the capacitor voltage is being regulated at $55\ V$ without any disutrbances whatsoever. Since the MMC is operating near its maximum condition, it is expected that the arm voltages will include all 6 levels of the expected discrete waveform. That is, the amplitude of the arm voltages should reach up to $275\ V$. Furthermore, as discussed in Section 2.1, the MMC operating at its rated conditions shows 6 distinct voltage levels.

Based on all of the waveforms presented in this chapter, it can be concluded that the simulation model constructed in PSCAD has been successfully implemented and the theory presented in Chapter 2 has been validated. In the following chapter, the results of an MMC constructed in the lab will be presented, and the theory will be further validated using similar tests.
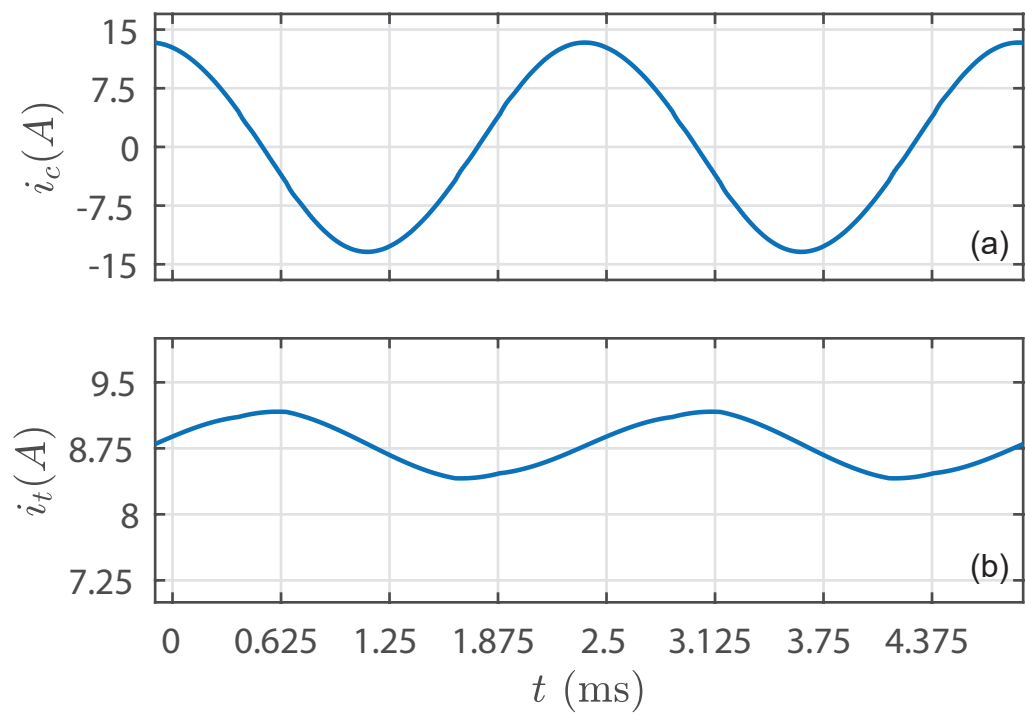
Figure 3.16: Steady-state current waveforms for (a) i_t and (b) i_c at $i_t = 8.33\ A$.
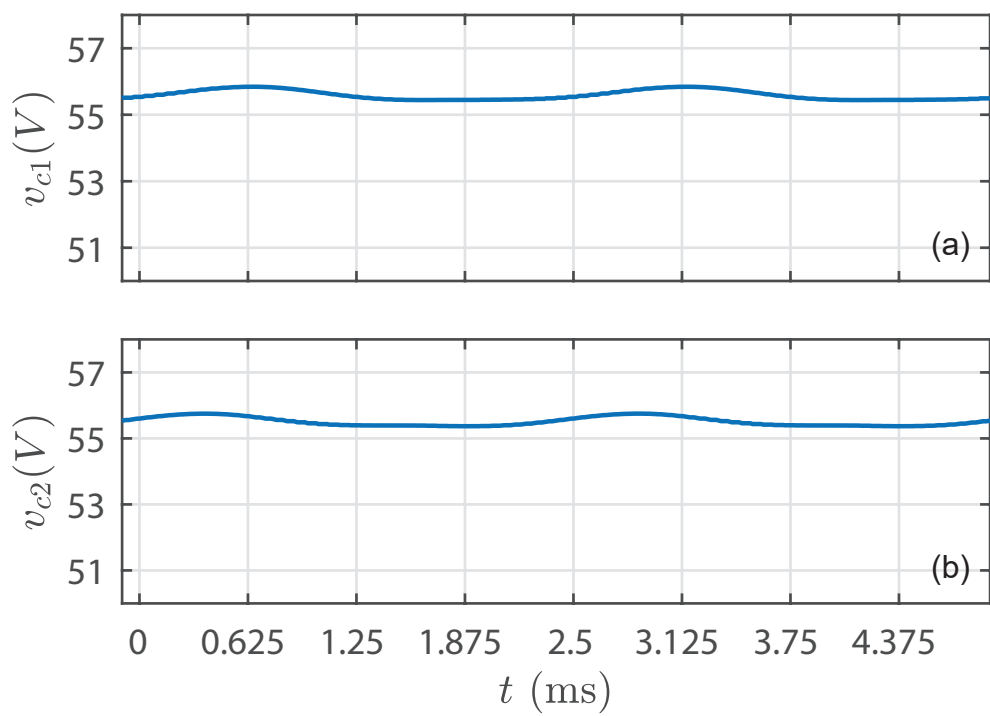
Figure 3.17: Capacitor voltage waveforms (a) v_{c_1} and (b) v_{c_2} in the steady-state condition of Case 5.
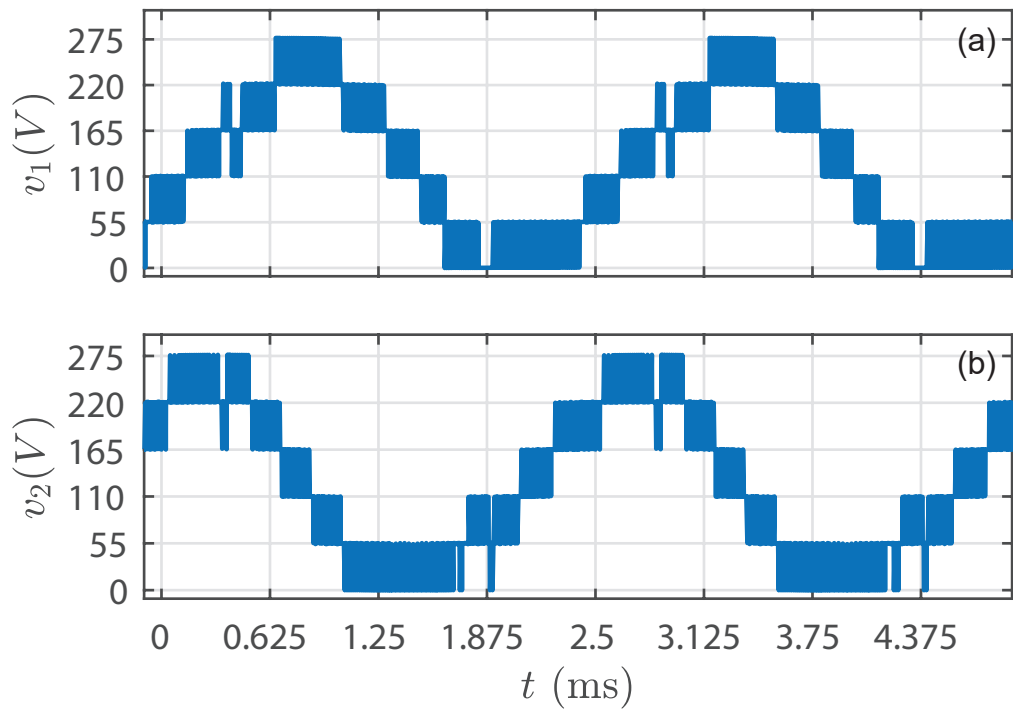
Figure 3.18: Arm voltages (a) v_1 and (b) v_2 in the steady-state condition of Case 5.

Chapter 4

Experimental Setup of MMC

Having conducted a series of thorough tests in the simulation, the final step was to put together an experimental setup of the MMC. First, the assembly of the MMC posed a fair bit of challenges and required careful design in order to have an overall system that operated in harmony, and so it is worthwhile to discuss the physical details of the setup. Once the setup was complete, the MMC was first tested with a single submodule per arm in order to confirm overall operation of the system. Next, the full converter with five submodules per arm was assembled and tested. In both cases, the system was connected to a National Instruments CompactRIO (cRIO-9082) platform in order to provide control and other auxiliary functions. The details pertaining to the NI platform can be found in Appendix A. Finally, the waveforms obtained during the experimentation process have been presented in this section and will be compared to their simulation counterparts.

4.1   Physical Implementation

The main challenge presented by the MMC was the size of the converter as a whole. While the circuit boards themselves were fairly small, the number of boards required in order to create the entire converter resulted in a large volume of connections and components. A complete graphical layout of the circuit boards used in this setup can be seen in Fig. 4.1. As the figure suggests, there were four types of boards each with their own unique functionality. The boards can be summarized as:

- **Submodule Board:** This board houses a submodule of the MMC. While the configuration used in this experiment was half-bridge, the submodule is capable of being reconfigured in order to operate as a full-bridge as well. The submodule capacitor is also a part of this board. This board also performs other functions such as precharging of the submodule capacitor, controlling the nature of the gating pulses being supplied to the bridge, and transmitting readings of the capacitor voltage to the rest of the system.

- **Interface Board:** The purpose of this board is to translate the measured quantities from the submodule board to the appropriate levels for the NI-cRIO platform and vice versa. For example, the gating pulses that are provided to the submodule
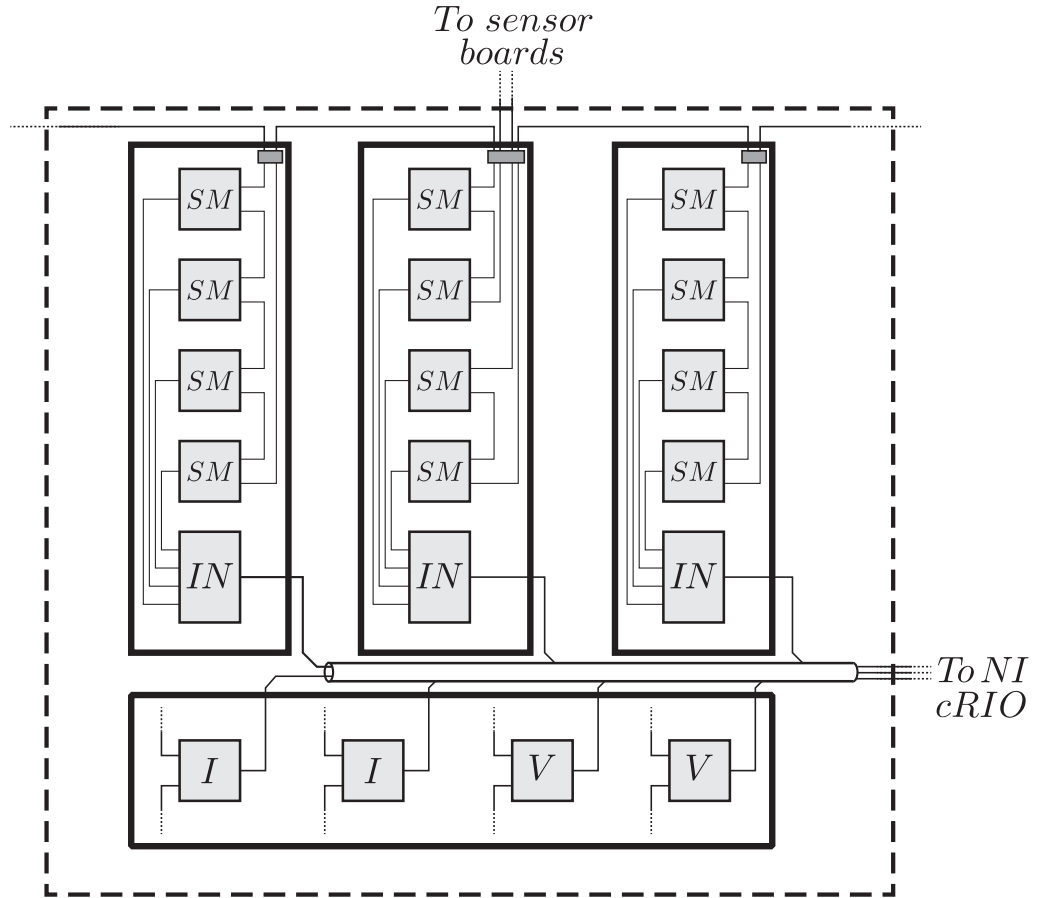
Figure 4.1: High-level layout and connection diagram of the MMC assembled in the cabinet. The board labels SM, IN, V, and I, signify the submodule, interface, voltage sensor, and current sensor boards, respectively

board from the NI-cRIO are first provided to the interface board from the cRIO, and then translated and routed to the submodule board. Also, the voltage measurements of the submodule capacitor taken from the submodule board (which are in the form of a pulse width modulated signal) are converted into analog voltages according to the requirements of the cRIO.

- **Current Sensor Board:** As the name suggests, this board is used to measure the current in the MMC. Its main purpose is to measure the currents i_1 and i_2 of the MMC arms. Each board was designed to have a large bandwidth and two channels. Again, this board was designed in order to function with the requirements of the NI-cRIO platform.

- **Voltage Sensor Board:** This board was designed in order to measure the voltages v_{dc_1} and v_{dc_2} and provide the data to the NI-cRIO for further processing. The board is capable of operating under several different magnitudes of voltages.

The configuration seen in Fig. 4.1 was assembled in a cabinet using DIN rails and other hardware, and the fully assembled system can be seen in Appendix C. Due to the large number of connections and close proximity of the boards to one another, the assembly had to be done meticulously while paying close attention to potential issues such as EMI. In order to mitigate such issues, all cables used in the setup for data transfer (i.e., voltage/current readings, gating pulse timings, etc) were shielded, with the shields appropriately grounded. Still, it was found in such cases that the noise generated by EMI was substantial and harmful, so further measures were taken to ground individual boards directly to the chassis of the cabinet.

Next, in order to ensure bidirectional power flow in the system, the power supplies connected to v_{dc_1} and v_{dc_2} were augmented using dump loads such that they could sink and source power. These dump loads were assembled outside of the cabinet and connected across the power supplies. Still, amount of power that could be sunk was limited due to the ratings of these resistors, and the number of resistors available. Furthermore, in order to minimize the effects that any disturbances had on the power supplies, the external terminals of the converter were augmented with LC filters such that the power supplies would provide a steady DC voltage.

Having discussed the details of the physical implementation of the MMC, the following sections will present the results obtained from the experimental tests. Then, the results will be compared directly with the same test cases in the simulation.

4.2 Single-Level Configuration

Initially, the MMC was configured such that it only had a single submodule per arm. This was done to confirm that the system was set up correctly and operating as expected. The large number of connections and wires meant that it would be quite easy to make a mistake. By only including a single submodule per arm, the fundamental operation of the control platform with the electrical circuit could be tested in a straightforward manner. Furthermore, as discussed in Section 2.1 since the operation of the MMC does

not depend on the number of submodules, the entire system can be tested to ensure that it operates as expected, and once everything has been confirmed, additional submodules can be included and the system can be expanded. It should also be added that for most of the tests carried out at this stage, the capacitor voltages were fixed using an external power supply in order to simplify the control and test individual parts of the overall algorithm. Once the current control loops were tested and confirmed to be operating correctly, the capacitor loops were closed and the system was allowed to run on its own.

Since the number of submodules was decreased in this configuration, the system was first scaled down accordingly in order to ensure that the hardware was not damaged. To do so, a conversion ratio of 0.5 was maintained, but the voltages v_{dc_1} and v_{dc_2} were set to $40\ V$ and $20\ V$ respectively. While the magnitude of the power under this configuration was minuscule and insignificant, it was an important stepping stone in order to confirm that the control algorithm was being executed correctly.

As the physical setup could not be probed as freely as the simulation, only a handful of quantities and measurements could be used in order to troubleshoot the converter and confirm that it was functioning correctly. The most critical aspect of the converter that was measured was the output current i_t whose step response to a $1\ A$ reference can be seen in Fig. 4.2.

The waveform clearly exhibits a first order response with the desired time constant of $10\ ms$ as previously calculated and simulated. Next, the capacitor loops were closed by removing the external power supplies. To ensure that the capacitor loops were regulating as they should, the setpoints of the capacitor voltages were changed while monitoring the response. Fig. 4.3 shows the response of the capacitor voltage to a step change in its reference voltage from $30\ V$ to $50\ V$. As the response shows, the capacitor voltage was perfectly regulated with the expected negligible ripple voltage. The arm voltage waveforms in this configuration were simply square waves with a frequency of $16\ kHz$, and so they offer little value to this discussion and have been omitted.

In this section, the results pertaining to the single level configuration of the experimental setup were presented and the desired operation was confirmed. In the following section, the results of the complete five-level converter will be presented.
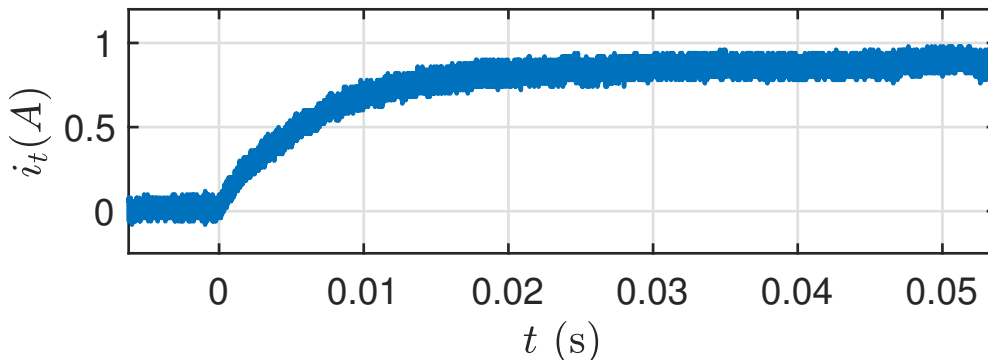

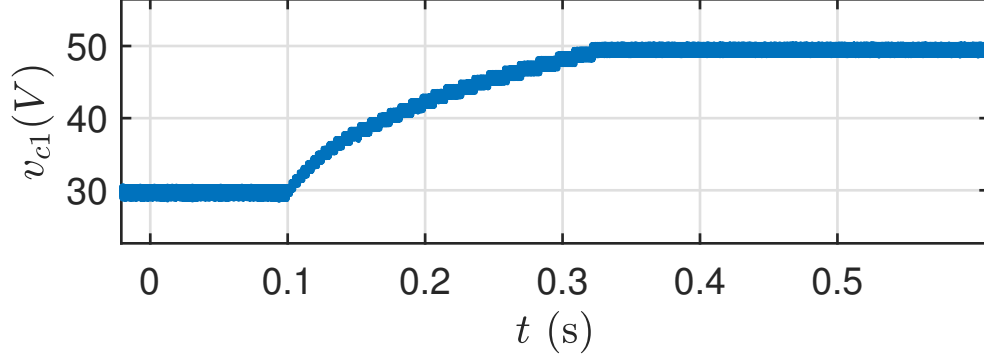Figure 4.2: Step response of i_t to a 1 A reference for the single level configuration.

Figure 4.3: Response of the capacitor voltage to a step change from 30 V to 50 V.

4.3   Five-Level Configuration

Finally, the system was configured in its entirety as a five-level converter. Since the number of submodules was increased from one to five, the voltage levels were also increased to a magnitude similar to that of the simulation seen in Chapter 3. So, the voltages v_{dc_1} and v_{dc_2} were set to 240 V and 120 V to maintain the 0.5 conversion ratio, and the capacitor voltages were regulated at 50 V due to limitations on the hardware. In order to achieve a similar operation as that of the simulation, v_m was set to 80 V. Given these conditions, the arm voltage v_1 can be seen in Fig. 4.4. As expected the multilevel waveform has 6 levels, and the discrete steps in the waveform are 50 V each. Next, the step response of the output current for a reference of 2 A can be seen in Fig. 4.5. It should be noted that the experimental step changes were limited to 2 A per step in order to avoid subjecting the converter to large changes in current, as it was found that in some cases, larger step changes caused issues with the power supplies and their stability. In order to provide comparison, the simulation results for the case where i_t changes from 0 to 2 A has been included as a subplot in the same figure. As mentioned previously the sinking and sourcing capabilities of both v_{dc_1} and v_{dc_2} were of interest, and so the case where the current i_t becomes negative was also of interest. In this case, the magnitude of the current was limited as the dump load that was attached to the power supply for v_{dc_1} was not capable of handling a very large power. Therefore, a setpoint of -2 A was chosen,
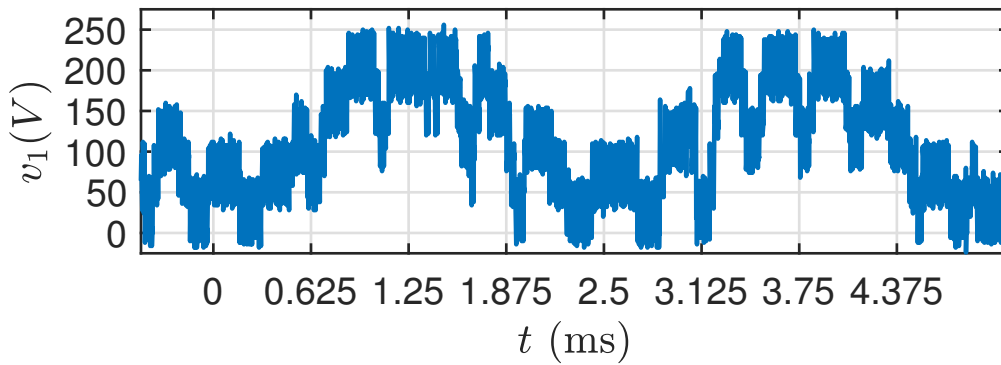

Figure 4.4: Voltage waveform for v_1 in the five-level configuration.
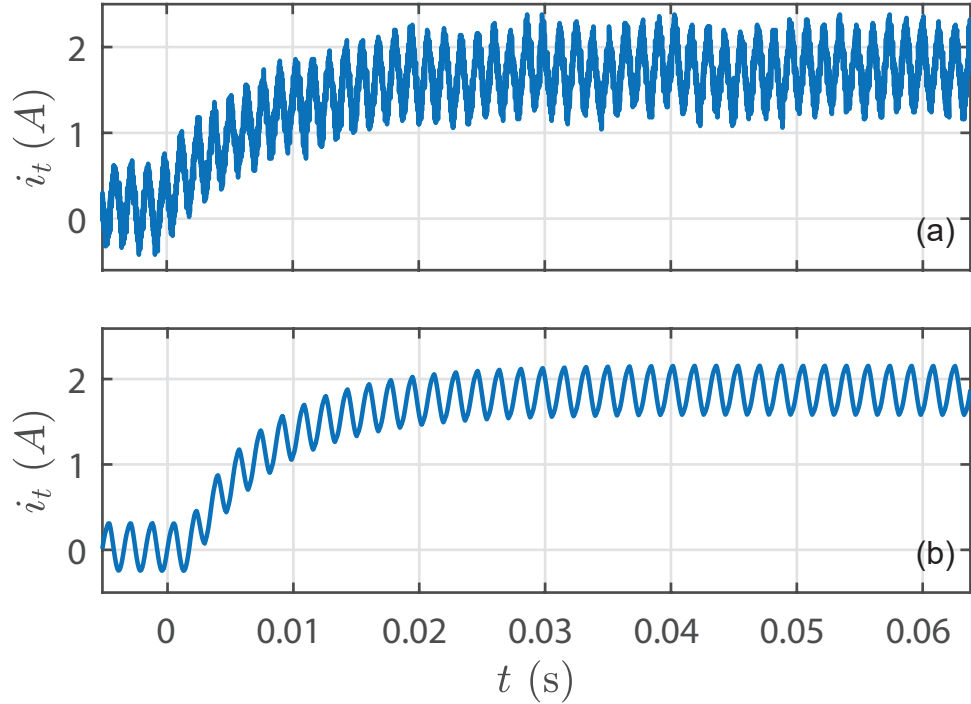
59

Figure 4.5: Step response of i_t for a change in reference from 0 to 2 A: (a) experimental, (b) simulation.

and the resulting waveform can be seen along with its corresponding simulation result in Fig. 4.6. Upon inspection of the waveforms in Fig. 4.5 and 4.6 it is quite clear that there is a substantial agreement between the two waveforms. The only apparent difference between the two is the ripple on the two waveforms. In the case of the experiment, the ripple is almost double that of the simulation. It is expected that the ripple would be higher in the experiment due to the nonidealities associated with the practical system. However, it is possible that the inductor L_f caused some problems as it was created using four 20 mH, and one 5 mH inductor. Still, the experimental results agree well with the simulation results. Finally, the voltages of two randomly chosen capacitors (one from each arm) can be seen in Fig. 4.7. The waveforms show that the capacitor voltages are being regulated at their setpoint of 50 V with some small and expected ripple.

In this chapter, the details of the experimental setup were presented along with the results of two different experimental configurations. Since the cases tested in the experiment were different than those of of Chapter 3, the step responses of the currents for the cases tested in the experiment were generated and compared directly to the experiment. Overall, the results obtained in the experiment and simulation were in agreement with one another.
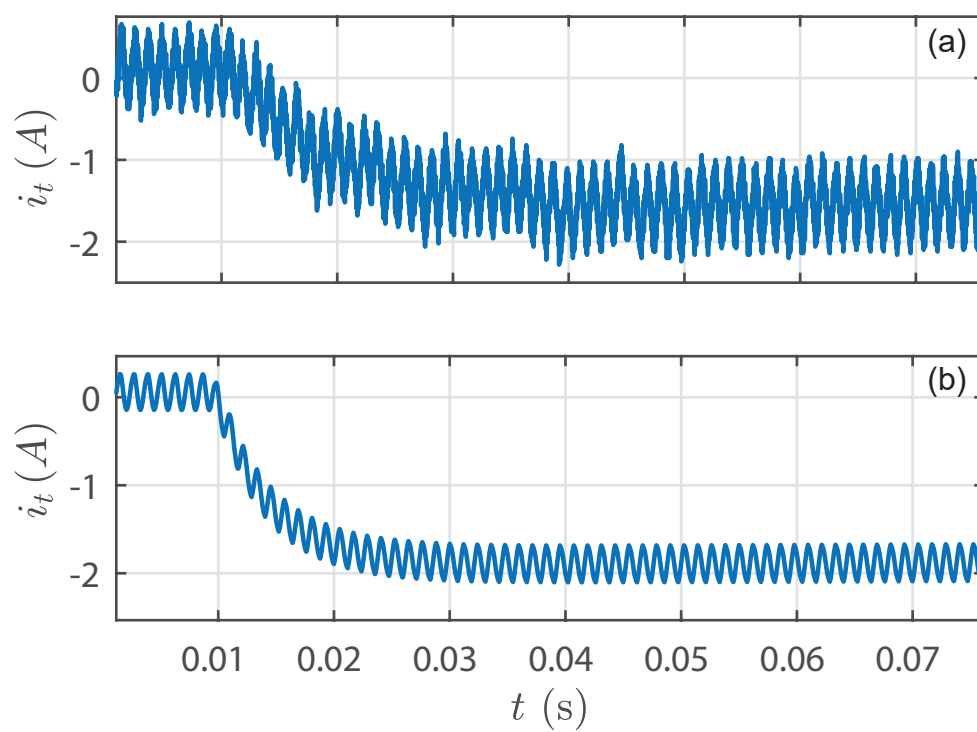
Figure 4.6: Step response of i_t for a change in reference from 0 to -2 A: (a) experimental, (b) simulation
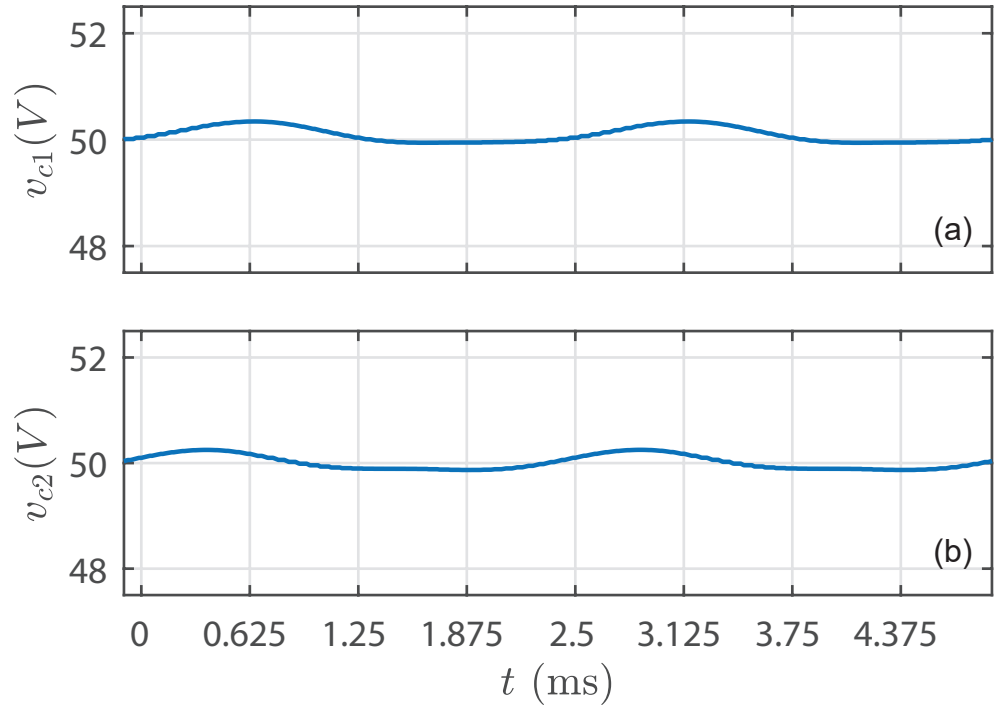
Figure 4.7: Steady state voltage waveform of capacitors in the five level configuration. v_{c_1} corresponds to the voltage of a capacitor in the upper arm while v_{c_2} corresponds to the voltage of a capacitor in the lower arm.

Chapter 5

Conclusion and Future Work

Based on the previous three chapters, it is possible to conclude that the objectives of the thesis have been met. That is, a modular multilevel converter implemented as a DC-DC converter using a current control technique was successfully implemented both in simulation and experiment. Furthermore, the theoretical concepts that were proposed in Chapter 2 have been verified in through simulation and experiment in Chapter 3 and Chapter 4 respectively.

At this point in time, the possibilities of future works can be discussed. In particular, the system presented can be expanded to consider the following scenarios:

- Expansion from a single phase system to a three phase system which can eliminate the need for large filter inductances such as L_f used in this thesis. As the AC components in the converter are controllable, expanding the system to have three phase legs means that the AC component of each leg can be controlled. Thus, setting the relative phase shifts of these components to 120° will theoretically result in the sum of the ripples on the currents to be zero. Hence, L_f can be made much smaller, if not removed altogether. Furthermore, the expansion to a three-phase system would allow for the control to be implemented in the orthogonal coordinate frame [49].

- Implementation of full-bridge submodules such that the arm voltages can also be negative and that the overall power transfer capability of the converter can be increased.

- The cost associated with the NI-cRIO and compilation time would warrant the use of other control platforms such as those based on the ARM Cortex architectures.

- The use of wide-bandgap semiconductor switches in order to achieve considerably higher switching frequency such that a more compact converter can be designed with more efficient control.

Appendix A

Practical Considerations of Control Implementation

As the main contribution of this work was a control technique for the MMC, the details relating to the practical implementation of this control scheme are of particular importance. The purpose of this appendix is to highlight the aspects of the control platform used in this work. In Chapter 4, it was mentioned that the means by which the converter was controlled was the FPGA-based National Instruments CompactRIO-9082 platform. This platform consists of a chassis that holds up to 8 National Instruments I/O cards referred to as C-Series Modules, and is connected to a host PC via an Ethernet cable. The programming of the cRIO is done through the NI LabVIEW software which is a graphical programming language, and executed on either the real-time processor, or FPGA.

The functions performed by the cRIO in this setup can be simplified into two main categories: reading analog input data, and writing to digital outputs. Therefore, the means by which this control platform is interfaced with the converter are digital output modules and analog input modules. In order to keep the system versatile, the converter was assembled with the intention that the full-bridge configuration of the submodules would be used. In doing so, a smaller subset of connections could be activated if the half-bridge was desired, while still maintaining the capability of running in a full-bridge, which meant that the NI-cRIO had to house a large number of wires in order to perform all of the desired functions. While the cRIO itself only holds 8 NI I/O cards (each with up to 8 pins depending on the type of I/O), the NI-9144 Ethercat CompactRIO Slave Chassis which can hold up to 8 additional I/O cards was also used. A summary of the NI I/O cards used in this system can be seen in Table A.1. As far as the programs that were

Table A.1: NI C-Series modules used in this system.

Card Number	Function	Channels
NI-9474	Digital Output	8
NI-9423	Digital Input	8
NI-9263	Analog Input	4

run on the cRIO are concerned, they can be broken into two main programs, one for the

real-time processor, and the other for the FPGA. Based on the technical documents, the real-time processor is better suited for less complex and non-deterministic tasks, while the FPGA is used for more demanding calculations. Therefore, the structure of the program used for the control was two main programs, referred to as virtual instruments (or VIs) in LabVIEW, where one was run on the real-time processor as a supervisory program, while other ran on the FPGA and was responsible for performing the control calculations, PWM, and generating the gating pulses for the submodules. The main challenge associated with this task was the synchronization of the two programs, since the program running on the real-time was responsible for reading the data from the converter, translating it into the appropriate form, and passing it to the FPGA for further processing, and all of this had to be done within a fixed amount of time. Furthermore, due to the fact that the slave chassis was used to expand the I/O, the complexity of the synchronization was increased.

In LabVIEW, programs are created by placing functional blocks inside of loops. The characteristics of these loops vary based on requirements, but they can still be classified as traditional "while" or "for" loops. For the program to be completely synchronized, the individual loops running in the different parts of the cRIO had to all be doing so harmoniously. Of course, some loops hold higher priorities than others depending on the task they are performing, and so they were the most time-critical of all. In this case, the most critical loop was the one running on the FPGA that was responsible for the control, PWM, and gating pulses. In LabVIEW, this was implemented using a "single-cycle timed loop" (SCTL) which is essentially a while loop that runs with a period of 25 ns (corresponding to the 40 MHz clock frequency of the FPGA). One of the convenient aspects of LabVIEW is that it has a class of built-in functions which are used in such loops to ensure that all of the calculations are done within a single cycle. Then, this loop can be placed in another loop, or can be made to only run once another loop finishes it's cycle, which then controls how often the SCTL loop runs. Of course, there is an upper bound of 40 MHz on this loop, but this was more than sufficient for the system constructed in this thesis. So in this work, the SCTL was used to compare the references of the arm voltages to the carriers and generate the gating pulses. In order to do so, all of the control calculation was done in a previous loop that was running such that the entire process of reading the converter voltage/current to generating the gating pulse was done at a sampling rate of 32 kHz.

Next, it is worthwhile to discuss the details of the supervisory program, referred to herein as the RT VI (real-time virtual instrument), since it was responsible for coordinating the flow of the overall control scheme. The main functions performed by the RT VI were the collection and routing of data, sending commands to initiate the start-up sequence, monitoring the system for faults while it ran, and most importantly, initiating the desired safety protocols in order to ensure that the system was not damaged in the troubleshooting stages. First, the start-up sequence that was detailed in Chapter 4 was implemented using the RT VI. Using digital output commands generated by the RT VI, the submodules were charged and enabled through an on-board Arduino Pro Mini. Once the system was ready to begin operation, the command was sent from the RT VI to the FPGA VI to begin firing the pulses and deploy the control algorithm.

Furthermore, the RT VI had several limits set in place in order to prevent damage during testing. These limits were integrated in a way such that the programs would not fire pulses or begin the startup sequence so long as the fault had not been cleared. One such protection which was extremely useful once the multilevel system was put together was the limit on the capacitor voltage. Due to the selected components, the submodule capacitors were only rated for 80 V. In order to ensure that they were not damaged, the capacitor voltages were constantly monitored and compared with a user-defined upper limit, in this case, 60 V. If any capacitor under any circumstances ever hit that ceiling of 60 V, the system would stop firing pulses, and revert to a safe state until the capacitor voltage decreased to a safe level, and the fault flag was cleared by the user.

Appendix B

A Study on Phase-Shifted PWM

During the course of this experiment, the expected shape of the arm voltages v_1 and v_2 was called into question on a number of occasions. As such, a Simulink model was put together in order to better understand the shapes of the voltages that were seen both in the PSCAD simulation, and the experimental setup. The following figures consider a PS-PWM scheme which uses five carriers to correspond with the five levels of the MMC presented in this thesis. Then, the DC and AC components of the modulation index, m^{dc} and m^{ac}, have been varied in order to understand how the output waveform changes in each case. In each case, the change in levels of the output corresponds to the insertion of an additional submodule into the string. The results for the variation in the DC component of the modulation index can be seen in Fig. B.1 to Fig. B.5.

Based on Fig. B.1 through Fig. B.5, it is clear that increasing m^{dc} from 0 to 1 results in a square wave with a pulse whose width is dependent on the duty cycle, as in the case of the single carrier PWM. However, the main difference is the DC offset which exists here. In a typical single carrier PWM, only the width of the pulse varies. In this case, the multiple carriers add together in order to shift the DC component of the waveform. Next, in order to understand how the AC component of the modulation index impacts the output waveform, the outputs due to different values of m^{ac} can be seen in Fig. B.6 to Fig. B.9. In this case, $m^{dc} = 0.5$ so that the sinusoid can have a maximum swing. Since there are 5 levels, the output waveform can reach a maximum of 5.

From Fig. B.6 through Fig. B.9, it can be seen that increasing m^{ac} results in the introduction of more discrete steps in the waveform. This behaviour is expected as the output waveform should mimic a sinusoid. In Fig. B.7, the waveform is approaching it's upper and lower limit, and when $m^{ac} = 0.6$ as it does in Fig. B.8, the waveform begins to saturate at the top and bottom as it exceeds the maximum value.

Based on this study, the similarities and differences between the PS-PWM and PWM techniques is evident. Overall, the PS-PWM behaves similar to the PWM technique, with the main difference being that the addition of multiple carriers adds a layer of complexity to the overall operation.
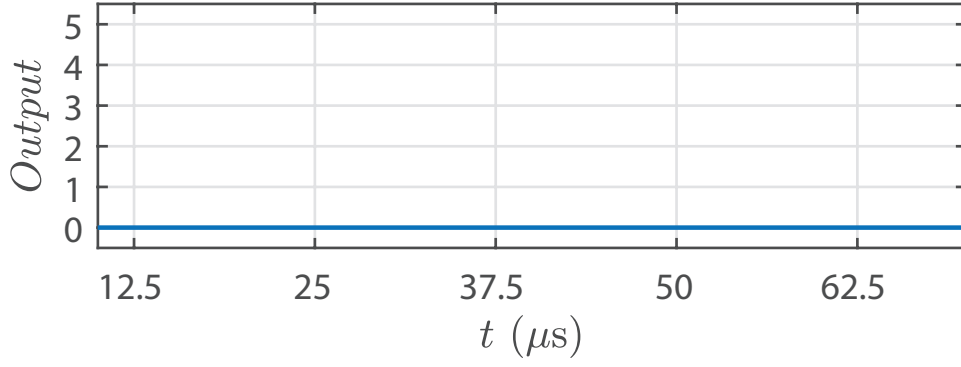
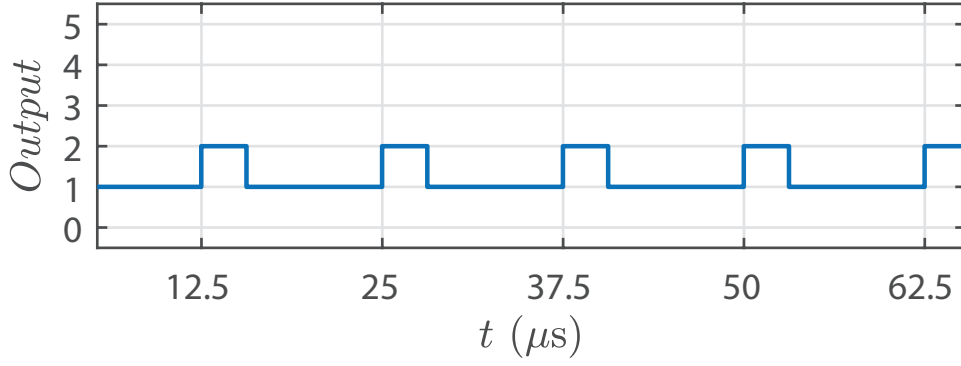Figure B.1: PS-PWM waveform for $m^{dc} = 0$ and $m^{ac} = 0$.

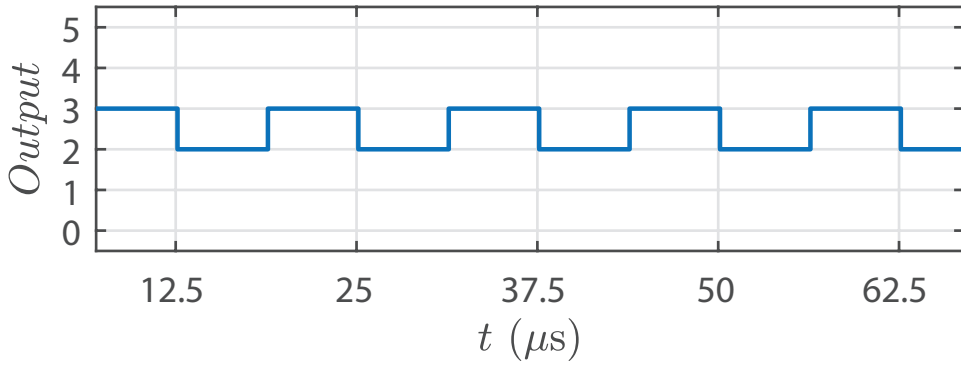Figure B.2: PS-PWM waveform for $m^{dc} = 0.25$ and $m^{ac} = 0$.

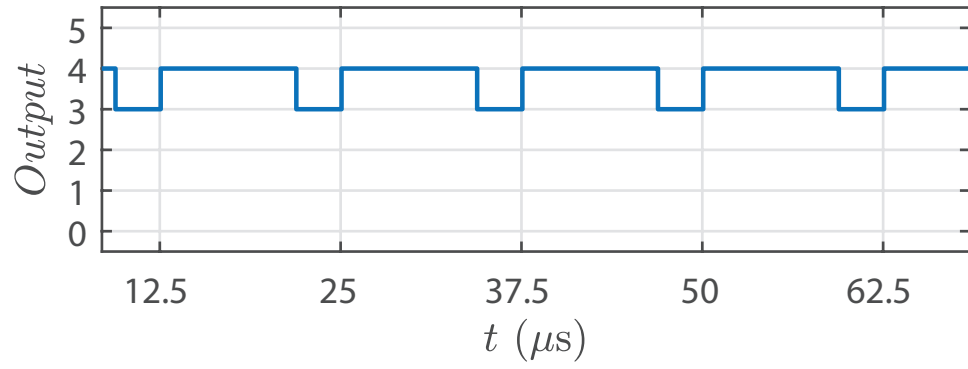Figure B.3: PS-PWM waveform for $m^{dc} = 0.5$ and $m^{ac} = 0$.

Figure B.4: PS-PWM waveform for $m^{dc} = 0.75$ and $m^{ac} = 0$.
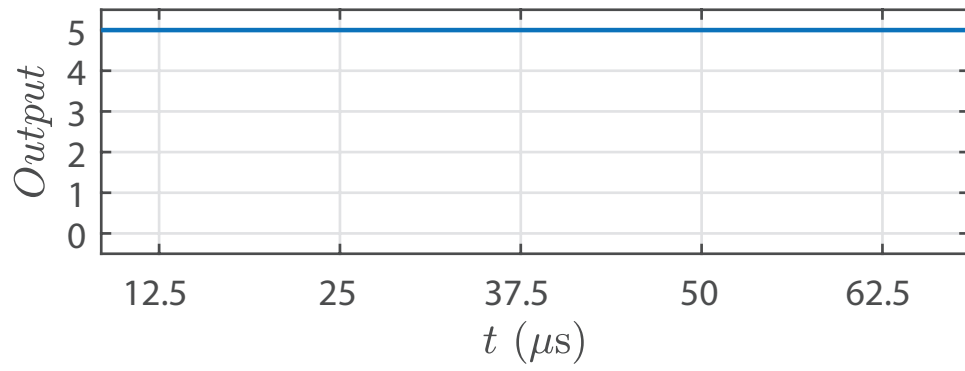

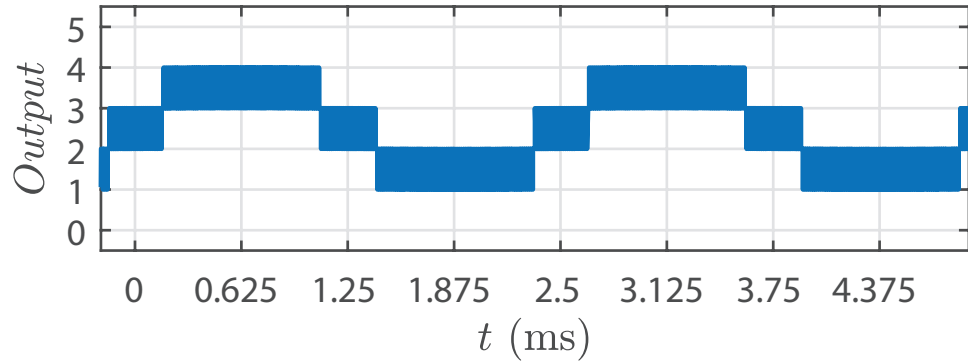Figure B.5: PS-PWM waveform for $m^{dc} = 1$ and $m^{ac} = 0$.

Figure B.6: PS-PWM waveform for $m^{dc} = 0.5$ and $m^{ac} = 0.25$.
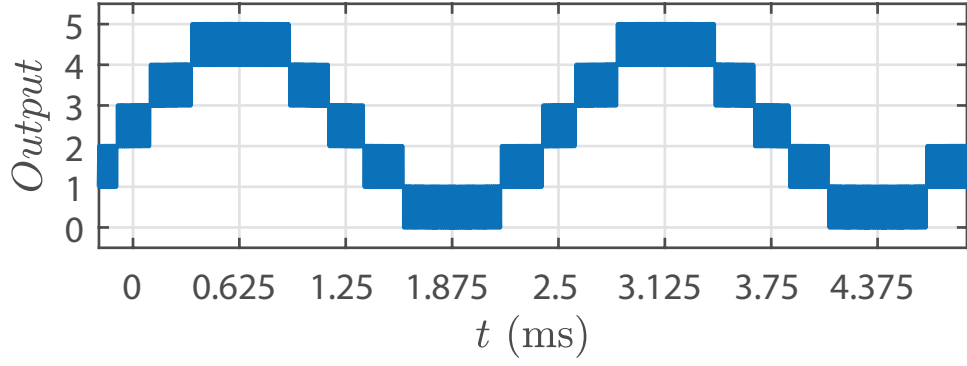
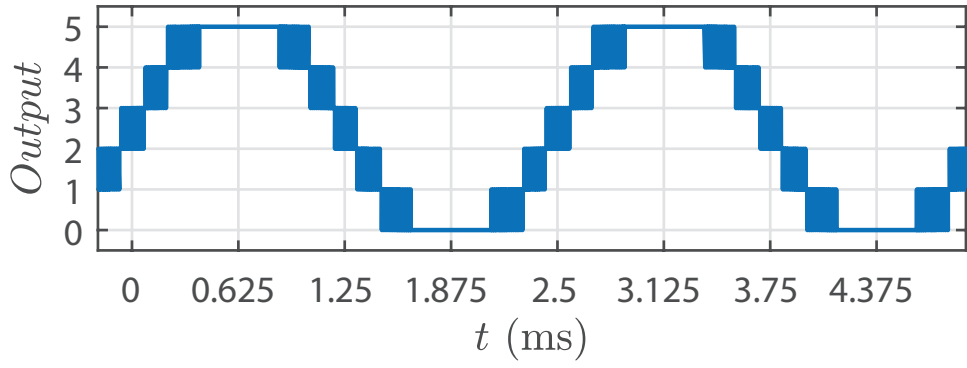Figure B.7: PS-PWM waveform for $m^{dc} = 0.5$ and $m^{ac} = 0.4$.

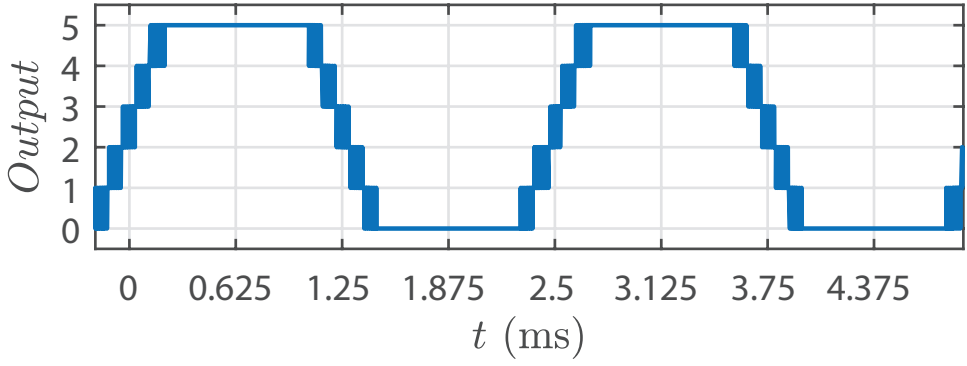Figure B.8: PS-PWM waveform for $m^{dc} = 0.5$ and $m^{ac} = 0.6$.

Figure B.9: PS-PWM waveform for $m^{dc} = 0.5$ and $m^{ac} = 1$.

Appendix C

Details of Experimental Setup

This appendix contains a set of pictures of the physical converter setup constructed in the lab. In particular, the boards used and the final converter assembled inside a cabinet can be seen in Fig. C.1 through C.9. A detailed description of each board's functionality can be seen in Section 4.1.
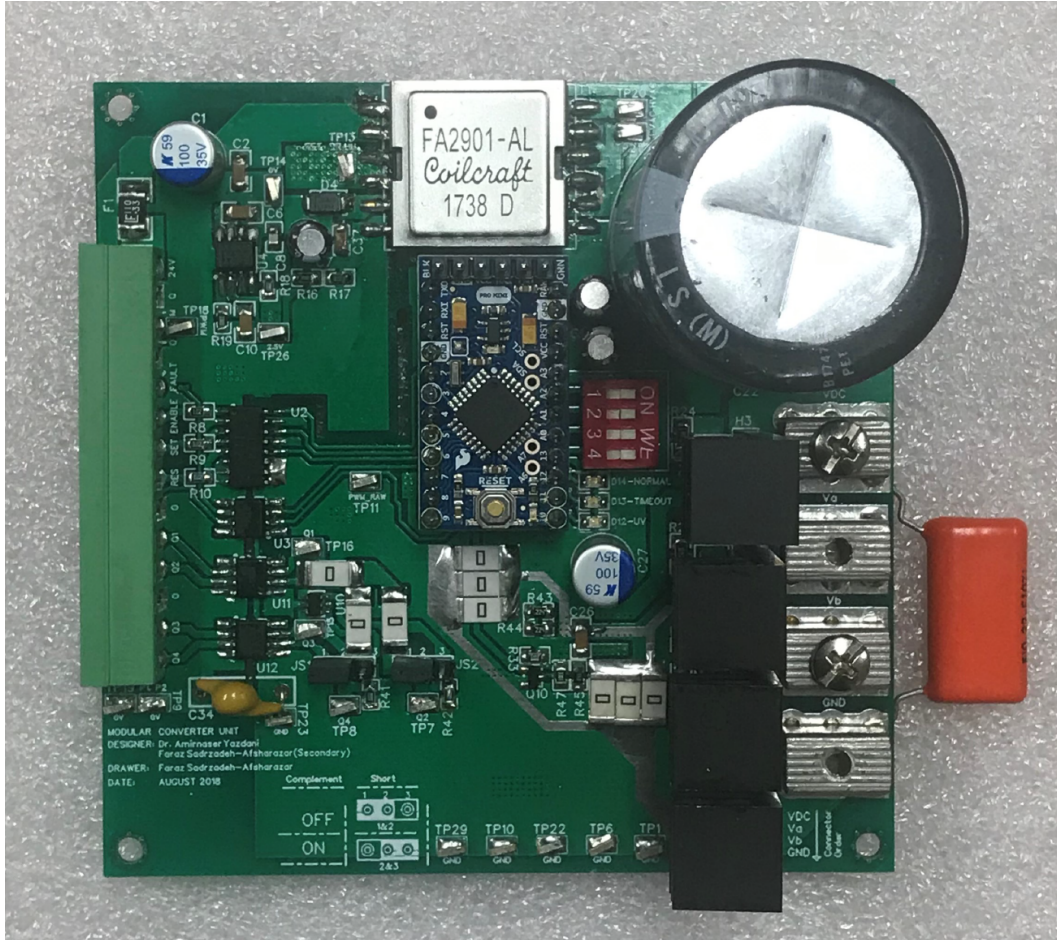
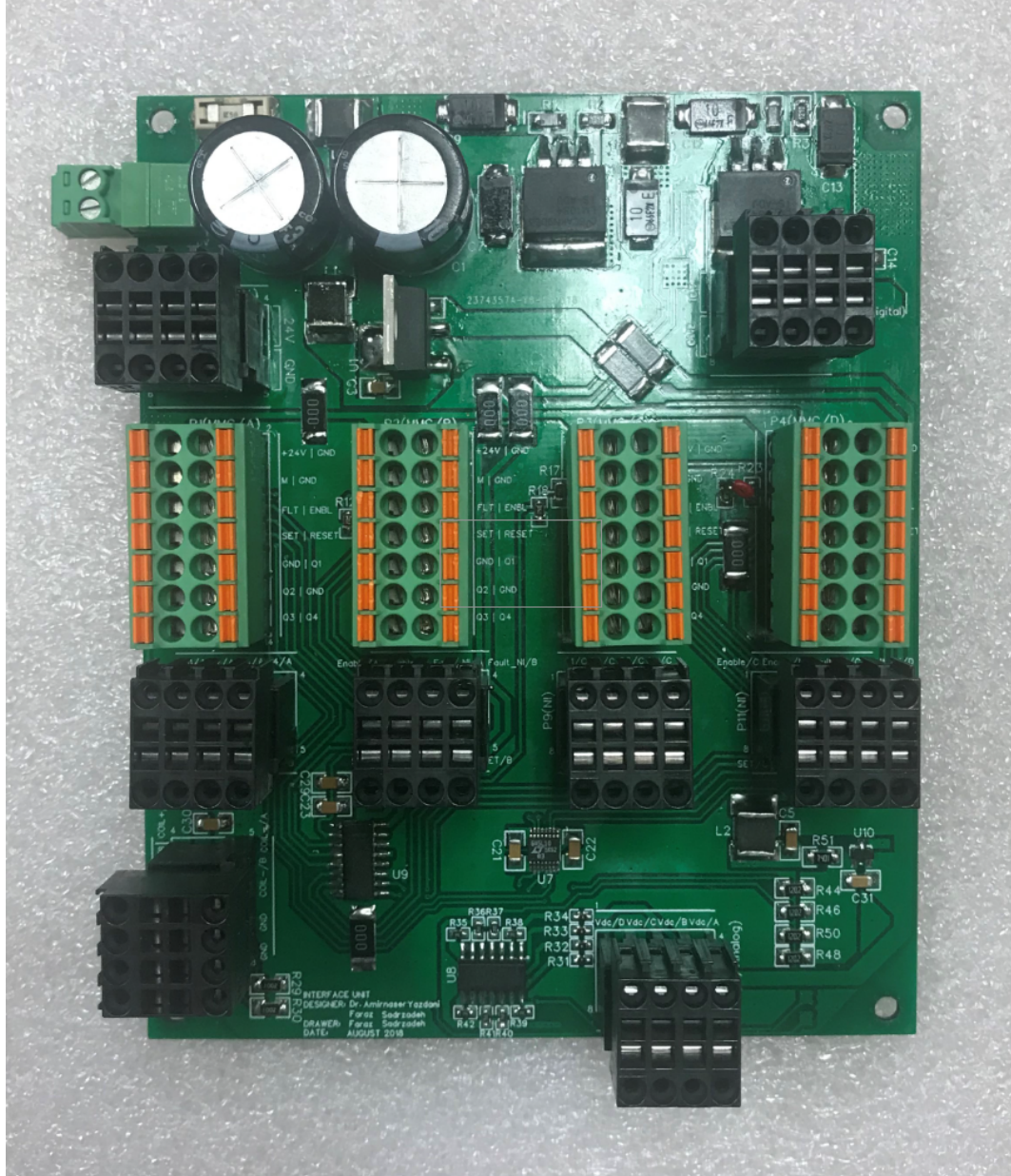Figure C.1: Experimental circuit board of the submodule.

Figure C.2: Experimental PCB of the interface board.
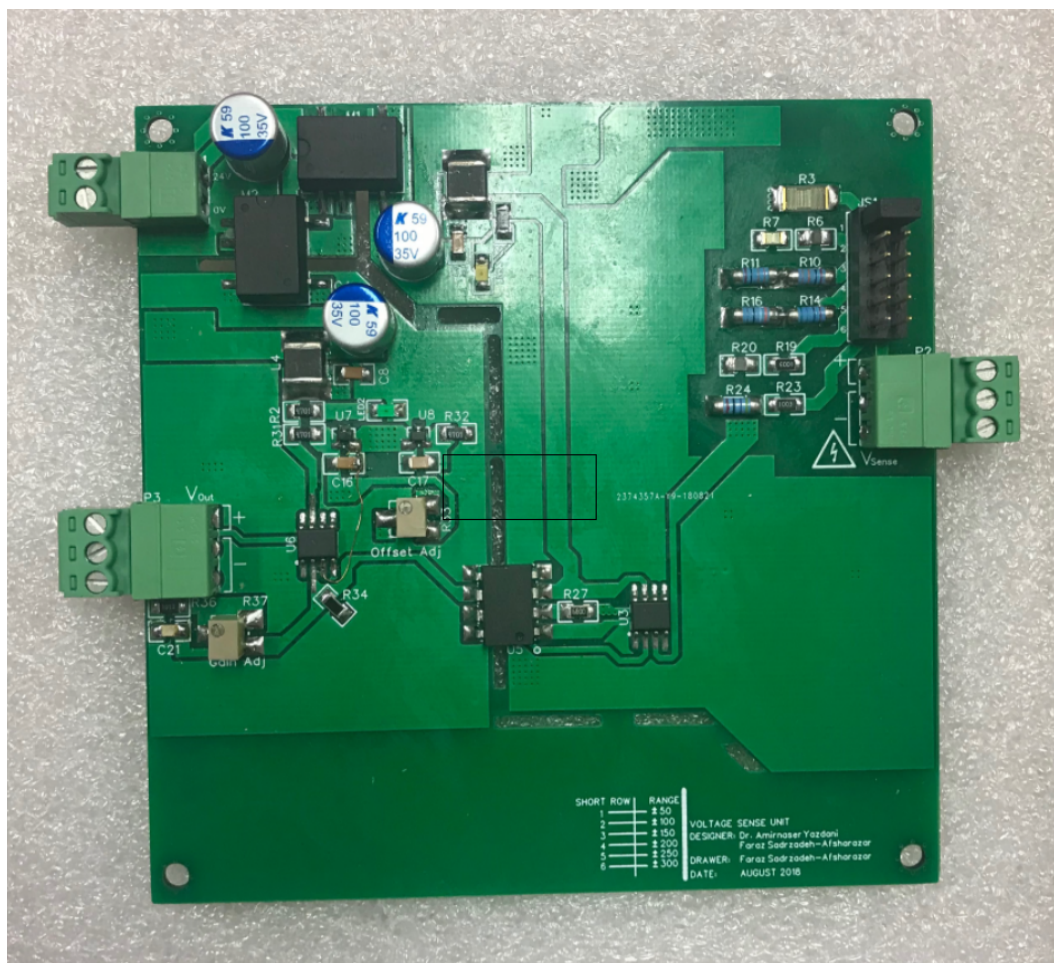
Figure C.3: Experimental PCB of the voltage sensor board.
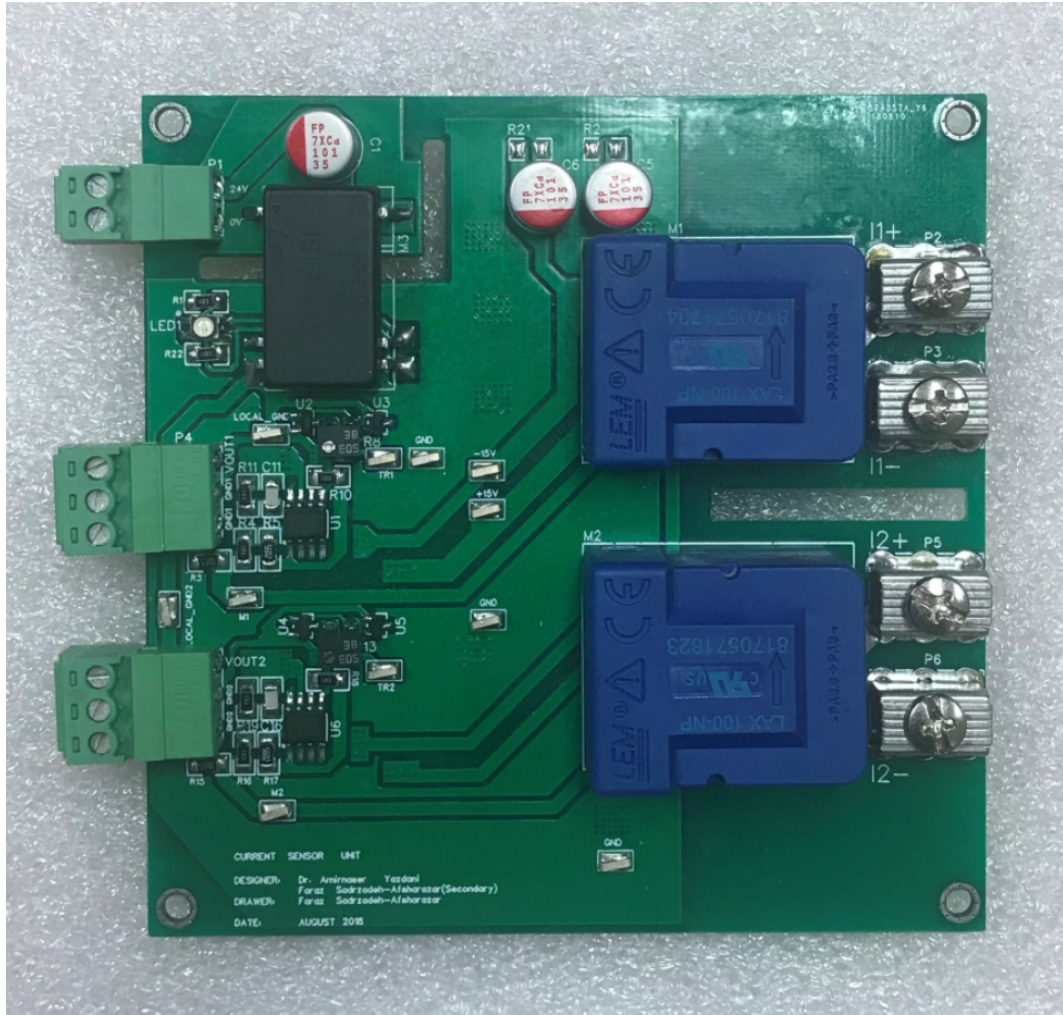
Figure C.4: Experimental PCB of the current sensor board.

Figure C.5: National Instruments CompactRIO-9082 installed inside of the cabinet and connected to the converter.

Figure C.6: Submodule and interface boards connected and assembled inside the cabinet.

Figure C.7: Inductors and contactors used in the converter.

Figure C.8: A top-down view of the inside of the cabinet.

Figure C.9: The fully assembled cabinet as seen from the outside.

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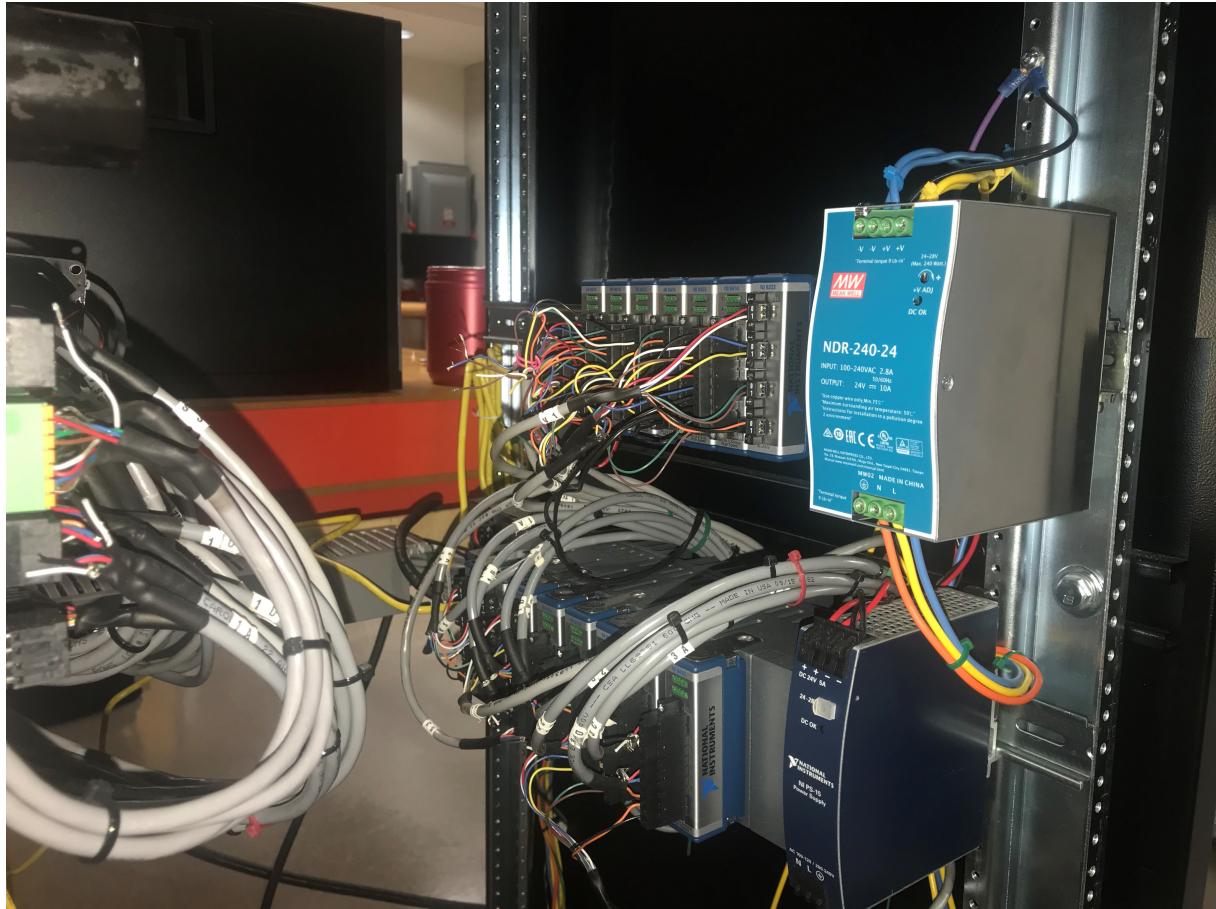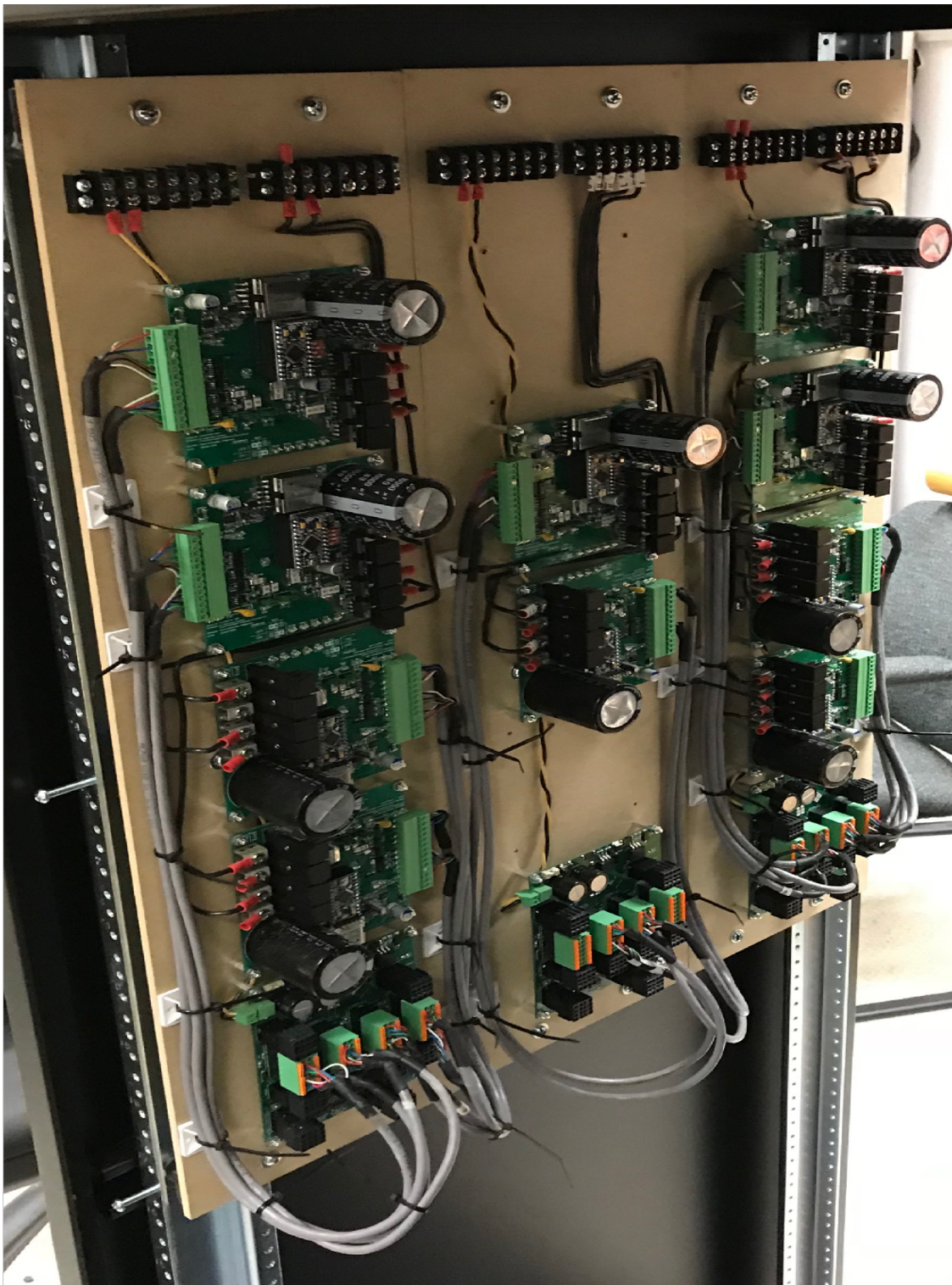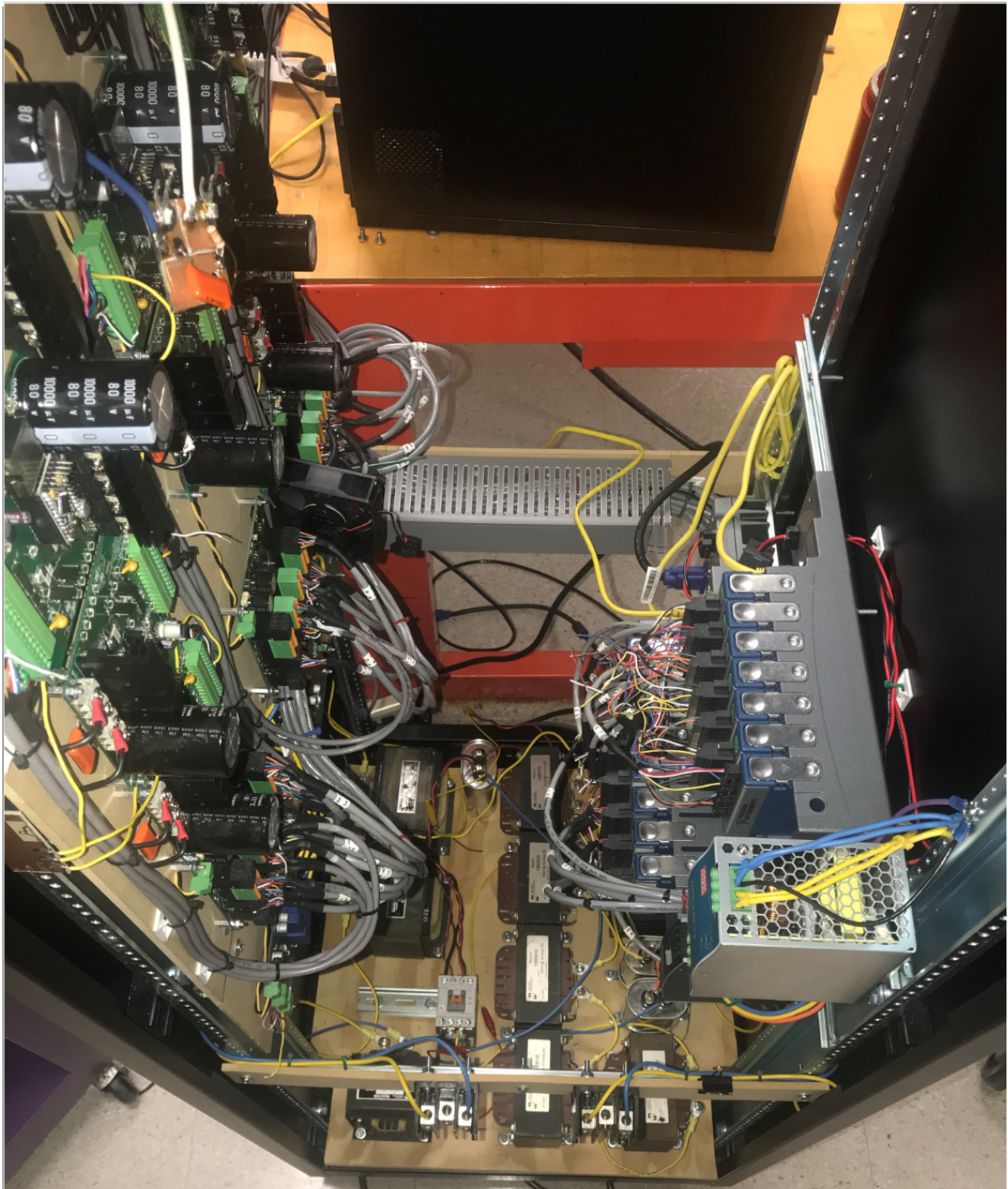
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