NOTE TO USERS

SPACE VECTOR MODULATION FOR

THREE-LEVEL NEUTRAL POINT CLAMPED INVERTER

By

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SPACE VECTOR MODULATION FOR THREE-LEVEL NEUTRAL POINT CLAMPED INVERTER

ABSTRACT

For most medium voltage high power applications, Neutral Point Clamped (NPC) three-level inverter is a preferred choice due to its advantages such as low cost, light weight and compact size. Space vector modulation is widely used in real-time digital control for power converters. It is especially suitable for use in NPC multilevel inverters due to its good harmonic profile, flexibility and easy digital implementation. This thesis focuses on the space vector modulation for high power three-level NPC inverter, where the switching frequency of the semiconductor devices is normally below 1000Hz to reduce the power loss of the switching devices.

The conventional space vector modulation (SVM) scheme for the three-level NPC inverter produces even order harmonics in the output voltages, which are not desirable for most industrial applications. In this thesis, the mechanism of even order harmonic generation is analyzed. A new space vector modulation scheme, which can eliminate all the even order harmonics, is proposed. The performance of the new design is investigated and simulation results are provided for the verification purpose. The harmonic and THD profiles are compared with those of the conventional SVM scheme. The elimination of even order harmonics is achieved at the expense of a slight increase in the switching frequency. The proposed space vector modulation scheme can be applied to other types of converters for

the even order harmonic elimination.

An algorithm is developed to mitigate the neutral point potential deviation, which is a common problem in the NPC inverters. The simulation results show that this algorithm is suitable for both conventional and the proposed space vector modulation schemes.

ACKNOWLEDGEMENTS

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Chapter 1

Introduction

With the technology advancements in semiconductor devices such as high-voltage insulated gate bipolar transistors (IGBT) and gate controlled thyristors (GCT), modern multi-megawatt variable frequency drives are increasingly used in petrochemical, mining, steel & metals, transportation and other industries to conserve electric energy, increase productivity and improve product quality.

There are a number of high-power drive manufacturers around the world, including ABB (Switzerland), Siemens (Germany), Toshiba (Japan), Rockwell Automation (Canada), General Electric (US), ASI Robicon (US) and Alstom (France). These companies use various power converter technologies in their drive products. For instance, ABB produces three-level neutral point clamped inverter fed drives, Rockwell manufactures GCT current source inverter based drives, Robicon promotes cascaded H-bridge multilevel inverter technology, Toshiba uses multilevel NPC/H-bridge hybrid inverters, and Alstom is developing flying-capacitor multilevel inverter drives. All these drive systems operate at medium voltage (MV) levels, typically from 2300V to 7200V. This thesis focuses on high power three-level neutral point clamped inverter using space vector modulation with even order harmonic elimination.

1.1 Multilevel Voltage Source Inverter Fed Drives

1.1.1 Neutral Point Clamped Inverters Fed Drives

A simplified configuration of a three-level neutral point clamped (NPC) inverter fed drive is shown in Fig. 1.1. Some manufacturers use GCTs as switching devices while others use IGBTs or injection enhanced gate transistors (IEGT) in the inverter [1-3]. The device switching frequency is normally around 500Hz. In the dc link, the dc capacitor is split into two, providing a neutral point *N*. The diodes connected to the neutral point are referred to as clamping diodes, which clamp the inverter terminal voltage to the neutral point potential. Due to the clamping function of the diodes, the maximum voltage on each of the switches is *E*, which is half of the dc link voltage for the three-level inverter.

Depending on the drive system design requirements, it is optional to use one or two DC voltage sources [1,2]. With two DC voltage sources, the dc capacitor voltage is fixed. Otherwise, the dc capacitor voltage is floating, and certain measures should be in place to minimize the neutral point potential deviation.

The three-level NPC inverter based drive offers the following features and drawbacks.

- **No Dynamic Voltage Sharing Problem.** The switches in the NPC inverter do not have dynamic voltage sharing problem mainly due to the use of clamping diodes;
- **Low Harmonics Distortion.** The inverter is capable of producing three-level inverter terminal voltages with respect to the neutral pint *N* and five-level line-to-line voltages. Compared with the conventional two-level inverter, the NPC inverter is able to produce better output voltage waveforms with lower THD;

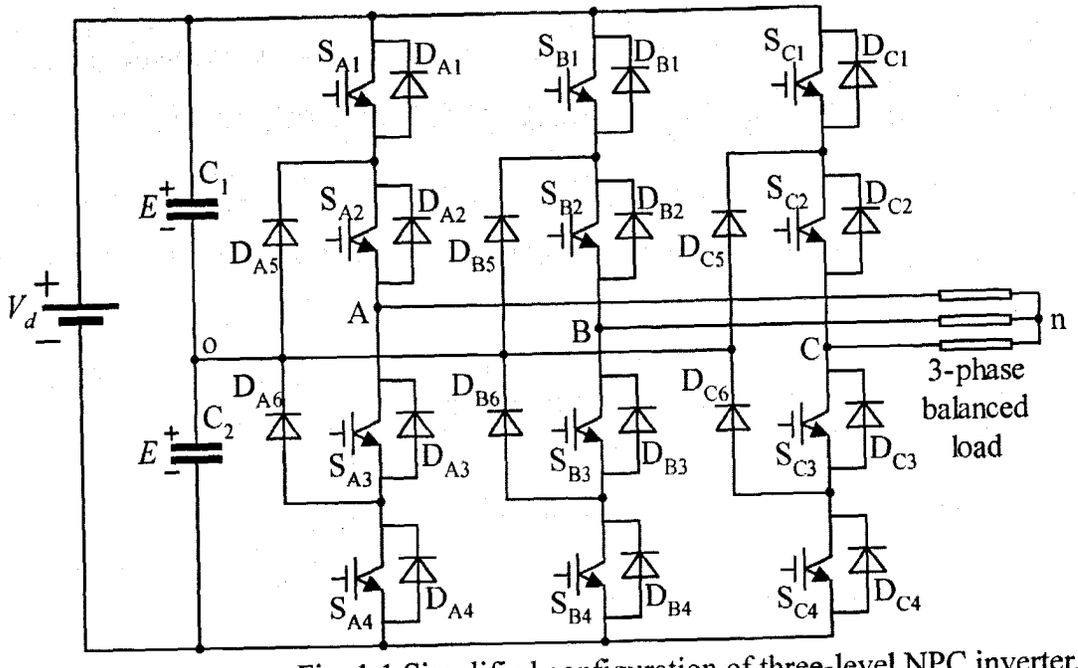
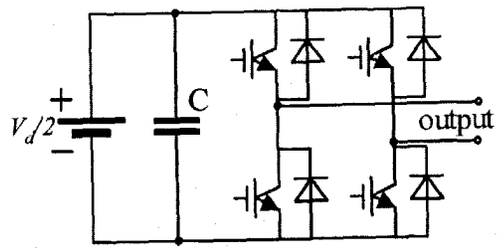
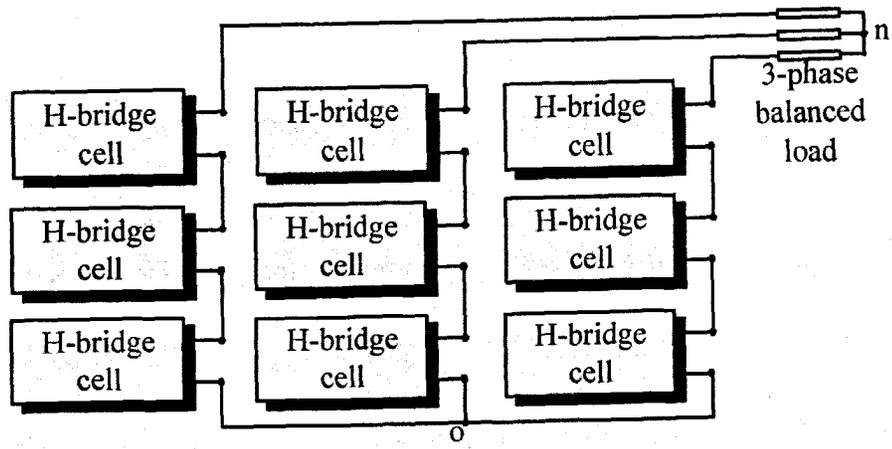


Fig. 1.1 Simplified configuration of three-level NPC inverter.



(a) Power cell for cascaded H-bridge inverter



(b) Topology of seven-level cascaded H-bridge inverter

Fig. 1.2 Simplified topologies of cascaded H-bridge multilevel inverter.

- **Provision for four-quadrant operation**. Majority of the MV drives do no need regenerative operation capability. For more advanced applications where regeneration capability is necessary, the same topology can be applied to the rectifier working as the DC voltage source;

- **Possible neutral point potential deviation**. With the neutral potential left floating [2], the neutral point potential may vary and the dc link voltage may not be equally divided between the two dc capacitors. Special measures should be taken when designing the PWM schemes to prevent such deviations, which makes the PWM pattern design more complicated; and

- **Additional clamping diodes**. The NPC inverter requires clamping diodes. The number of clamping diodes can be calculated by $3(m\text{-}1)(m\text{-}2)$, where m is the number of voltage levels. For a three-, four- or five-level NPC inverter, the number of the clamping diodes is 6, 18 and 36, respectively. The substantial increase in the clamping diodes makes the four-level and five-level inverters impractical for industrial use.

1.1.2 Cascaded H-bridge Inverter Based Drive

Cascaded H-bridge multilevel inverter is one of the popular converter topologies used in megawatt drives [4-6]. It is composed of multiple units of power cells as shown in Fig. 1.2(a). Each power cell is mainly composed of an H-bridge inverter powered by a three-phase diode rectifier connected to an isolated secondary winding of a phase shafting (zigzag) transformer.

The power cells in one inverter phase are normally connected in cascade on their ac output side to achieve high voltage operation and low harmonic distortion. The number of power cells in a drive is mainly determined by the operating voltage and manufacturing cost. For

instance, in ac drives with a rated line-to-line voltage of 2300V, the seven-level inverter in Fig. 1.2(b) can be used, where the inverter has a total of nine power cells using 600V class components [4]. The use of identical power cells leads to a modular structure, which is an effective means for cost reduction. The number of voltage levels in a cascaded H-bridge inverter, m, can be found from $m=(2H+1)$, where H is the number of H-bridge cells per phase. The cascaded H-bridge inverters with seven to eleven voltage levels are most widely used in industry.

The multilevel inverter requires a number of isolated dc supplies, each of which feeds a power cell. The dc supplies are normally obtained from multipulse diode rectifiers [7]. For the seven- and nine- and eleven-level inverters, 18-, 24- and 30-pulse diode rectifiers can be used, respectively.

The cascaded H-bridge multilevel inverter fed drive has a number of features, including:

- **Low voltage THD and dv/dt**. The inverter output voltage waveform is formed by several small voltage steps (levels), and distributed sinusoidally over time, resulting in a low THD and dv/dt;
- **Modular structure**. The multilevel inverter is composed of multiple units of identical H-bridge power cells, which is an effective means for reducing the manufacturing cost;
- **High voltage operation without switching devices in series**. The power cells are connected in cascade to withstand high ac voltages. There are no voltage sharing problems among the switching devices;
- **Low line current THD**. The low-order harmonic currents produced by diode rectifiers are cancelled by the phase shifting transformer, assuring compliance with IEEE Standard 519-1992; and

- **Optional degrees of redundancy**. The modular nature of the drive allows optional degrees of redundancy. An electronic bypass switch can short the output of a defective power cell such that the current from the remaining cells can reach the motor.

There are some drawbacks associated with the drive:

- **A large number of isolated dc supplies**. The dc supplies for the cascaded H-bridge inverter are usually obtained from a multipulse diode rectifier employing an expensive phase shifting transformer with a nine to eighteen sets of secondary windings;
- **Large number of cables**. The cascaded H-bridge inverter fed drive require 27 to 54 cables connecting the transformer secondary windings to the power cells. It is expensive to place the transformer away from the drive. If the transformer can be located outside the electrical equipment room, the physical space for the drive can be smaller, and the losses from the transformer are not dissipated into the electrical room, allowing a much lower rating for the room's cooling equipment; and
- **No regenerative operation capability**. None of the cascaded H-bridge inverter fed drives currently operating in the field has regenerative operation capability. It is technically possible to design a multilevel regenerative PWM rectifier that provides isolated dc supplies for the inverter [8,9]. However, the manufacturing cost of such a drive will be too high to be accepted by its user.

1.1.3 Flying Capacitor Inverter Fed Drive

As shown in Fig. 1.3, the flying-capacitor multilevel inverter can be easily constructed by adding dc capacitors to the two-level inverter [10]. Therefore, it preserves some of the features of the two-level inverter such as modular design. Like other multilevel inverters, the flying-capacitor inverter also features low THD and dv/dt in the inverter output voltage.

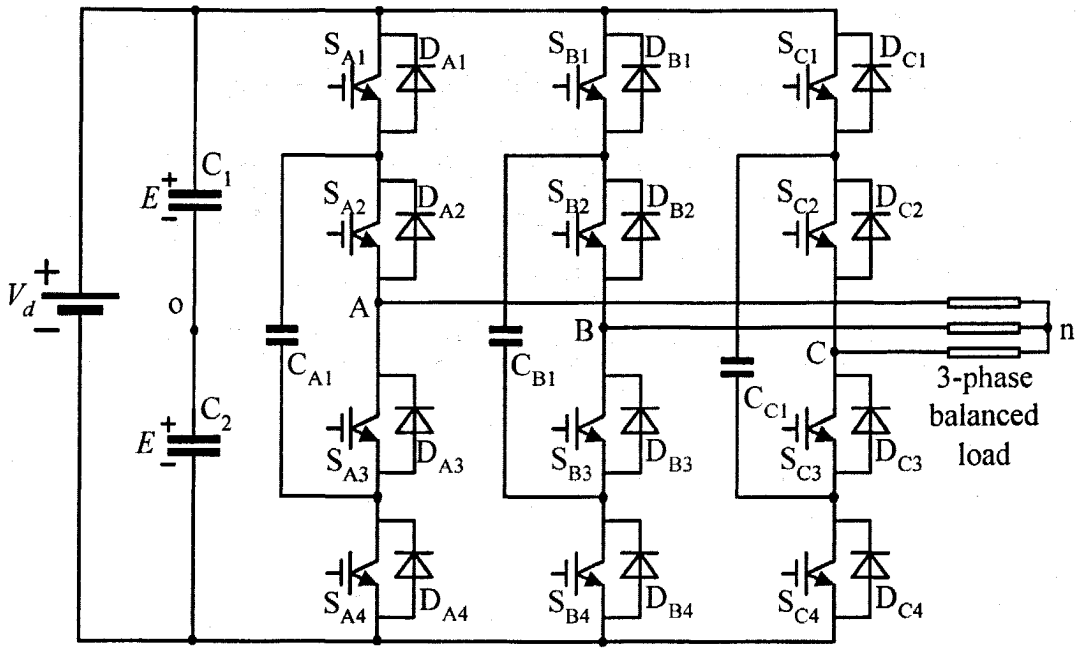


Fig. 1.3 Simplified power circuit of three-level flying capacitor inverter.

The main drawbacks include a) difficulties to balance the voltages on the dc capacitors, b) complex switching pattern design, and c) necessity of isolated pre-charging circuits for the dc capacitors. It is these drawbacks that prevent this topology from a widespread application in high-power drive systems.

1.2 Modulation Techniques for the High Power Multilevel Inverter

The modulation schemes for the multilevel voltage source inverters can be generally classified into carrier based modulation and space vector modulation.

1.2.1 Carrier Based Modulation

There are two commonly-used carrier based modulation schemes: phase-shifted and voltage-shifted modulations. In general, a multilevel inverter with m voltage levels requires $(m-1)$ triangular carriers. The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with the carrier waves.

a) Phase-shifted Modulation

All the triangular carriers of phase-shifted modulation have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by $\phi_{cr} = 360°/(m-1)$. Fig. 1.4 shows the principle of the phase-shifted modulation for the seven-level cascaded H-bridge inverter. The triangular carriers v_{cr1} to v_{cr6} are compared with phase A modulation wave v_{mA} to generate gate signals.

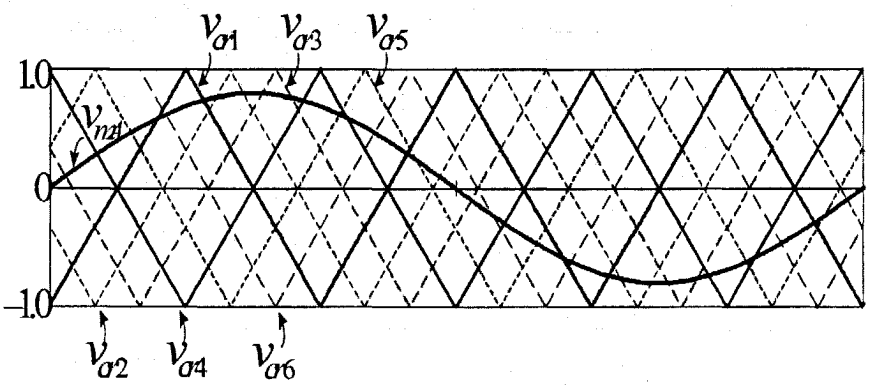


Fig. 1.4 Phase-shifted modulation scheme for a seven-level inverter.

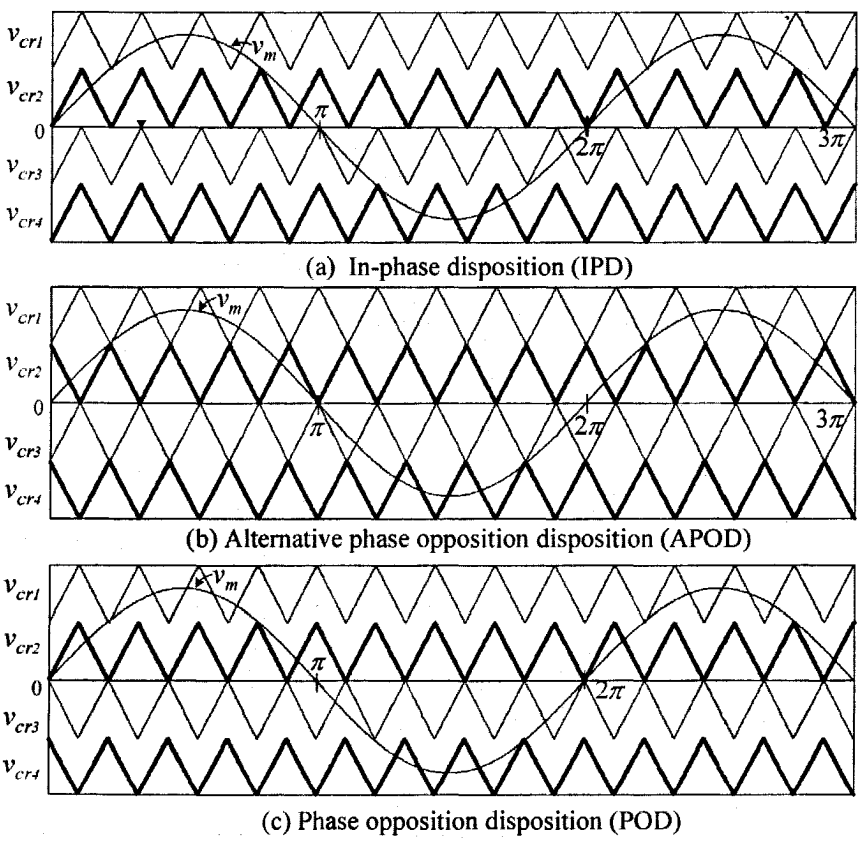


Fig. 1.5 Voltage-shifted modulation schemes for a five-level inverter.

b) Voltage-shifted Modulation

All of the (m-1) triangular carriers of voltage shifted modulation have the same frequency and amplitude. They are vertically disposed such that the bands they occupy are contiguous. Fig. 1.5 shows three schemes for the voltage-shifted modulation for a five-level inverter: (a) In-Phase Disposition (IPD), where all carriers are in phase; (b) Alternative Phase Opposition Disposition (APOD), where all carriers are alternatively in opposition disposition; and (c) Phase Opposition Disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference.

1.2.2 Space Vector Modulation

Space vector modulation (SVM) is one of the preferred real-time modulation techniques and is widely used for digital control of rectifiers and inverters. For a given inverter (or rectifier) topology, there are a certain number of switching states. Each switching state produces a defined inverter output voltage, which can be represented by stationary voltage vectors in space. A collection of all the space vectors forms a space vector diagram. A reference voltage vector rotates in space within the space vector diagram. For a given position in space, the reference vector can be approximated by three nearest stationary vectors, based on which the gating signals for the switches in the inverter can be generated. Therefore, when the reference vector rotates in space for one revolution, the inverter output voltage changes one fundamental cycle. The magnitude of the inverter fundamental output voltage corresponds to length of the reference vector while its frequency corresponds to the rotating speed of the reference vector. [11, 12] For the three-level NPC inverter, the space vector diagram is shown in Fig. 1.6.

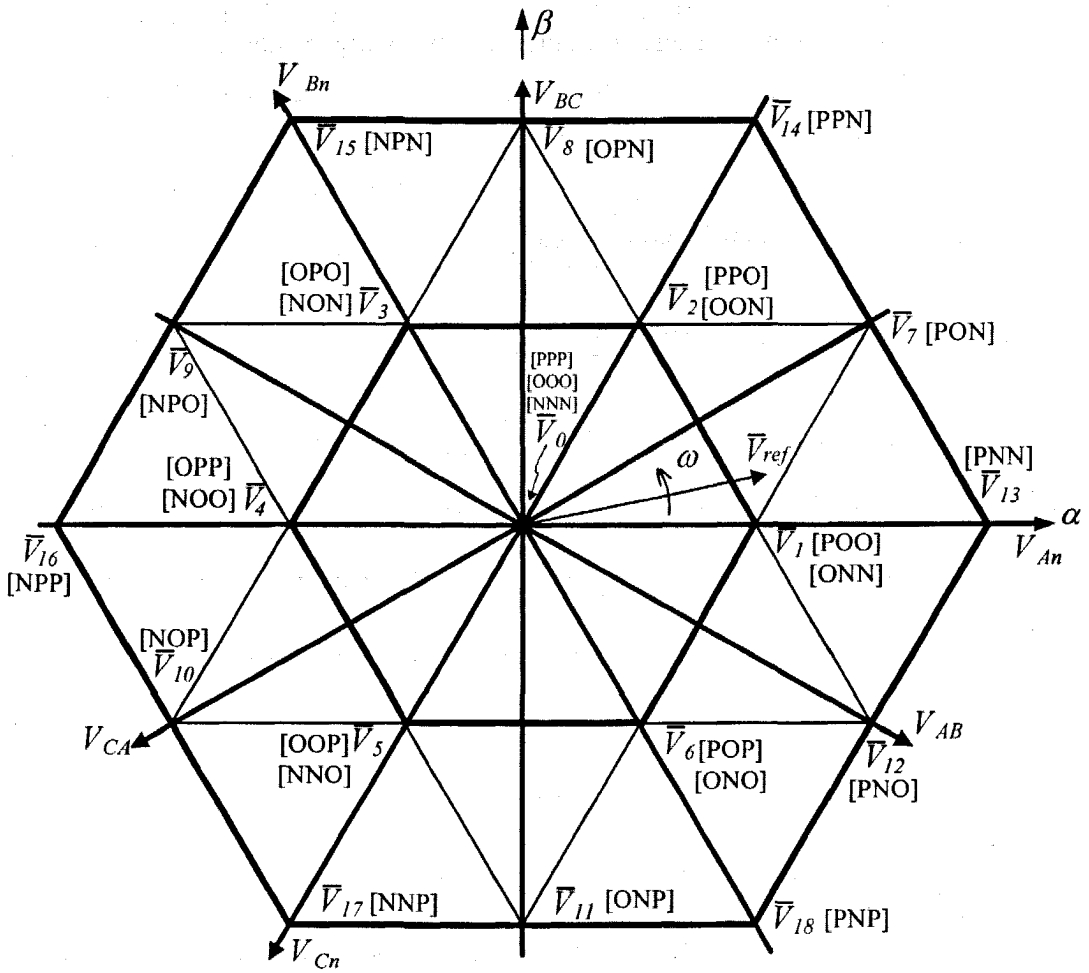


Fig. 1.6 Space vectors ($\overline{V}_0 \sim \overline{V}_{18}$) and reference vector ($\overline{V}_{ref}$) for three-level inverters.

The space vector modulation in general provides the following features:

- Low harmonics distortion,
- Effective neutral point potential control, and
- Easy digital implementation.

However, the traditional space vector modulation scheme produces even order harmonics in the output voltages of the multilevel inverter, which is not desired for most industrial applications. Especially, if SVM scheme is used for three-level NPC rectifier, it produces even order harmonics in the input currents, which can not satisfy the IEEE standards 519-1992. These standards are included in Appendix I for reference. The problem of even order harmonics can be solved by a new scheme proposed in this thesis.

1.3 Research Objectives

The simulation investigations find that the undesired even order harmonics are produced by the traditional space vector modulation for three-phase three-level NPC inverter. From literature survey, it was found that the generation mechanism of the even harmonics had not been studied and there is neither any algorithm to solve this problem. Furthermore, the deviation of the neutral point potential should also be mitigated for the three-level NPC inverter. Hence, the objectives of this thesis are to

- reveal the generation mechanism of the even order harmonics in the output voltages of the traditional space vector modulated three-phase three-level NPC SVM inverter,
- develop a new SVM scheme to eliminate the even order harmonics in the three-level NPC inverter, and

- develop a control algorithm to correct the neutral point potential deviation in the three-level NPC inverter.

1.4 Thesis outline

This thesis consists of five chapters. In the first chapter, a critical review on high power multilevel inverters and modulations schemes is conducted, and the objectives of the thesis are presented.

Chapter 2 introduces the three-phase three-level NPC inverter and the principle of the SVM. Following the discussion of the power circuit and switching states of the NPC inverter, the space vectors corresponding to the inverter switching states are presented. The dwell time calculation and switching pattern design are introduced. The impacts of the redundant switching states to the neutral point potential are analyzed. A closed-loop control algorithm is developed to correct the deviation of the inverter neutral point potential.

Chapter 3 investigates the performance of the three-level NPC SVM inverter by simulations. The Simulink models for the proposed power circuit and SVM scheme are simulated. The harmonic analyses are conducted to obtain the THD profiles. The closed-loop control of the neutral point potential is verified.

Chapter 4 presents the elimination of the even order harmonics in the output voltages of the NPC inverter. The mechanism of the even order harmonic generation in the traditional SVM method is revealed. A new SVM scheme is developed for the elimination of the even order harmonics. The effectiveness of the new scheme is verified by simulations. The closed-loop control for the neutral point potential is demonstrated that the neutral point potential deviations can be cancelled.

Chapter 5 provides the conclusions of this thesis research and suggestions for the future study.

Chapter 2

Space Vector Modulation for Three-Level Neutral Point Clamped Inverter

Space Vector Modulation (SVM) is one of the preferred modulation schemes used in three-level Neutral Point Clamped (NPC) inverter, which can offer good harmonic profile, extended linear operation range, effective neutral point potential control and easy digital implementation. In SVM, a reference vector is approximated by the nearest stationary space vectors, which represent the switching states of the inverter. Therefore, the amplitudes of the inverter output voltages can be controlled by the magnitude of the reference vector while the fundamental frequency corresponds to the rotating speed of the reference vector.

This chapter presents the general principle of the space vector modulation for three-level neutral point clamped inverter. The circuit structure and the switching states of the three-level NPC inverter are introduced. The space vectors, reference vector, dwell time calculation, switching state sequence, and neutral point potential control of the NPC inverter are also presented.

2.1 Three-level Neutral Point Clamped Inverter

The three-level NPC inverter features higher operating voltage without devices in series, better output voltage THD, and lower electromagnetic interference (EMI). Therefore, it is increasingly used in high power applications. In this section, the power circuit and the switching states of this type of inverter are introduced.

2.1.1 Power Circuit of Three-Level NPC Inverter

The simplified power circuit of three-level NPC inverter is shown in Fig. 2.1. There are four switching devices (S_{X1}~S_{X4}), four anti-parallel diodes (D_{X1}~D_{X4}) and two clamping diodes (D_{X5} and D_{X6}) in each leg, where the subscript X represents legs A, B or C, respectively. For example, S_{A1} stands for the switching device in leg A connected to the positive bus. The DC capacitor splits into two to produce a neutral point o, so that a single DC voltage source can be used in the three-level NPC inverter. If two identical DC voltage sources are connected to the inverter as shown in Fig. 2.2 (a), the neutral point potential is fixed at zero. However, when a single DC voltage source is used as shown in Fig. 2.2 (b), deviations of the neutral point potential may occur. It causes unbalanced voltage stress on the switching devices and also introduces some undesired harmonics to the output voltages. Therefore the performance of the inverter is deteriorates. A solution to this problem will be discussed in detail in Section 2.2.5.

2.1.2 Per-phase Switching States

In three-level NPC inverters, the phase voltage is defined as the voltage between the phase output and the neutral point o, and is determined by three per-phase switching states, [P], [O] and [N], which are shown in Fig. 2.3.

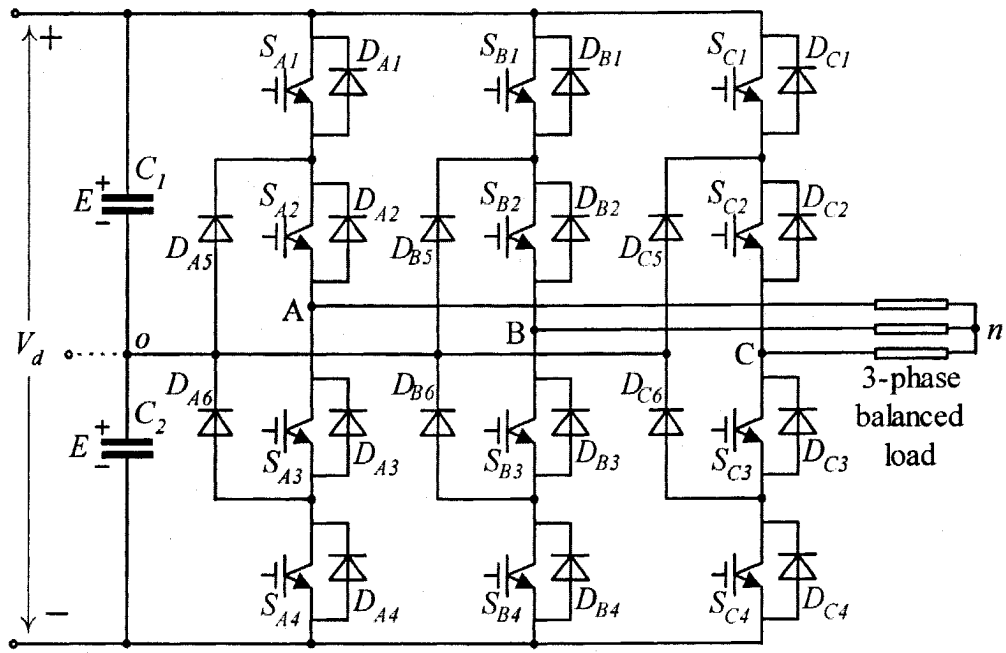
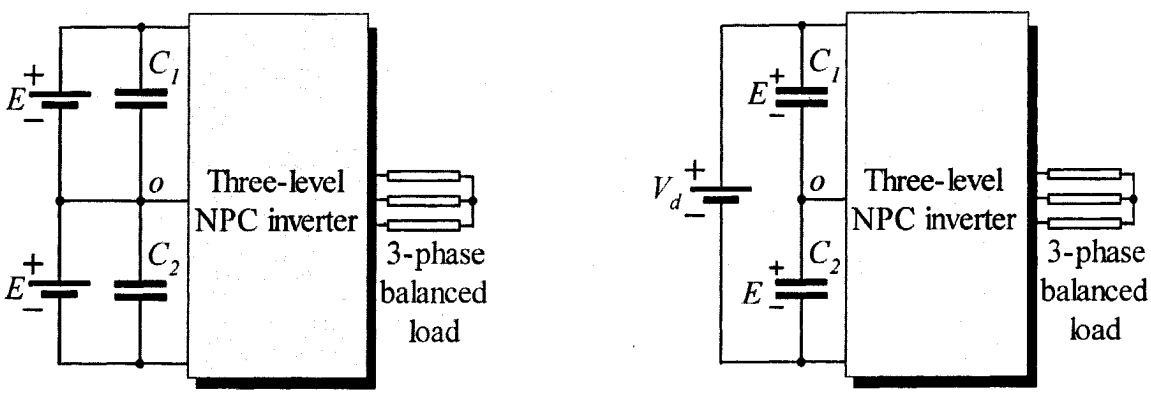


Fig. 2.1 Simplified power circuit of NPC three-level inverter.



(a) two identical DC voltage sources

(b) one DC voltage source

Fig. 2.2 Two options of the DC voltage source.

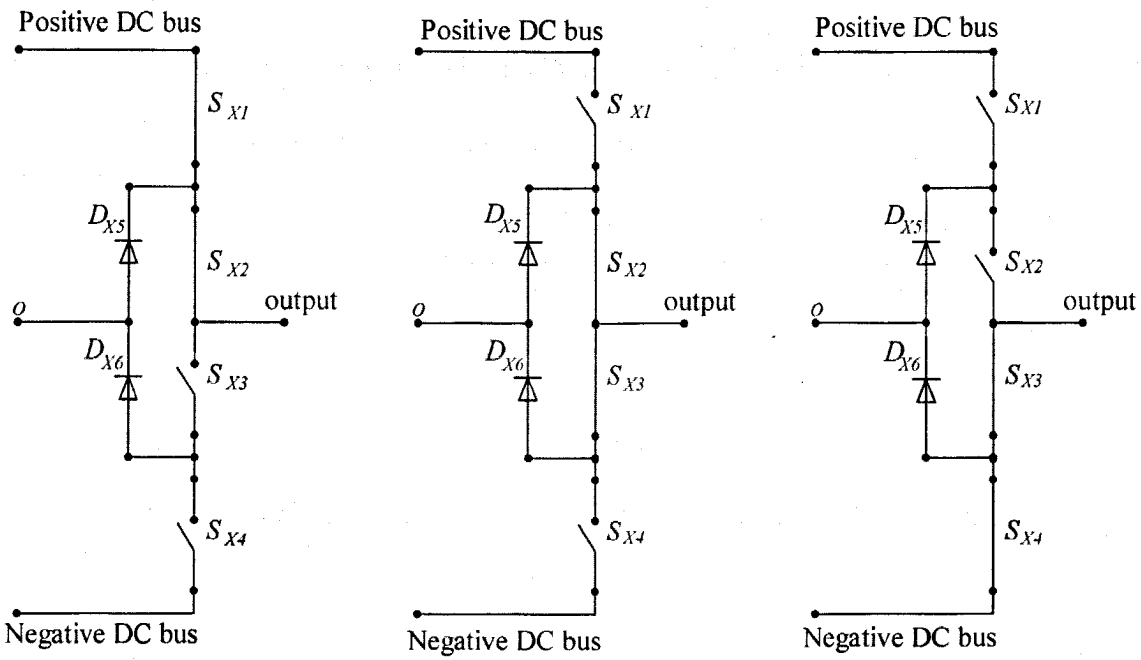


Fig. 2.3 Three switching states of each phase.

Table 2-1 Switching states of each phase in three-level NPC inverter

Switching state	S_{X1}	S_{X2}	S_{X3}	S_{X4}	Inverter phase voltage V_{Xo}
[P]	On	On	Off	Off	$+V_d/2$
[O]	Off	On	On	Off	0
[N]	Off	Off	On	On	$-V_d/2$

- **[P] state**

In this state, the upper two switching devices, S_{X1} and S_{X2}, are on and the lower two, S_{X3} and S_{X4}, are off. Since the upper clamping diode D_{X5} is reversely biased, it is turned off. The anode of the lower clamping diode D_{X6} is floated because of the off-state of S_{X3} and S_{X4}. Thus the output of the phase is connected to the positive DC bus through S_{X1} and S_{X2}. As a result, the phase voltage is $+V_d/2$.

- **[O] state**

In this state, S_{X1} and S_{X4} are off while S_{X2} and S_{X3} are on. The output of the phase is connected to neither positive pole nor negative pole of the DC link. When the phase current is positive (flowing out of inverter), the current can flow through D_{X5} and S_{X2} from the inverter neutral point, so that the output voltage is clamped at neutral point. Similarly, when the phase current is negative (flowing into inverter), D_{X6} and S_{X3} clamp the output voltage to zero. Therefore, the phase output voltage in this state is clamped at zero.

- **[N] state**

In this state, S_{X1} and S_{X2} are turned off, while S_{X3} and S_{X4} are in on-state. As reversely biased, D_{X6} is inconductive. S_{X1} and S_{X2} disconnect the cathode of D_{X5}. S_{X3} and S_{X4} connect the output to the negative DC bus. Hence, the output phase voltage is $-V_d/2$ in this state.

The above discussed three per-phase switching states are listed in Table 2-1. It can be observed that the operations of switching devices in the same leg, such as a pair of S_{X1} and S_{X3} or a pair of S_{X2} and S_{X4}, are complementary. When one of them in a pair is switched on, the other in the same pair must be off. The both-on or both-off situation of the complementary devices is not allowed.

The transition between [P] state and [N] state is prohibited. Therefore, the dynamic voltage

sharing problem could be avoided in the three-level NPC inverter. Furthermore, the magnitude of step changes of the output voltages in the three-level NPC inverter is $V_d/2$, which is only half of that in traditional two-level inverters. As a result, less EMI is generated.

2.1.3 Inverter Switching States

Since the proposed NPC inverter has three per-phase switching states, there exist 27 switching states in the three-phase inverter, which are shown in Table 2-2.

In Table 2-2, the three capital letters in the brackets represent the switching states of inverter legs A, B and C. For example, the inverter switching state [PON] means phase A is in [P] state, phase B is in [O] state and phase C is in [N] state. Thus the inverter phase voltages, v_{Ao}, v_{Bo} and v_{Co}, are $V_d/2$, 0 and - $V_d/2$, respectively.

The line-to-line voltages, v_{AB}, v_{BC} and v_{CA}, can be obtained through the inverter phase voltages:

$$\begin{cases} v_{AB} = v_{Ao} - v_{Bo} \\ v_{BC} = v_{Bo} - v_{Co} \\ v_{CA} = v_{Co} - v_{Ao} \end{cases} \tag{2.1-1}$$

The voltage between the 3-phase balanced load neutral point n and the inverter neutral point o is:

$$v_{no} = (v_{Ao} + v_{Bo} + v_{Co})/3 \tag{2.1-2}$$

And the phase voltages of 3-phase balanced load can be obtained by either:

$$\begin{cases} v_{An} = v_{Ao} - v_{no} \\ v_{Bn} = v_{Bo} - v_{no} \\ v_{Cn} = v_{Co} - v_{no} \end{cases} \tag{2.1-3}$$

Table 2-2 Three-phase switching states of three-level NPC inverter

Group No.	Switching state [ABC]	Inverter phase voltage			Line-to-line voltages			Load neutral voltage	Load phase voltages		
		v_{Ao}	v_{Bo}	v_{Co}	v_{AB}	v_{BC}	v_{CA}	v_{no}	v_{An}	v_{Bn}	v_{Cn}
0	[NNN]	$-V_d/2$	$-V_d/2$	$-V_d/2$	0	0	0	$-V_d/2$	0	0	0
	[OOO]	0	0	0				0			
	[PPP]	$V_d/2$	$V_d/2$	$V_d/2$				$V_d/2$			
1	[POO]	$V_d/2$	0	0	$V_d/2$	0	$-V_d/2$	$V_d/6$	$V_d/3$	$-V_d/6$	$-V_d/6$
	[ONN]	0	$-V_d/2$	$-V_d/2$				$-V_d/3$			
2	[PPO]	$V_d/2$	$V_d/2$	0	0	$V_d/2$	$-V_d/2$	$V_d/3$	$V_d/6$	$V_d/6$	$-V_d/3$
	[OON]	0	0	$-V_d/2$				$-V_d/6$			
3	[OPO]	0	$V_d/2$	0	$-V_d/2$	$V_d/2$	0	$V_d/6$	$-V_d/6$	$V_d/3$	$-V_d/6$
	[NON]	$-V_d/2$	0	$-V_d/2$				$-V_d/3$			
4	[OPP]	0	$V_d/2$	$V_d/2$	$-V_d/2$	0	$V_d/2$	$V_d/3$	$-V_d/3$	$V_d/6$	$V_d/6$
	[NOO]	$-V_d/2$	0	0				$-V_d/6$			
5	[OOP]	0	0	$V_d/2$	0	$-V_d/2$	$V_d/2$	$V_d/6$	$-V_d/6$	$-V_d/6$	$V_d/3$
	[NNO]	$-V_d/2$	$-V_d/2$	0				$-V_d/3$			
6	[POP]	$V_d/2$	0	$V_d/2$	$V_d/2$	$-V_d/2$	0	$V_d/3$	$V_d/6$	$-V_d/3$	$V_d/6$
	[ONO]	0	$-V_d/2$	0				$-V_d/6$			
7	[PON]	$V_d/2$	0	$-V_d/2$	$V_d/2$	$V_d/2$	$-V_d$	0	$V_d/2$	0	$-V_d/2$
8	[OPN]	0	$V_d/2$	$-V_d/2$	$-V_d/2$	V_d	$-V_d/2$	0	0	$V_d/2$	$-V_d/2$
9	[NPO]	$-V_d/2$	$V_d/2$	0	$-V_d$	$V_d/2$	$V_d/2$	0	$-V_d/2$	$V_d/2$	0
10	[NOP]	$-V_d/2$	0	$V_d/2$	$-V_d/2$	$-V_d/2$	V_d	0	$-V_d/2$	0	$V_d/2$
11	[ONP]	0	$-V_d/2$	$V_d/2$	$V_d/2$	$-V_d$	$V_d/2$	0	0	$-V_d/2$	$V_d/2$
12	[PNO]	$V_d/2$	$-V_d/2$	0	V_d	$-V_d/2$	$-V_d/2$	0	$V_d/2$	$-V_d/2$	0
13	[PNN]	$V_d/2$	$-V_d/2$	$-V_d/2$	V_d	0	$-V_d/2$	$-V_d/6$	$2V_d/3$	$-V_d/3$	$-V_d/3$
14	[PPN]	$V_d/2$	$V_d/2$	$-V_d/2$	0	V_d	$-V_d$	$V_d/6$	$V_d/3$	$V_d/3$	$-2V_d/3$
15	[NPN]	$-V_d/2$	$V_d/2$	$-V_d/2$	$-V_d$	V_d	0	$-V_d/6$	$-V_d/3$	$2V_d/3$	$-V_d/3$
16	[NPP]	$-V_d/2$	$V_d/2$	$V_d/2$	$-V_d$	0	V_d	$V_d/6$	$-2V_d/3$	$V_d/3$	$V_d/3$
17	[NNP]	$-V_d/2$	$-V_d/2$	$V_d/2$	0	$-V_d$	V_d	$-V_d/6$	$-V_d/3$	$-V_d/3$	$2V_d/3$
18	[PNP]	$V_d/2$	$-V_d/2$	$V_d/2$	V_d	$-V_d$	0	$V_d/6$	$V_d/3$	$-2V_d/3$	$V_d/3$

or:

$$\begin{cases} v_{An} = (v_{AB} - v_{CA})/3 \\ v_{Bn} = (v_{BC} - v_{AB})/3 \\ v_{Cn} = (v_{CA} - v_{BC})/3 \end{cases} \tag{2.1-4}$$

According to the line-to-line voltages and the load phase voltages, the inverter switching states are classified into 19 groups as shown in Table 2-2, in which some groups have two or three inverter switching states although their inverter phase voltages are different. Particularly, group 0 has three inverter switching states, and each of group 1 to group 6 contains two switching states.

2.2 Space Vector Modulation

This section presents the general principles of the SVM applied in the presented three-phase three-level NPC inverter. The space vectors, reference vector, dwell time calculation, space vector selection and switching state sequence of the inverter are discussed. A mitigation algorithm for solving neutral point potential deviations is proposed in detail as well.

2.2.1 Space Vectors of Three-Level NPC Inverter

According to the 3-phase-to-2-phase frame transformation [11], the output voltages of the three-phase three-level NPC inverter can be represented by space vectors in the α-β frame:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{3} \\ 0 & \sin\frac{2\pi}{3} & \sin\frac{4\pi}{3} \end{bmatrix}\begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} \tag{2.2-1}$$

where v_α and v_β are the real and imaginary components of the space vector.

The space vector can be written as:

$$\overline{V} = | \overline{V} | e^{j\gamma} \quad (2.2\text{-}2)$$

where $| \overline{V} | = \sqrt{v_\alpha^2 + v_\beta^2}$, (2.2-3)

$$\gamma = \tan^{-1}\left(\frac{v_\beta}{v_\alpha}\right), \quad (2.2\text{-}4)$$

$| \overline{V} |$ is the magnitude, and γ is the phase angle of the space vector.

Based on Eqs. (2.2-1) to (2.2-4), space vectors corresponding to the switching states of the inverter can be obtained as shown in Table 2-3. Eq. (2.2-1) is used to calculate the α and β components of the space vectors, after substituting the load phase voltages produced by the switching states. The magnitude and the phase angle of the space vectors can be obtained from Eqs. (2.2-3) and (2.2-4), respectively. For instance, the load phase voltages in switching state [PON] are $V_d/2$, 0 and $-V_d/2$. Substituting them into Eq. (2.2-1), v_α and v_β are obtained as $V_d/2$ and $\sqrt{3}\,V_d/6$. According to Eq. (2.2-2), the space vector corresponding to this switching state is $\sqrt{3}\,V_d/3\, e^{j\pi/6}$, where the magnitude is $\sqrt{3}\,V_d/3$, and the phase angle is $\pi/6$. In Table 2-3, this space vector is shown as $\overline{V}_7$, which is corresponding to the switching state [PON]. Other space vectors can be acquired similarly. Fig. 2.4 illustrates the diagram of all space vectors, which are listed in Table 2-3.

Based on their magnitudes, the 19 space vectors correspond to the 27 switching states of the three-level NPC inverter, which can be further classified into four types, zero vector, small vectors, medium vectors, and large vectors, as shown in Table 2-3 and Fig. 2.4.

Table 2-3 Space vectors and corresponding switching states

space vector						Switching state	Load phase voltages		
Name		V_α	V_β	Magnitude	Phase angle		v_{An}	v_{Bn}	v_{Cn}
$\bar{V}_0$		0	0	0	0	[PPP] [OOO] [NNN]	0	0	0
$\bar{V}_1$	$\bar{V}_{1P}$ $\bar{V}_{1N}$	$V_d/3$	0	$V_d/3$	0	[POO] [ONN]	$V_d/3$	$-V_d/6$	$-V_d/6$
$\bar{V}_2$	$\bar{V}_{2P}$ $\bar{V}_{2N}$	$V_d/6$	$\sqrt{3}\,V_d/6$		$\pi/3$	[PPO] [OON]	$V_d/6$	$V_d/6$	$-V_d/3$
$\bar{V}_3$	$\bar{V}_{3P}$ $\bar{V}_{3N}$	$-V_d/6$	$\sqrt{3}\,V_d/6$		$2\pi/3$	[OPO] [NON]	$-V_d/6$	$V_d/3$	$-V_d/6$
$\bar{V}_4$	$\bar{V}_{4P}$ $\bar{V}_{4N}$	$-V_d/3$	0		π	[OPP] [NOO]	$-V_d/3$	$V_d/6$	$V_d/6$
$\bar{V}_5$	$\bar{V}_{5P}$ $\bar{V}_{5N}$	$-V_d/6$	$-\sqrt{3}\,V_d/6$		$4\pi/3$	[OOP] [NNO]	$-V_d/6$	$-V_d/6$	$V_d/3$
$\bar{V}_6$	$\bar{V}_{6P}$ $\bar{V}_{6N}$	$V_d/6$	$-\sqrt{3}\,V_d/6$		$5\pi/3$	[POP] [ONO]	$V_d/6$	$-V_d/3$	$V_d/6$
$\bar{V}_7$		$V_d/2$	$\sqrt{3}\,V_d/6$	$\sqrt{3}\,V_d/3$	$\pi/6$	[PON]	$V_d/2$	0	$-V_d/2$
$\bar{V}_8$		0	$\sqrt{3}\,V_d/3$		$\pi/2$	[OPN]	0	$V_d/2$	$-V_d/2$
$\bar{V}_9$		$-V_d/2$	$\sqrt{3}\,V_d/6$		$5\pi/6$	[NPO]	$-V_d/2$	$V_d/2$	0
$\bar{V}_{10}$		$-V_d/2$	$-\sqrt{3}\,V_d/6$		$7\pi/6$	[NOP]	$-V_d/2$	0	$V_d/2$
$\bar{V}_{11}$		0	$-\sqrt{3}\,V_d/3$		$3\pi/2$	[ONP]	0	$-V_d/2$	$V_d/2$
$\bar{V}_{12}$		$V_d/2$	$-\sqrt{3}\,V_d/6$		$11\pi/6$	[PNO]	$V_d/2$	$-V_d/2$	0
$\bar{V}_{13}$		$2V_d/3$	0	$2V_d/3$	0	[PNN]	$2V_d/3$	$-V_d/3$	$-V_d/3$
$\bar{V}_{14}$		$V_d/3$	$\sqrt{3}\,V_d/3$		$\pi/3$	[PPN]	$V_d/3$	$V_d/3$	$-2V_d/3$
$\bar{V}_{15}$		$-V_d/3$	$\sqrt{3}\,V_d/3$		$2\pi/3$	[NPN]	$-V_d/3$	$2V_d/3$	$-V_d/3$
$\bar{V}_{16}$		$-2V_d/3$	0		π	[NPP]	$-2V_d/3$	$V_d/3$	$V_d/3$
$\bar{V}_{17}$		$-V_d/3$	$-\sqrt{3}\,V_d/3$		$4\pi/3$	[NNP]	$-V_d/3$	$-V_d/3$	$2V_d/3$
$\bar{V}_{18}$		$V_d/3$	$-\sqrt{3}\,V_d/3$		$5\pi/3$	[PNP]	$V_d/3$	$-2V_d/3$	$V_d/3$

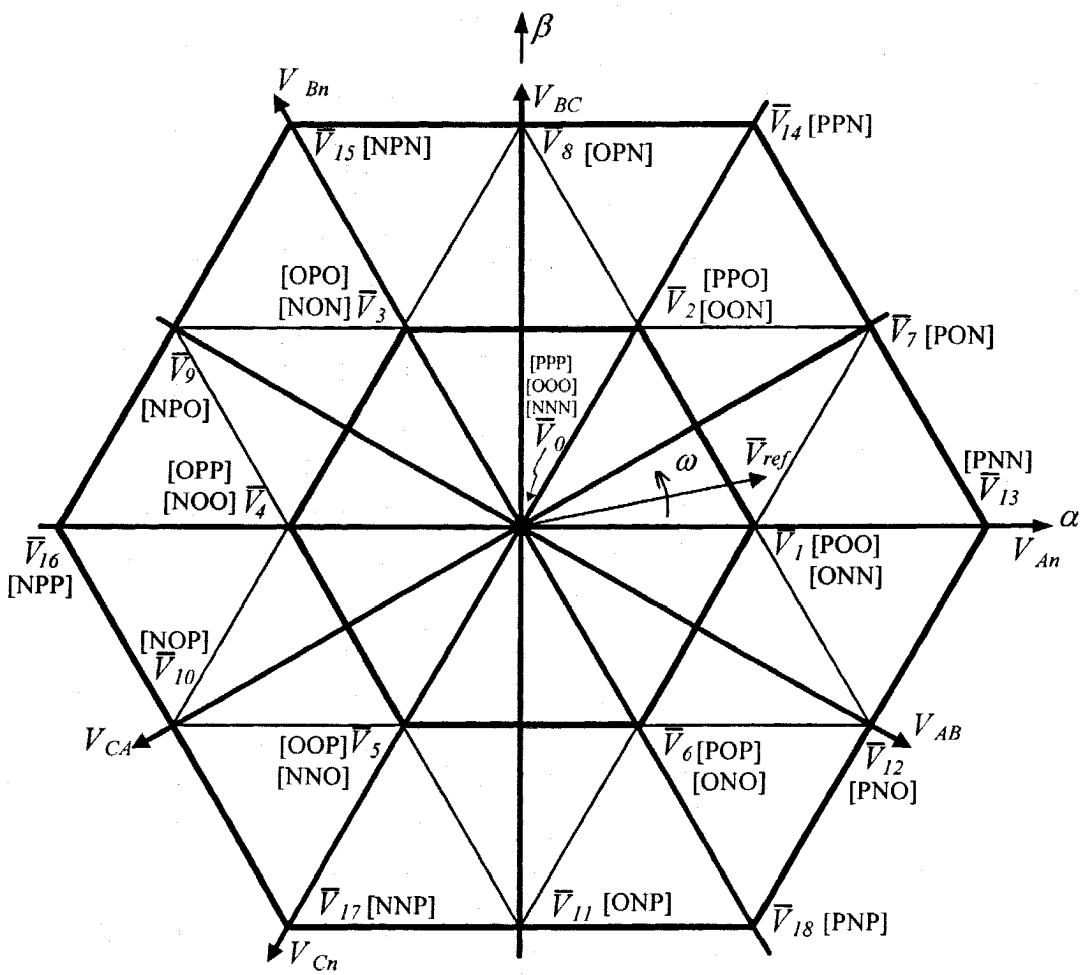


Fig. 2.4 Space vectors of the three-level NPC inverter.

The zero vector corresponds redundantly to three switching states, [PPP], [OOO] and [NNN] since these switching states produce zero load voltages. For the same reason, it can be found that each small vector has two redundant switching states. For instance, small vector $\bar{V}_1$ corresponds redundantly to two switching states [POO] and [ONN]. Depending on whether the switching states contain [P] state or [N] state, the small vectors are further classified as [P] type small vector or [N] type small vectors. For example, because of containing a [P] state, [POO] is classified as a [P] type small vector, which is called as $\bar{V}_{1P}$. Similarly, [ONN] is sorted as a [N] type small vector, named as $\bar{V}_{1N}$. The redundancy of switching states offers not only flexibility in switching pattern design, but also a method for the inverter neutral point potential control, which is discussed in detail in Sections 2.2.4 and 2.2.5.

2.2.2 Reference Vector and Space Vector Modulation

The output voltages of the three-phase three-level NPC inverter can be represented by a reference vector $\bar{V}_{ref}$, shown in Fig. 2.4.

Space vector modulation can be realized by approximating $\bar{V}_{ref}$ with space vectors based on 'voltage-second balancing' principle. The product of $\bar{V}_{ref}$ and T_s equals to the sum of the selected space vectors multiplied by their time intervals within each sampling period:

$$\bar{V}_{ref} \times T_s = \Sigma(\bar{V}_i \times T_i) \qquad (2.2\text{-}5)$$

$$T_s = \Sigma(T_i) \qquad (2.2\text{-}6)$$

where $\bar{V}_i$ and T_i represent a space vector and its dwell time to approximate $\bar{V}_{ref}$.

Normally, the nearest three space vectors are selected in order to reduce the harmonic distortion. The dwell times of the selected space vectors need to be calculated for the SVM implementation.

2.2.3 Dwell Time Calculation

To facilitate the space vector selection and the dwell time calculation, the space diagram is divided into six sectors (I to VI) as illustrated in Fig. 2.5. Each of these sectors can be further divided into four regular triangle regions (1 to 4). When the reference vector $\overline{V}_{ref}$ is located in a certain region, the space vectors on the vertexes of this region should be selected. For the purpose of switching pattern design, region 1 and 2 are further divided into two sub regions, sub-region a and sub-region b. The dwell time can be calculated from Eqs. (2.2-5) and (2.2-6) by substituting the reference vector and the selected space vectors into them.

a) Dwell Time Calculation in Region 2

When the reference vector is located in region 2 of sector I, as shown in Fig. 2.6, the space vectors used to approximate the reference vector are $\overline{V}_1$, $\overline{V}_2$ and $\overline{V}_7$. Their dwell times are T_a, T_c and T_b, respectively. Therefore, Eqs. (2.2-4) and (2.2-5) can be rewritten as:

$$\overline{V}_{ref} \times T_s = \overline{V}_1 \times T_a + \overline{V}_2 \times T_c + \overline{V}_7 \times T_b , \qquad (2.2\text{-}7)$$

$$T_s = T_a + T_c + T_b, \qquad (2.2\text{-}8)$$

where $\overline{V}_{ref}$, $\overline{V}_1$, $\overline{V}_2$ and $\overline{V}_7$ can be calculated as:

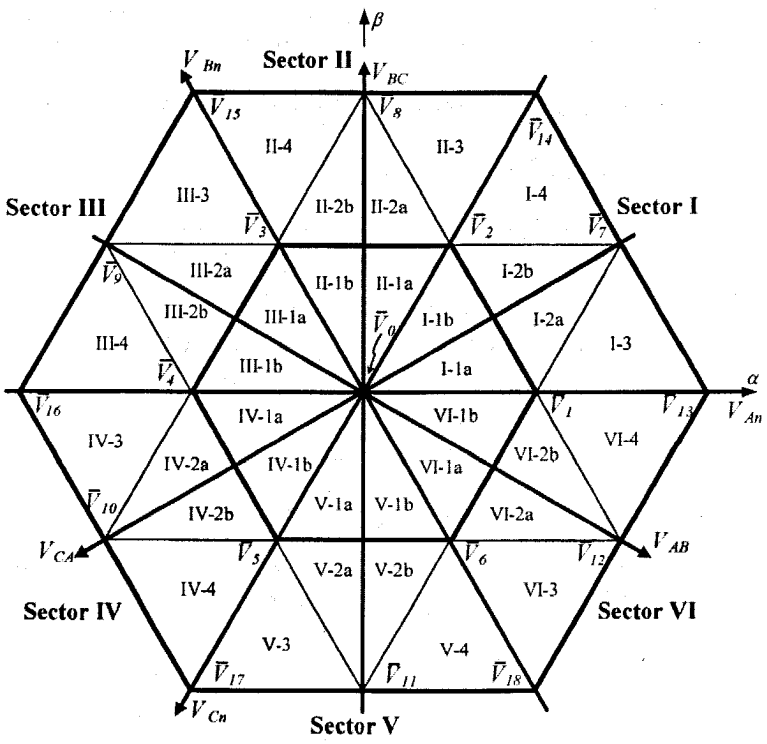


Fig. 2.5 Division of the space diagram.

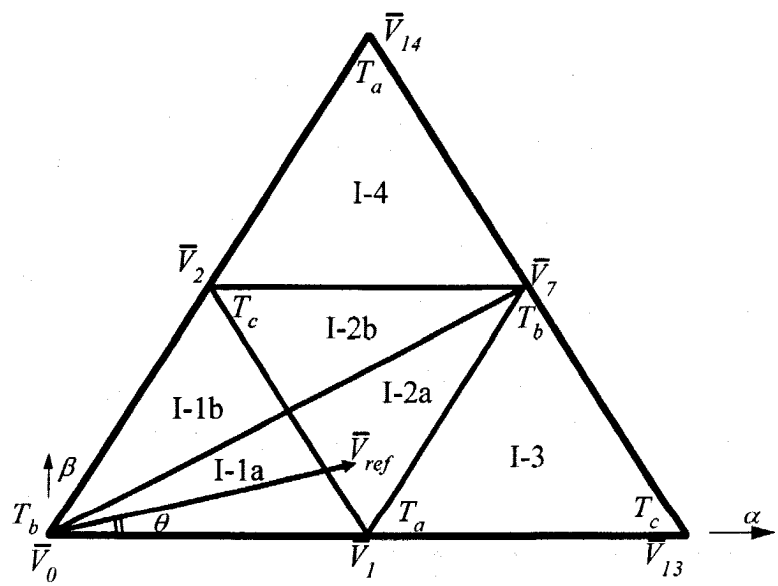


Fig. 2.6 Reference vector in I-2.

$$\begin{cases} \bar{V}_{ref} = |\bar{V}_{ref}| \times \cos(\theta) + j \times |\bar{V}_{ref}| \times \sin(\theta), \\ \bar{V}_1 = V_d / 3 \times \cos(0) + j \times V_d / 3 \times \sin(0), \\ \bar{V}_2 = V_d / 3 \times \cos(\pi/3) + j \times V_d / 3 \times \sin(\pi/3), \\ \bar{V}_7 = \sqrt{3}\ V_d/3 \times \cos(\pi/6) + j \times \sqrt{3}\ V_d/3 \times \sin(\pi/6). \end{cases} \quad (2.2\text{-}9)$$

Substituting Eqs. (2.2-9) into (2.2-7), two equations are obtained by splitting the real part and imaginary part:

$$\text{Re:} \quad |\bar{V}_{ref}| \times \cos(\theta) \times T_s = V_d/3 \times T_a \times \cos(0) + \sqrt{3}\, V_d/3 \times \cos(\pi/6) \times T_b + V_d/3 \times \cos(\pi/3) \times T_c \quad (2.2\text{-}10)$$

$$\text{Im:} \quad |\bar{V}_{ref}| \times \sin(\theta) \times T_s = V_d/3 \times T_a \times \sin(0) + \sqrt{3}\, V_d/3 \times \sin(\pi/6) \times T_b + V_d/3 \times \sin(\pi/3) \times T_c \quad (2.2\text{-}11)$$

These two equations are the same as:

$$|\bar{V}_{ref}| \times \cos(\theta) \times T_s = V_d/3 \times T_a + V_d/2 \times T_b + V_d/6 \times T_c, \quad \text{and} \quad (2.2\text{-}12)$$

$$|\bar{V}_{ref}| \times \sin(\theta) \times T_s = \sqrt{3}\, V_d/6 \times T_b + \sqrt{3}\, V_d/6 \times T_c. \quad (2.2\text{-}13)$$

From Eqs. (2.2-8), (2.2-12) and (2.2-13), the dwell time of selected space vectors can be solved below

$$\begin{cases} T_a = T_s \times [1 - 2\sqrt{3}\, |\bar{V}_{ref}| / V_d \times \sin(\theta)], \\ T_b = T_s \times [2\sqrt{3}\, |\bar{V}_{ref}| / V_d \times \sin(\pi/3 + \theta) - 1], \\ T_c = T_s \times [1 - 2\sqrt{3}\, |\bar{V}_{ref}| / V_d \times \sin(\pi/3 - \theta)]. \end{cases} \quad (2.2\text{-}14)$$

b) Dwell Time Calculation in Other Regions

Following the same procedures as shown above, the equations for dwell time calculations in other regions are derived. In region 1, they are:

$$\begin{cases} T_a = T_s \times 2\sqrt{3}\,|\bar{V}_{ref}| / V_d \times \sin(\pi/3-\theta) \\ T_b = T_s \times [1-2\sqrt{3}\,|\bar{V}_{ref}| / V_d \times \sin(\pi/3+\theta)] \\ T_c = T_s \times 2\sqrt{3}\,|\bar{V}_{ref}| / V_d \times \sin(\theta) \end{cases} \quad (2.2\text{-}15)$$

For region 3, the dwell times are:

$$\begin{cases} T_a = T_s \times [2-2\sqrt{3}\,|\bar{V}_{ref}| / V_d \times \sin(\pi/3+\theta)] \\ T_b = T_s \times 2\sqrt{3}\,|\bar{V}_{ref}| / V_d \times \sin(\theta) \\ T_c = T_s \times [2\sqrt{3}\,|\bar{V}_{ref}| / V_d \times \sin(\pi/3-\theta) - 1] \end{cases} \quad (2.2\text{-}16)$$

When the reference vector is in region 4, we have:

$$\begin{cases} T_a = T_s \times [2\sqrt{3}\,|\bar{V}_{ref}| / V_d \times \sin(\theta) - 1] \\ T_b = T_s \times 2\sqrt{3}\,|\bar{V}_{ref}| / V_d \times \sin(\pi/3-\theta) \\ T_c = T_s \times [2-2\sqrt{3}\,|\bar{V}_{ref}| / V_d \times \sin(\pi/3+\theta)] \end{cases} \quad (2.2\text{-}17)$$

2.2.4 Switching Sequence Design

With the proper space vector selected and their dwell time calculated, the switching state sequence of the space vector modulation for the three-level NPC inverter needs to be designed. Generally, two design criteria have to be met during the switching sequence design in order to achieve the minimum device switching frequency.

1. The transition from one switching state to the next should involve only two switches, one being turned off and the other being turned on; and
2. The transition from one triangular region to the next should involve minimum number of switching.

a) Seven-Segment Scheme

As a commonly used SVM technique, seven-segment scheme meets these criteria. In the seven-segment scheme, the nearest three space vectors are used in the seven segments of

each sampling period to approximant $\bar{V}_{ref}$. Among these three space vectors, there is at least one small vector, whose two redundant switching states both are used. In region 3 and region 4, there is only one small vector available. It would be the only choice. In region 1 and region 2, there are two small vectors. The small vector with longer dwell time is called the dominant small vector, whose two redundant switching states both are applied. However, only one switching state corresponding to the other small vector is chosen to meet the design criteria. The sub-regions a and b of regions 1 and 2 are used to select the dominant small vector. The small vector on the vertex of the sub-region is the dominant small vector. For example, in sub-region I-1a, switching states [POO] and [ONN], both corresponding to dominant small vector $\bar{V}_1$, are used with [OON], which is one of the redundant switching states of the non-dominant small vector $\bar{V}_2$.

Attentions have to be paid to the arrangement of switching state sequence to meet the design criteria. Table 2-4 gives an example of switching state sequences in I-1a. It can be seen that there is only one phase changing the switching state during each transition. The per-phase switching state change is between [O] and [P] or between [O] and [N], which involves two switching devices, one is turning on, another is turning off. Therefore, the first criterion is met. Based on this switching state sequence, the SVM during a sampling period in I-1a is illustrated in Fig.2.7

Table 2-4 Seven segments in sub-region I-1a

Segment	I-1a	
	Space vector & switching state	Time interval
1st	$\bar{V}_{1N}$ [ONN]	$T_a/4$
2nd	$\bar{V}_{2N}$ [OON]	$T_c/2$
3rd	$\bar{V}_0$ [OOO]	$T_b/2$
4th	$\bar{V}_{1P}$ [POO]	$T_a/2$
5th	$\bar{V}_0$ [OOO]	$T_b/2$
6th	$\bar{V}_{2N}$ [OON]	$T_c/2$
7th	$\bar{V}_{1N}$ [ONN]	$T_a/4$

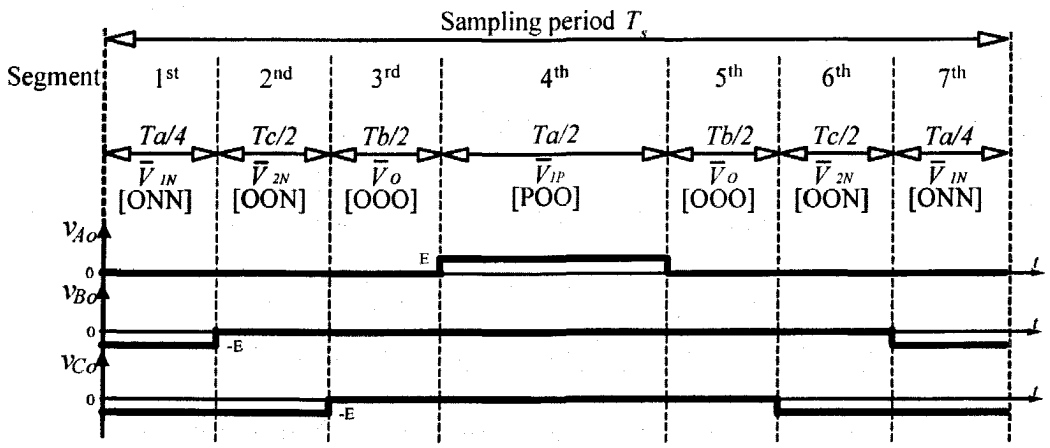


Fig. 2.7 Space vector modulation in I-1a.

b) Two Patterns of Switching State Sequence

Seven-segment scheme has two patterns for switching state sequence in each region or sub-region, Pattern I and II, of which both can meet the first design criterion. But the switching state sequences based on these two patterns are different. For example, in the sub-region I-1a, illustrated in Table 2-5, the first four switching states of Pattern I in I-1a are [ONN], [OON], [OOO] and [POO]. In the $\alpha-\beta$ frame, the direction of their sequence is counter clockwise. On the contrary, this direction of the first four switching states in Patter II is clockwise. Fig. 2.8 shows the difference between the sequence directions of the two patterns.

c) Switching Pattern Design for the Entire Space Vector Diagram

In order to meet the second design criterion, the switching patterns of the NPC inverter in the conjunctive areas should be determined based on the pattern selection of a region or sub-region. For example, when Pattern I is used in I-1a, it can be seen from Table 2-5 that the last switching state of Pattern I in I-1a is [ONN]. On the other hand, [OON] is the first switching state of the Pattern I in I-1b, while [PPO] is the first state of Pattern II in the same area. Obviously, Pattern I in I-1b should be chosen since, from [ONN] to [OON], there is only one phase changing switching state during the transition from I-1a to I-1b. Similarly, the pattern in I-2a can be easily determined because the reference vector may turn form I-1a into I-2a. Based on these rules, the patterns of all the regions or sub-regions in the entire diagram could be determined one by one. Fig. 2.9 illustrates the directions of the entire space diagram after Pattern I is selected in I-1a. The switching pattern design of entire space diagram is given in Appendix I.

Table 2-5 Two patterns of switching state sequence in I-1a

Segment	Pattern I	Pattern II
1st	$\bar{V}_{1N}$ [ONN]	$\bar{V}_{1P}$ [POO]
2nd	$\bar{V}_{2N}$ [OON]	$\bar{V}_{0}$ [OOO]
3rd	$\bar{V}_{0}$ [OOO]	$\bar{V}_{2N}$ [OON]
4th	$\bar{V}_{1P}$ [POO]	$\bar{V}_{1N}$ [ONN]
5th	$\bar{V}_{0}$ [OOO]	$\bar{V}_{2N}$ [OON]
6th	$\bar{V}_{2N}$ [OON]	$\bar{V}_{0}$ [OOO]
7th	$\bar{V}_{1N}$ [ONN]	$\bar{V}_{1P}$ [POO]

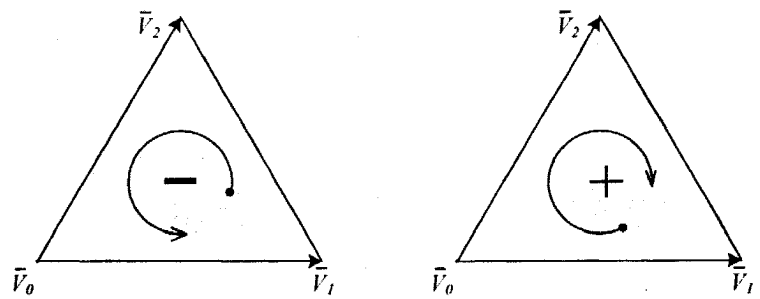


Fig. 2.8 Directions of switching sequence in I-1a based on the two patterns.

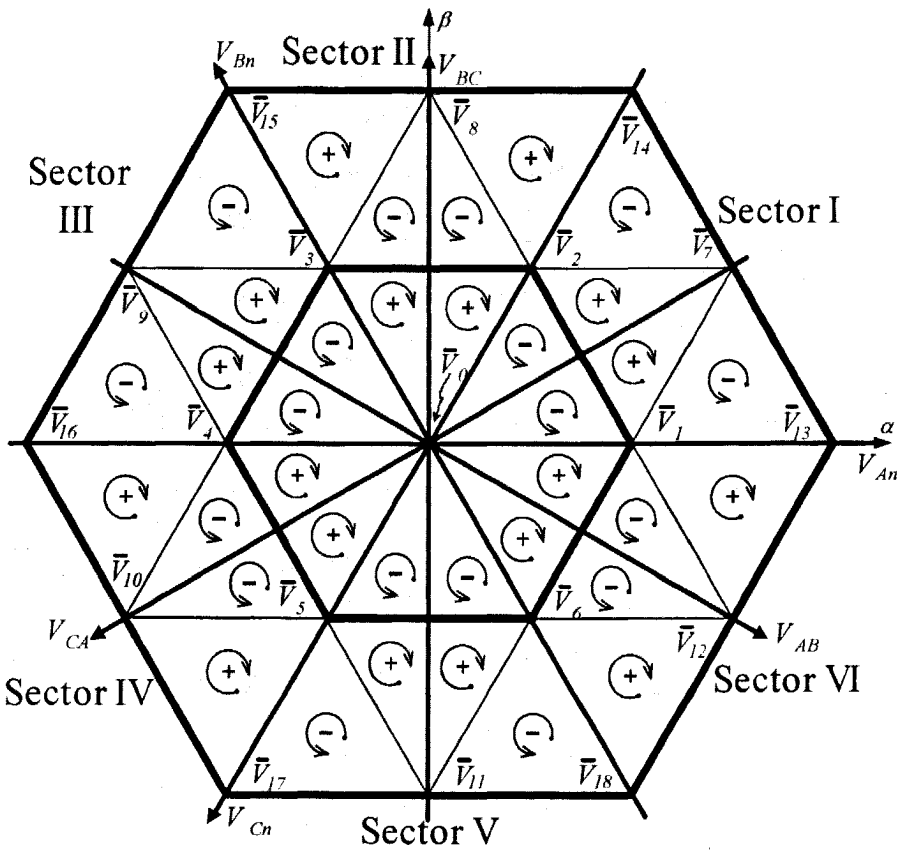


Fig. 2.9 Directions of the switching sequence for pattern I.

2.2.5 Neutral Point Potential Control

As a common problem of NPC inverters, the neutral point potential deviation may occur when a three-level NPC inverter uses a single DC voltage source. It causes unbalanced voltage stress on the switching devices and also introduces some undesirable harmonics to the phase output voltages. However, seven-segment scheme can mitigate this problem by using closed-loop control.

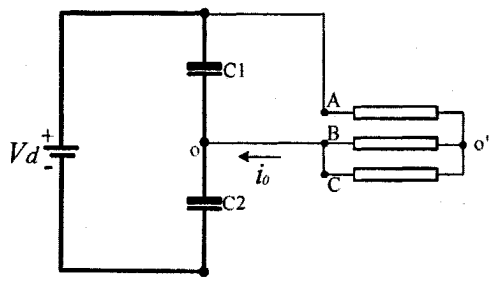
a) Neutral Point Potential Deviation

There are some reasons for the deviation of the neutral point potential, such as imbalances in DC capacitors or discharge resisters, dead time implementation and elimination of minimum pulse of the gating signals.

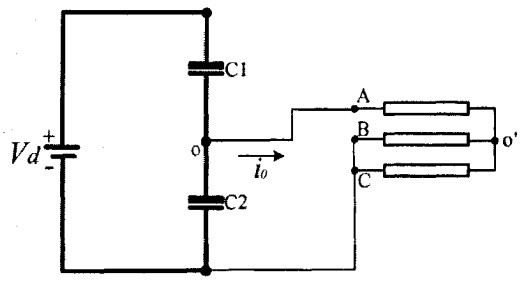
Some switching states also cause the neutral point potential deviations because of the neutral point current i_o, which changes the charges and the voltages of the DC capacitors. Fig. 2.10 shows the simplified circuits and the current directions caused by the redundant switching states of $\bar{V}_1$. It can be seen that the directions of neutral point currents could be opposite with the same load. These redundant switching states have opposite influences to the neutral point potential. Note that each pair of other redundant switching states has opposite impacts as well.

b) Closed-loop Control of Neutral Point Potential

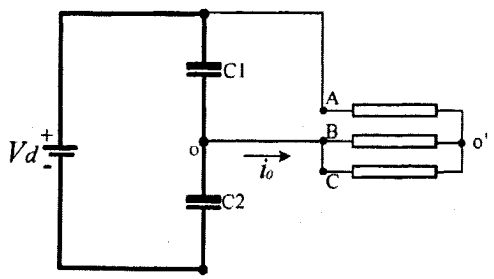
Since each pair of the redundant switching states of the three-level NPC inverter impact the neutral point potential oppositely, they can be used for the neutral point potential control by shifting a part of the duty time between the pair of the redundant switching states.



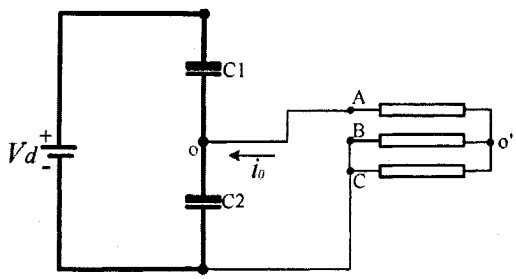
(a) [POO] with load in motoring mode



(b) [ONN] with load in motoring mode



(c) [POO] with load in regenerating mode



(d) [ONN] with load in regenerating mode

Fig. 2.10 Neutral point potential deviation under redundant switching states of $\overline{V}_1$.

For the purpose of the neutral point potential control, Δt is defined as the percentage of the time intervals of the first and the seventh segments that would be shifted to the forth segment:

$$\begin{cases} t_1' = t_1 \times (1 - \Delta t) \\ t_7' = t_7 \times (1 - \Delta t) = t_1 \times (1 - \Delta t) \\ t_4' = t_4 + t_1 \times \Delta t + t_7 \times \Delta t = t_4 + t_1 \times \Delta t \times 2 \end{cases} \tag{2.2-18}$$

where t_1, t_4 and t_7 are the time intervals of 1st, 4th and 7th segments before the adjustment, t_1', t_4' and t_7' are those after the adjustment.

Since one of the redundant switching states is used in the first and the last segments, the other is assigned to the forth segment, the adjustment of their time intervals does not change the total dwell time of the small vector corresponding to these redundant switching states:

$$\begin{aligned} t_1' + t_4' + t_7' &= t_1 \times (1 - \Delta t) + t_1 \times (1 - \Delta t) + t_4 + t_1 \times \Delta t \times 2 \\ &= t_1 + t_4 + t_7 \end{aligned} \tag{2.2-19}$$

It should be noted that the direction of this time interval adjustment, represented by the sign of Δt, is determined by two factors: 1) the pattern of the seven-segment scheme, in which the redundant switching states exchange their segments; 2) the mode of load, in which the influence of the same switching state could be reversed.

Based on the above discussions, a scheme of the neutral point potential closed-loop control is designed as shown in Fig. 2.11, in which the Δt is obtained based on the difference between the two capacitor voltages.

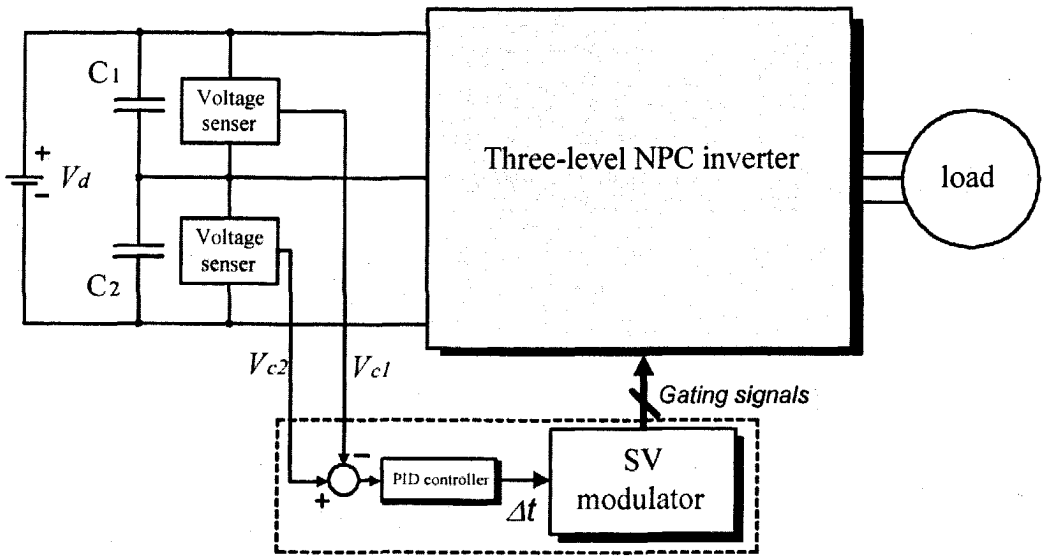


Fig. 2.11 Closed-loop control of neutral point potential.

2.3 Summary

The principle of the space vector modulation for the three-level neutral point clamped inverter was introduced in this chapter. The power circuit and the switching states of the three-level NPC inverter were described. The space vectors of the three-phase three-level NPC inverter were presented. The space vector selection method was introduced and the dwell time calculation equations were derived. Based on the requirement of minimizing the device switching frequency, the switching state sequence of the inverter was developed. A neutral point potential closed-loop control system was designed by utilizing redundant switching states.

Chapter 3

Simulations and Harmonic Analysis

Featuring time-saving, low-cost and risk-free, simulation process becomes an important tool in developing and designing a power electronics system. Established in the MATLAB/Simulink platform, the simulation study of the space vector modulation (SVM) scheme for the three-phase three-level neutral point clamped (NPC) inverters is presented in this chapter. The power circuit and the SVM scheme of the inverter are modeled. The harmonic and THD profiles of the output voltages of the NPC inverter are investigated. Furthermore, the closed-loop neutral point potential control algorithm presented in the previous chapter is verified.

3.1 Modeling of Simulations

The simulation modeling of the SVM scheme for the three-phase three-level NPC inverter includes two steps, the function block design and the controller S-function programming.

3.1.1 Function Blocks

Built up from the basic units included in the Simulink libraries, the function blocks form the simulation model of the SVM three-level NPC inverter are shown in Fig. 3.1, where five sub-systems including power supply, three-level NPC inverter, load, reference generator and gating signals generator are illustrated.

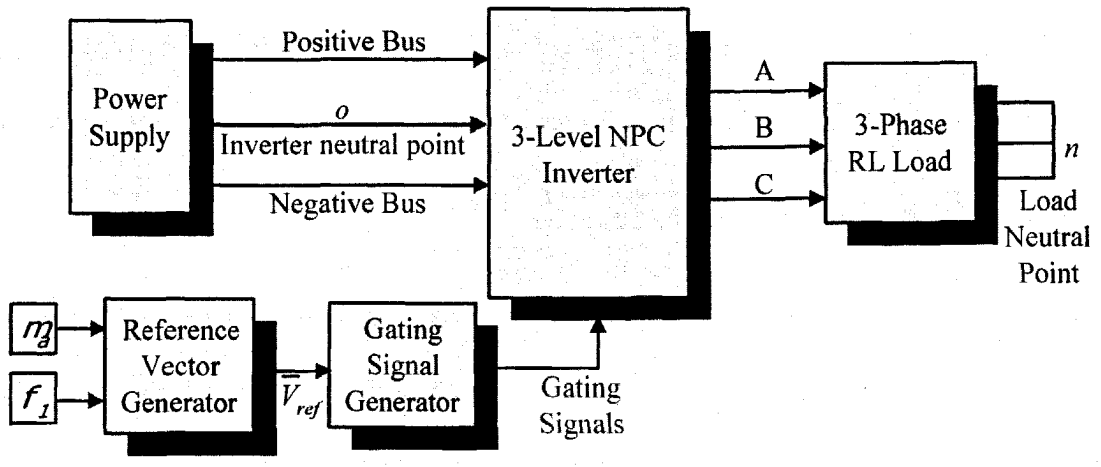


Fig. 3.1 Simulation model of space vector modulated Three-level NPC Inverter.

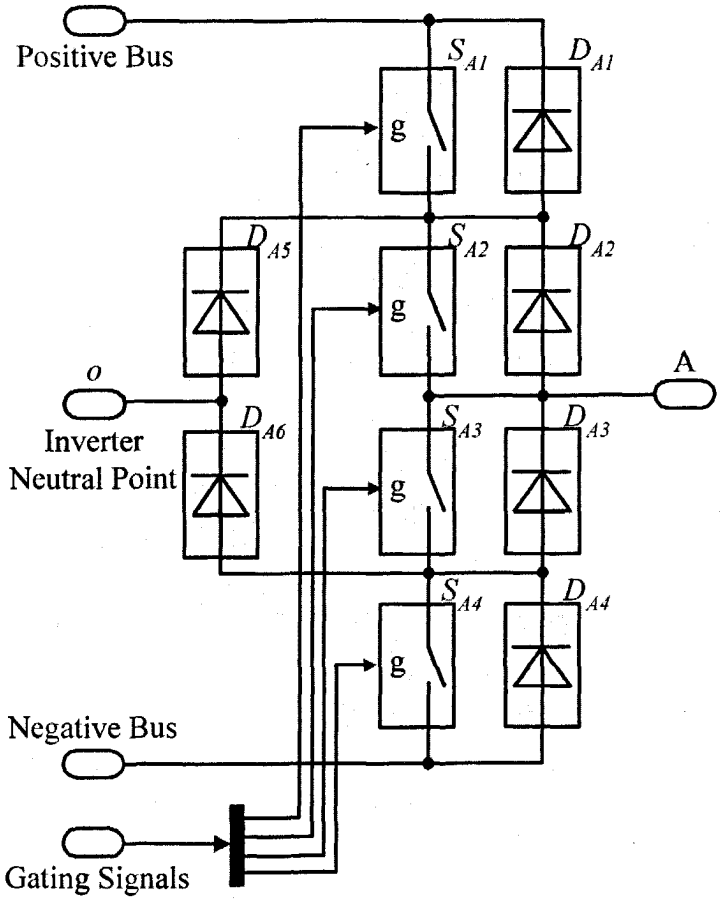


Fig. 3.2 Configuration of phase A in Three-level NPC Inverter sub-system.

a) Power Supply

To investigate the ideal performance of the inverter, two identical DC voltage sources are connected in series in the block *Power Supply*.

b) Three-level Neutral Point Clamped Inverter

According to the power circuit introduced in previous chapter, a three-phase three-level NPC inverter is designed in the block *3-Level NPC Inverter* in Fig. 3.1. The configuration of one of the three identical legs in the inverter is shown in Fig. 3.2.

c) Load

The block *3-Phase RL Load* in Fig. 3.1 contains a balanced three-phase RL load, in which the values of the resistances and inductions can be preset.

d) Reference Vector Generator

The reference vector, output of the block *Reference Vector Generator*, is generated based on the settings of the amplitude modulation index m_a and the fundamental frequency f_1:

$$\bar{V}_{ref} = |\bar{V}_{ref}| \, e^{j\gamma}, \qquad (3.1\text{-}1)$$

where $|\bar{V}_{ref}|$ is the length of $\bar{V}_{ref}$ and γ is the phase angle of $\bar{V}_{ref}$,

$$|\bar{V}_{ref}| = \sqrt{3} \times m_a \times V_d \ / 3, \qquad (3.1\text{-}2)$$

$$\gamma = 2\pi \times f_1 \times t. \qquad (3.1\text{-}3)$$

e) Gating Signal Generator

Based on the magnitude and the phase angle of the reference vector produced by the block *Reference Vector Generator*, the gating signals to the inverter in Fig. 3.1 are generated by the block *Gating Signal Generator*, of which the details are illustrated in Fig. 3.3, where a S-function block, introduced later, is applied.

3.1.2 S-function Programming

According to the SVM scheme introduced in Chapter 2, the S-function block in the *Gating Signal Generator* is coded based on the programming flowchart shown in Fig. 3.4. The program of the S-function block can be loaded by the simulation systems or the timer preset by the sampling period. At the beginning of each sampling interval, the space vector selection and dwell time calculation are processed based on the values of the reference vector at the middle-point of the sampling interval.

In the simulation, the gating signals of the inverter are generated based on the switching states, which are obtained from the pre-designed look up tables according to the segment and sector numbers. Only the end of the simulation can stop the gating program.

3.2 Waveforms and Harmonic Analysis

In the following simulations, the parameters of the power supply and the load are given by:

Rated output power rating:	1MAV
RL loads (each phase):	R=17.3Ω (1.1033 pu.)
	L=2.3mH (0.0553 pu.)
DC input voltage rating (total):	5600V

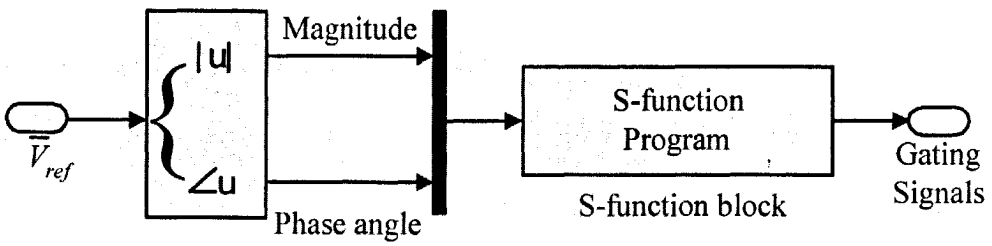


Fig. 3.3 Gating signal generator sub-system.

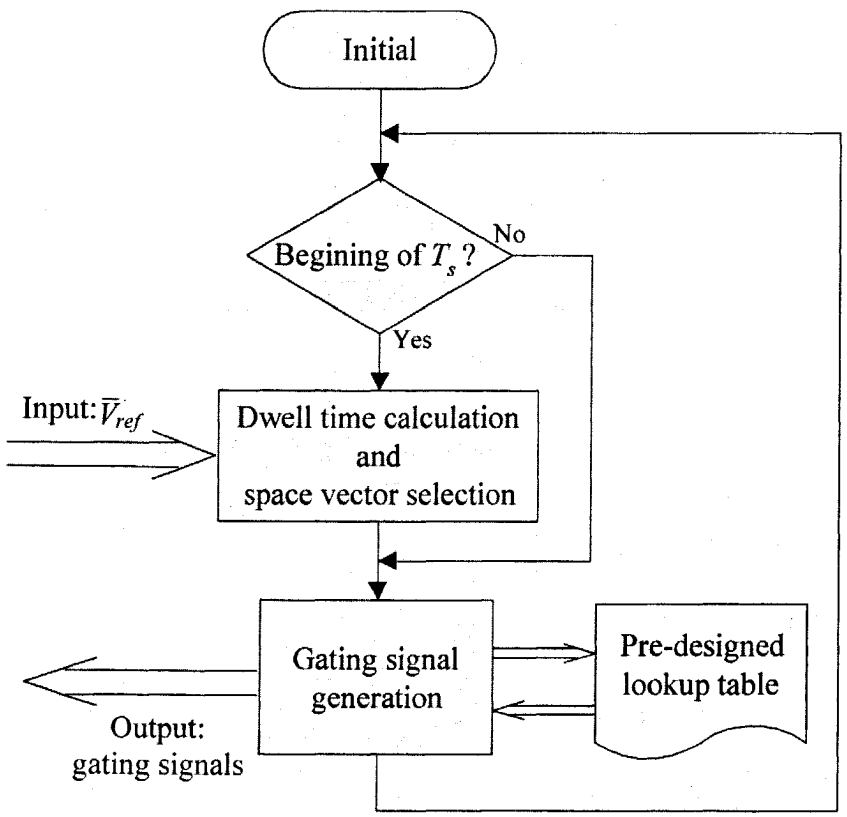


Fig. 3.4 Flowchart of S-function program.

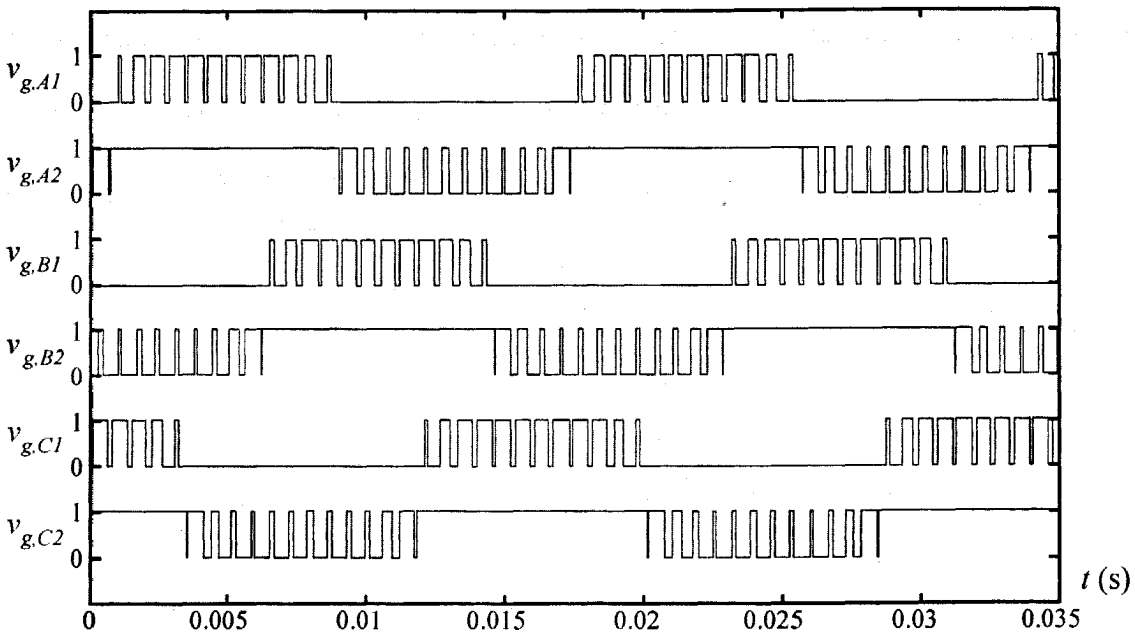
Different parameters of the amplitude modulation index m_a, fundamental frequency f_1 and sampling frequency f_{sa}, are simulated to investigate the performances under different operating conditions. Note that the frequency modulation index $m_f = f_{sa} / f_1$ is set as an integer in following simulations, i.e. the so-called synchronous sampling method, in which the number of sampling intervals in each fundamental period is always an integer, is applied in this thesis.

3.2.1 Simulated Waveforms

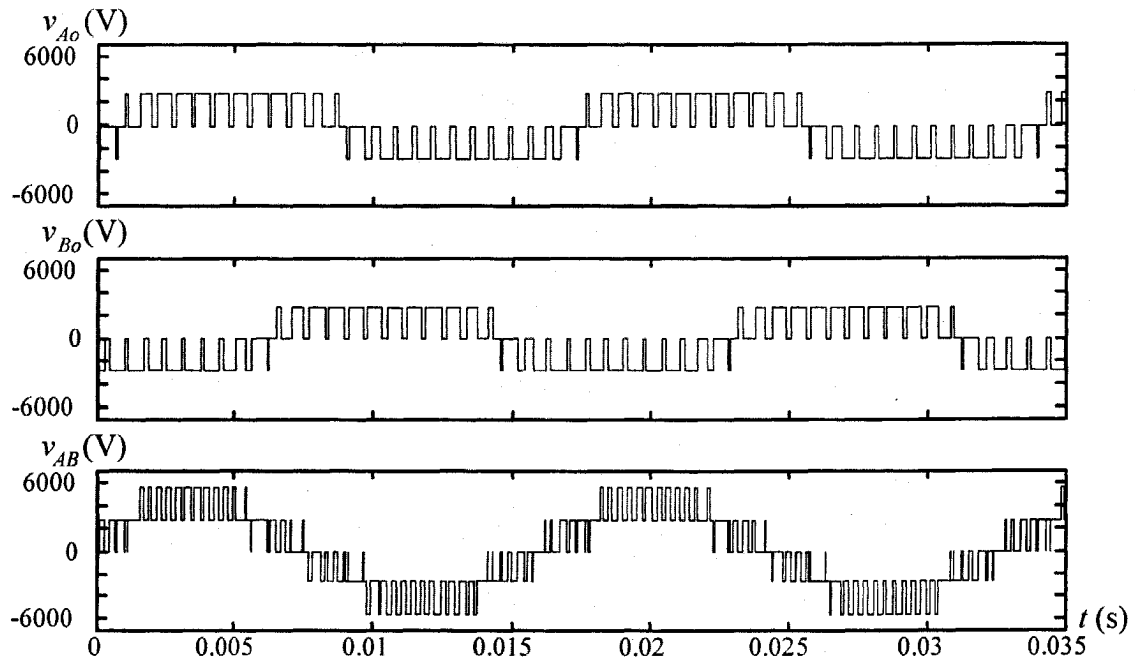
Following simulation parameters are preset:

Modulation index:	m_a=0.8,
Fundamental frequency:	f_1=60Hz, and
Sampling frequency:	f_{sa}=1440Hz.

The frequency modulation index $m_f = f_{sa} / f_1$ is 24, and the inverter switching frequency f_{sw} is $f_{sa}/2$=720Hz. Fig. 3.5 shows the simulation results, which include gating signals, inverter output phase voltages v_{Ao} and v_{Bo}, the inverter line-to-line voltage v_{AB}, the voltage between the neutral point of the balanced three-phase load and that of the inverter v_{no}, the load phase voltage v_{An}, and the output current i_A. Especially, since the operations of the 3rd and the 4th switching devices are complementary with those of the 1st and the 2nd devices in the same leg, respectively, the gating signals of 1st and 2nd devices of all the legs are shown in Fig. 3.5(a). The inverter output phase voltages and line-to-line voltage are shown in Fig. 3.5(b), in which the phase voltages v_{Ao} and v_{Bo} have three levels, and the line-to-line voltage v_{AB} has five levels. In Fig. 3.5(c), it can be noticed that the voltage of the neutral point difference v_{no} has five levels, while the load phase voltage v_{An} has nine levels. Due to the filter effect of the RL load, the waveforms of i_A, shown in Fig. 3.5(d), looks closer to a sinusoidal wave than that of the load phase voltage v_{An}.

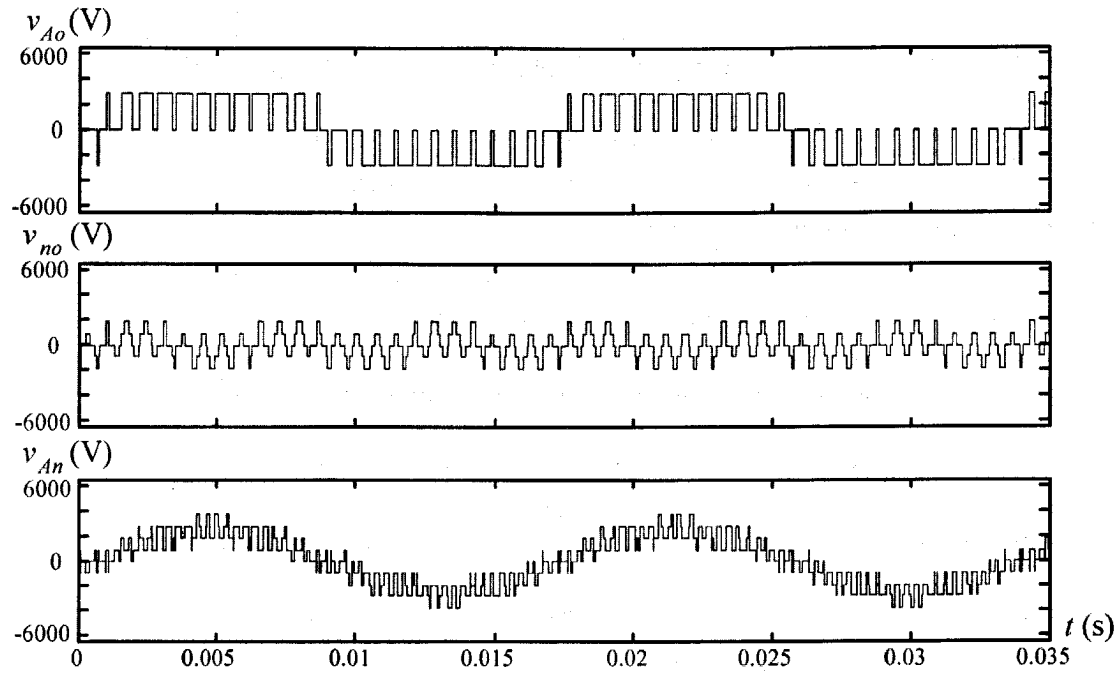


(a) Gating signals

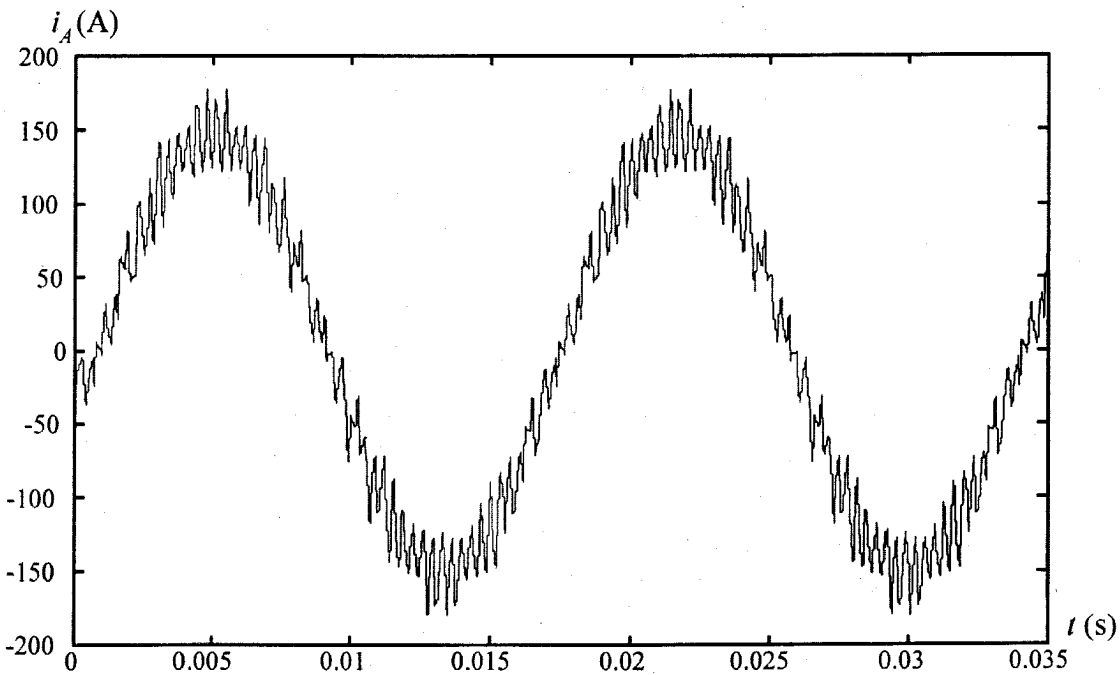


(b) v_{Ao}, v_{Bo} and v_{AB}

Fig. 3.5 Simulated waveforms (to be continued)



(c) v_{Ao}, v_{no} and v_{An}



(d) i_A

Fig. 3.5 Simulated waveforms (continued).

3.2.2 Harmonic Analysis

The harmonic components of the line-to-line voltage v_{AB} are analyzed based on the fast Fourier transformation function offered by MATLAB.

a) Fundamental Component and THD

The waveform of the line-to-line voltage v_{AB}, simulated in section 3.2.1, and its spectrum are shown in Fig. 3.6. Similarly, simulations and the harmonic analyses for different amplitude index m_as are processed to obtain the relationship between m_a and the total harmonic distortion (THD). The simulation waveforms and the harmonic spectrums are shown in Fig. 3.6 to Fig. 3.9. The simulation conditions, rms values of the fundamental component $V_{AB1,rms}$ of the inverter line-to-line voltages and the THDs are listed in Table 3-1.

The line-to-line voltages have only three levels with less than 0.5 m_as, for example m_a=0.4 and m_a=0.2. Because only zero vectors and small vectors are used to approximate the reference vector when the reference vector is rotating only in the inner regions, the line-to-line voltages of the inverter looks as those of a traditional two-level inverter in these cases.

Table 3-1 Harmonic analyses under different amplitude modulation index m_a

Figure	Fig. 3.6	Fig. 3.7	Fig. 3.8	Fig. 3.9
m_a	0.8	0.6	0.4	0.2
f_1 (Hz)	60	60	60	60
f_{sa} (Hz)	1440	1440	1440	1440
$V_{AB1,rms}$(V)	3162.2	2368.4	1583.2	788.1
THD	38.93%	45.72%	77.82%	148.9%

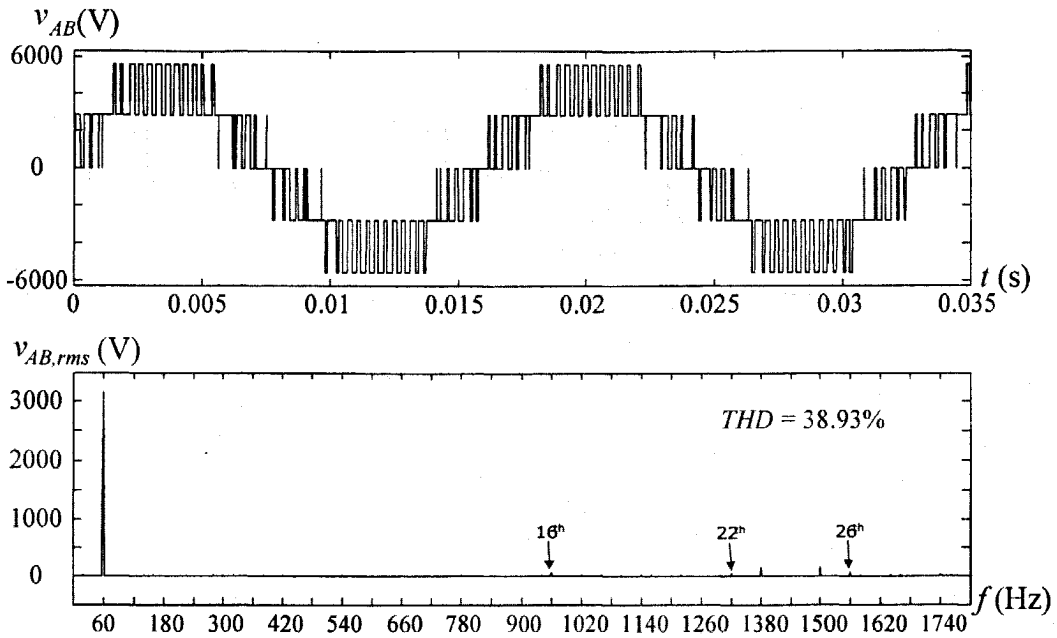


Fig. 3.6 Waveform and spectrum of v_{AB} (m_a=0.8, f_1=60Hz, f_{sa}=1440Hz).

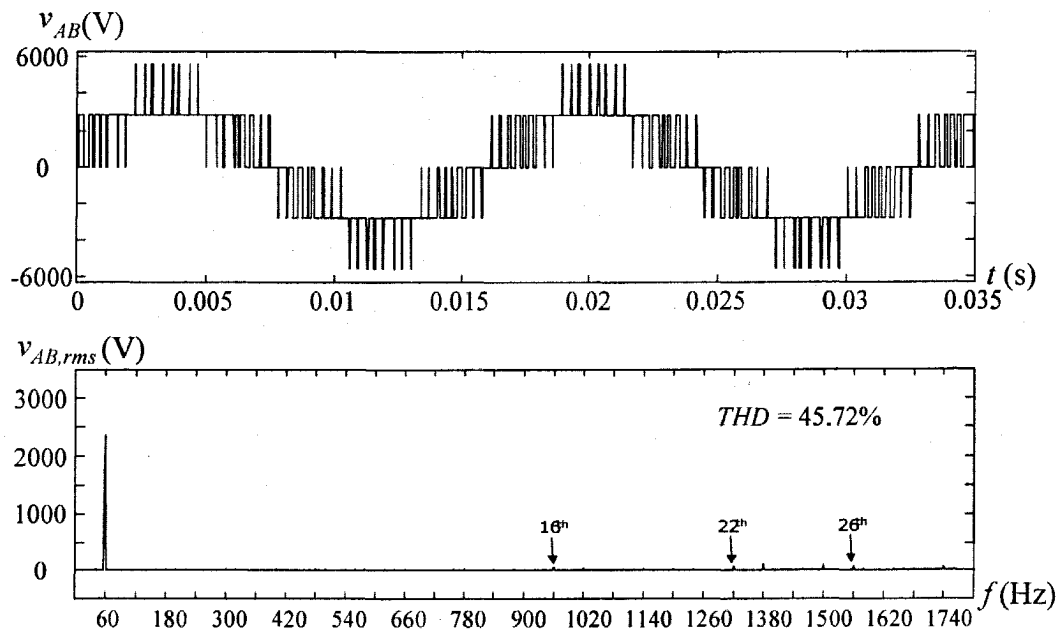


Fig. 3.7 Waveform and spectrum of v_{AB} (m_a=0.6, f_1=60Hz, f_{sa}=1440Hz).

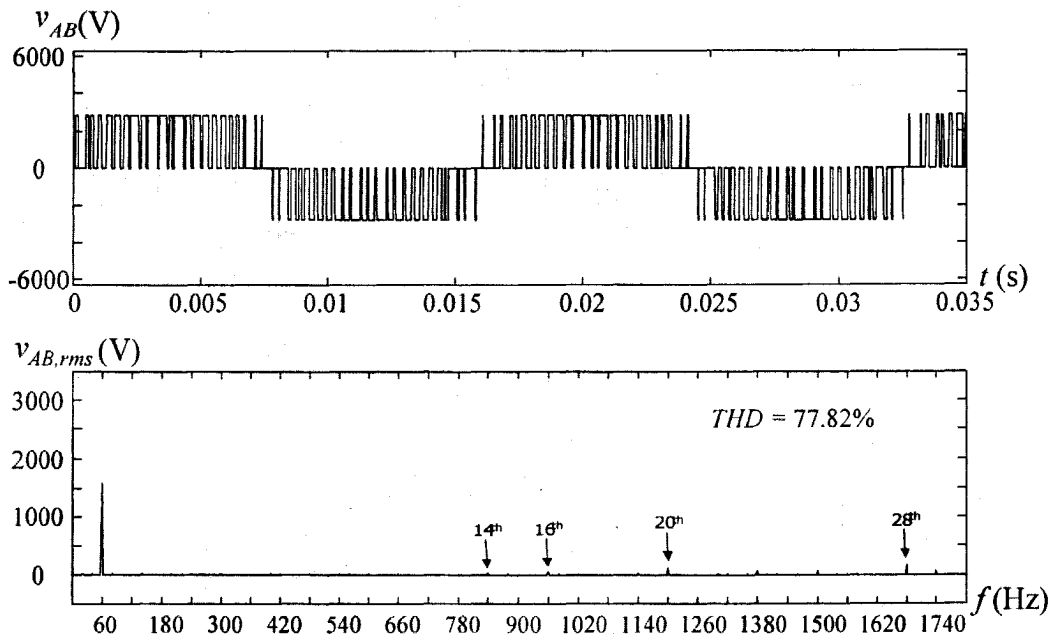


Fig. 3.8 Waveform and spectrum of v_{AB} (m_a=0.4, f_1=60Hz, f_{sa}=1440Hz).

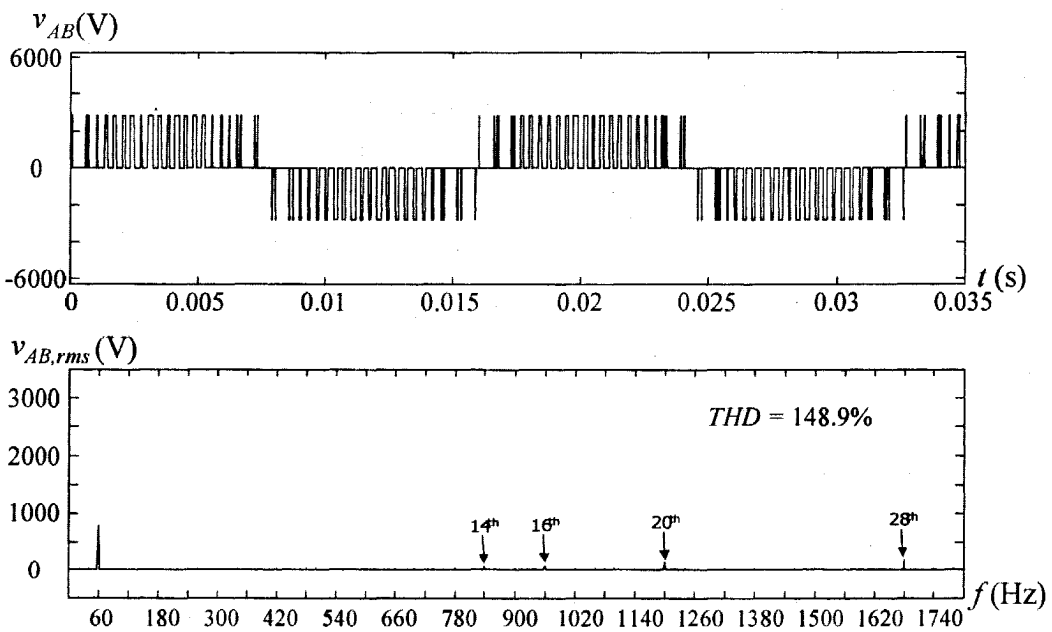


Fig. 3.9 Waveform and spectrum of v_{AB} (m_a=0.2, f_1=60Hz, f_{sa}=1440Hz).

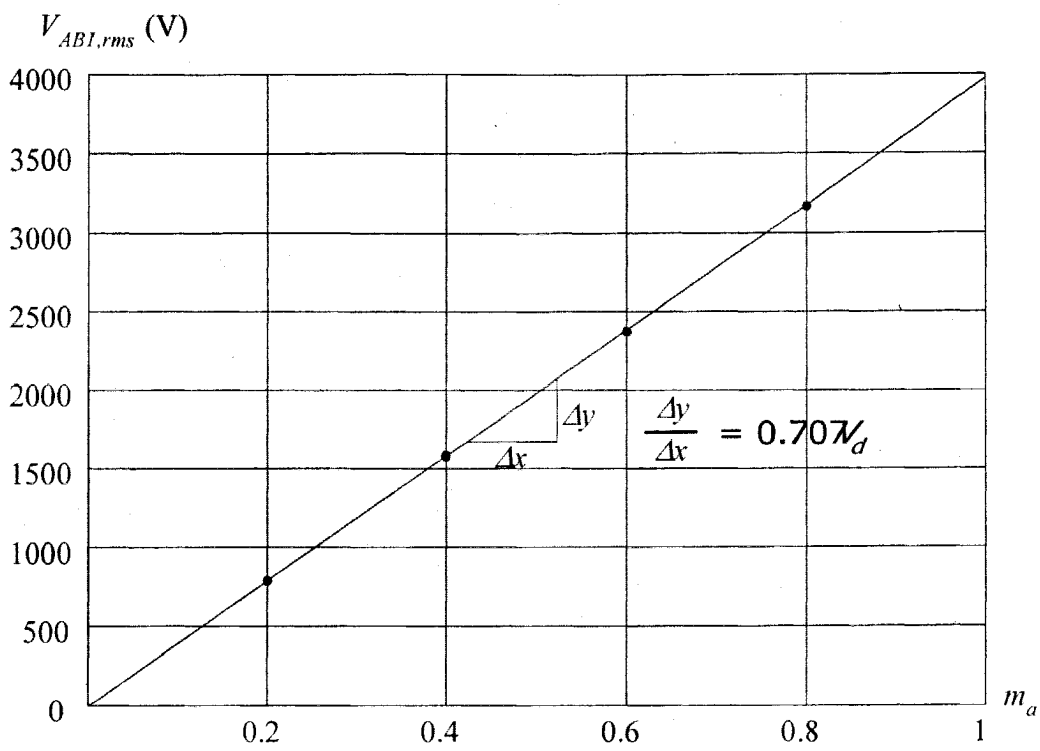


Fig. 3.10 Linear relationship between $V_{AB1,rms}$ and m_a.

Table 3-1 shows the THD is higher when the amplitude modulation index m_a is smaller. Based on the values in Table 3-1, a linear relationship between $V_{AB1,rms}$ and m_a is illustrated in Fig. 3.10, and given as:

$$V_{AB1,\,\mathrm{rms}} = 0.707 \times V_d \times m_a \qquad (3.2\text{-}1)$$

Furthermore, the inverter line-to-line voltages in above simulations contain some even order harmonics, which are noted in Fig. 3.6 to Fig. 3.9.

b) Even Order Harmonics

In order to illustrate the even order harmonics in the low frequency band more clearly, cases of the three-level NPC inverter working under a lower sampling frequency (720Hz) are simulated. The waveforms and the spectrums of the inverter line-to-line voltages are shown in Fig. 3.11 and Fig. 3.12, in which the fundamental frequencies are 60Hz and 30 Hz, respectively. The even order harmonics are particularly noted in these two figures.

3.3 Harmonic and THD Profiles

Sweeping the amplitude modulation index m_a from 0 to 1, with fixed frequency modulation index m_f, the harmonic and THD profiles of the three-level NPC inverter can be obtained. Three groups of profiles are acquired based on different values of m_f: 1) m_f = 24 (f_{sa} = 1440Hz and f_1 = 60Hz); 2) m_f = 18 (f_{sa} = 1080Hz and f_1 = 60Hz); and 3) m_f = 12 (f_{sa} = 720Hz and f_1 = 60Hz). The sextuple m_fs are used herein is to ensure the even distribution of the sampling period in the six sectors, i.e. each of the six sectors contains the same number of the sampling periods. The harmonic analyses of above three m_fs reveal that the line-to-line voltages have both even order and odd order harmonics. The harmonic and the THD profiles are shown in Fig. 3.13 to Fig. 3.18. In the harmonic profiles, those beyond 20^{th} order harmonics are not included because they can be easily filtered by a small filter in practice.

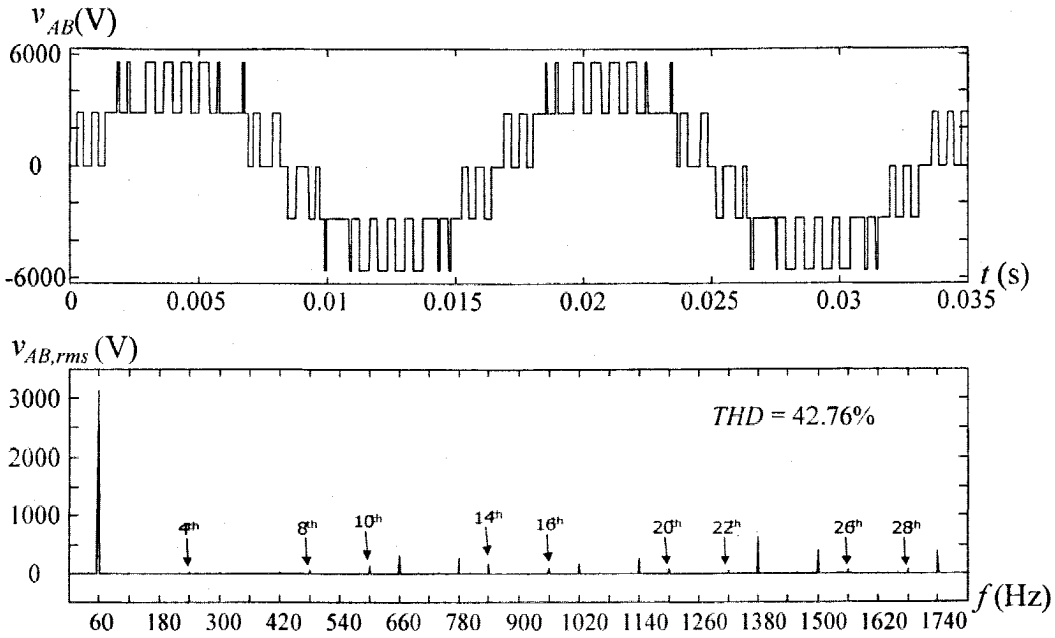


Fig. 3.11 Waveform and spectrum of v_{AB} (m_a=0.8, f_1=60Hz, f_{sa}=720Hz).

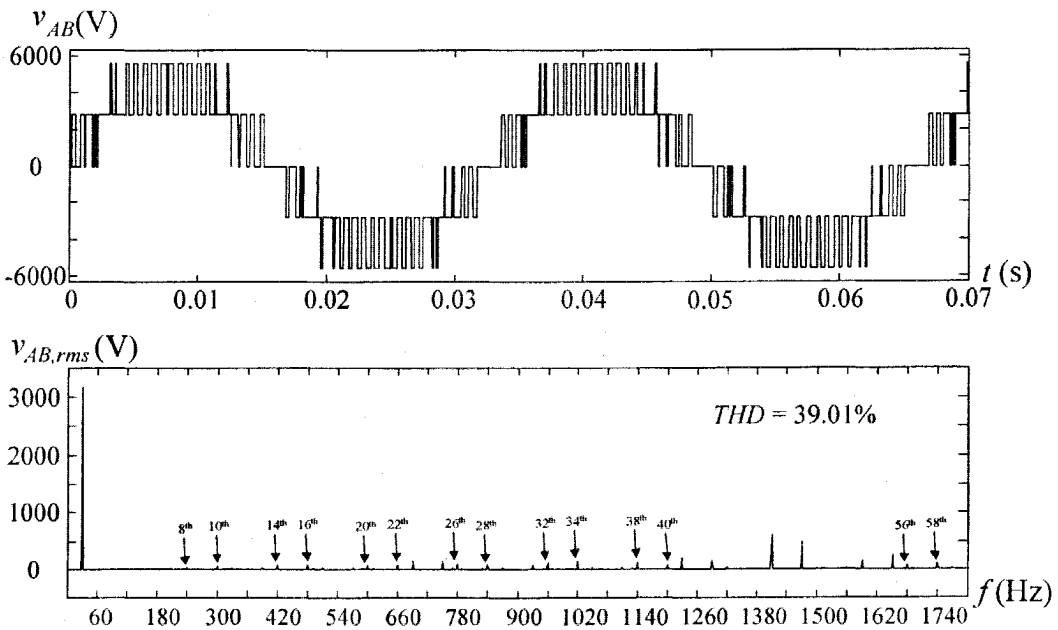
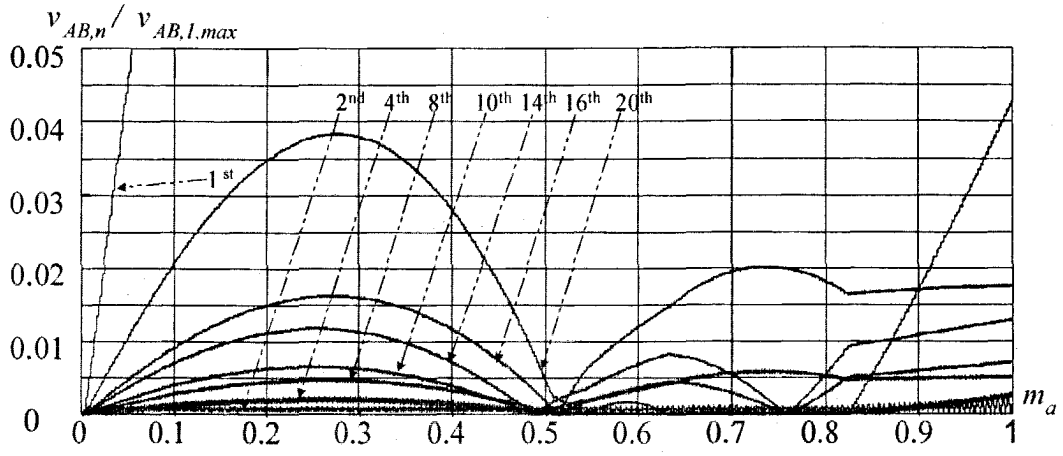
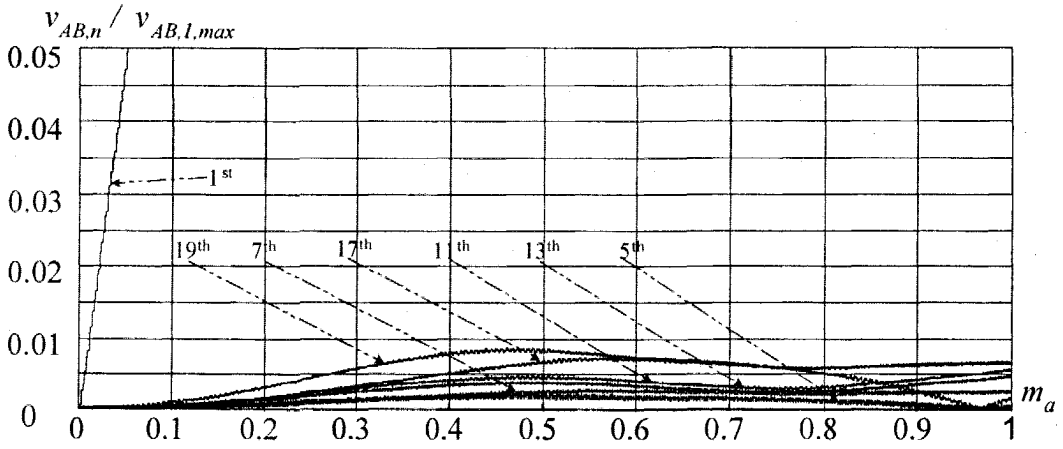


Fig. 3.12 Waveform and spectrum of v_{AB} (m_a=0.8, f_1=30Hz, f_{sa}=720Hz).



(a) Even order harmonic profile



(b) Odd order harmonic profile

Fig. 3.14 Harmonic profile (f_1=60Hz, f_{sa}=1440Hz).

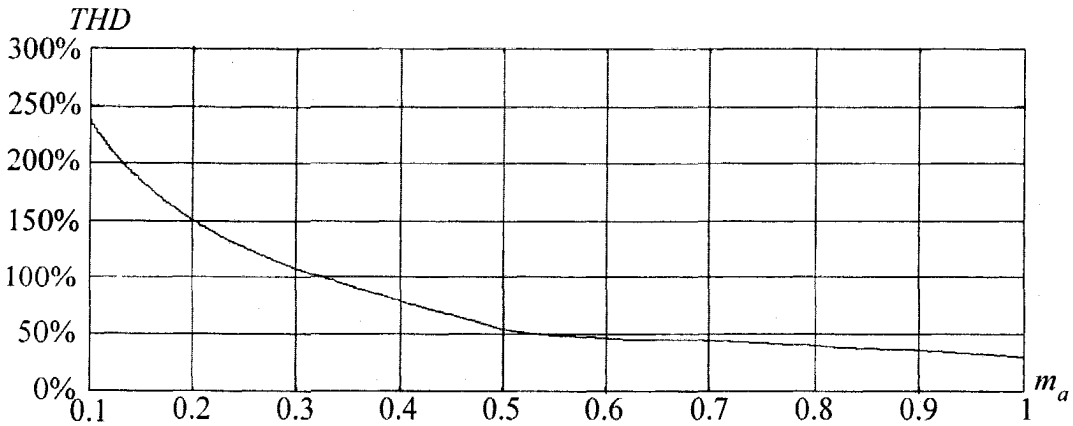
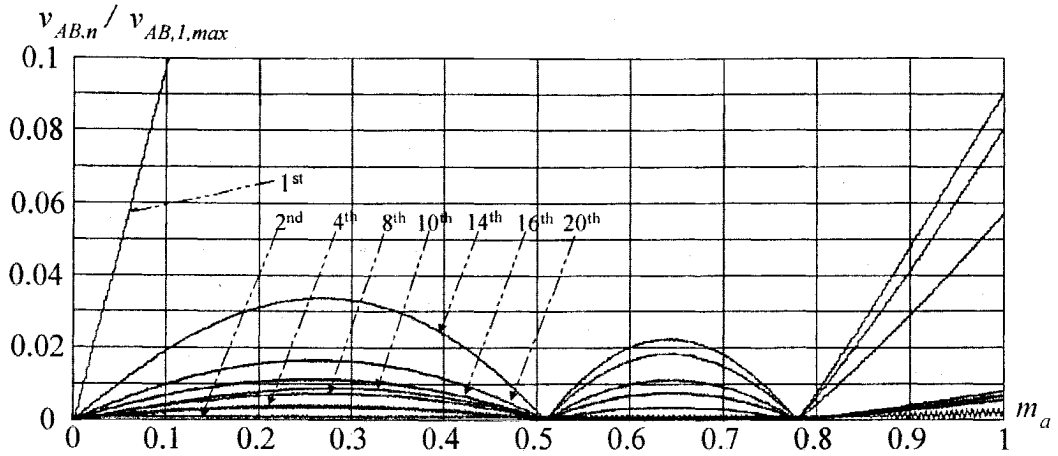
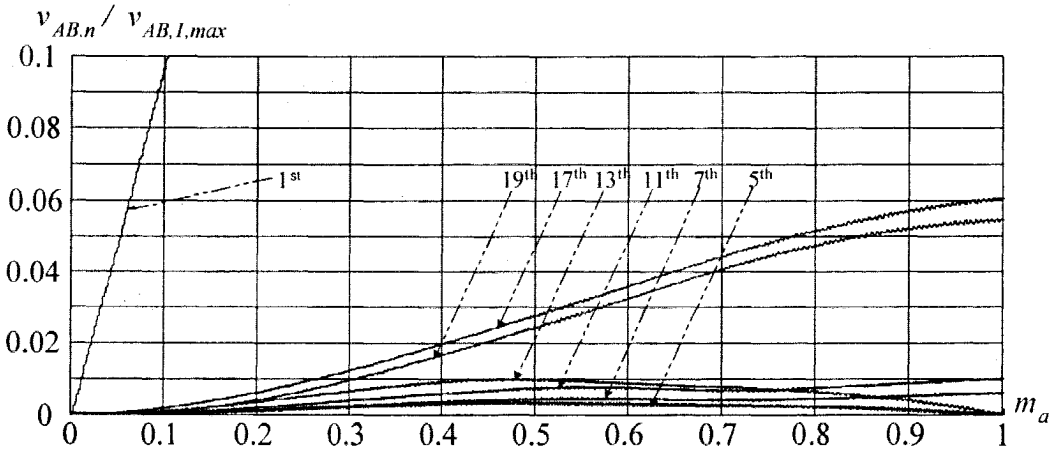


Fig. 3.15 THD profile (f_1=60Hz, f_{sa}=1440Hz).



(a) Even order harmonic profile



(b) Odd order harmonic profile

Fig. 3.16 Harmonic profile (f_1=60Hz, f_{sa}=1080Hz).

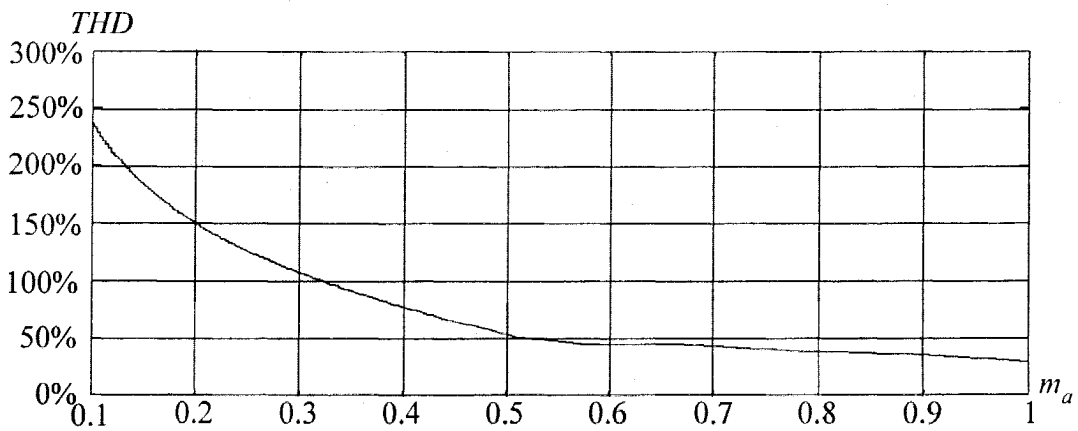
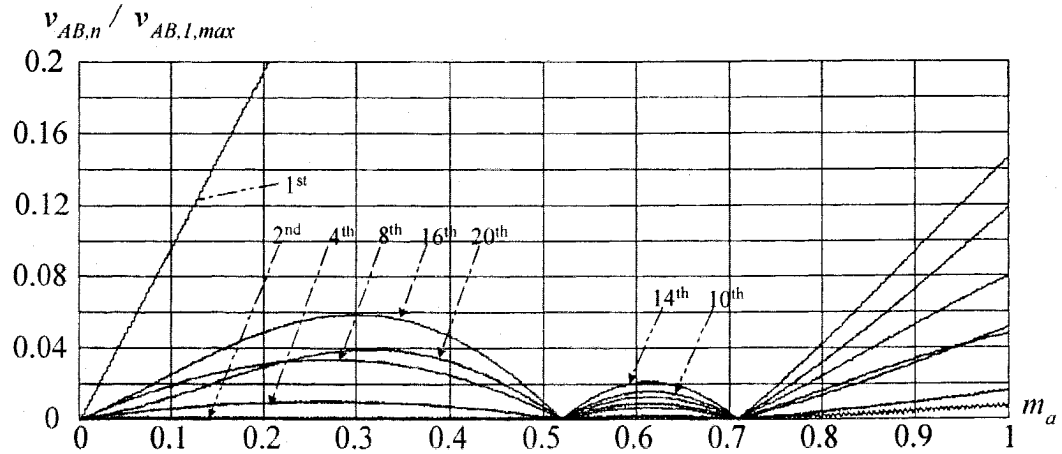
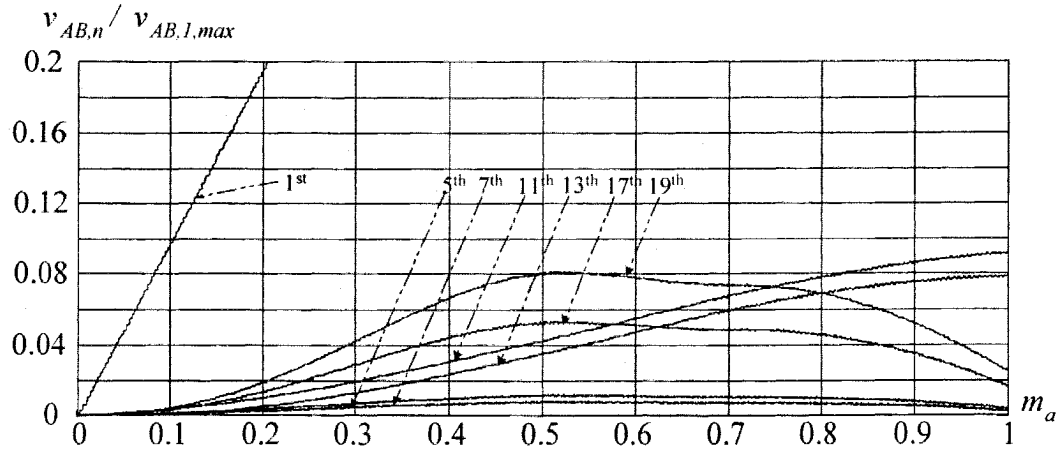


Fig. 3.17 THD profile (f_1=60Hz, f_{sa}=1080Hz).



(a) Even order harmonic profile



(b) Odd order harmonic profile

Fig. 3.18 Harmonic profile (f_1=60Hz, f_{sa}=720Hz).

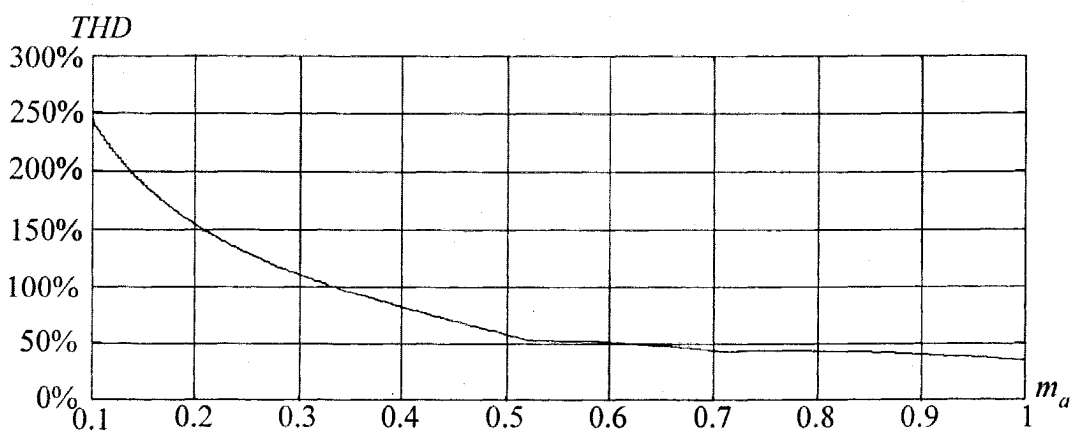


Fig. 3.19 THD profile (f_1=60Hz, f_{sa}=720Hz).

From the harmonic profiles of each case, the even order harmonics are obvious and much larger than close-by odd order ones. For example, in Fig. 3.14, when m_a=0.8, the 16th order harmonic, about 0.016 of the maximum of the fundamental component $V_{AB1,rms}$, is much larger than those of the 17th and the 19th odd order harmonics. The reasons of this phenomenon on even order harmonics is discussed in Chapter 4, in which a new space vector modulation scheme for solving this problem is developed as well.

The THD profiles show that THD of the inverter line-to-line voltage will be decreased when m_a is increased. The comparison among these THD profiles shows that THD value is slightly higher with smaller m_f, which is coincident with the theory.

3.4 Neutral Point Potential Control

As mentioned in Chapter 2, the neutral point potential may deviate when a single DC voltage source is applied as the power supply with two DC capacitors. To solve this problem, a closed-loop neutral point potential control scheme is proposed in Fig. 2.13. In order to realize the control, the PID parameters should be properly tuned. However, since the PID tuning technique is not the main focus herein, the simulations in this section are just designed to demonstrate that the neutral point potential deviation can be corrected according to the mathematical derivations in Section 2.2.5. Therefore, only proportional control is used, and a trial-and-error method is applied to pick up the P parameter. In the simulations, when a large value of P is selected, a voltage oscillation on the DC capacitor occurs; when P is around 0.004, the amplitude of the oscillation becomes stable. In the following simulations, 0.0015 is selected to reduce the amplitude of the oscillation.

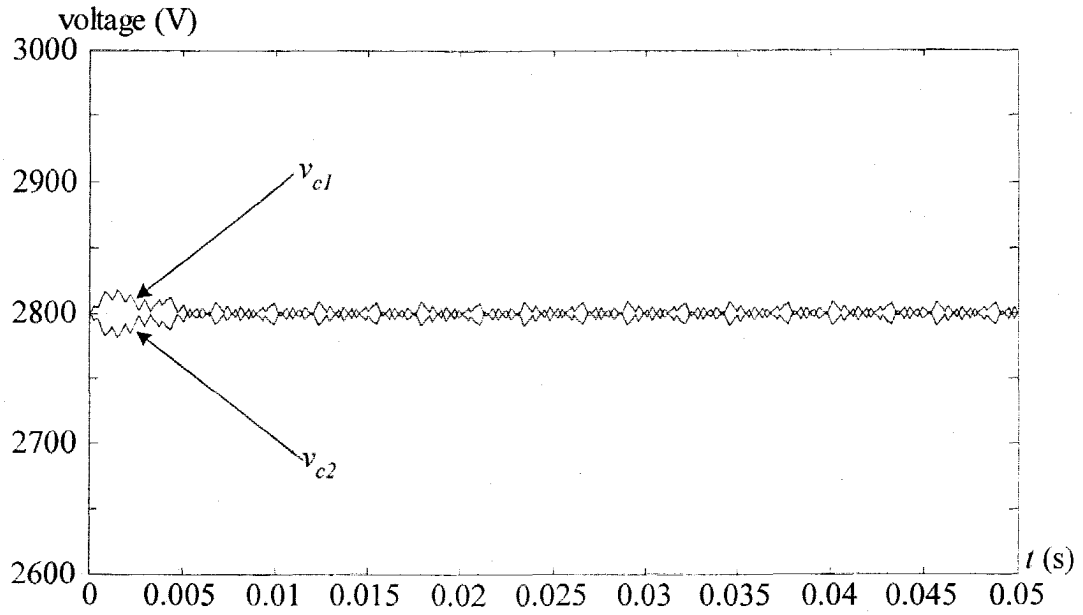


Fig. 3.20 Closed-loop controlled capacitor voltages with same DC capacitors.

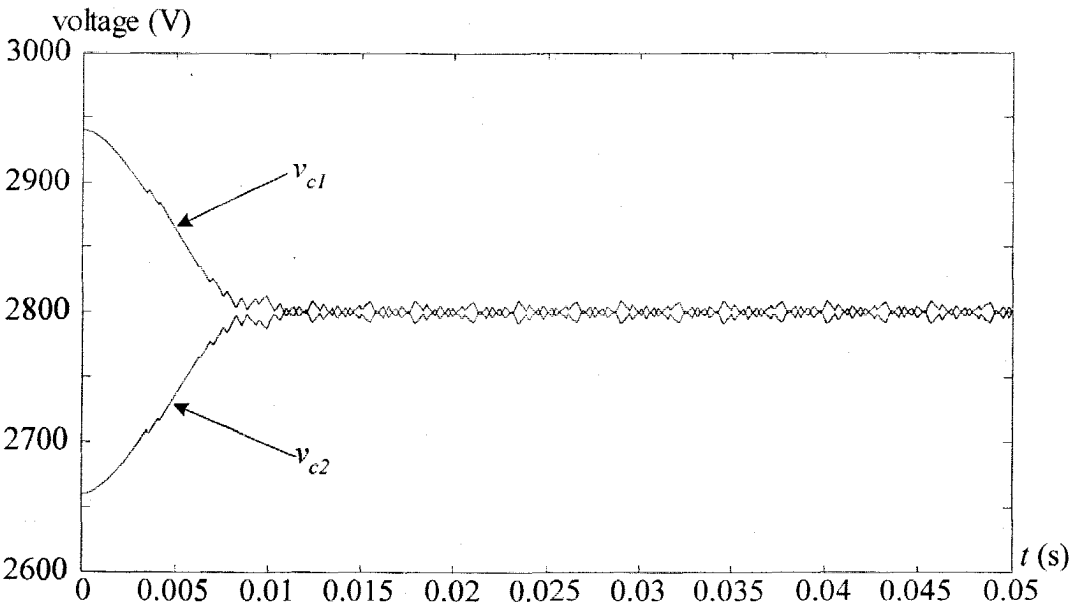


Fig. 3.21 Closed-loop controlled capacitor voltages with different DC capacitors.

As shown in Fig. 3.20 and Fig. 3.21, two conditions of the closed-loop neutral point potential control are simulated: 1) using two identical DC capacitors, 2400μF × 2; and 2) applying two different DC capacitances, 2280μF and 2520 μF, 95% and 105% of 2400μF, where m_a=0.8, f_1=60Hz, and f_{sa}=1440Hz in both cases. From the simulation waveforms, it can be noticed that the DC capacitor voltages converge quickly at 2800V. Therefore, the closed-loop control scheme proposed to correct the neutral point potential deviation is practical.

3.5 Summary

In this chapter, the space vector modulation three-phase three-level NPC inverter was simulated and analyzed on the MATLAB platform. The Simulink models for the space vector modulated NPC inverter were developed. The harmonic components in the inverter output voltage waveforms were analyzed. It was revealed by the investigation that the conventional space vector modulation produces both odd and even order harmonics in the inverter output voltages. The effectiveness of the neutral point potential control was verified as well.

Chapter 4

Even Order Harmonic Elimination

The harmonic analysis in previous chapter shows that the output voltages of the three-level space vector modulated NPC inverter contain even order harmonics, which is not desired in industrial applications. In this chapter, the generation mechanism of even order harmonics is analyzed and a new SVM algorithm is proposed to solve the problem. Simulation models of the new algorithm are developed, and the harmonic analysis is conducted, which shows that the new scheme is able to eliminate all the even order harmonics. In addition, the closed-loop control of neutral point potential in the new SVM scheme is verified.

4.1 Mechanism of Even Order Harmonic Generation

This section focuses on the mechanism of even order harmonic generation.

4.1.1 Half-wave Symmetry

Any periodic waveforms can be expressed by a Fourier series [13] as:

$$f(t) = a_0/2 + \Sigma\,[a_n \cos(n\,\omega_1 t) + b_n \sin(n\,\omega_1 t)] \qquad (4.1\text{-}1)$$

where n=1 to ∞,

$\omega_1 = 2\,\pi\,/T$, T is the period of $f(t)$,

$$a_n = 2/T \int_0^T [\ f(t)\cos(n\omega_1 t)\ ]dt,\ n= 0,1,2,3,\ldots \text{ and}$$

$$b_n = 2/T \int_0^T [\ f(t)\sin(n\omega_1 t)\ ]dt,\quad n= 1,2,3,\ldots$$

Eq. (4.1-1) can also be rewritten as:

$$f(t) = c_0 + \Sigma\, c_n \cos(n\omega_1 t - \gamma_n) \qquad (4.1\text{-}2)$$

where $c_n = \sqrt{a_n^2 + b_n^2}$, and

$$\gamma_n = \tan^{-1}(b_n / a_n).$$

In order to ensure $f(t)$ has no even order harmonic, the amplitude of the even order harmonics c_n (n = 2, 4, 6, 8...) must be zero, where:

$$a_n = 2/T \int_0^T [\ f(t)\cos(n\omega_1 t)\ ]dt = 0, \text{ where } n = 2, 4, 6, 8\ldots \qquad (4.1\text{-}3)$$

and:

$$b_n = 2/T \int_0^T [\ f(t)\sin(n\omega_1 t)\ ]dt = 0, \text{ where } n = 2, 4, 6, 8\ldots \qquad (4.1\text{-}4)$$

Eqs. (4.1-3) and (4.1-4) can be fulfilled only if:

$$f(t) = -f(t + T/2) \qquad (4.1\text{-}5)$$

or in the phase angle format of Eq. (4.1-5):

$$f(\gamma) = -f(\gamma+\pi) \qquad (4.1\text{-}6)$$

From Eqs. (4.1-5) and (4.1-6), it is clear that a function contains no even order harmonic only if its waveform is half-wave symmetrical.

4.1.2 Even Order Harmonics Generation

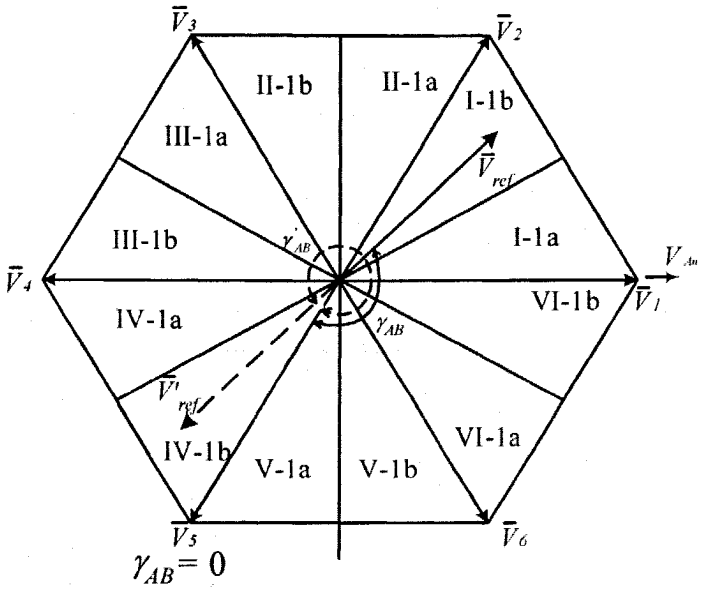
As shown in Chapter 3, the voltage waveforms of the traditional SVM scheme are not half-wave symmetrical so that they can not meet Eq. (4.1-5) or (4.1-6). According to the discussion of 4.1.1, these voltages contain even order harmonics.

In order to present the mechanism of the even order harmonic generation clearly, two sampling periods of the traditional SVM algorithm are picked for examples. As shown in Fig. 4.1(a), the reference vector is located respectively in I-1b and IV-1b, in which the fundamental components of the output voltages are out of phase, i.e.,

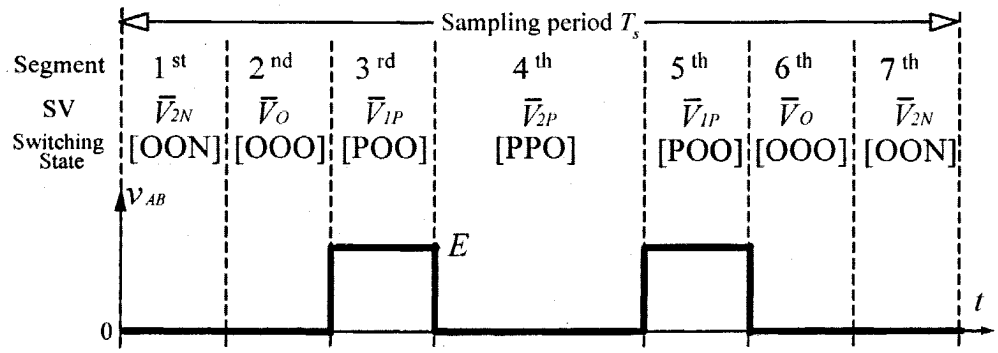
$$\gamma'_{AB} = \gamma_{AB} + \pi \qquad (4.1\text{-}7)$$

The waveforms of line-to-line voltage v_{ab} in these two circumstances can be given as shown in Fig. 4.1 (b) and (c), respectively. According to Section 4.1.1, the voltage waveforms in these two sampling periods supposed to meet the requirement of Eqs. (4.1-5) and (4.1-6) such that v_{ab} has no even order harmonics. However, in the 2^{nd}, 3^{rd}, 5^{th} and 6^{th} segments, the voltage waveforms do not fulfill the requirement of the half-wave symmetry, which is presented by Eqs. (4.1-5) and (4.1-6). This implies that the even order harmonics in the output voltage are introduced by the traditional SVM scheme.

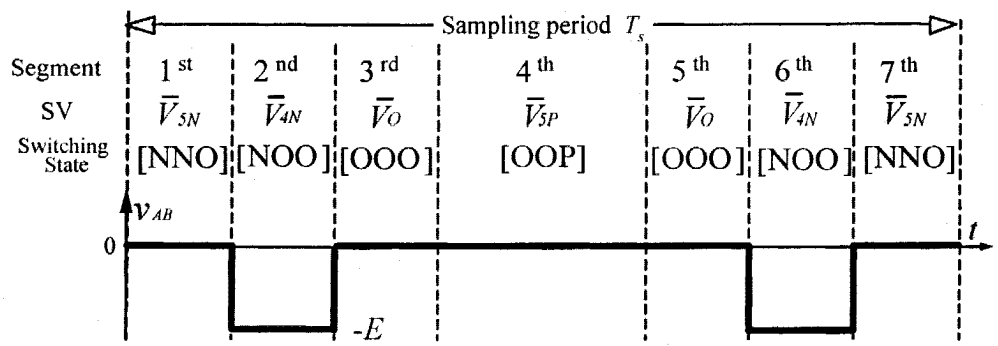
The same problem occurs to the inverter output voltages in other regions. For example, assuming the amplitude modulation index m_a is 0.4 and the frequency modulation index m_f is 12, thus in each fundamental cycle there are 12 sampling periods, each of which presents a reference vector in an inner sub-region shown in Fig. 4.1(a). Consequently, the waveforms of the phase voltage v_{ao} and the line-to-line voltage v_{ab} can be obtained as shown in Fig. 4.2, in which both of them are not half-wave symmetrical so that they both have even order harmonics.



(a) $\bar{V}_{ref}$ in I-1a and IV-1a



(b) I-1b



(c) IV-1b

Fig. 4.1 Space vector modulation and waveforms of v_{AB} in I-1b and IV-1b.

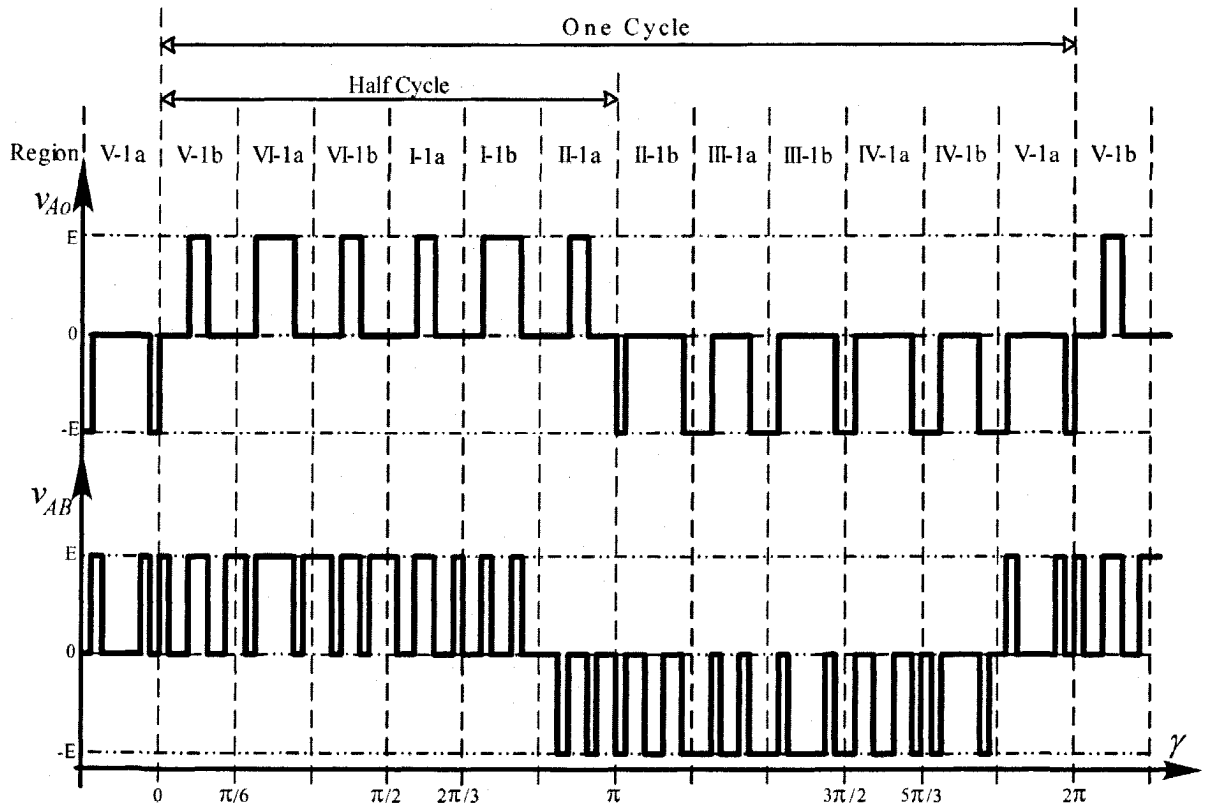


Fig. 4.2 Waveforms of v_{Ao} and v_{AB} generated by traditional scheme (m_a=0.4, m_f=12).

On the other hand, the analysis of the space vector in the α–β frame can also find out the mechanism of the even order harmonic generation in the inverter outputs. The on-duty space vectors in the corresponding segments of the out-of-phase sampling periods sometimes are not symmetrical to each other with the original point. For instance, as shown in Fig. 4.1, the vector $\overline{V}_o$ (in the 2nd segment of I-1b) and the vector $\overline{V}_{4N}$ (in the 2nd segment of V-1b), located in the corresponding segments of two out-of-phase sampling periods, are not symmetrical to each other with the original point. Therefore, their components on the voltage axes don't have same amplitudes and opposite directions. Consequently, the output voltage waveforms are not half-wave symmetrical, resulting in even order harmonics n the inverter output voltages.

However, from Fig. 4.1, it can be noticed that each on-duty space vector has a symmetrical vector used in the out-of-phase sampling periods, although not all of them appear in the corresponding segments. As shown in Fig. 4.1(b) and Fig. 4.1(c), for example,

1. $\overline{V}_2$ in the 1st and the 7th segments of I-1b is symmetrical to $\overline{V}_5$ in the 1st and the 7th segments of IV-1b;
2. $\overline{V}_1$ in the 3rd and the 5th segments of I-1b is symmetrical to $\overline{V}_4$ in the 2nd and the 6th segments of IV-1b; and
3. $\overline{V}_0$ in the 2nd and the 6th segments of I-1b is symmetrical to $\overline{V}_0$ in the 3rd and the 5th segments of IV-1b.

As a conclusion, the even order harmonics in the output voltages are naturally caused by the switching sequence of the traditional seven-segment SVM scheme.

4.2 New Space Vector Modulation Algorithm

As concluded in previous section, the even order harmonics exist in the inverter output voltages because the switching sequence of the traditional seven-segment SVM scheme can not produce half-wave symmetrical waveforms. However, it is also noticed that each on-duty space vector has a symmetrical vector used in the out-of-phase sampling periods. Hence, it is possible to produce a half-wave symmetrical waveform by rearranging the switching sequence.

In Fig. 4.1(c), by switching the 2nd and 3rd, and the 5th and 6th segments in IV-1b, respectively, a new sequence is obtained as shown in Table 4-1, in which the switching sequence in I-1b is also included for comparison. Apparently, the two v_{AB} waveforms of I-1b and IV-1b in Fig. 4.3 are half-wave symmetrical and meet the requirement of Eqs. (4.1-5) and (4.1-6). Therefore, the problem of even order harmonic in these two sub-regions has been solved.

Similarly, the switching sequences are rearranged in all of the shaded areas as shown in Fig. 4.4. Accordingly, the switching pattern design of the new scheme is attached in Appendix II. The waveforms of v_{Ao} and v_{AB} in Fig. 4.2 can be improved as shown in Fig. 4.5, in which both of them are quarter-wave symmetrical:

$$f(t) = f(T/2 - t) = -f(t + T/2) = -f(T - t) \tag{4.1-8}$$

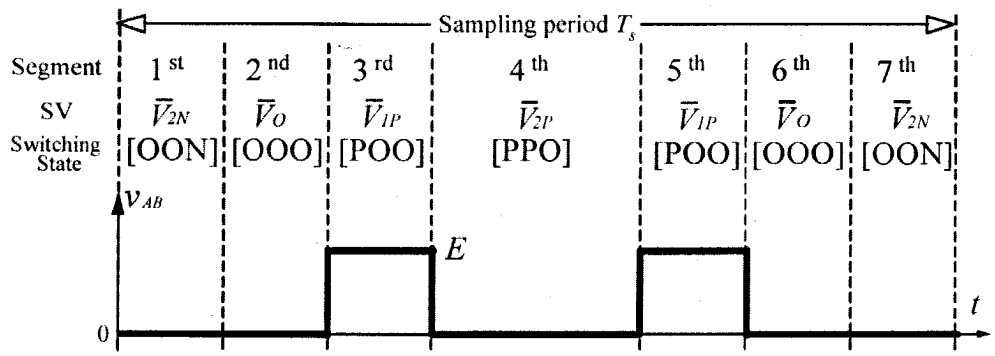
or in the phase angle format:

$$f(\gamma) = f(\pi - \gamma) = -f(\gamma + \pi) = -f(2\pi - \gamma) \tag{4.1-9}$$

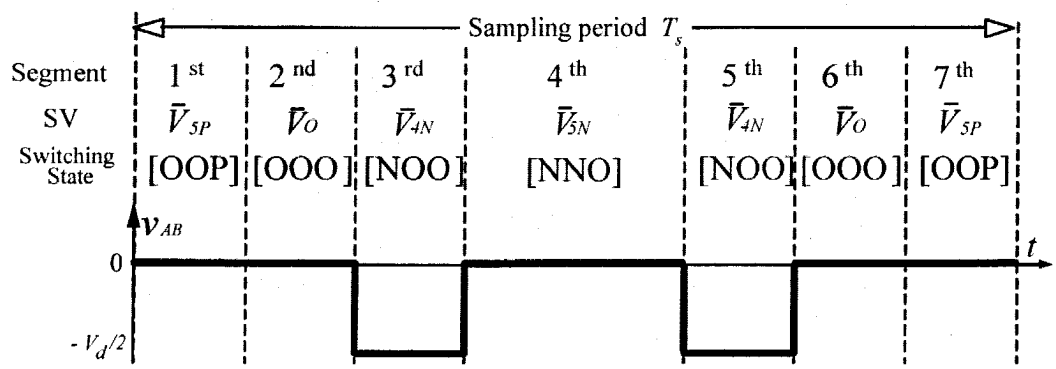
Eqs. (4.1-8) and (4.1-9) also meet the requirements of half-wave symmetry. Therefore, there is no even order harmonics in the waveforms of v_{Ao} and v_{AB}.

Table 4-1 New switching sequence in I-1b and IV-1b.

Segment	I-1b	IV-1b
1st	$\overline{V}_{2N}$ [OON]	$\overline{V}_{5P}$ [OOP]
2nd	$\overline{V}_{0}$ [OOO]	$\overline{V}_{0}$ [OOO]
3rd	$\overline{V}_{1P}$ [POO]	$\overline{V}_{4N}$ [NOO]
4th	$\overline{V}_{2P}$ [PPO]	$\overline{V}_{5N}$ [NNO]
5th	$\overline{V}_{1P}$ [POO]	$\overline{V}_{4N}$ [NOO]
6th	$\overline{V}_{0}$ [OOO]	$\overline{V}_{0}$ [OOO]
7th	$\overline{V}_{2N}$ [OON]	$\overline{V}_{5P}$ [OOP]



(a) space vector modulation in I-1b



(b) space vector modulation in IV-1b

Fig. 4.3 Space vector modulation and waveforms of v_{AB} in I-1b and IV-1b.

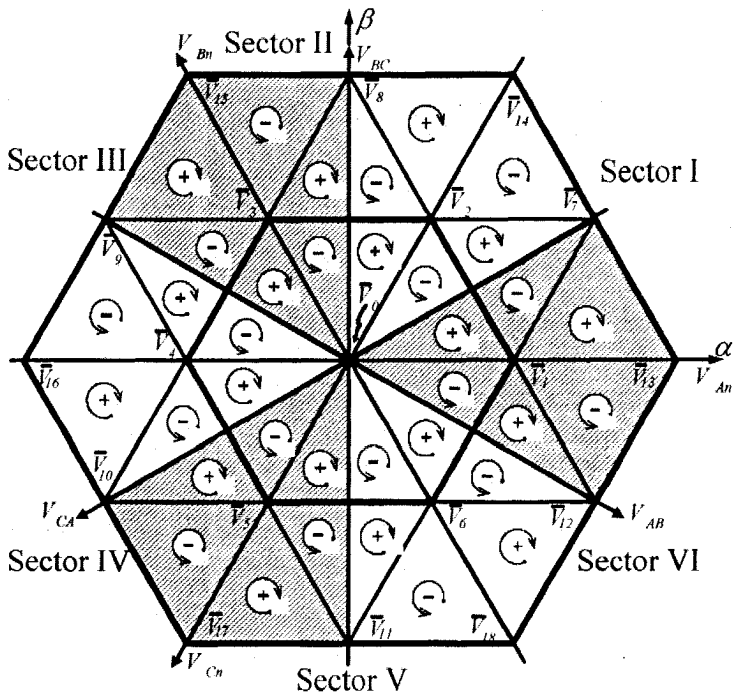


Fig. 4.4 Switching sequence directions of new scheme.

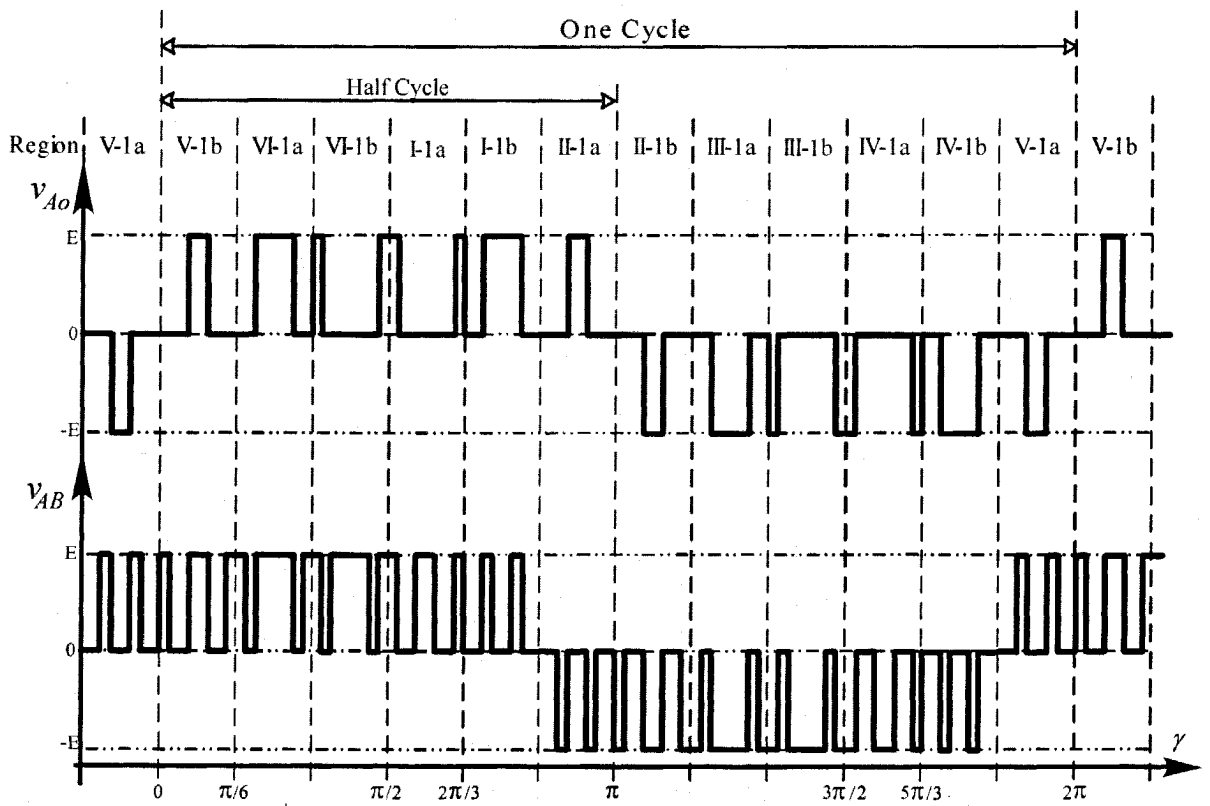


Fig. 4.5 Waveforms of v_{Ao} and v_{AB} generated by new scheme (m_a=0.4, m_f=12).

The proposed new seven-segment SVM scheme contains the same switching states in each sampling period, including the redundant switching states, as those of the traditional SVM algorithm. Only the switching sequence is rearranged to fulfill the half-wave symmetry of the waveforms so as to eliminate the even order harmonics of the inverter output voltages. Hence, the closed-loop neutral point potential control can also be applied to the new scheme. A special attention should be paid to the sign of Δt in the shaded areas shown in Fig.4.4 should be reversed since the redundant switching states exchange their segments.

It should be noted that there is a slight increase of the average device switching frequency in the new scheme. The increase is one half of the fundamental frequency.

The proposed new SVM scheme can also be applied to any other types of multilevel converters for even order harmonic elimination.

4.3 Simulations of the New Algorithm

The proposed new SVM scheme is simulated in this section. In order to verify the elimination of the even order harmonics, the harmonic and THD profiles of the simulation results are presented.

4.3.1 New Space Vector Modulation Model

The Simulink block diagram of the new scheme is the same as that of the traditional scheme in Chapter 3, because the improvement of the scheme is located in modifying the switching sequence, which is coded in the S-function block shown in Fig. 3.3. Based on Fig. 4.4 and compared to the previous S-function program, the new one should:

1) modify the pre-designed look-up table to get the new phase switching state;

2) switch the time intervals of the corresponding segments in the shaded areas; and

3) reverse the sign of the Δt in the shaded areas.

The modified program of the S-function block is attached in Appendix III.

4.3.2 Harmonic and THD Profiles

In order to evaluate the performances of the new SVM scheme, the simulation waveforms and harmonic spectrums of the v_{AB} are shown in Fig. 4.6 and Fig. 4.7, of which the simulation conditions are the same as those of Fig. 3.11 (m_a=0.8, f_1=60Hz, f_{sa}=720Hz) and Fig. 3.12 (m_a=0.8, f_1=30Hz, f_{sa}=720Hz), respectively.

The waveforms of the v_{AB} shown in Fig. 4.6 and Fig. 4.7 are half-wave symmetrical. The harmonic spectrums of the v_{AB} show that only the odd order harmonics are left in the new scheme.

Similar to the simulations in Section 3.3, the harmonic and THD profiles under different simulation conditions of the proposed new SVM scheme are acquired and shown in Fig. 4.8 to Fig. 4.13. Compared with the harmonic profiles of the traditional scheme, all even order harmonics in the new scheme are eliminated. However, the odd order harmonics are increased at the same time. The THD profiles of the output voltages in the new scheme have equivalent features to those of the traditional scheme under the same operating conditions.

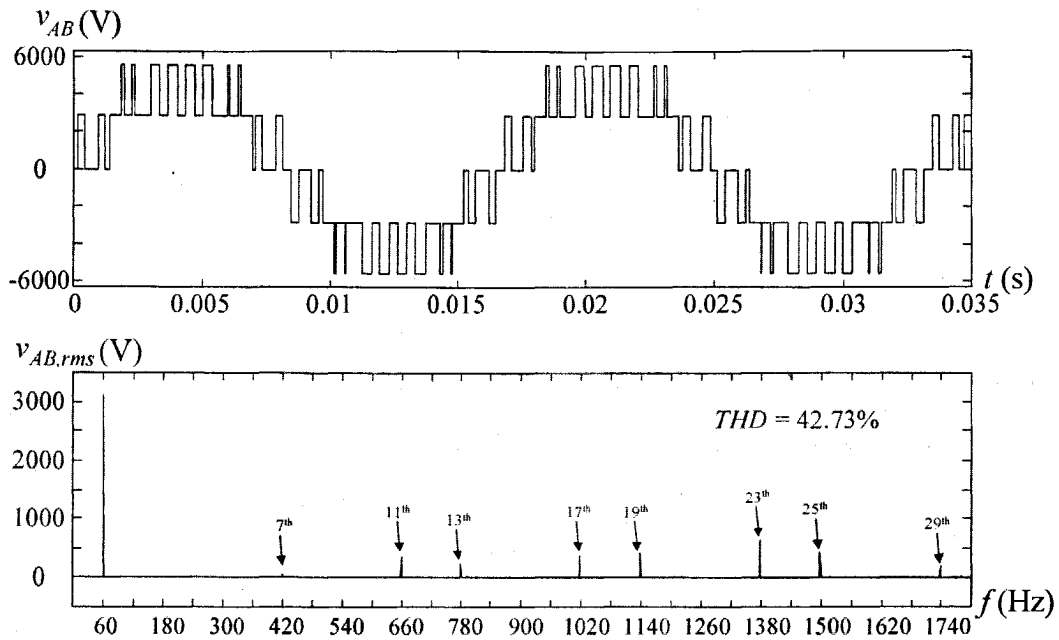


Fig. 4.6 Waveform and spectrum of v_{AB} (m_a=0.8, f_1=60Hz, f_{sa}=720Hz).

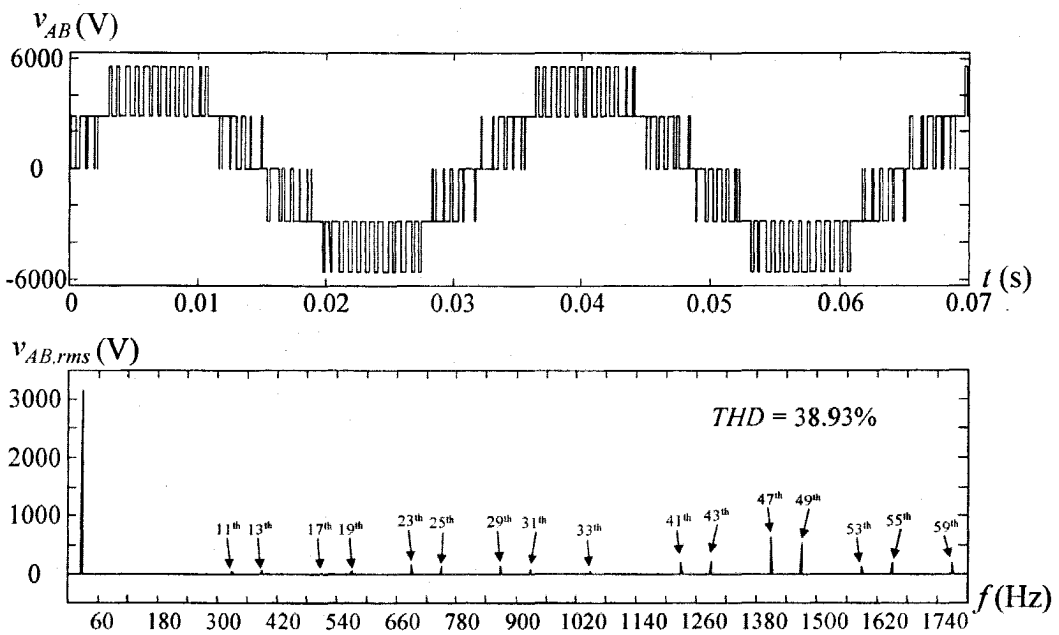
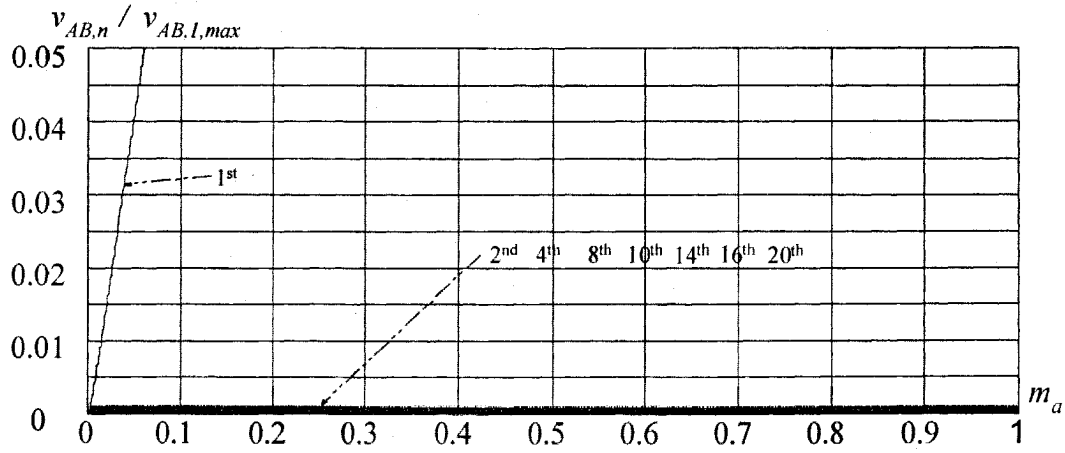
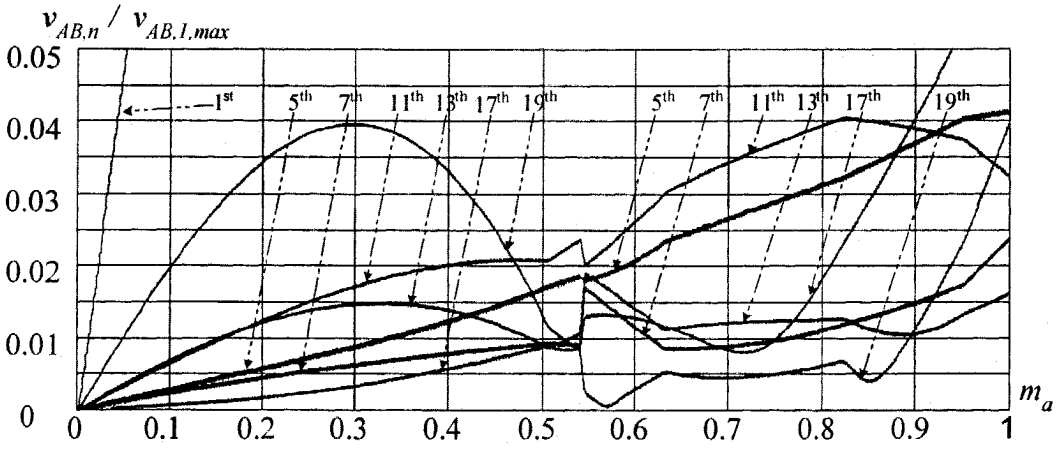


Fig. 4.7 Waveform and spectrum of v_{AB} (m_a=0.8, f_1=30Hz, f_{sa}=720Hz).



(a) Even order harmonic profile



(b) Odd order harmonic profile

Fig. 4.8 Harmonic profile (f_1=60Hz, f_{sa}=1440Hz).

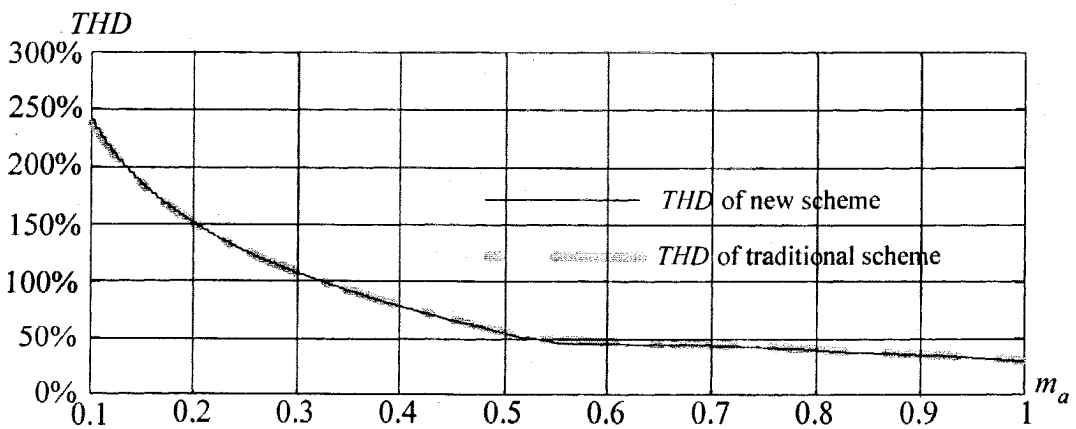
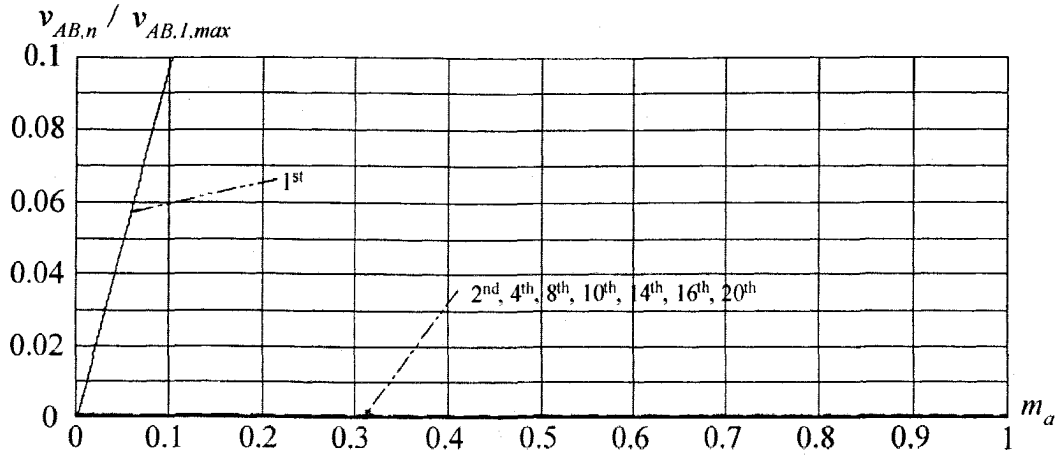
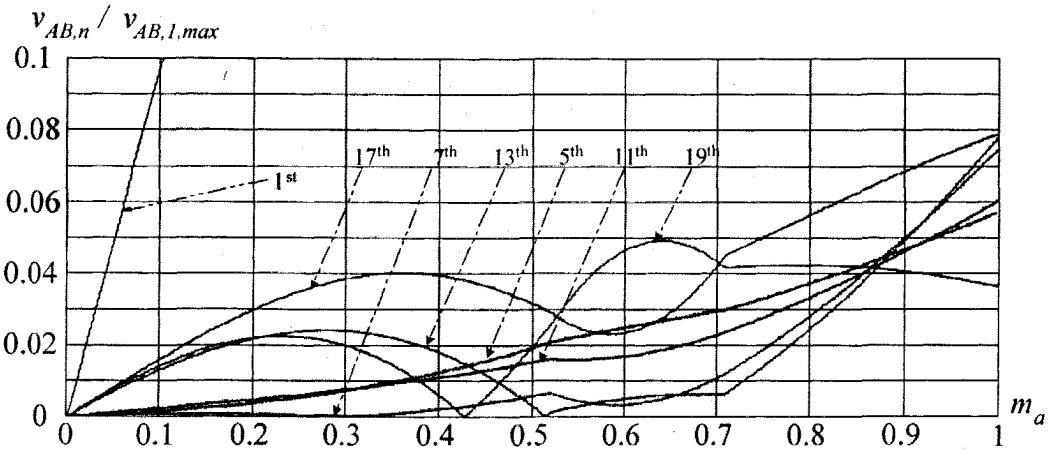


Fig. 4.9 THD profile (f_1=60Hz, f_{sa}=1440Hz).



(a) Even order harmonic profile



(b) Odd order harmonic profile

Fig. 4.10 Harmonic profile (f_1=60Hz, f_{sa}=1080Hz).

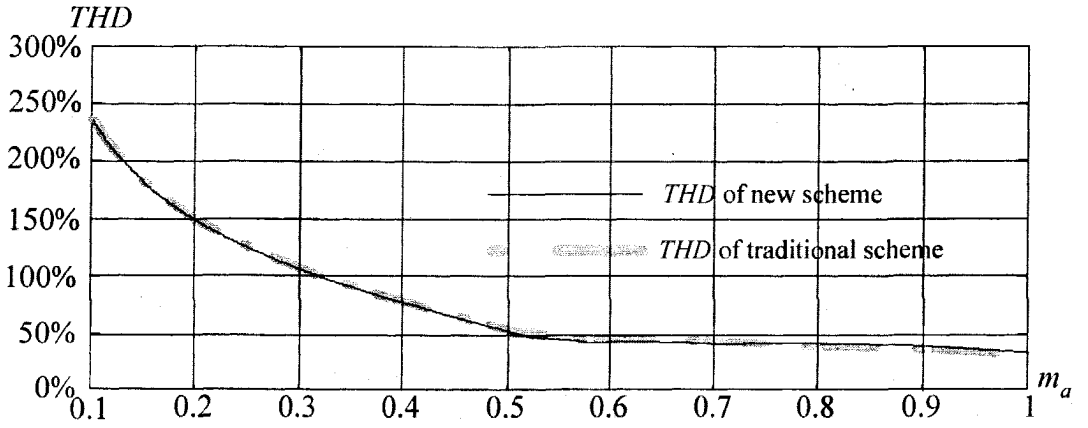
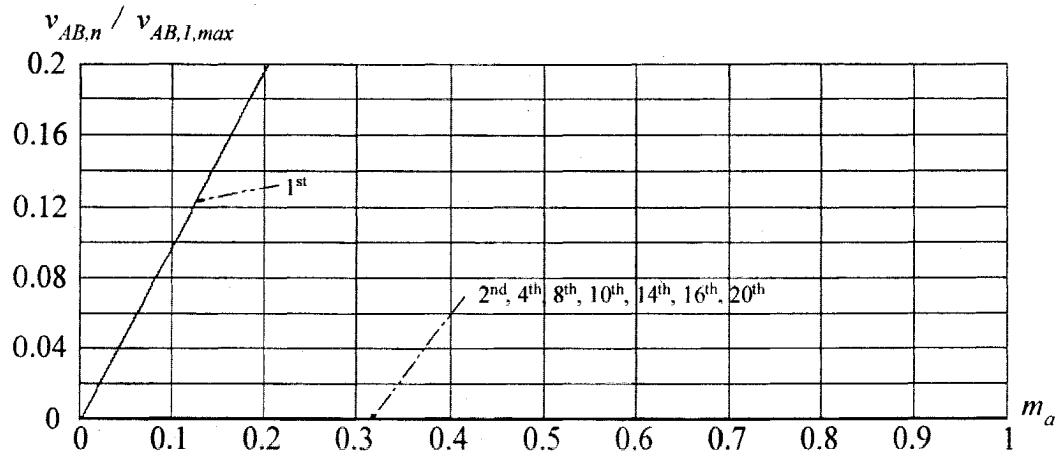
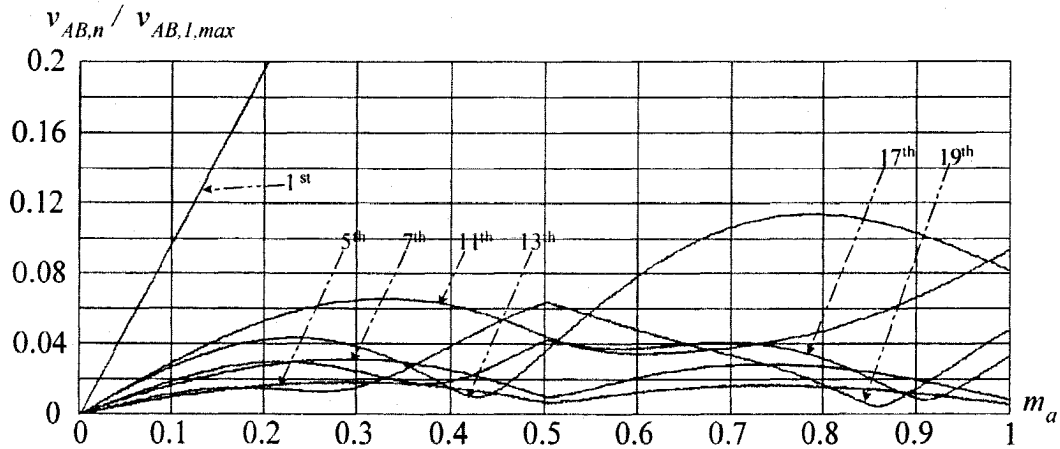


Fig. 4.11 THD profile (f_1=60Hz, f_{sa}=1080Hz).



(a) Even order harmonic profile



(b) Odd order harmonic profile

Fig. 4.12 Harmonic profile (f_1=60Hz, f_{sa}=720Hz).

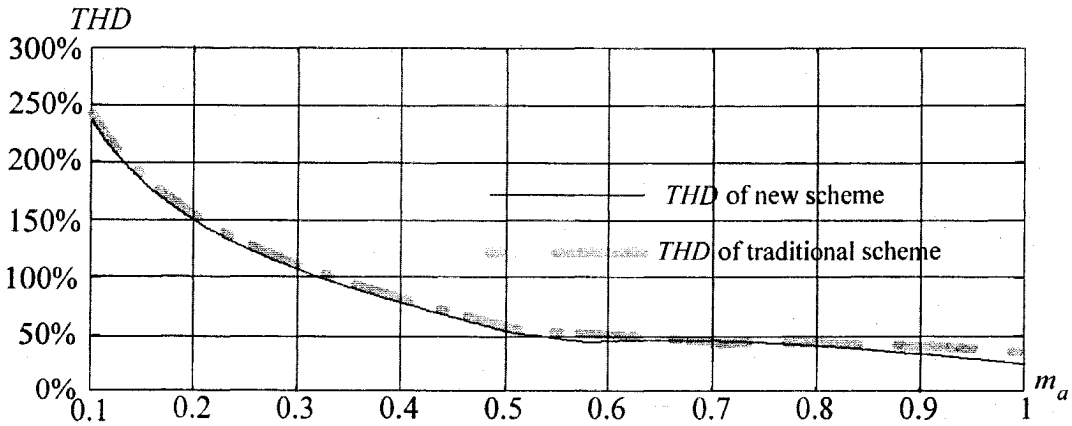


Fig. 4.13 THD profile (f_1=60Hz, f_{sa}=720Hz).

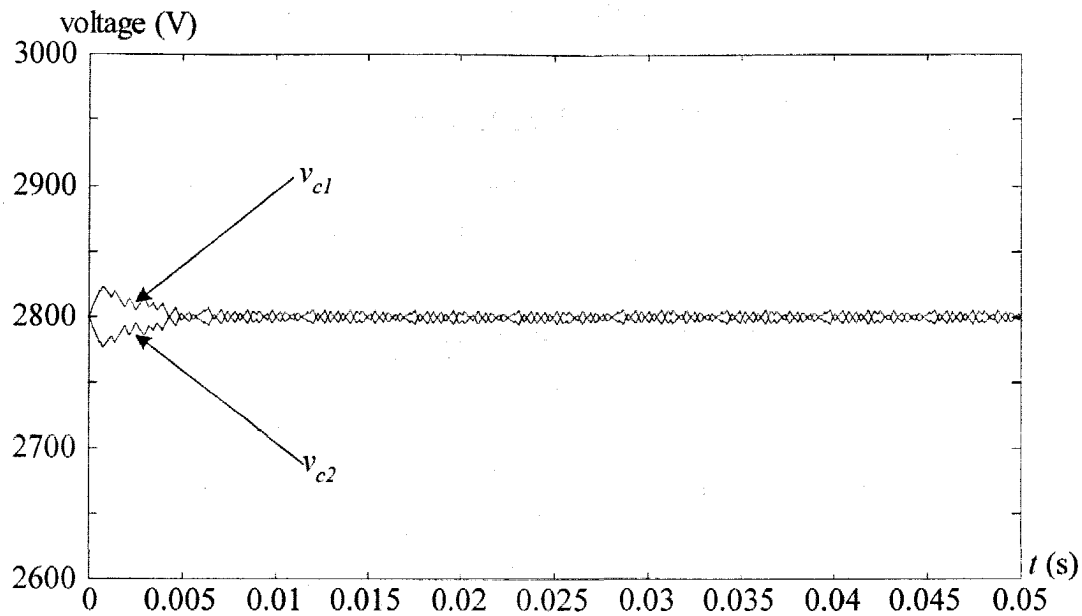


Fig. 4.14 Voltages of same DC capacitors with neutral point potential control.

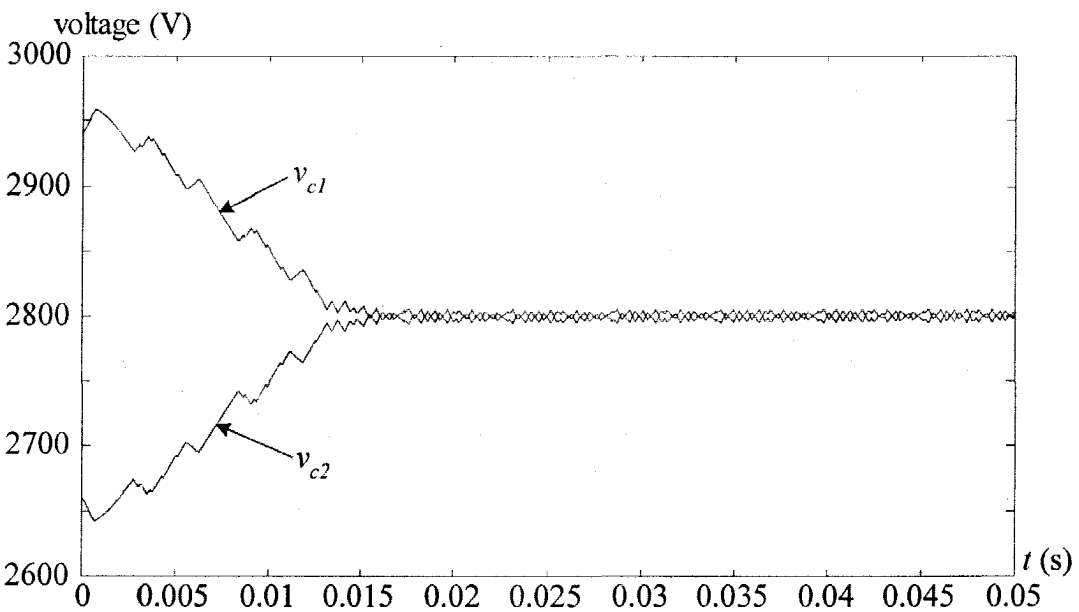


Fig. 4.15 Voltages of different DC capacitors with neutral point potential control.

4.4 Neutral Point Potential Control

Similar to the traditional SVM scheme used in Section 3.4, the closed-loop neutral point potential control is applied to the proposed new SVM scheme. It is also simulated to verify the performance. The simulation parameters are kept the same as those in Section 3.4: m_a= 0.8, f_1= 60Hz, f_{sa}= 1440Hz and P = 0.015. Under the first condition similar to that of Fig. 3.20, the simulation model uses two identical DC capacitors with the capacitance of 2400μF. The voltages over the two DC capacitors are illustrated in Fig. 4.14, in which the neutral point potential is controlled. In the second case shown in Fig. 3.21, the capacitances of the two DC capacitors are 2280μF and 2520μF, respectively. The voltage waveforms of two DC capacitors are shown in Fig. 4.15, where the neutral point potential is corrected as well.

4.5 Summary

In this chapter, the mechanism of the even order harmonic generation in the output voltages of the three-level NPC inverter modulated by the traditional SVM scheme was analyzed. A novel SVM scheme was proposed to eliminate those undesired harmonics. The effectiveness of the propose scheme was verified by simulations. The voltage THD profiles of the proposed scheme were investigated and the results were compared with those of the traditional scheme. Finally, the application of the closed-loop neutral point potential control in the new scheme was verified. The proposed SVM scheme can also be applied to any other types of multilevel converters for even order harmonic elimination.

Chapter 5

Conclusions

This thesis focuses on the space vector modulation (SVM) schemes with even order harmonic elimination for three-phase three-level neutral point clamped (NPC) inverters. The main contributions of this thesis are as follows:

1. The mechanism of the even order harmonic generation in the inverter output voltages is revealed. From the mathematical and simulation analyses, this thesis research has discovered that the even order harmonics in the output voltages of the NPC inverter are produced by asymmetrical waveforms caused by the improper switching sequence of the traditional SVM scheme.
2. A new SVM scheme is developed to eliminate the even order harmonics. The new scheme can produce symmetrical inverter output voltage waveforms. As a result, all the even order harmonics are eliminated. The harmonic performance of the NPC inverter operating under various conditions is investigated, and the THD profile of the new scheme is provided. The proposed SVM scheme can also be applied to any other types of multilevel converters for even order harmonic elimination.
3. An algorithm for the closed-loop control of the inverter neutral point potential is proposed. The cause of neutral point potential deviation is analyzed. The deviation is corrected by using redundant switching states in the SVM scheme. This proposed control algorithm has been verified by simulations.

Recommended future works:

- The proposed SVM scheme and neutral point potential control for the three-level NPC inverter are verified by experiments; and
- The proposed SVM scheme can also be applied to NPC rectifiers for the purpose of even order harmonic elimination. It is recommended that the input power factor control and the output DC voltage control for the rectifier are investigated.

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Appendix I

Harmonic limits in IEEE standards 519-1992

Table 10.3
Current Distortion Limits for General Distribution Systems (120 V Through 69 000 V)

Maximum Harmonic Current Distortion in Percent of I_L						
	Individual Harmonic Order (Odd Harmonics)					
I_{sc}/I_L	<11	11≤*h*<17	17≤*h*<23	23≤*h*<35	35≤*h*	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Even harmonics are limited to 25% of the odd harmonic limits above.

Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.

*All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L.

where

I_{sc} = maximum short-circuit current at PCC.
I_L = maximum demand load current (fundamental frequency component) at PCC.

Table 10.4
Current Distortion Limits for General Subtransmission Systems (69 001 V Through 161 000 V)

Maximum Harmonic Current Distortion in Percent of I_L						
	Individual Harmonic Order (Odd Harmonics)					
I_{sc}/I_L	<11	11≤*h*<17	17≤*h*<23	23≤*h*<35	35≤*h*	TDD
<20*	2.0	1.0	0.75	0.3	0.15	2.5
20<50	3.5	1.75	1.25	0.5	0.25	4.0
50<100	5.0	2.25	2.0	0.75	0.35	6.0
100<1000	6.0	2.75	2.5	1.0	0.5	7.5
>1000	7.5	3.5	3.0	1.25	0.7	10.0

Even harmonics are limited to 25% of the odd harmonic limits above.

Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.

*All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L.

where

I_{sc} = maximum short-circuit current at PCC.
I_L = maximum demand load current (fundamental frequency component) at PCC.

Table 10.5
Current Distortion Limits for General Transmission Systems (>161 kV), Dispersed Generation and Cogeneration

	Individual Harmonic Order (Odd Harmonics)					
I_{sc}/I_L	<11	11≤h<17	17≤h<23	23≤h<35	35≤h	THD
<50	2.0	1.0	0.75	0.3	0.15	2.5
≥50	3.0	1.5	1.15	0.45	0.22	3.75

Even harmonics are limited to 25% of the odd harmonic limits above.

Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.

*All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L.

where

I_{sc} = maximum short-circuit current at PCC.
I_L = maximum demand load current (fundamental frequency component) at PCC.

Appendix II

Switching Pattern Design based on Traditional Scheme

Segment	Time interval	I-1a		I-2a		I-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]
2nd	*Tc/2*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{13}$	[PNN]
3rd	*Tb/2*	$\overline{V}_{0}$	[OOO]	$\overline{V}_{7}$	[PON]	$\overline{V}_{7}$	[PON]
4th	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]
5th	*Tb/2*	$\overline{V}_{0}$	[OOO]	$\overline{V}_{7}$	[PON]	$\overline{V}_{7}$	[PON]
6th	*Tc/2*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{13}$	[PNN]
7th	*Ta/4*	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]

Segment	Time interval	I-1b		I-2b		I-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]
2nd	*Tb/2*	$\overline{V}_{0}$	[OOO]	$\overline{V}_{7}$	[PON]	$\overline{V}_{7}$	[PON]
3rd	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{14}$	[PPN]
4th	*Tc/2*	$\overline{V}_{2P}$	[PPO]	$\overline{V}_{2P}$	[PPO]	$\overline{V}_{2P}$	[PPO]
5th	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{14}$	[PPN]
6th	*Tb/2*	$\overline{V}_{0}$	[OOO]	$\overline{V}_{7}$	[PON]	$\overline{V}_{7}$	[PON]
7th	*Tc/4*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]

Segment	Time interval	II-1a		II-2a		II-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]
2nd	*Tb/2*	$\overline{V}_{0}$	[OOO]	$\overline{V}_{8}$	[OPN]	$\overline{V}_{8}$	[OPN]
3rd	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{14}$	[PPN]
4th	*Tc/2*	$\overline{V}_{2P}$	[PPO]	$\overline{V}_{2P}$	[PPO]	$\overline{V}_{2P}$	[PPO]
5th	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{14}$	[PPN]
6th	*Tb/2*	$\overline{V}_{0}$	[OOO]	$\overline{V}_{8}$	[OPN]	$\overline{V}_{8}$	[OPN]
7th	*Tc/4*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]

Segment	Time interval	II-1b		II-2b		II-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]
2nd	*Tc/2*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{15}$	[NPN]
3rd	*Tb/2*	$\overline{V}_{0}$	[OOO]	$\overline{V}_{8}$	[OPN]	$\overline{V}_{8}$	[OPN]
4th	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]
5th	*Tb/2*	$\overline{V}_{0}$	[OOO]	$\overline{V}_{8}$	[OPN]	$\overline{V}_{8}$	[OPN]
6th	*Tc/2*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{15}$	[NPN]
7th	*Ta/4*	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]

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Segment	Time interval	III-1a		III-2a		III-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]
2nd	*Tc/2*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{15}$	[NPN]
3rd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{9}$	[NPO]	$\overline{V}_{9}$	[NPO]
4th	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]
5th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{9}$	[NPO]	$\overline{V}_{9}$	[NPO]
6th	*Tc/2*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{15}$	[NPN]
7th	*Ta/4*	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]

Segment	Time interval	III-1b		III-2b		III-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{9}$	[NPO]	$\overline{V}_{9}$	[NPO]
3rd	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{16}$	[NPP]
4th	*Tc/2*	$\overline{V}_{4P}$	[OPP]	$\overline{V}_{4P}$	[OPP]	$\overline{V}_{4P}$	[OPP]
5th	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{16}$	[NPP]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{9}$	[NPO]	$\overline{V}_{9}$	[NPO]
7th	*Tc/4*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]

Segment	Time interval	IV-1a		IV-2a		IV-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{10}$	[NOP]	$\overline{V}_{10}$	[NOP]
3rd	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{16}$	[NPP]
4th	*Tc/2*	$\overline{V}_{4P}$	[OPP]	$\overline{V}_{4P}$	[OPP]	$\overline{V}_{4P}$	[OPP]
5th	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{16}$	[NPP]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{10}$	[NOP]	$\overline{V}_{10}$	[NOP]
7th	*Tc/4*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]

Segment	Time interval	IV-1b		IV-2b		IV-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]
2nd	*Tc/2*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{17}$	[NNP]
3rd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{10}$	[NOP]	$\overline{V}_{10}$	[NOP]
4th	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]
5th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{10}$	[NOP]	$\overline{V}_{10}$	[NOP]
6th	*Tc/2*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{17}$	[NNP]
7th	*Ta/4*	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]

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Segment	Time interval	V-1a		V-2a		V-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]
2nd	*Tc/2*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{17}$	[NNP]
3rd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{11}$	[ONP]	$\overline{V}_{11}$	[ONP]
4th	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]
5th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{11}$	[ONP]	$\overline{V}_{11}$	[ONP]
6th	*Tc/2*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{17}$	[NNP]
7th	*Ta/4*	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]

Segment	Time interval	V-1b		V-2b		V-4	
		vector	switching state	vector	switching state	vector	switching state
1	*Tc/4*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]
2	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{11}$	[ONP]	$\overline{V}_{11}$	[ONP]
3	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{18}$	[PNP]
4	*Tc/2*	$\overline{V}_{6P}$	[POP]	$\overline{V}_{6P}$	[POP]	$\overline{V}_{6P}$	[POP]
5	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{18}$	[PNP]
6	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{11}$	[ONP]	$\overline{V}_{11}$	[ONP]
7	*Tc/4*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]

Segment	Time interval	VI-1a		VI-2a		VI-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{12}$	[PNO]	$\overline{V}_{12}$	[PNO]
3rd	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{18}$	[PNP]
4th	*Tc/2*	$\overline{V}_{6P}$	[POP]	$\overline{V}_{6P}$	[POP]	$\overline{V}_{6P}$	[POP]
5th	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{18}$	[PNP]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{12}$	[PNO]	$\overline{V}_{12}$	[PNO]
7th	*Tc/4*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]

Segment	Time interval	VI-1b		VI-2b		VI-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]
2nd	*Tc/2*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{13}$	[PNN]
3rd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{12}$	[PNO]	$\overline{V}_{12}$	[PNO]
4th	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]
5th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{12}$	[PNO]	$\overline{V}_{12}$	[PNO]
6th	*Tc/2*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{13}$	[PNN]
7th	*Ta/4*	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]

(End of Appendix I)

Appendix III

Switching Pattern Design based on New Scheme

Segment	Time interval	I-1a		I-2a		I-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{7}$	[PON]	$\overline{V}_{7}$	[PON]
3rd	*Tc/2*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{13}$	[PNN]
4th	*Ta/2*	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]
5th	*Tc/2*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{13}$	[PNN]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{7}$	[PON]	$\overline{V}_{7}$	[PON]
7th	*Ta/4*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]

Segment	Time interval	I-1b		I-2b		I-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{7}$	[PON]	$\overline{V}_{7}$	[PON]
3rd	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{14}$	[PPN]
4th	*Tc/2*	$\overline{V}_{2P}$	[PPO]	$\overline{V}_{2P}$	[PPO]	$\overline{V}_{2P}$	[PPO]
5th	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{14}$	[PPN]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{7}$	[PON]	$\overline{V}_{7}$	[PON]
7th	*Tc/4*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]

Segment	Time interval	II-1a		II-2a		II-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{8}$	[OPN]	$\overline{V}_{8}$	[OPN]
3rd	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{14}$	[PPN]
4th	*Tc/2*	$\overline{V}_{2P}$	[PPO]	$\overline{V}_{2P}$	[PPO]	$\overline{V}_{2P}$	[PPO]
5th	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{14}$	[PPN]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{8}$	[OPN]	$\overline{V}_{8}$	[OPN]
7th	*Tc/4*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]

Segment	Time interval	II-1b		II-2b		II-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{8}$	[OPN]	$\overline{V}_{8}$	[OPN]
3rd	*Tc/2*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{15}$	[NPN]
4th	*Ta/2*	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]
5th	*Tc/2*	$\overline{V}_{2N}$	[OON]	$\overline{V}_{2N}$	[OON]	$\overline{V}_{15}$	[NPN]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{8}$	[OPN]	$\overline{V}_{8}$	[OPN]
7th	*Ta/4*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]

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Segment	Time interval	III-1a		III-2a		III-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{9}$	[NPO]	$\overline{V}_{9}$	[NPO]
3rd	*Tc/2*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{15}$	[NPN]
4th	*Ta/2*	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]	$\overline{V}_{3N}$	[NON]
5th	*Tc/2*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{15}$	[NPN]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{9}$	[NPO]	$\overline{V}_{9}$	[NPO]
7th	*Ta/4*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]

Segment	Time interval	III-1b		III-2b		III-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{9}$	[NPO]	$\overline{V}_{9}$	[NPO]
3rd	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{16}$	[NPP]
4th	*Tc/2*	$\overline{V}_{4P}$	[OPP]	$\overline{V}_{4P}$	[OPP]	$\overline{V}_{4P}$	[OPP]
5th	*Ta/2*	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{3P}$	[OPO]	$\overline{V}_{16}$	[NPP]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{9}$	[NPO]	$\overline{V}_{9}$	[NPO]
7th	*Tc/4*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]

Segment	Time interval	IV-1a		IV-2a		IV-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{10}$	[NOP]	$\overline{V}_{10}$	[NOP]
3rd	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{16}$	[NPP]
4th	*Tc/2*	$\overline{V}_{4P}$	[OPP]	$\overline{V}_{4P}$	[OPP]	$\overline{V}_{4P}$	[OPP]
5th	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{16}$	[NPP]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{10}$	[NOP]	$\overline{V}_{10}$	[NOP]
7th	*Tc/4*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]

Segment	Time interval	IV-1b		IV-2b		IV-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{10}$	[NOP]	$\overline{V}_{10}$	[NOP]
3rd	*Tc/2*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{17}$	[NNP]
4th	*Ta/2*	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]
5th	*Tc/2*	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{4N}$	[NOO]	$\overline{V}_{17}$	[NNP]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{10}$	[NOP]	$\overline{V}_{10}$	[NOP]
7th	*Ta/4*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]

(to be continued)

(Continue of last page)

Segment	Time interval	V-1a		V-2a		V-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{11}$	[ONP]	$\overline{V}_{11}$	[ONP]
3rd	*Tc/2*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{17}$	[NNP]
4th	*Ta/2*	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]	$\overline{V}_{5N}$	[NNO]
5th	*Tc/2*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{17}$	[NNP]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{11}$	[ONP]	$\overline{V}_{11}$	[ONP]
7th	*Ta/4*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]

Segment	Time interval	V-1b		V-2b		V-4	
		vector	switching state	vector	switching state	vector	switching state
1	*Tc/4*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]
2	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{11}$	[ONP]	$\overline{V}_{11}$	[ONP]
3	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{18}$	[PNP]
4	*Tc/2*	$\overline{V}_{6P}$	[POP]	$\overline{V}_{6P}$	[POP]	$\overline{V}_{6P}$	[POP]
5	*Ta/2*	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{5P}$	[OOP]	$\overline{V}_{18}$	[PNP]
6	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{11}$	[ONP]	$\overline{V}_{11}$	[ONP]
7	*Tc/4*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]

Segment	Time interval	VI-1a		VI-2a		VI-3	
		vector	switching state	vector	switching state	vector	switching state
1st	*Tc/4*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{12}$	[PNO]	$\overline{V}_{12}$	[PNO]
3rd	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{18}$	[PNP]
4th	*Tc/2*	$\overline{V}_{6P}$	[POP]	$\overline{V}_{6P}$	[POP]	$\overline{V}_{6P}$	[POP]
5th	*Ta/2*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{18}$	[PNP]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{12}$	[PNO]	$\overline{V}_{12}$	[PNO]
7th	*Tc/4*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]

Segment	Time interval	VI-1b		VI-2b		VI-4	
		vector	switching state	vector	switching state	vector	switching state
1st	*Ta/4*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]
2nd	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{12}$	[PNO]	$\overline{V}_{12}$	[PNO]
3rd	*Tc/2*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{13}$	[PNN]
4th	*Ta/2*	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]	$\overline{V}_{1N}$	[ONN]
5th	*Tc/2*	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{6N}$	[ONO]	$\overline{V}_{13}$	[PNN]
6th	*Tb/2*	$\overline{V}_{O}$	[OOO]	$\overline{V}_{12}$	[PNO]	$\overline{V}_{12}$	[PNO]
7th	*Ta/4*	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]	$\overline{V}_{1P}$	[POO]

(End of Appendix II)

Appendix IV

S-funtion Program used in Gating Signal Generator based on New Scheme

```
function [sys,x0,str,ts] = Model_I(t,x,u,flag,sfq,deadtime)          %sfp: sample frequency
ct_period =1/sfq;                                                      %ct_period: sample time
deadtime=deadtime;                                                          %interlock deadtime
switch flag,
  %%%%%%%%%%%%%%%%%%%
  % Initialization %
  %%%%%%%%%%%%%%%%%%%
  % Initialize the states, sample times, and state ordering strings.
  case 0
    [sys,x0,str,ts]=mdlInitializeSizes(t,x,u,ct_period);
  %%%%%%%%%%%%%%%%%%%
  % Main function and Data update %
  %%%%%%%%%%%%%%%%%%%
  case 2
    sys=mdlUpdate(t,x,u,ct_period,deadtime);
  %%%%%%%%%%
  % Outputs %
  %%%%%%%%%%
  % Return the outputs of the S-function block.
  case 3
    sys=mdlOutputs(t,x,u);
  case {1, 4, 9 }
    sys=[];
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  % Unexpected flags (error handling)%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  % Return an error message for unhandled flag values.
  otherwise
    error(['Unhandled flag = ',num2str(flag)]);
end
% end timestwo
%=============================================================================
% mdlInitializeSizes
% Return the sizes, initial conditions, and sample times for the S-function.
%=============================================================================
function [sys,x0,str,ts] = mdlInitializeSizes(t,x,u,ct_period)
sizes = simsizes;
sizes.NumContStates  = 0;
sizes.NumDiscStates  = 25;
sizes.NumOutputs     = 12;
sizes.NumInputs      = 6;                  % In Model I, this line is: sizes.NumInputs  =2;
sizes.DirFeedthrough = 5;
sizes.NumSampleTimes = 2;
sys = simsizes(sizes);
str = [];
x0  = zeros(1);
ts  = [ct_period,0;0,0];
% end mdlInit.ialize Sizes
```

```
%=============================================================================
% mdl discrete state
% Return the output vector for the S-function
%=============================================================================
function sys=mdlUpdate(t,x,u,ct_period,deadtime)
%input:u1:vector length,u2:vector angle
%       For Model II: u3:capacitor voltage u4:P parameter, u5: I parameter, u6: D parameter
%       ct_period:sample time, deadtime:interlock deadtime
%interval parameters: dwell times: x1=t1,x2=t3,x3=t3
%                           x4=global region number
%                           x5=sample time, x6=delta t
%           gating: x7=g_a_1, x8=g_a_2, x9=g_a_3, x10=g_a_4
%                           x11=g_b_1,x12=g_b_2,x13=g_b_3,x14=g_b_4
%                           x15=g_c_1,x16=g_c_2,x17=g_c_3,x18=g_c_4
%                           x19=interlock flag, x20=interlock start time
sys(1:25)=x(1:25);
%calculation of dwell time
if rem(t,ct_period)/ct_period < 1e-3,
%vector angle liner
vangle=rem(u(2),2*pi);
if vangle < 0,
    vangle=vangle+2*pi;
end
%section number
sno= round(3*vangle/pi+.5);
%interval angle
ivangle=vangle-(sno-1)*pi/3;                                    % thita
%dwell time in region 2
ta=ct_period*(1-2*u(1)*sin(ivangle));                           % ta
tb=ct_period*(2*u(1)*sin(ivangle+pi/3)-1);                      % tb
tc=ct_period*(1-2*u(1)*sin(pi/3-ivangle));                      % tc
%interval region number and dwell time in each region
if ta<0,
    irno=6;                                                     % ta'<0,   =>in region 4
    t3=ct_period*(2*u(1)*sin(ivangle)-1);
    t2=ct_period*2*u(1)*sin(pi/3-ivangle);
  t1=ct_period*(2-2*u(1)*sin(ivangle+pi/3));
else
    if tc<0,
        irno=3;                                                 % ta'>=0,tc'<0,   =>in region 3
        t1=ct_period*(2-2*u(1)*sin(ivangle+pi/3));
        t2=ct_period*2*u(1)*sin(ivangle);
        t3=ct_period*(2*u(1)*sin(pi/3-ivangle)-1);
    else
        if tb<0,                                                % ta',tc'>=0, tb'<0,   =>in region 1
            if ivangle>pi/6,
                irno=2;         % ta',tc'>=0, tb'<0, interval angle > pi/6,   =>in region 1b
                t3=ct_period*2*u(1)*sin(pi/3-ivangle);
                t2=ct_period*(1-2*u(1)*sin(ivangle+pi/3));
                t1=ct_period*2*u(1)*sin(ivangle);
            else
                irno=1;         % ta',tc'>=0, tb'<0, interval angle <= pi/6,   =>in region 1a
                t1=ct_period*2*u(1)*sin(pi/3-ivangle);
                t2=ct_period*(1-2*u(1)*sin(ivangle+pi/3));
                t3=ct_period*2*u(1)*sin(ivangle);
            end
```

```
        else                                                                    %   ta',tb',tc'>=0,
=> in region 2
            if ivangle>pi/6,
                irno=5;         % ta',tc'>=0, tb'<0, interval angle > pi/6,   =>in region 2b
                if rem(sno,2)<1e-2,                                         %in sector II, IV or VI
                    t1=tc;
                    t3=ta;
                        t2=tb;
                else                                                        %in sector I, III or V
                    t1=ta;
                    t2=tb;
                        t3=tc;
                end
            else
                irno=4;         % ta',tc'>=0, tb'<0, interval angle <= pi/6,   =>in region 2a
                    t1=ta;
                    t2=tb;
                        t3=tc;
            end
        end
    end
end
%global region number
grno=(sno-1)*6+irno;
sys(1)=t1;
sys(2)=t2;
sys(3)=t3;
sys(4)=grno;
sys(5)=ct_period;
%Begin of delta t: only for Model II. Delete this part for Model I.
p=u(4);
dt= (2800-u(3))*p;
sys(6)=dt*(-1)^(sno+floor(ivangle*6/pi));
end
% End of delta t: only for Model II. Delete this part for Model I.
if x(5)>0,                  %normal condition other than the beginning
%interval time
it= rem (t,x(5));
%seven time intervals corrected with delta t
t1=x(1)/4-x(1)*x(6);                        % In Model I, this line is: t1=x(1)/4;
t2=x(2)/2+t1;
t3=x(3)/2+t2;
t4=x(1)/2+x(1)*x(6)*2+t3;                   % In Model I, this line is: t4=x(1)/2+ t3;
t5=x(3)/2+t4;
t6=x(2)/2+t5;
%on-duty vector interval number
if it > t6,
    ivn=1;
else
    if it > t5,
        ivn=2;
    else
        if it > t4,
            ivn=3;
        else
```

```
            if it > t3,
                ivn=4;
            else
                if it > t2,
                    ivn=3;
                else
                    if it > t1,
                        ivn=2;
                    else
                        ivn=1;
                    end
                end
            end
        end
    end
end
%in duty vector global number
gvn = ivn + x(4) * 4 - 4;
%tables of switching states
A=[2 1 1 1 1 1 2 2 2 2 2 1 2 2 1 1 1 2 2 2 1 2 2 2 1 1 1 2 1 1 1 0 1 1 2 2 1 1 1 2 1 1 1 0 1 1 0 0 1 1 0 0 0 1 1 1 1 0
0 0 1 0 0 0 0 0 1 1 0 0 0 1 0 1 1 1 1 1 0 0 0 0 0 1 0 0 1 1 1 0 0 0 1 0 0 0 1 1 1 0 1 1 1 2 1 1 0 0 1 1 1 0 1 1 1 2 1 1
2 2 1 1 2 2 2 1 1 1 1 2 2 2 1 2 2 2 2 2 1 1 2 2 2 1];
B=[1 1 1 0 1 1 1 2 1 1 0 0 1 1 1 0 1 1 1 2 1 1 2 2 1 1 2 2 2 1 1 1 1 2 2 2 1 2 2 2 2 2 1 1 2 2 2 1 2 1 1 1 1 1 2 2 2 2
2 1 2 2 1 1 1 2 2 2 1 2 2 2 1 1 1 2 1 1 1 0 1 1 2 2 1 1 1 2 1 1 1 0 1 1 0 0 1 1 0 0 0 1 1 1 1 0 0 0 1 0 0 0 0 0 1 1 0 0
0 1 0 1 1 1 1 1 0 0 0 0 0 1 0 0 1 1 1 0 0 0 1 0 0 0];
C=[1 1 0 0 0 1 1 1 1 0 0 0 1 0 0 0 0 0 1 1 0 0 0 1 0 1 1 1 1 1 0 0 0 0 0 1 0 0 1 1 1 0 0 0 1 0 0 0 1 1 1 0 1 1 1 2 1 1
0 0 1 1 1 0 1 1 1 2 1 1 2 2 2 2 1 1 1 1 1 2 1 2 2 2 1 2 2 2 2 2 1 1 2 2 2 1 2 1 1 1 1 1 2 2 2 2 2 1 2 2 1 1 1 2 2 2 1 2
2 2 1 1 1 2 1 1 1 0 1 1 2 2 1 1 1 2 1 1 1 0 1 1 0 0];
%switching states
pa = A(gvn);
pb = B(gvn);
pc = C(gvn);
%gate signals
if pa==2,
    g(1)=1;
    g(2)=1;
    g(3)=0;
    g(4)=0;
end
if pa==1,
    g(1)=0;
    g(2)=1;
    g(3)=1;
    g(4)=0;
end
if pa==0,
    g(1)=0;
    g(2)=0;
    g(3)=1;
    g(4)=1;
end
if pb==2,
    g(5)=1;
    g(6)=1;
    g(7)=0;
    g(8)=0;
```

```
end
if pb==1,
      g(5)=0;
      g(6)=1;
      g(7)=1;
      g(8)=0;
end
if pb==0,
      g(5)=0;
      g(6)=0;
      g(7)=1;
      g(8)=1;
end
if pc==2,
      g(9)=1;
      g(10)=1;
      g(11)=0;
      g(12)=0;
end
if pc==1,
      g(9)=0;
      g(10)=1;
      g(11)=1;
      g(12)=0;
end
if pc==0,
      g(9)=0;
      g(10)=0;
      g(11)=1;
      g(12)=1;
end
%interlock dead zone
for i=1:12,
if x(i+6) ~= g(i),          %should jump
            if x(19) ==0,                %first time
            sys(19)=1;              %set start flag
            sys(20)=t;              %start time
            end
      if g(i)==0,
            sys(i+6)=0;             %jump down
      end

      if t > sys(20)+deadtime,      %deadtime over
            sys(7:18)=g(1:12);        %all jump
            sys(19)=0;                  %reset start flag
      end
end
end
end                                                  %end of normal condition
%=============================================================================
% mdlOutputs
% Return the output vector for the S-function
%=============================================================================
function sys = mdlOutputs(t,x,u)
sys(1:12) = x(7:18);
```