A SPECIAL HIGH-FREQUENCY SOFT-SWITCHED DC/DC POWER SUPPLY FOR GCT GATE DRIVER

by

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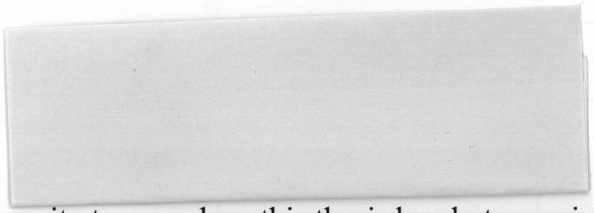

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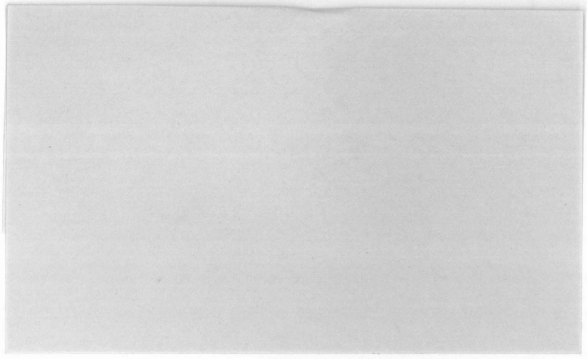

A Special High-Frequency Soft-Switched DC/DC Power Supply for GCT Gate Driver

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ABSTRACT

This thesis is devoted to the development of a novel parallel isolated power supply (PIPS) for the gate driver of integrated Gate Commutated Thyristors (GCT). The proposed PIPS is essentially a special high frequency soft switched DC/DC converter, integrating six parallel isolated power supplies in one module where each power supply generates a regulated dc supply for the GCT gate driver. In commercial GCT power supplies, a high-voltage isolation transformer is indispensable but highly inefficient in terms of cost and size, which can be significantly improved by the optimized transformer. In all, this design strives to achieve a general power supply for powering up the gate drivers of all types of GCT devices in all MV applications with minimal changes in configuration.

In this thesis, the configuration of PIPS is presented and its operating principle is elaborated. The transformer optimization procedure satisfying the voltage isolation requirement for GCT gate drivers is extensively discussed. The performance of PIPS, including the front end DC/DC converter, zero voltage switching phase-shift full bridge (ZVS-PS-FB) converter, and the optimization of the transformer, is verified by simulations and experiments where a 360W laboratory prototype is built for the experimental use.

ACKNOWLEDGEMENTS

Dedicated to the memory of my father, who gave me life and showed me the key to success.

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CHAPTER 1: INTRODUCTION

High power converters with power rating from 0.4MW to 40MW at the medium voltage level of 2.3KV to 13.8KV are widely adopted in industry. Applications of these converters can be found in medium voltage (MV) drives, static reactive compensators (STATCOM), and dynamic voltage restorers (DVR) [1-2]. In high power converters, high power Insulated Gate Bipolar Transistors (IGBTs) and integrated Gate Commutated Thyristors (GCTs) have been broadly used since late 1990s. These new generation switching devices become very popular in the main areas of high-power electronics due to their superior switching characteristics, reduced power losses, and ease of gate control. Currently, the voltage and current rating of IGBT devices can reach 6.6kV/0.6KA or 1.7KV/3.6KA, while the ratings of GCTs can be up to 6KV/6KA, indicating that GCTs are more suitable for higher power applications.

The GCT device is essentially a high power GTO (Gate Turn Off) integrated with a specially designed gate driver [3]. The gate driver has an extremely low gate inductance, which leads to great improvement on the GCT turn-off capability over conventional GTOs. There are two types of GCTs, namely, symmetrical GCT and asymmetrical GCT. The symmetrical GCT is mainly used for current source converters. Fig. 1-1 shows the block diagram of a GCT device. The gate driver, which is normally powered by a 20V dc supply, converts the gate signals generated by the digital controller into required GCT gating currents. Asymmetrical GCT gate drivers are generally employed in voltage source converters where the reverse voltage-blocking capability is not required [4-6]. The power supply input for the asymmetrical GCT will be different, since the voltage operation of gate drivers for these two types of GCTs differs. In order to simplify the control interface and reduce the system cost, a rectifier and voltage regulator are further integrated in the gate driver board. It allows the direct connection to an isolation transformer with an ac square-wave output voltage ranging from $28V$ to $40V$ ($15kHz$ to $100kHz$) [6]. It is also possible to supply the gate unit with dc voltage.

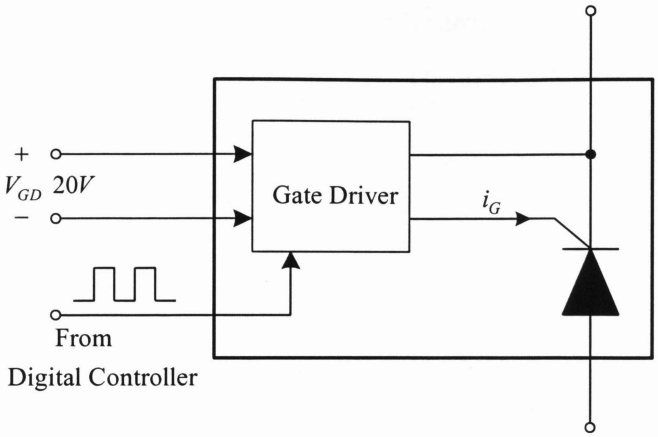


Fig. 1-1: GCT block diagram.

Fig. 1-2 illustrates a CSI drive using a single-bridge PWM current source rectifier (CSR) as a front end, where 36 GCT devices are employed. The rectifier and inverter have an identical topology using symmetrical GCTs. With the GCT voltage rating of 6000V and two GCTs connected in series in each of the converter branches, the drive is capable of operating at the utility voltage of 4160V (line-to-line). For higher operating voltages, the number of series connected devices can be increased while the converter topology remains unchanged. For example, three GCTs can be in series for the 6600V drives [1]. Typically, the number of GCT devices employed in MV applications is 6, 12, 24, or 36.

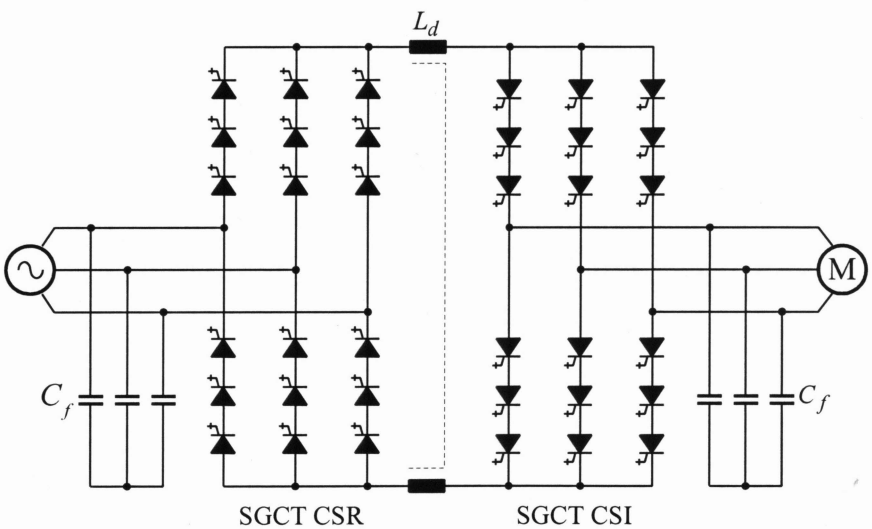


Fig. 1-2: A typical 4160-V CSI drive with a PWM rectifier and inverter.

Fig. 1-3 displays the topology of GCT-based Current Source Rectifiers (CSR) commonly used in medium voltage drives as a front-end converter [7]. The line inductance L_s and filter capacitor C_f form a low pass filter to attenuate harmonics generated by the CSR. The dc choke L_d is used to smooth the dc current.

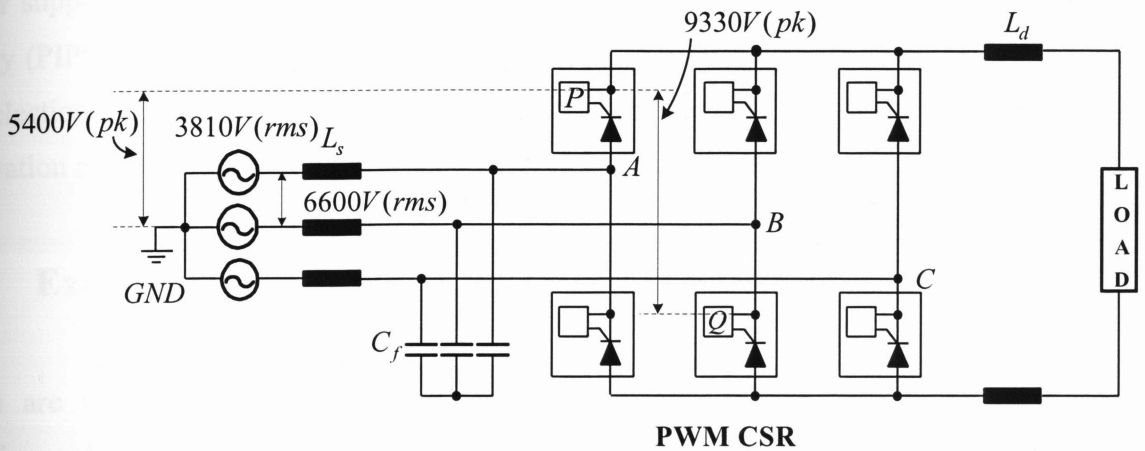


Fig. 1-3: PWM current source rectifier (CSR).

Since the gate driver is connected to the cathode and the gate of the GCT device, the gate driver and its power supply are at the same potential of the GCT. For example, in a $6600V$ system, the voltage of gate driver P with respect to ground GND is $5400V(peak)$, and the voltage between gate driver P and gate driver Q is $9330V(peak)$. As a result, high voltage isolation for the power supply is required.

To fulfill the isolation requirement, separate power supplies insulated by isolation transformers are adopted for GCT gate drivers. These isolation transformers are quite expensive and bulky, which causes an increase in the manufacturing cost and physical volume of the power converters.

In order to decrease the system cost and power supply size for the GCT gate driver, self-powered supply (SPS) techniques are proposed in the literature. SPS seems to be the ideal solution where the energy from the power converter or snubber circuits of the switching devices is used to power the GCT gate drivers such that the isolation transformers can be eliminated for system cost reduction. However, SPS bears a major drawback which is the limited application in

medium voltage MV-CSR converters. It motivates us to seek for a general solution for the power supply in GCT gate driver applications.

In what follows, a review on the existing power supply technologies is provided, including the pros and cons of each technology in GCT gate driver applications. The absence of a general power supply for GCT gate drives indicates the need for the proposed parallel isolated power supply (PIPS), which overcomes the drawbacks of the existing power supplies. Discussions on the selection of DC/DC converter for the proposed PIPS are the focus of Section 1.2. Finally, the motivation and objectives, and the organization of this thesis are presented.

1.1 Existing Power Supplies for GCT Gate Drivers

There are two types of power supplies for GCT gate drivers, the commercial isolation transformer based power supplies and the self-powered supplies. In this section, these two types of power supplies are introduced, discussed, and compared.

1.1.1 Commercial Power Supply for GCT Gate Drivers

A commercial power supply for a switching device gate driver is normally composed of an isolation transformer, a rectifier, and a dc-dc converter. Fig. 1-4 depicts the typical block diagram of this type of power. Depending on GCT's current capability, the power rating of the GCT gate driver is normally in the range of $10W$ to $60W$. The isolation transformer converts a utility ac to a lower ac voltage, which is then converted into a dc voltage by the rectifier. This dc voltage may vary with the utility voltage and/or the load conditions, and thus it is further stabilized to power the gate driver by a dc-dc converter.

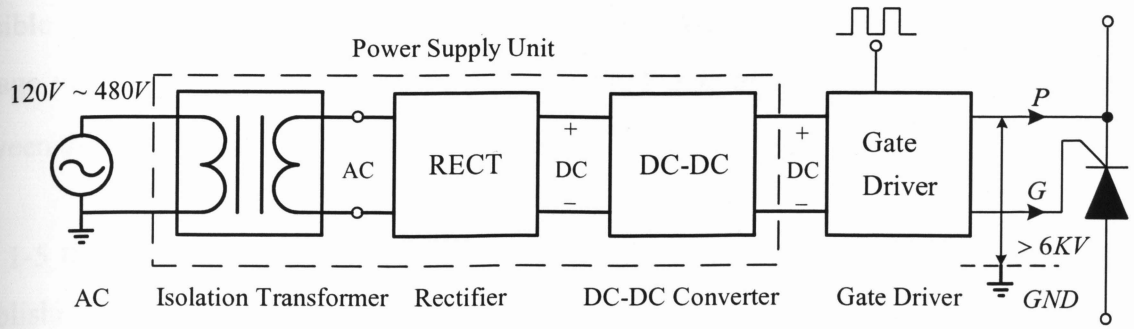


Fig. 1-4: Block diagram of the commercial gate driver power supply for GCT devices.

Another important function of the isolation transformer is to provide isolation between utility power supply and the gate driver. Since the voltage between the switching device and the ground of the utility power supply can be a few thousands volts in MV applications, the isolation transformer must be specially designed and manufactured. Hence the cost of such a transformer is high and its physical size is large.

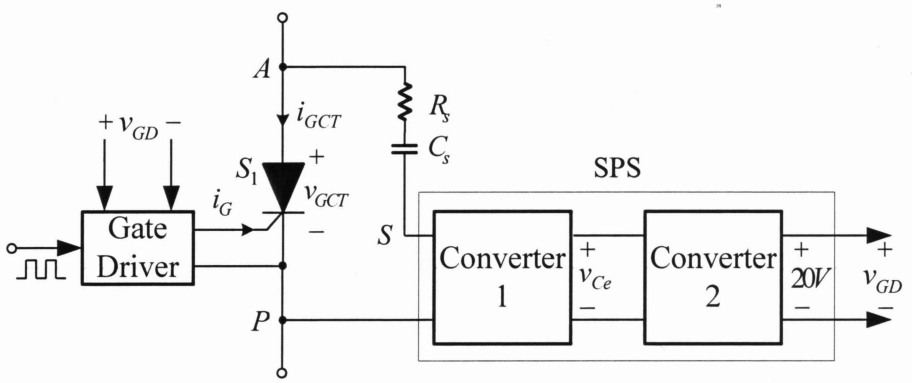
1.1.2 Self-Powered Supply (SPS) for GCT Gate Drivers

To reduce the cost and volume of gate driver supplies, several self-powered supply (SPS) techniques were proposed in the literature for SCR, GTO and GCT [8-13]. The purpose of these techniques is to utilize the energy from power circuits or snubber circuits to power the gate drivers, instead of using energy transferred from the utility power supply via isolation transformers. As a result, the isolation transformers are avoided and the associated cost and physical occupancy are saved. The discussions in this section are restricted to the SPS technique for GCT devices since the scope of this thesis is the design of power supply for GCT gate drivers.

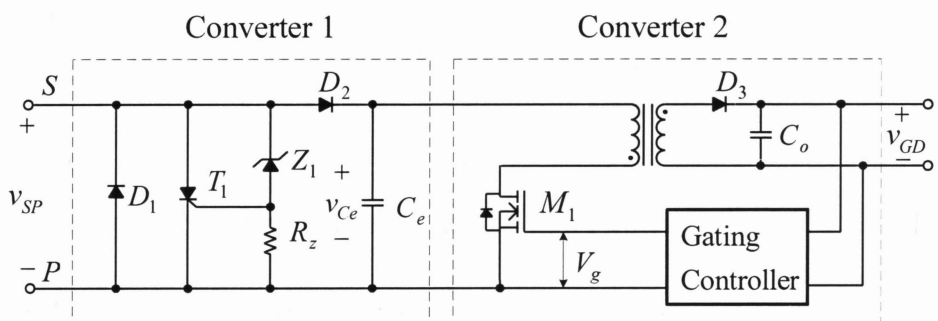
The block diagram of the proposed self-powered supply for GCT gate driver in medium voltage current source rectifier (MV-CSR) is shown in Fig. 1-5 (a). The supply consists of two converters: Converter 1 and Converter 2. The main functions of Converter 1 are to transfer the energy from the snubber capacitor C_s to the energy-storage capacitor C_e and to minimize

possible interference to the snubber circuit operation. Converter 2 converts the unregulated dc voltage v_{Ce} to a regulated dc voltage v_{GD} for the GCT gate driver, and also provides insulation between the snubber circuit and the gate driver.

Fig. 1-5 (b) illustrates a circuit diagram of the proposed SPS [13]. When a positive voltage is established between the terminals S and P, a current flows through diode D_2 to charge the energy storage capacitor C_e. Once v_{Ce} reaches its maximum value $V_{\max}$, set by the zener diode Z_1, the diode Z_1 will breakdown and conduct, causing thyristor T_1 to conduct. The current from S to P is thus diverted from C_e to T_1. In this case, diode D_2 is reverse-biased, preventing C_e from discharging through T_1. When the voltage between S and P becomes negative, the diode D_1 will conduct, providing a current path for the snubber circuit. Moreover, in order to minimize the impact of the SPS on the snubber operation, C_e should be much greater than C_s.



(a) Block diagram.



(b) Circuit diagram of SPS.

Fig. 1-5: Circuit diagram of the self-powered supply for GCT gate drivers.

Converter 2 is essentially a flyback converter, which converts the unregulated dc voltage on C_e to a regulated dc voltage v_{GD} for the gate driver. This converter consists of a power MOSFET, a high-frequency transformer and a controller. The transformer produces a step-down voltage and provides the required isolation (hundreds of volts) between the RC snubber circuit and the GCT gate driver. Based on the output feedback, the duty cycle of the MOSFET is controlled, so that the dc output voltage of the converter v_{GD} is regulated at $20V$.

This scheme features a regulated dc supply for the GCT gate drivers in MV-CSR applications. However, there are several drawbacks associated with the SPS design. One drawback is that the SPS for GCT gate driver can only be used for CSR in MV applications. Another limitation is that the SPS has small impact on the operation of the snubber since SPS is in series with snubber. In addition, the mounting of SPS for GCT gate drivers in CSR is difficult. It is therefore concluded that SPS is not an ideal candidate for GCT gate driver power supply.

The above drawbacks of the existing power supplies for GCT gate drivers motivate us to develop a general power supply to power all types of GCT devices (symmetrical and asymmetrical) in all MV applications such as CSI, CSR, VSI, etc. The proposed power supply supports six GCT devices in one module as depicted in Fig. 1-3. To accomplish this design, an appropriate isolated DC/DC converter should be chosen to reduce the cost and size for system preservation, and meet the voltage isolation requirement for GCT devices. In Section 1.2, the key aspects of DC/DC converter are investigated and the most desirable isolated DC/DC converter for the proposed power supply is discussed.

1.2 DC/DC Converter for The Proposed Power Supply

DC/DC Converter design tends to be a process of making tradeoffs between converter size, cost, and performance. This procedure motivates and guides the designer towards choosing a suitable type of converter. Since six power supplies are placed in one unit in the proposed design, an effective and efficient DC/DC converter design is indispensable. A simplified block diagram of the proposed power supply is drawn in Fig. 1-6. It is important to keep the front end DC/DC

converter operating at high switching frequency and high efficiency, so that the transformer with high voltage isolation requirement for GCT devices can be optimized and all six power supplies can be place in one module.

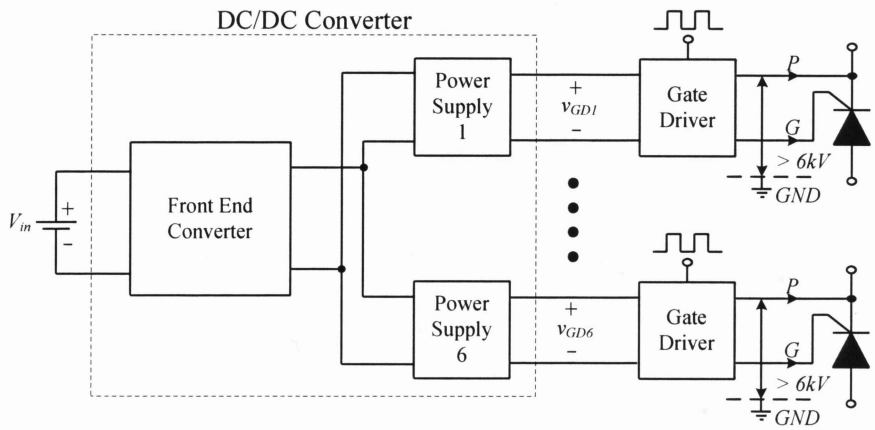


Fig. 1-6: Simplified block diagram of the proposed power supply for 6 GCT gate drivers.

At higher switching frequency, the size of the required magnetic components may be decreased, leading to the reduction in raw material costs along with the converter bearing less physical volume. These factors render the proposed power supply a highly economical solution particularly from the viewpoint of the whole-system conservation.

1.2.1 Circuit Topologies

It is of paramount importance to minimize the cost of components, by choosing a reasonable isolated DC/DC converter topology for proposed power supply. There are many high frequency topologies for isolated DC/DC converters such as push pull, forward, flyback, half-bridge, full-bridge [14], [15]. After comparing all these topologies, full-bridge is selected as the most appropriate topology for the parallel isolated power supply. For one thing, full-bridge is capable of handling higher power, and the supply isolation between the input and output of the GCT gate drivers is superior with respect to other topologies for this application. The main transformers of full-bridge can operate under full symmetry of volt-seconds, which eliminates the saturation of

the transformer and greatly reduces the size of the transformers [15]. For another, full-bridge topology can easily achieve zero voltage switching (ZVS) controlled by a phase-shift controller, resulting in an increase in the efficiency and reliability. Therefore, the full-bridge topology is chosen as the optimal isolated DC/DC converter for the proposed power supply. The transformer optimization for high voltage isolation for GCT gate drivers is rendered easier by the converter operating in full-bridge topology.

1.2.2 DC/DC Efficiency Improvement

Improving the efficiency, reliability and flexibility of the DC/DC power converter while maintaining or decreasing cost, may provide a solution to the general conservation goal. There exist many design principles that may be adapted for use in achieving this goal. Operating a converter using a constant switching frequency allows the magnetic components and the filter design to be optimized, resulting in increased the overall efficiency and decreased size of these components [14-16]. Efficiency in a power system may also be improved by ensuring that the switching duty cycle operates the closest possible to 50%, which reduces the stress on components within the system. In [17], a duty cycle significantly less then 50% was linked to decreased efficiency and poor transient response performance in comparison to operating at 50% duty cycle. A small duty cycle also limits switching frequency in a power conditioning system since malfunction can happen due to the extremely short conduction times [18]. One concept that can be beneficial for enhancing efficiency in power system design is operating at a higher switching frequency. This diminishes the cost and size of the power converter while improving the reliability and efficiency of the system, although these benefits can be voided if effects of increased frequency-dependent losses, switching losses, output capacitance losses and gate losses are not counteracted.

1.2.3 Higher Switching Frequency

It is well documented that converters designed with higher switching frequencies can reduce the size and weight of transformers and filter components together with improving transient response

[15]. At a higher switching frequency, smaller size of the magnetic components may give rise to lower raw material costs and less volumed converter. These factors can potentially improve the economics of power electronics applications in terms of system conservation.

Although higher switching frequency leads to benefits such as cost and reliability, these benefits can quickly be voided by the decrease in efficiency due to increased switching. Obviously, high switching frequencies result in increased switching losses responsible for nullifying the aforementioned advantages of the higher switching frequency. To realize the benefits of a high switching frequency, switching losses must be eliminated and a common and effective approach for achieving this involves the implementation of Zero Voltage Switching (ZVS) [16], [17], [18]. ZVS is a technique that removes switching losses by ensuring that the switch voltage is roughly zero during the switch transition. The employment of ZVS technique produces higher efficiency through the removal of switching losses, allowing all the benefits of higher switching frequency to be realized. In the next section, a brief survey is presented to explain the choice of ZVS as the soft switching technique for the proposed power supply.

1.2.4 Soft Switching Techniques

The main trend in achieving higher power density for switched mode power supplies is the increase in switching frequency. Hard-switched converters cannot operate above an upper frequency due to switching losses. This upper frequency is about 70-80*kHz* for MOSFETs and about 20-30*kHz* for IGBTs if power ratings of several kilowatts are considered [19]. The switching losses in DC/DC converters can be reduced by using snubbers, quasi-resonant or fully resonant circuits, or soft-switching circuits [20]. Soft switching is preferred because of the following advantages: 1) simpler control circuits, 2) simpler power circuit, 3) simpler analysis, 4) better exploitation of the power transistors and rectifier diodes, 5) high efficiency, and 6) low EMI. At power levels high enough to justify the use of four controlled switches, probably the best choice is the full bridge soft-switching forward converter [21-25], which is controlled by phase-shifted (four state) PWM. The soft switching PWM converter is defined as the combination of converter topologies and switching strategies that result in zero-voltage and/or zero-current switching in. This type of soft switching converter has been referred to by different

names in the literature, such as pseudo-resonant, quasi-resonant, resonant transition, clamped voltage topologies and so forth. In these converters, the resonant transition is employed merely for a short switching interval. The output voltage is usually controlled by PWM with constant switching frequency.

Soft switching PWM converters can be classified as follows: 1) ZCS (Zero Current Switching) PWM converters, 2) ZVS ZCS PWM converters, and 3) ZVS (Zero Voltage Switching) PWM converters. The ZCS PWM converters can be derived from the ZVS PWM converters by applying the duality principle. These converters are attractive for applications with high output voltage, *e.g.*, power factor correction circuits, where the rectifiers suffer from severe reverse recovery problems when conventional PWM, ZVS-QRC, or ZVS-PWM converter techniques are used. The efficiency of the converter drops significantly at low line and heavy load since the switches begin to lose zero current switching. The zero-voltage zero-current switching (ZVZCS) PWM converters are derived from the full-bridge phase shifted zero-voltage (FB-PS-ZVS) PWM converters. The PS-ZVS PWM converter is often used in many applications in that this topology permits all switching devices to operate under zero-voltage switching by using circuit parasitic such a transformer leakage inductance and devices junction capacitance. However, due to phase-shifted PWM control, the converter has a disadvantage that circulating current flows through a transformer and switching devices during freewheeling intervals. The ZVZCS DC/DC PWM converter can operate very well at nominal load, but is not capable of operating over wide load range (from no-load conditions to short circuit) with zero-voltage or zero-current switching for all power switches. Auxiliary circuits are needed in order to achieve soft switching at no-load conditions and at short circuit. The ZVS PWM converter is controlled by the phase-shifted PWM technique. To solve the problems of conventional pulse width modulated (PWM) dc-dc converters, several high-frequency (HF) isolated soft-switching (including resonant) converters have been developed in the past [22, 24], [26-29]. These converters have reduced size, weight, and cost. Variable-frequency control used in resonant converters suffers from several disadvantages.

To overcome these problems, fixed-frequency resonant and soft-switching PWM converters emerged as an active area of research [22, 24], [26-29]. Among these converters, the most

popular configuration is the ZVS phase-shifted bridge converter. The ZVS PWM converter exhibits low primary-side switching loss and generated EMI. Furthermore, the ZVS technique can be used to increase the converter efficiency. For instance, at high-power levels, the full-bridge (FB) ZVS phase shift DC/DC converter has been an attractive choice, since it provides high-power density with high efficiency and low electromagnetic interference [20, 21, 23, 24]. Besides the constant frequency operation with linear output characteristics, it integrates the stray elements (junction capacitances and leakage inductance). In addition, this converter incorporates the advantages of low-conduction losses present in hard switching technology, as well as small-switching losses provided by soft-switching technology [20, 21]. As mentioned above, compared to other topologies such as ZCS-PWM and ZVS ZCS-PWM, ZVS-PWM is the most appealing and desirable soft switching technique. With ZVS, the converter can achieve a switching frequency of up to several kilo-Hertz, which is an attractive feature and ideal property for the design and implementation of the proposed power supply.

1.3 Motivation and Objectives

Based on the previous discussions, the motivation and objectives of this thesis are addressed in this section. Recall from Fig. 1-3 that the minimum number of GCT devices in medium voltage current source inverter (CSI) or medium voltage current source rectifier (CSR) is six. Each GCT device normally requires a specially designed power supply for its gate driver. Moreover, the commercial GCT power supplies are quite expensive and bulky since they have to provide an electrical isolation of a few thousand volts through a high-voltage isolation transformer. To reduce the cost and size of the power supplies for GCT gate drivers, self-powered supply (SPS) without isolation transformers are proposed in the literature. However, the SPS design for GCT gate drivers is restricted to Current Source Rectifier (CSR) in MV applications and cannot be adopted for GCTs in other converter topologies. Furthermore, the SPS-produced small impact on the operation of the snubber circuit of medium voltage converter is undesirable.

1.3.1 Contributions

This thesis is dedicated to the development of a general power supply with low cost, compact size, and high efficiency, for all MV applications where the GCT gate driver is indispensable. Based on the extensive literature survey on the existing power supply for all high power semiconductor switches (SCR, GTO, IGBT, ETO, and GCT) [8-13], the proposed PIPS is demonstrated to be a unique design where six parallel isolated power supplies with optimized transformers are implemented in one unit to supply six GCT devices with high voltage isolation level requirement. To be elaborative, the proposed power supply is designed to feature a high frequency soft switched DC/DC converter, which can deliver the maximum power at high efficiency giving rise to high power density and compact size. As a result, the cost of the major components such as high voltage isolation transformers, filters, and heat sink can be avoided. In addition, operating at high switching frequency and high efficiency results in less complex optimization for the transformer and lower cost attributed to the employment of ferrite transformers. Simulations and experiments will be leveraged to indicate the practicality and effectiveness of the proposed PIPS for the GCT gate driver. Detailed potential contributions to addressing the challenges in the PIPS design are discussed in the following section.

1.3.2 Objectives

This thesis aims to present a simple, general, and cost-effective power supply for six GCT devices (symmetrical and asymmetrical) employed in MV applications. The potential contributions or main objectives of this thesis thus lie in the design and implementation of PIPS, which are achieved by providing solutions to the following challenges and difficulties:

1. **Need for general power supply in GCT gate driver applications**—It may not be difficult to come up with a design specifically coping with the issues present in a particular application scenario, where the issues will have limited impact, as in the case of self-powered supply techniques applied in (certain type of) GCT gate drivers. On the other hand, it would be much more challenging, if not impossible, to invent a generally-applicable technique which must deal with all possible issues in a wider range of applications and the potentially broader impact of these issues. As the main goal and mission of this thesis, the

proposed parallel isolated power supply strives to address the challenge of designing such a general technique for all MV applications where the GCT gate driver is indispensable.

2. **High power required for GCT power supply**—Depending on the GCT current rating, the power required for GCT power gating is usually around $60W$. There are 6 GCT devices in the CSI or CSR for MV applications and the power supply module with 6 parallel isolated power supplies requires $360W$ output power.

3. **Transformer optimization for high voltage isolation level between input and output of the power supply**—The most important issue in designing the proposed power supply is the transformer design optimization. Since the power supply will be adopted in applications where high voltage isolation level is required, the transformer need be capable of producing an isolation level of up to several kilovolts, while bearing low cost and small size.

4. **Regulated output voltage**—Most of the GCT devices require a stable output voltage of 20V with a maximum error of $\pm 0.5V$. Therefore, the output voltage of each isolated power supply in the proposed PIPS should be controlled with desirable voltage regulation.

5. **Reduced cost and size**—The cost and size of a commercial product are the key elements in attracting wide industrial adoptions, which directly determine the success and usefulness of such product. The proposed power supply is by no means an exception. In the proposed PIPS, it is important to minimize the cost of the components such as transformers, output filters, and heat sinks, by choosing a high frequency and high efficiency isolated DC/DC converter topology for high voltage isolation transformers, the difficulty of which is exaggerated when six parallel isolated power supplies are placed in one unit.

6. **High efficiency and high frequency operation**—As mentioned in Section 1.2.2, high switching frequency introduces many desirable features to the converter but also results in increased switching losses as the byproduct. To fully realize the benefits of high switching frequency, one of which being the increased efficiency of the converter, switching losses must be eliminated or suppressed to an acceptable level. A common and effective approach

for achieving this involves the implementation of Zero Voltage Switching (ZVS), the employment of which can potentially produce the required efficiency for the converter through the removal of the byproduct.

7. **Simulation and experiments**—To facilitate the analysis and design of the proposed PIPS, a suitable and comprehensive simulation model for the proposed PIPS should be developed. In addition to the simulations, experiments must be extensively conducted to verify the simulation results and the performance of the proposed power supply for GCT gate drivers, through building and testing the prototype of the power supply.

1.4 Thesis Organization

This thesis consists of five chapters. The background information pertinent to comprehending the proposed parallel isolated power supply is presented in this chapter, including the introduction of the GCT device, the review on the existing power supply techniques for GCT gate drivers, and the brief survey on the topologies and techniques for the DC/DC converter. According to the review and survey, clear choices on the power supply technique, the converter topology, and the switching technique are stated. The main objectives of the thesis are defined, with associated challenges and difficulties identified and discussed.

In Chapter 2, the proposed novel parallel isolated power supply (PIPS) for GCT gate drivers is introduced. The operating principle of the PIPS circuit is elaborated. Theoretical analysis and design guide for PIPS is also provided. Furthermore, the detailed optimization procedure for the design of the high voltage isolation transformer is presented.

Chapter 3 focuses on the modeling and analysis of the proposed power supply. The performance of PIPS is then investigated through simulations, which verify the key component selection and the maximum achievable efficiency with the optimized transformers, and assist in the calculation of total power losses.

Chapter 4 provides experimental evaluation of the proposed PIPS. A laboratory prototype is designed and built to test the performance of the proposed power supply. Extensive experiments on the optimized transformers with different core sizes are then conducted. Detailed discussions on the experimental results, comprising observations and their indications, are also included in this chapter.

Finally, Chapter 5 concludes this thesis. A summary of the results are presented, along with a review of the contributions and possible suggestions for future work.

CHAPTER 2: PRINCIPLE OF PARALLEL ISOLATED POWER SUPPLY (PIPS) FOR GCT GATE DRIVER

This chapter starts with an introduction to the novel isolated power supply for GCT gate drivers, followed by detailed discussions on its operating principle. The design requirements for the proposed supply are also elaborated. In addition, the optimization procedure for high voltage isolation level transformers required for GCT gate drivers is presented.

2.1 Introduction

Due to the limitations of the aforementioned approaches introduced in Chapter 1 and the special gating requirements for GCT devices, none of the existing solutions in the literature can be readily employed for GCT gate unit supply under all different MV converter topologies (not only CSR) [8-13]. In order to reduce the cost of main components (such as high voltage isolation transformers), compact size, and simple circuit implementation, a novel parallel isolated power supply (PIPS) for GCT gate drivers, is therefore proposed and described in this chapter. The design features a general power supply for GCT devices used in different converter topologies where high voltage insulation level is required, e.g., Medium Voltage Neutral Point Clamped or PWM CSI converters. The proposed power supply is a high frequency soft switched DC/DC converter with 6 parallel high voltage isolation level transformers that operate at $165kHz$ switching frequency. The proposed PIPS obtains power from a ($50V$-$80V$) dc input voltage. Each channel of PIPS regulates a 20Vdc supply to drive the GCT gating circuits at very high voltage isolation level and very high efficiency. Consequently, the expensive and bulky isolation transformers used in commercial power supplies for GCT gate drivers can be eliminated.

2.2 Technical Requirements and Configuration of the Proposed PIPS

Parallel Isolated Power Supply (PIPS) was initiated as an effort to reduce the cost on the existing power supply for GCT gate drivers. It is of paramount importance to minimize the cost of components for the proposed power supply, by choosing a reasonable isolated DC/DC converter topology for high voltage isolation transformer. At higher switching frequency, the size of the magnetic components required may be decreased leading to a reduction in raw material costs, along with the converter bearing less physical volume. These factors render the proposed power supply, a highly economical solution particularly from the viewpoint of the whole-system conservation.

2.2.1 Technical Requirements

Each GCT device normally requires a specially designed power supply for its gate driver. Accordingly, the proposed PIPS should meet following requirements.

1. The power required for the GCT gate driver

The GCT power gating is usually around $60W$. A major portion of the required energy is transferred to the gate driver during the GCT turn-off. Another portion of the energy is dissipated for turning on the GCT device, including the generation of turn-on pulse and back-porch current. The third portion, around $5W$, is the gate driver component dissipation. Obviously, the supply should be designed to fulfill a total power of $360W$ for 6 GCT gate drivers.

2. Regulated output voltage

Since the load conditions in different switching periods of the gate driver are distinct, and the voltage requirement ($20 \pm 0.5V$) of the power supply for GCT gate drivers is critical, the output voltage of the designed PIPS must be regulated in order to achieve reliable GCT switching.

3. Transformer optimization with high voltage isolation level required for GCT gate driver

The optimization for the high voltage isolation transformer is imperative because the transformer must provide an isolation level of up to several kilovolts for GCT gate drivers, at low cost and small size. Such optimization is achievable by using ferrite core, which is chosen due to its low-cost and low-loss characteristics when used for transformers in the frequency range of $20kHz$ to $1MHz$.

4. High efficiency and high frequency operation

The proposed power supply must operate at high frequency and high efficiency to optimize the transformer. As mentioned in Section 1.2.2, high switching frequency introduces many desirable features to the converter but also results in increased switching losses as the byproduct. To fully realize the benefits of high switching frequency, one of which being the increased efficiency of the converter, switching losses must be eliminated or suppressed to an acceptable level. A common and effective approach for achieving this involves the implementation of Zero Voltage Switching (ZVS), the employment of which can potentially produce the required efficiency for the converter through the removal of the byproduct.

The novel parallel isolated power supply is designed based on the above requirements. The circuit configuration and analysis are given in following sections.

2.2.2 PIPS Configuration

1. PIPS block diagram

The block diagram of the proposed power supply is shown in Fig. 2-1. The supply consists of two converters. Converter 1 consists of main block ZVS-PS-FB (high frequency zero voltage switching phase-shift full-bridge) and six parallel isolated channels (Ch1 to Ch6).

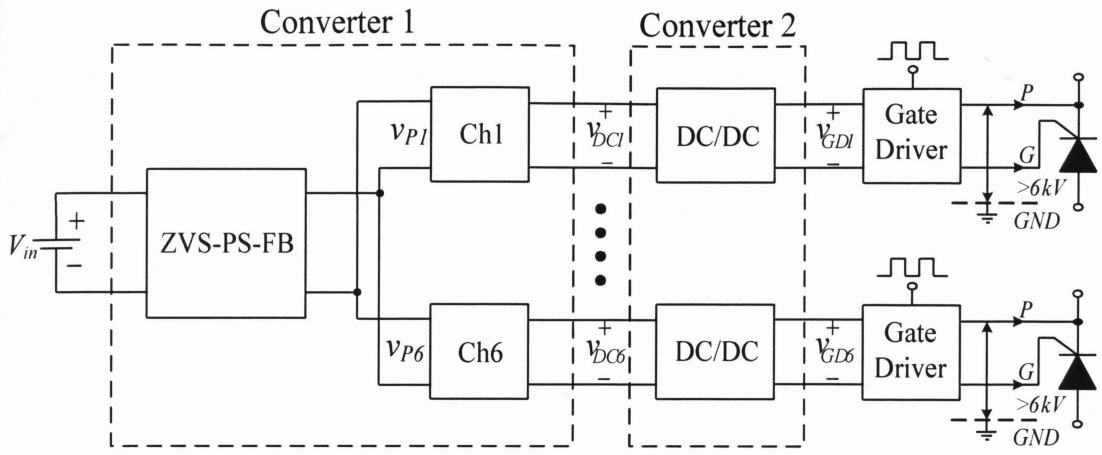


Fig. 2-1: Block diagram of the parallel isolated power supply for GCT gate drivers.

The main function of Converter 1 is to supply rated power for all GCT gate drivers at very high voltage isolation level (a few thousands volts) through a high voltage isolation transformer. In addition, Converter 1 is used to maintain the output dc voltage (v_{DC1} to v_{DC6}) of each channel under wide input dc voltage range V_{in} not subject to load variation. Since there is no output voltage feedback with respect to the load changes for each channel in Converter 1, Converter 2 is added for output voltage regulation. Converter 2 consists of 6 DC/DC converters. As a result, the output dc voltage of each channel in Converter 1 is regulated to dc voltage (v_{GD1} to v_{GD6}) for the GCT gate driver by the DC/DC functionality of Converter 2.

2. PIPS circuit diagram

The circuit diagram of the proposed PIPS is drawn in Fig. 2-2. One of the main challenges in the design of PIPS lies in Converter 1, which is essentially a high-frequency zero voltage switching phase-shift full-bridge DC/DC converter.

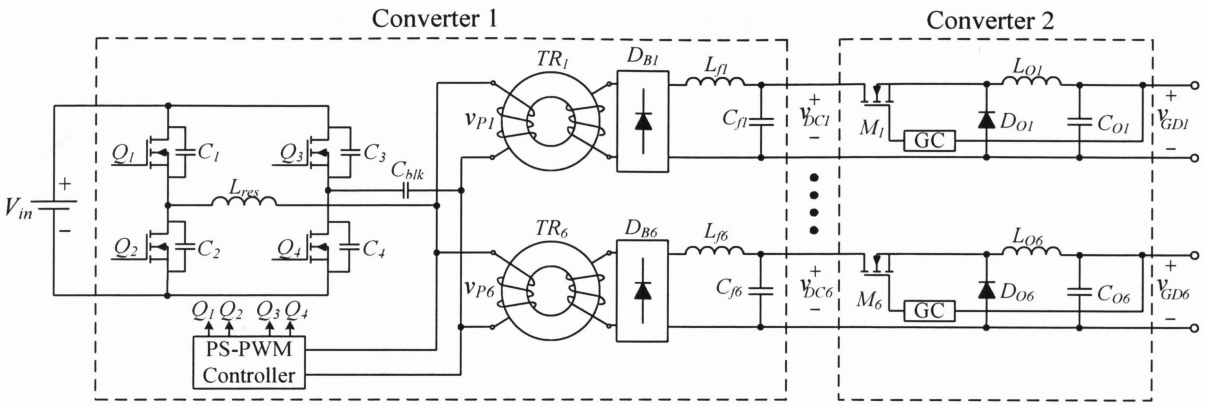


Fig. 2-2: Circuit diagram of the parallel isolated power supply for GCT gate drivers.

Phase-shift full-bridge generates high frequency quasi-square wave voltage for all its 6 parallel ferrite transformer (TR_1 to TR_6) connections, since ferrite transformer operating at high frequency. The circuit of Converter 1 can be further described in detail as follows:

- The gating for the 4 power MOSFETs (Q_1 to Q_4) of the ZVS-PS-FB converter is generated by phase-shift PWM (PS-PWM) controller which operates under voltage mode control feedback.
- The resonant inductance L_{res} (in most case the leakage inductance of transformer) requires operation in Zero Voltage Switching (ZVS) in conjunction with output parasitic capacitances of MOSFET switches (C_1 to C_4).
- A DC blocking capacitor C_{blk} is used for blocking any DC components of the primary current.
- Six parallel isolated channels (Ch1 to Ch6) each has high frequency ferrite toroidal transformer T_{R1}, diode bridge DB_1, filter L_{f1} and C_{f1}. The output voltage of each channel (v_{DC1} to v_{DC6}) is regulated with respect to input dc voltage change V_{in}.

Converter 2 consists of 6 DC/DC step-down buck converters, each of which steps down the output voltage of one channel of Converter 1 (v_{DC1} to v_{DC6}) to a regulated dc voltage (v_{GD1} to v_{GD6}) for the GCT gate driver. Each DC/DC in converters 2 is integrated with FET and gating controller and has output filters (L_{O1}, C_{O1} to L_{O6}, C_{O6}). Based on the output feedback for each DC/DC in Converter 2, the duty cycle of the MOSFET is controlled, such that the dc output voltage of each DC/DC converter (v_{GD1} to v_{GD6}) is regulated at $20V$.

2.2.3 Converter 1 for The Supply of Power with High Voltage Isolation

Converter 1 is a high frequency soft switched DC/DC converter which is utilized to supply rated power with an electrical isolation of a few thousand volts for six GCT gate drivers. As mentioned in Chapter 1, there are many advantages of employing ZVS-PS-FB as the isolated converter topology for proposed power supply. The ZVS-PS-FB converter achieves zero switching loss under heavy load conditions at higher switching frequency with a low component count, leading to the high efficiency of the converter.

In addition, operating Converter 1 at high switching frequency and high efficiency facilitates the optimization of the transformer for high voltage isolation, and hence enables the adoption of low-cost and small-sized ferrite transformers and the placement of six isolated power supplies in one module.

Furthermore, ZVS-PS-FB is capable of handling the power rating of more than $1kW$. In other words, ZVS-PS-FB can easily supply the required power if it is later on needed to add another group of 6 parallel high voltage isolation level transformers to the proposed PIPS, in one unit, i.e., supplying power for 12 GCT gate drivers. This is the key advantage and functionality of ZVS-PS-FB in reducing the cost of the power supply with minimum number of components.

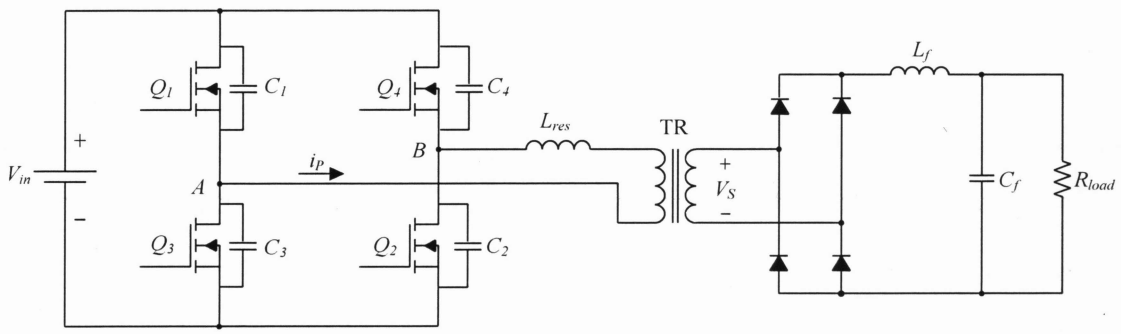
Besides the aforementioned merits, this section also outlines the operation principle, converter analysis and transformer design for zero voltage switching phase-shift full-bridge (ZVS-PS-FB) converter, followed by detailed optimization procedure for the high voltage isolation level transformer.

1. Principle of operation

In order to reduce the size and the weight of magnetic components, it is desirable to increase the switching frequency for DC-DC converters. When conventional PWM converters operate at high frequencies, the circuit parasitics have negative effects on the converter performance [30]. Switching losses increase in high power applications and snubbers and/or other means of

protection are required, which introduces significant losses and decreases the efficiency. In the case of the conventional full bridge converter, the diagonally opposite switches (Q_1 and Q_2, or Q_3 and Q_4) are turned on and off simultaneously. In the FB-PWM converter, when all four switches are turned off, the load current freewheels through the rectifier diodes [15]. In this case the energy stored in the leakage inductance of the power transformer causes severe ringing with MOSFET junction capacitances. This creates the need for using snubbers that increase the overall losses bringing down the efficiency. If snubbers are not used, the selection of the devices becomes more difficult as the voltage rating for these switches has to be much higher. As the voltage rating goes up, so do the conduction losses, the overall losses increase and the cost increases as well.

In order to minimize the parasitic ringing, the gate signals of Q_2 and Q_4 are delayed (phase-shifted) with respect to those of Q_1 and Q_3 [17], as shown in Figure 2-3, so that the primary of the transformer is either connected to the input voltage or shorted.



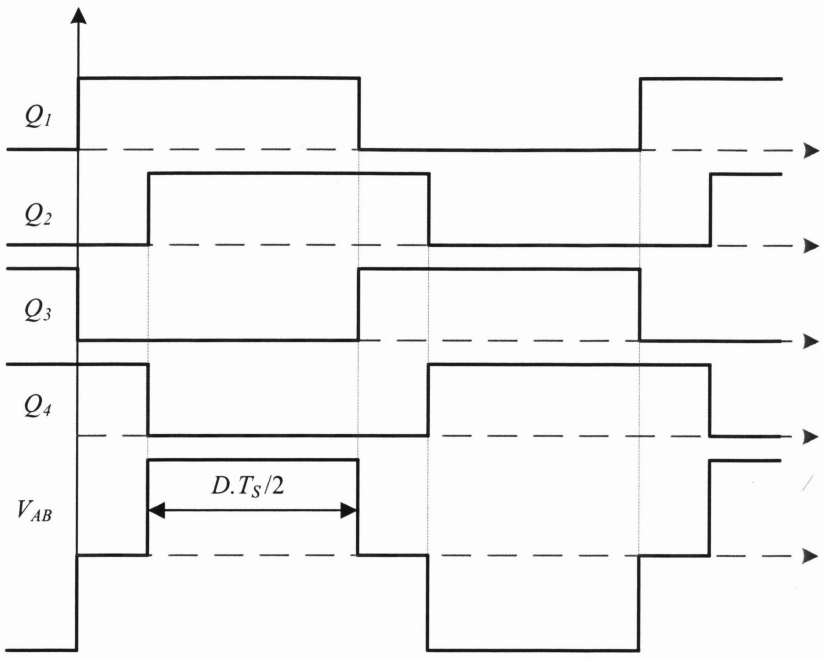


Fig. 2-3: Phase shifted FB-PWM converter.

The leakage inductance current is never interrupted, thus solving the problem of parasitic ringing associated with the conventional full-bridge PWM converter. The energy stored in the leakage inductance can be used to discharge the energy stored in the MOSFET junction capacitances to achieve zero voltage switching (ZVS) conditions for all four switches in the primary side. In this case, the converter requires no additional resonant components.

2. Converter analysis

The zero voltage switching phase-shift full-bridge (ZVS-PS-FB) converter provides ZVS for all four switches in the bridge. However, the mechanism by which ZVS is achieved is different for the two legs of the bridge. For transistors Q_2 and Q_4, the ZVS is provided by the resonance between the leakage inductance, L_{LK}, and the output capacitance of the switch.

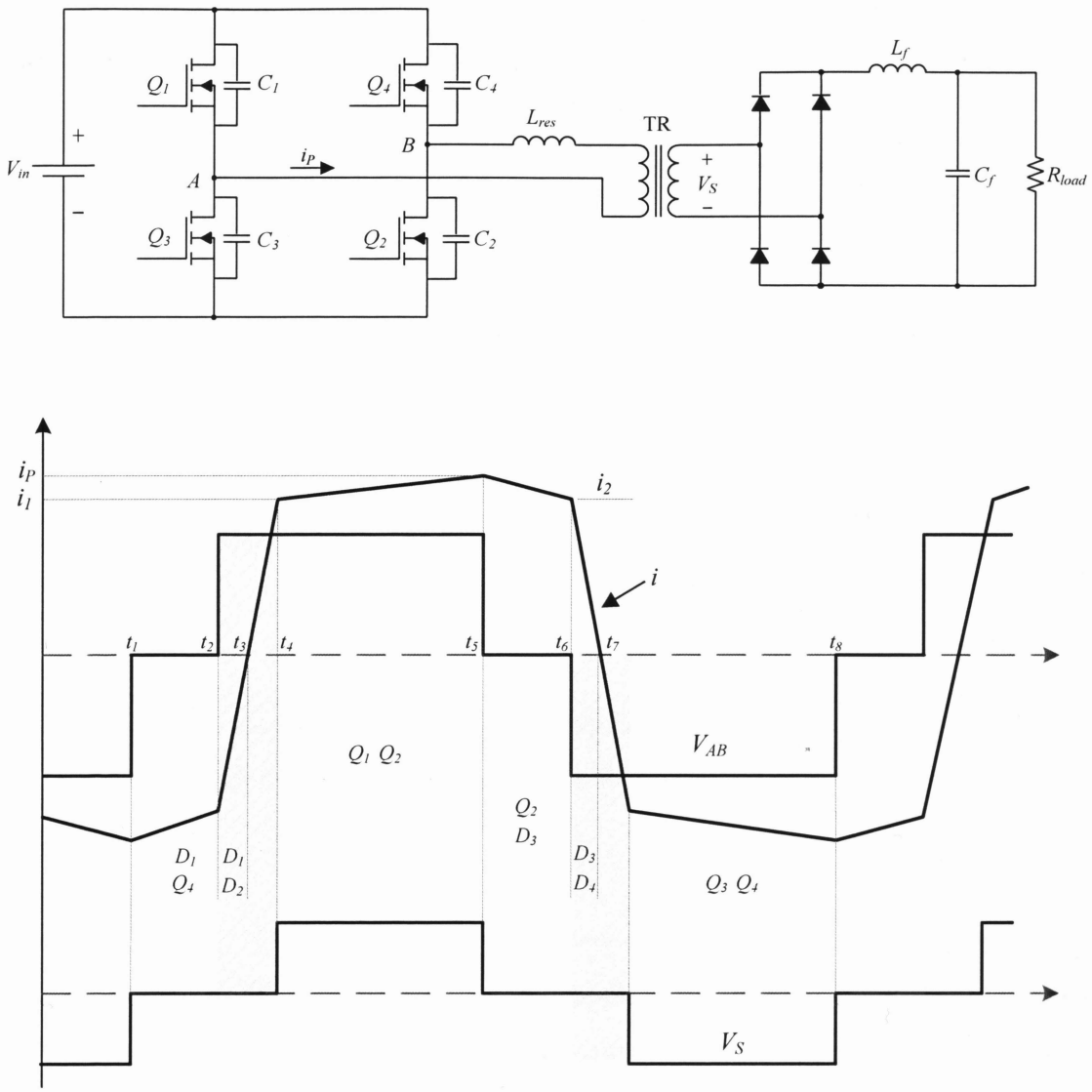


Fig. 2-4: Principle of operation of phase shifted FB-PWM converter.

The needed energy for achieving ZVS is given by

$$E = \frac{1}{2} L_{LK} I_2^{\,2} \geq \frac{4}{3} C_{mos} V_{in}^{\,2} + \frac{1}{2} C_{TR} V_{in}^{\,2} \quad , \qquad (2\text{-}1)$$

where I_2 is the current through the primary when Q_2 turns off as shown in Fig. 2-4, V_{in} is the input voltage, and C_{TR} is the transformer winding capacitance. The factor 4/3 represents twice the

energy stored in the nonlinear drain to the source capacitor, whose capacitance is inversely proportional to the square root of the voltage [17].

The resonance between L_{LK}, C_{mos}, and C_{TR} provides a sinusoidal voltage across the capacitances that reaches the maximum at one fourth of the resonant frequency period. The dead time between Q_2 and Q_4 must be set to $\delta t_{\max}$ to ensure that there is sufficient time to charge and discharge the capacitances. The dead time required to ensure ZVS with the maximum possible load range can be determined by the following equation:

$$\delta t_{\max} = \frac{T}{4} = \frac{\pi}{2}\sqrt{L_{LK} C}, \qquad (2\text{-}2)$$

Where $C = C_{mos} + C_{TR}$.

Whether ZVS can be achieved for Q_2 and Q_4 is dependent on the load level of the converter. For light loads, the current though L_{LK} when Q_2 and Q_4 are turned off may not be enough to turn on the anti-parallel diode.

For switches Q_1 and Q_3, ZVS is provided by a different mechanism. Before Q_1 is turned off the current in the primary is reaching its peak value. The primary current is the filter inductor current reflected to the primary. When Q_1 is turned off, the energy available for charging the output capacitance of Q_1 and discharging the output capacitance of Q_3 is the energy stored in L_{LK} and that in the output filter inductor. This energy in the output filter inductor is available because the filter inductor current does not freewheel through the rectifier until the voltage across the secondary has fallen to zero.

Since the energy in the filter inductor is large compared to the energy stored in the switch capacitances in the primary, the charging of the switches can be approximated by a linear charging with a constant current. Consequently, the dead time dt_1 required between the turn-off of Q_1 and turn-on of Q_3 can be determined by:

$$dt_1 I_P = 4 C_{mos} V_{in} \quad , \qquad (2\text{-}3)$$

where $4C_{mos}V_{in}$ corresponds to twice the charge stored in the nonlinear output capacitance of the MOSFET and I_P is the peak current in the output filter inductor reflected to the primary. The dead time can be calculated for the minimum I_P chosen to achieve ZVS. If load current is further reduced, the ZVS property cannot be maintained.

Critical current for ZVS—The ZVS for Q_1 and Q_3 can be achieved even at light loads because D_1 and D_3 can always be turned on by the energy stored in the output filter inductance. However, ZVS for Q_2 and Q_4 can only be achieved for a load current above the critical values, which is shown as:

$$I_{CRIT} = \sqrt{\frac{2}{L_{LK}}\left(\frac{4}{3}C_{mos}V_{in}^{2}+\frac{1}{2}C_{TR}V_{in}^{2}\right)} \tag{2-4}$$

The available current through L_{LK} at t_2 can be calculated by:

$$I_2 = \frac{N_S}{N_P}\left(I_{load}+\frac{\Delta I}{2}-\frac{V_{out}}{L_{LK}+L_f}(1-D)\frac{T}{2}\right) \tag{2-5}$$

Finally, ZVS is achieved for a load current so that $I_2 > I_{CRIT}$. The load current can be expressed as:

$$I_{load} \geq \frac{N_P}{N_S}I_{CRIT}-\frac{\Delta I}{2}+\frac{V_{out}}{L_{LK}+L_f}(1-D)\frac{T}{2} \tag{2-6}$$

3. Transformer Design

The most important step in designing PIPS is the transformer design for ZVS-PS-FB DC/DC converter (Converter 1) displayed in Fig. 2-3. Since this ZVS-PS-FB DC/DC converter will be adopted in applications where high voltage isolation level is required as shown in Fig. 2-2, the transformer need be capable of providing an isolation level of up to several kilovolts. Unfortunately, off-the-shelf transformers cannot directly suit the proposed power supply,

necessitating the need for designing an efficient transformer for the proper functioning of the converter. In particular, the transformer should operate at high switching frequency in order to reduce size and cost of magnetic components.

Due to the key role of this transformer, especially its cost and size efficiency, in the high voltage isolation level power supply design for GCT gate drivers, the next two sections are dedicated to extensive discussions on the importance of this transformer. Specifically, Section 2.2.4 provides analysis on the high cost and large size of the power supply for GCT gate drivers due to the high voltage isolation transformer, thereby emphasizing the necessity of transformer optimization in terms of cost and size. Section 2.2.5 accordingly presents the detailed optimization procedure yielding a high voltage isolation transformer with reduced cost and size, satisfying one of the major design goals of PIPS.

2.2.4 Cost and Size of High Voltage Isolation Level Transformer

The most important function of the isolation transformer is to provide isolation between the utility power supply and the gate driver. Since the voltage between the GCT device and the ground of the utility power supply can be a few thousands volts in MV applications, the isolation transformer must be specially designed and manufactured. In general, the cost of such transformers is high and the physical size is large. These inferiorities of the existing commercial power supplies motivate us to reduce the cost and size of high voltage isolation transformers for GCT gate driver power supplies.

Six parallel high frequency ferrite transformers are placed in one PCB unit to supply the minimum six GCT devices employed in MV applications. In addition, each of these transformers should meet the voltage isolation requirement for the GCT gate driver. In the next section, the optimization procedure for the high voltage isolation transformer is presented in great detail.

2.2.5 Optimization Procedure for the Transformer Design

The choice of magnetic for power transformers will be influenced by several factors including [30-32]: 1) circuit topology, usually chosen to yield the best combination of minimum power transistor off voltage and peak current stresses. Cost and component count must also be taken into account, 2) operating frequency of the circuit, 3) power requirements, 4) regulation, 5) cost, 6) efficiency, and 7) input/output voltage. These factors will determine the transformer core material, configuration, and size, as well as the winding parameters for the transformer.

The optimization of the high voltage isolation level transformer should be incorporated to reduce the number of primary and secondary winding turns and provide large distance gap between primary and secondary winding which would assist in enhancing the possibility of meeting the corona requirements (i.e., voltage isolation more than $9KV$). Consequently, potting the core for the transformer is unnecessary and hence the associated cost can substantially be reduced.

The optimization procedure for the high voltage isolation level transformer is described in what follows.

1. Transformer core material

Ferrite core is chosen as the material of the high frequency transformer due to its low-cost and low-loss characteristics for transformers in the frequency range of $20kHz$ to $1MHz$. Three low-loss materials, Magnetics R, P, and F, are engineered for optimum frequency and temperature performance in power applications. These materials provide superior saturation, high temperature performance, and low loss. Based on the results given by the manufacturer in Table 2-1, at the frequency of $100kHz$, flux density of $100mT$, and different temperature rises, R material outperforms all the other materials including P and F. As a result, R material was chosen to be the main core material which causes the lowest core loss and temperature rise.

Table 2-1: Core material characteristics.

Temperature Rise	Power loss P_L [mW/cm^3] @ f_{TR}=100[kHz], B_m=100[mT]		
ΔT_{Rise} [°C]	R	P	F
25	140	125	100
60	100	90	180
100	70	125	225
120	90	165	

2. Transformer core shape and size

In order to meet the design criteria for high voltage isolation level transformer, the core must be selected carefully. The toroidal core is opted for to satisfy the transformer design requirements, because toroidal core provides the most desirable voltage isolation level compared to other core shapes [31]. Ferrite toroids also offer high magnetic efficiency as: 1) there is no air gap, and 2) the cross-sectional area is uniform and does not need a bobbin [32]. Besides, the cost of toroid is lower than other shapes such as E, EP, and PQ. Another key design consideration is the core size. It should be selected to provide large distance gap between primary and secondary winding, in which case the corona between primary and secondary windings can be eliminated.

The power handling capability of a core is related to its area product, A_p, by the following equation, which can be written as:

$$A_P = \frac{P_t(10^4)}{K_f K_u B_m J f}, \qquad (2\text{-}7)$$

where P_t is the sum of the output power and the input power is assumed to be $200W$. The winding factor is $K_u = 0.3$ depending on the core shape and $K_f = 4$ for square wave. Typically, a good working level of current density ($J = 400A/cm^2$) is assumed.

The initial estimation for the operating frequency of the transformer (f_{TR}) is 100 kHz, which was derived as a reasonable and practical tradeoff between minimized core losses and reduced transformer volume. The operating flux density (B_m) is determined by the transformer operating frequency, allowable core loss (P_{fe}), and the core set volume (V_e). The initial value for B_m is set low in order to minimize core losses. Then, from Eq. (2-7), the area product A_p can be calculated.

Using the core selection table by the area product distribution W_aA_c, three cores, 43610, 43615, and 43825TC, from Magnetics Inc. were selected as shown in Table 2.2. The dimension of the toroidal core is shown in Fig. 2-5. These cores yield bigger area product than the original area product initially calculated in Eq. (2-7). The reason for selecting a bigger toroidal core is to increase the distance gap between primary and secondary windings, which in turn leads to the increased voltage isolation level of the transformer.

There are several types of available coating for toroids: Parylene Y, Nylon V, and Epoxy Z. The Z coating is chosen for toroid since it outperforms Y and V, in terms of a minimum voltage breakdown of 2000V (wire to wire) it offers and temperature that is rated to 200 $^{\circ}C$ continuous operation.

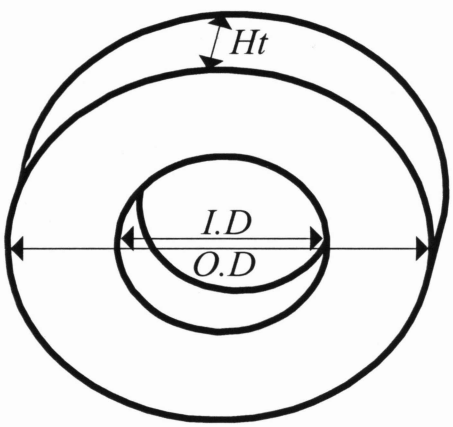


Fig. 2-5: Dimension of the toroidal core.

Table 2-2: Specifications of three different toroidal cores.

Part	O.D (mm)	I.D (mm)	H_t (mm)	l_e (mm^2)	A_c (mm^2)	V_e (mm^3)	W_aA_c (cm^4)	Coating
43610TC	36	23	10	89.7	62.6	5,616	2.61	Z
43615TC	36	23	15	89.6	95.9	8,366	3.93	Z
43825TC	38.1	19	18	82.8	231	19,304	6.58	Z

3. Number of turns

In order to meet other design criteria for the high voltage isolation level transformer, the number of turns on primary and secondary windings must be reduced. This can be fulfilled by operating at high frequency and choosing a core with a big cross-sectional area (43825TC).

In voltage transformer design, input/output voltages are known and thus the transformer ratio $N = \frac{V_P}{V_S}$ is given. The primary turns can be expressed using Faraday's Law:

$$N_P = \frac{V_{in(\min)} D_{\max} (10^4)}{A_C B_m f K_f} \quad , \qquad (2\text{-}8)$$

where A_c is a core cross-sectional area which can be found in Table 2-2. In this particular design: $V_{in(\min)} = 50V$, $D_{\max} = 0.9$. Therefore, the primary number of turns can be calculated from Eq. (2-8) as $N_P = 7$ turns.

The number of turns for each secondary winding is calculated based on the available volt-second product on the primary winding and the desired output voltage. The exact transformer primary to secondary turns ratio (N) is derived from the following relationships used for any buck-derived converter :

$$V_{out} = \frac{D_{\max}}{\frac{N_P}{N_S}} V_{in(\min)} \quad , \qquad (2\text{-}9)$$

where D_{max} is the maximum obtainable duty cycle of the converter, which occurs at the minimum input voltage, $V_{in(min)}$. V_{out} is the peak value of the output voltage, which is 24Vdc. Consider the duty cycle loss of 10% at the secondary winding of the transformer caused by the leakage inductance.

Substituting the turns ratio $N = \frac{N_P}{N_S}$ into Eq. (2-9), the following is obtained:

$$N = \frac{D_{\max}}{V_{out}} V_{in(\min)} \qquad (2\text{-}10)$$

$$= 1.75.$$

Therefore, the secondary number of turns is:

$$N_S = \frac{N_P}{N} = 4 \text{ turns}$$

Optimizing the number of turns at different operating frequencies with core 43825TC—Fig. 2-6 illustrates the relationship between the optimization of the number of primary and secondary turns, and different operating frequencies, at fixed input voltage and the operating flux density between $80mT$ and $100mT$.

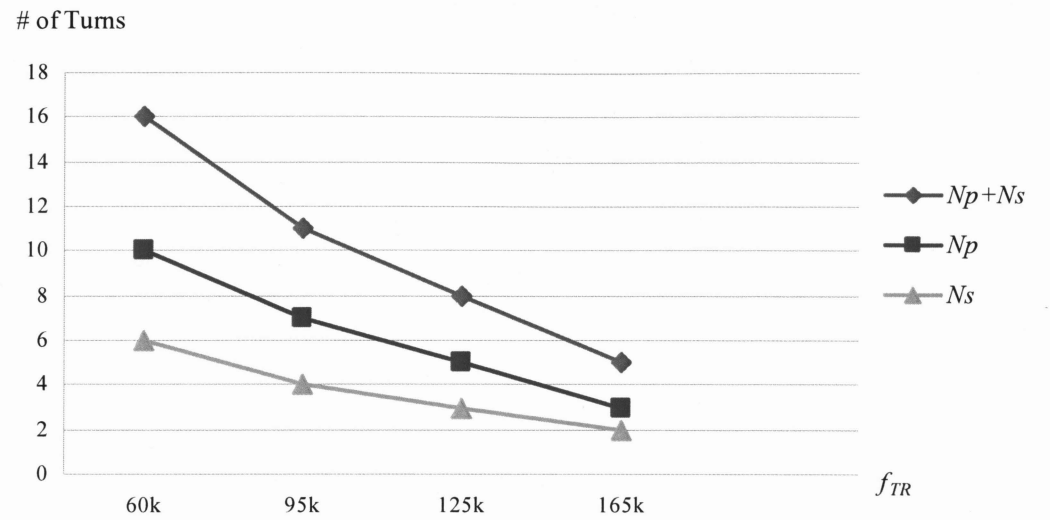


Fig. 2-6: Number of primary and secondary turns vs. operating frequency.

It is observed that as the operating frequency of the transformer increases, the number of turns on primary and secondary is reduced. The lowest number of primary and secondary turns is 3/2, which can be attained at the transformer operating frequency of $165kHz$ indicating that the phase-shift full-bridge DC/DC converter must operate at $330kHz$ clock frequency.

4. Wire size

The size of the wire is calculated based on the primary and secondary currents at current density $J = 400A/cm^2$ [31], [32]. The required number of primary and secondary strands is $S_{np} = 4\ x\ AWG\#23$ and $S_{ns} = 8\ x\ AWG\#23$, respectively. Generally, for high frequency transformer above $100kHz$, the stranded wire (litz wire) for transformer winding should be considered in order to reduce the skin effect losses. However, it is difficult to find litz wire with high voltage isolation coating. As a result, the wire with high isolation coating in the range of $20kV$ to $40kV$ is chosen to provide high voltage isolation level for the transformer as shown in table 2-3.

Table 2-3: High voltage isolation wire.

Wire #	Voltage rating	AWG	Temp	Miscellaneous
1	$20kV$	16	150	Thermal Wire & Cable
2	$40kV$	18	150	Thermal Wire & Cable
3	$30kV$	18	150	Thermal Wire & Cable
4	$30kV$	20	80	Thermal Wire & Cable

5. Discussion

The main issue in designing high voltage isolation level transformer is to reduce or eliminate the corona between primary and secondary windings to meet the BIL (basics insulation level) rating on the transformer. It serves as an assurance to routinely withstand power surges up to the given rating emanating from any number of common sources [34], [35]. The corona can be reduced by eliminating any air entrapped between primary and secondary windings of the transformer. It is realized by first evacuating the air between windings and then potting the core to meet the high voltage isolation requirement of several kilovolts. However, this process is fairly expensive and thus the transformer optimization goal, as mentioned above, is to reduce the cost incurred in this process. With the above optimization procedure, low number of winding turns, wide gap between primary and secondary windings, and high voltage isolation wire for winding, it is possible to satisfy the voltage isolation requirement for the GCT gate driver. The voltage isolation level of the transformer can be further improved by spraying a low-priced special insulating coating to eliminate the air entrapped between primary and secondary windings of the transformer.

2.2.6 Converter 2 for Regulated DC Output Voltage

Converter 1 alone without any output voltage feedback cannot regulate a stable output voltage of $20\pm0.5V$ (required for GCT gate drivers) at light load conditions. As shown in Fig. 2-7, the voltage regulation performs reasonably at full load, while poorly at very light load or open circuit, the reason being that there is no output voltage feedback with respect to the load changes.

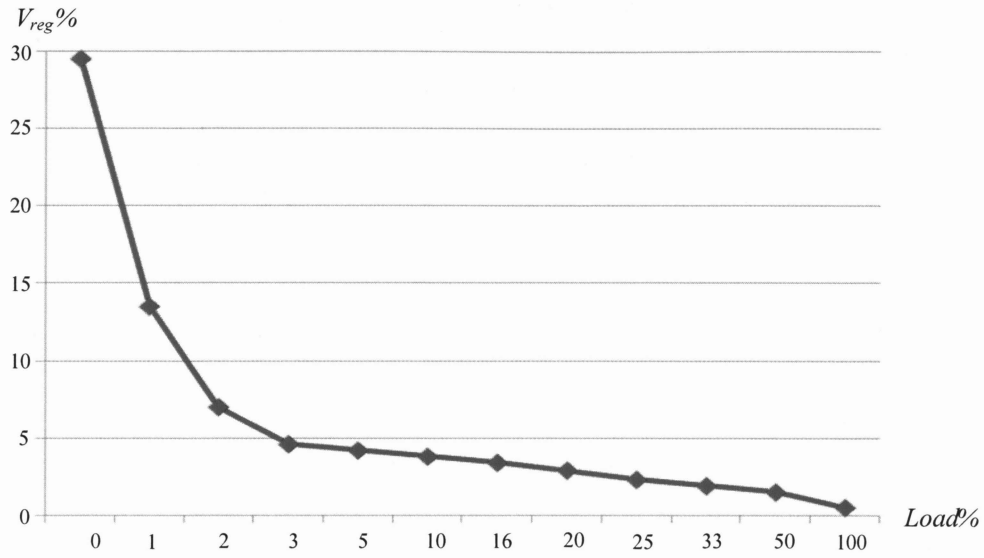


Fig. 2-7: Voltage regulation of Converter 1 without Converter 2.

As a result, the output voltage of the first converter tends to increase to the peak of the secondary overshoot voltage of the transformer at light load. Therefore, an additional DC/DC is cascaded to the output of each isolated power supply in Converter 1 at very low cost, small size, and high efficiency to tackle the problem, resulting in the voltage regulation effective from full load to open load under wide input voltage range for GCT gate drivers.

Converter 2 is a DC/DC step-down converter with integrated FET (TPS5430) from Texas Instruments as shown in Fig. 2-8. The main function of this DC/DC converter is to satisfy the GCT gate driver voltage regulation of 20V dc and the maximum power of $60W$ required for the GCT gate driver.

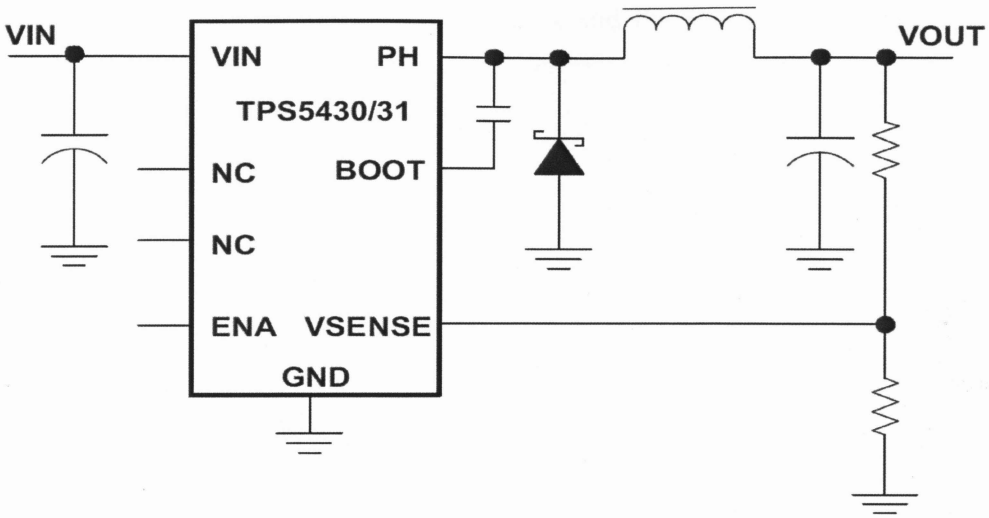


Fig. 2-8: Simplified schematic of DC/DC step-down converter.

The main features of this DC/DC converter are given as follows: 1) It operates under wide input voltage range of $23.6V$ to $36V$ to regulate $20V$ output voltage and $3A$ continuous ($4A$ Peak) output current; 2) It yields high efficiency for up to 97% enabled by $110m\Omega$ integrated MOSFET switch; 3) It has fixed $500kHz$ switching frequency for small filter size. Note that to reduce the design complexity and external component count, the TPS5430 feedback loop is internally compensated; and 4) the system is secured through overcurrent limiting, overvoltage protection, and thermal shutdown.

2.3 Summary and Discussion

In this chapter, a novel parallel isolated power supply (PIPS) for GCT gate drivers is proposed. The proposed design includes six parallel isolated power supplies (PIPS), each supplying a GCT gate driver at regulated 20Vdc. The supply is composed of two power converters, Converter 1 and Converter 2. The former is used to provide electrical isolation between each channel of PIPS and its gate driver, whereas the later is utilized to regulate the output voltage of the supply. This design features a general power supply for powering the gate drivers of switches used in different converter topologies where high voltage insulation level is required, such as Medium Voltage Neutral Point Clamped to PWM CSI converters.

Through the elaboration on the design requirements and the operating principle, the proposed power supply is shown to be able to power up the GCT gate driver. The optimization procedure for the high voltage isolation level transformer is discussed which eliminates the necessity of potting the torodial transformer, and substantially saves the costs on both potting and expensive/bulky commercial power supply.

CHAPTER 3: Component Selection and Efficiency Optimization for PIPS Using Pspice Simulation Model

This chapter starts with the development of a simplified simulation model for PIPS, using commercial software Pspice. In order to obtain accurate design and control, PIPS must first be properly modeled and simulated. With a suitable model in place, the performance of PIPS with optimized transformers (i.e., with minimized cost and size) and its maximum efficiency can be investigated. More importantly, the results of the simulations enable us to predict the performance of the converter and its controller before the actual building and deployment of the hardware, and to assure that all the selected components meet the requirements.

3.1 PIPS PSPICE Model

Fig. 3-1 illustrates the Pspice simulation model for PIPS. All selected components for the simulation model resemble the components used for hardware implementation. The first transformer is modeled as preparation for Pspice simulation. The powerful Pspice magnetic software is adopted to verify the transformer design calculation. Using Magnetic parts editor from Pspice, the value for the primary/secondary voltage, the secondary current, and the transformer frequency is input into the simulation. In the next step, the software will select proper flux density or prompt the designer for the core and flux density. Based on all the information fed to the software, the simulation generates all parameters needed such as the number of primary/secondary turns, the leakage inductances, the power losses, etc. At the end, the transformer model (TR_1 to TR_6) will be ready to add to the simulation model for testing.

There is an auxiliary low power branch connected in parallel with other 6 toroidal transformers. This auxiliary branch consists of a low power step-down voltage transformer VT, bridge rectifier D_{Ba}, small filter L_{fa} and C_{fa}, and low power dummy load R_d (0.4% of total power).

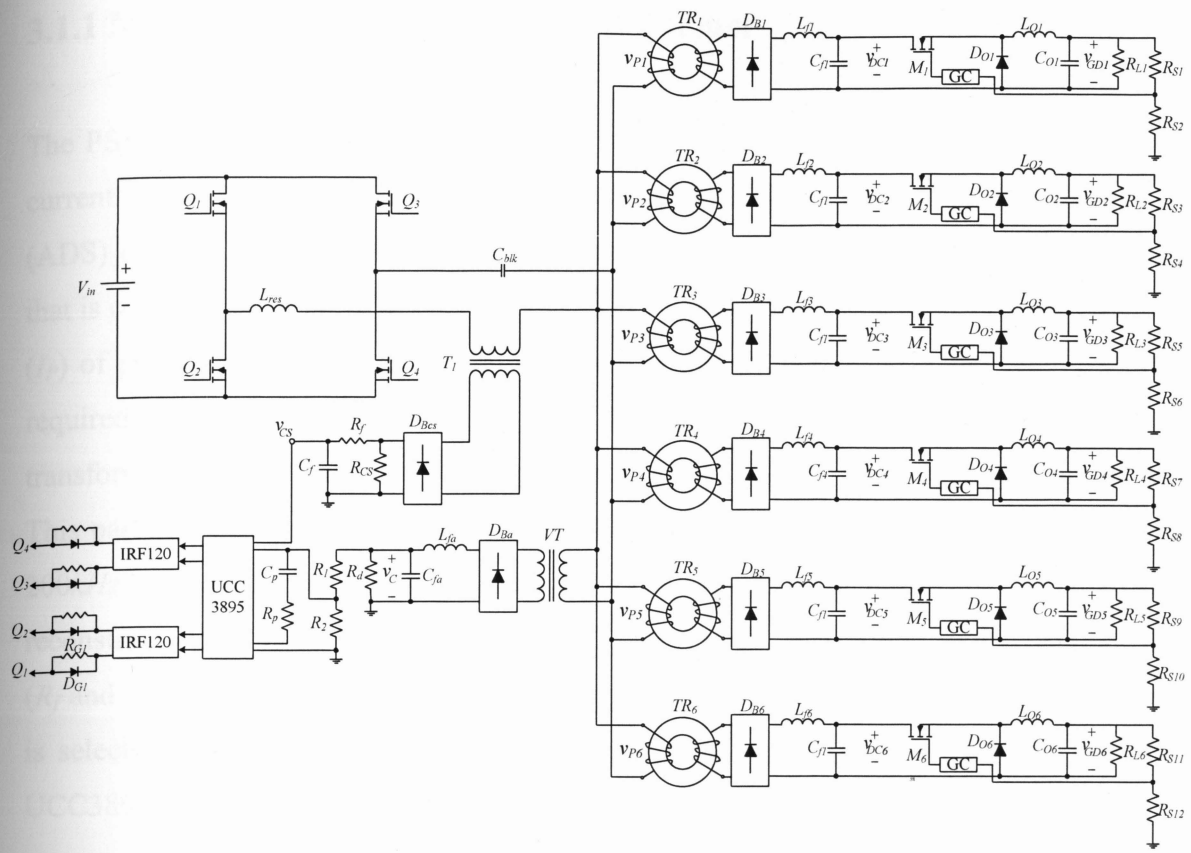


Fig. 3-1: Simulation Model for six parallel isolated power supplies (PIPS).

The auxiliary branch and phase-shift controller UCC3895 are utilized as a voltage feedback loop for PS-FB. Therefore, the output voltages of v_{DC1} to v_{DC6} are regulated with respect to the dc input voltage V_{in} of PS-FB. The controller IC, UCC3895, generates the appropriate turn on signals for all four MOSFET switches (IRFP250) of full-bridge through the gate drivers (IRF2110). The current sensing transformer (T_1) is located at primary side in series with TR_1-TR_6. The purpose of T_1 is to provide over-current protection and adaptive delay set of controller. A small R/C filter (R_C and C_C) is added to clean up the waveform which is input to the UCC3895's current sense pin. The second DC/DC converter is a step-down DC/DC converter to regulate $20V$ dc for the GCT gate drive.

3.1.1 Modeling of Current Sense Transformer

The PSpice simulation model assists in accurately verifying the circuitry design parameters of current sense transformer, which is leveraged for overcurrent protection and adaptive delay set (ADS) of UCC3895. Fig. 3-2 shows the detailed circuit modeling of current sense transformer that is connected to controller UCC3895. Current sense transformer T_1 senses the primary current (I_P) of phase-shift full-bridge PS-FB converter in the proposed PIPS and provides information required for overcurrent protection and ADS for the UCC3895 controller. The current transformer is model based on the actual part number PE-64977A, which has turn's ration 1:20. This part features low leakage inductance, 1250 VRMS isolation, operating frequency between $200kHz$ and $500kHz$, and $20A$ peak current sense capability. A full bridge diode array (D_1-D_4) reconstructs the signal referenced to the UCC3895 controller ground return. A small R/C filter (R_f and C_f) cleans up the waveform that is input to the IC's current sense (CS) pin. Resistor R_{CS} is selected such that a $2.5V$ peak signal corresponds to a 20% overload and will trigger the UCC3895 current limit protection circuit.

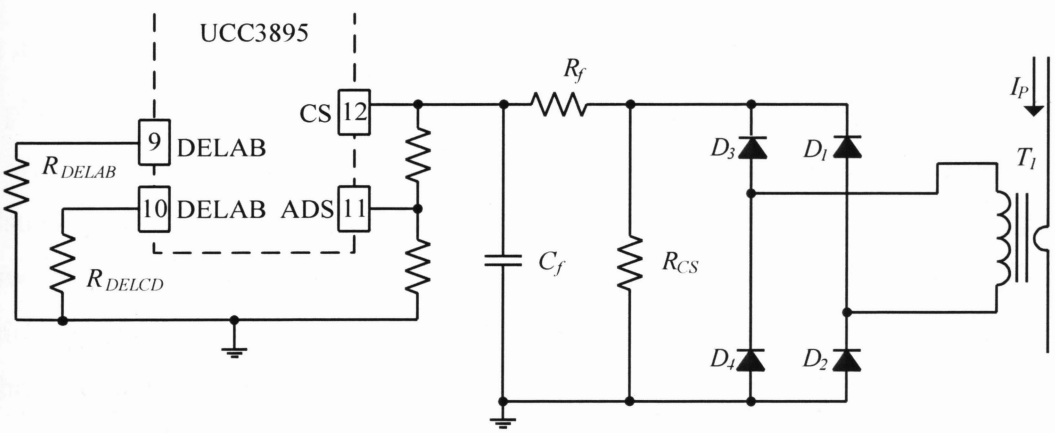


Fig. 3-2: Modeling of current sensing transformer with delay circuit.

The UCC3895 offers the added feature of adaptive delay set (ADS) and delay programming between complementary outputs (DELAB programs the dead time between the switching of OUTA and OUTB, and DELCD programs the dead time between OUTC and OUTD). The ADS

function serves to vary the delay time, which is necessary during the resonant transition period, as a function of load current. When more current is available to fully charge the equivalent resonant capacitance, less delay time is required, resulting in a longer effective duty cycle available for power transfer. At the CS pin of UCC3895, current sensing signal can be used for cycle-by-cycle current limiting and for overcurrent protection in all cases with a secondary threshold for output shutdown. To set the adaptive delay time accordingly, it is imperative to have the current sensing signal on the CS pin. The current sensing signal will trigger the current sense comparator at $2.0V$ and over current comparator at $2.5V$. In the normal condition, the signal on CS should be less than $2.0V$.

3.1.2 Verifying Circuitry Design Parameters for MOSFET Gate Driver

The PSpice simulation aids in the verification of the circuitry design parameters of the MOSFET gate driver. There are two options to drive the full bridge MOSFETs. One is the isolated gate driver transformer and the other is IR2110 or HIP2500 [36]. The isolation provided by the gate-driving transformer is unnecessary in this application and thus IR2110 is adopted rendering the design simpler.

Fig. 3-3 depicts the circuit diagram of MOSFET gate drivers, with the actual part IR2110 for two legs of phase-shift full-bridge (PS-FB) converter employed in PIPS. For MOSFETs, there is a point at which increasing gate-to-source voltage yields no significant reduction in switch forward drop. Usually, this occurs at about 7 to 9 volts. We should avoid overcharging the gate of the power switch because the higher the gate voltage, the longer it takes to turn off the device [36]. In addition, extra charge must be transferred, which dissipates more power both in the IR2110 and in the switch device.

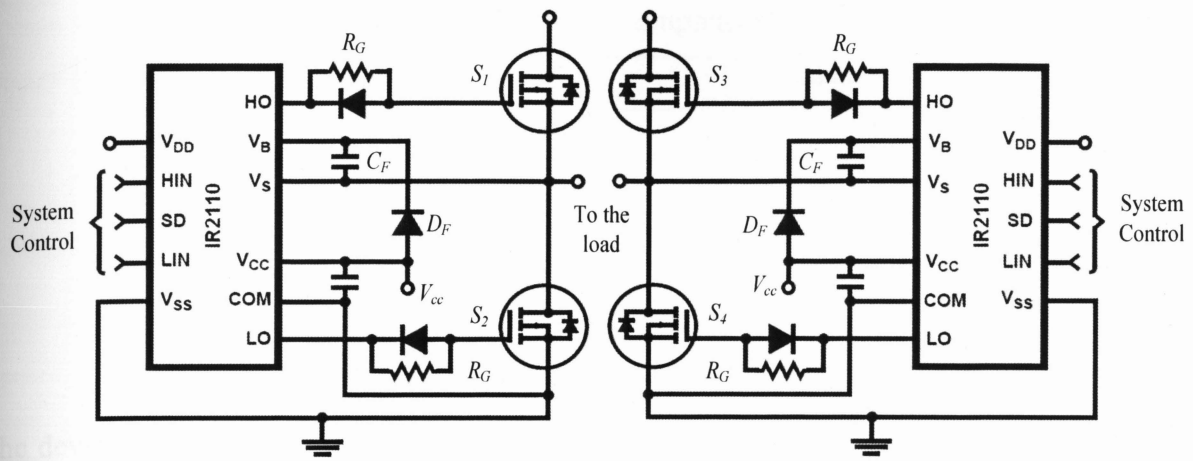


Fig. 3-3: The modeling of MOSFET gate driver circuit.

The upper bias is maintained by the bootstrap capacitor C_F between refresh cycles. A refresh cycle is defined as the time that elapses between conduction periods of the lower power switch and/or its body diode or flyback diode. Compromises are sometimes needed on the size of the bootstrap capacitor. For example, the capacitor should not be so large that an excessively long refresh period is required. Nor should it be so small that the voltage drops below the undervoltage trip point during the upper switch conduction period.

In any event, this capacitor C_F must have sufficient charge to dump into the bootstrap capacitor whenever the V_S terminal moves toward COM. This happens when the lower switch is on and usually whenever the upper switch has just been turned off. If R_G is too small, it tends to reduce the effective dead time and increase the shoot-through tendency. In addition, switching $\frac{dv}{dt}$ increases EMI. $R_G \times C_F$ time constant, if too large, causes excessive power device switching loss. Furthermore, under a big R_G, it may fail to hold the gate low when the opposing power device turns on, either tending to turn on the device prematurely or to slow the desired turn-off due to Miller Effect. One may need to bypass R_G with an anti-parallel signal diode. Table 3-1 displays the component specifications of the bootstrap circuit required for IR2110 as shown in Fig. 3-3.

Table 3-1 Specifications of bootstrap components for IR2110

Component	Definition	Number
C_F	Ceramic capacitor/0.5μF	2
C_G	Ceramic capacitor/10μF	2
D_F	1N4937/600V/1A	2
D_G	1N5817/50V/2A	4
R_G	15Ω	4

The devices in Table 3-1 are chosen based on the formulas and design guides for the bootstrap component selection for MOSFET gate driver IC (IR2110). The Pspice simulation verifies the performance of MOSFET gate driver based on the selected devices in Table 3-1.

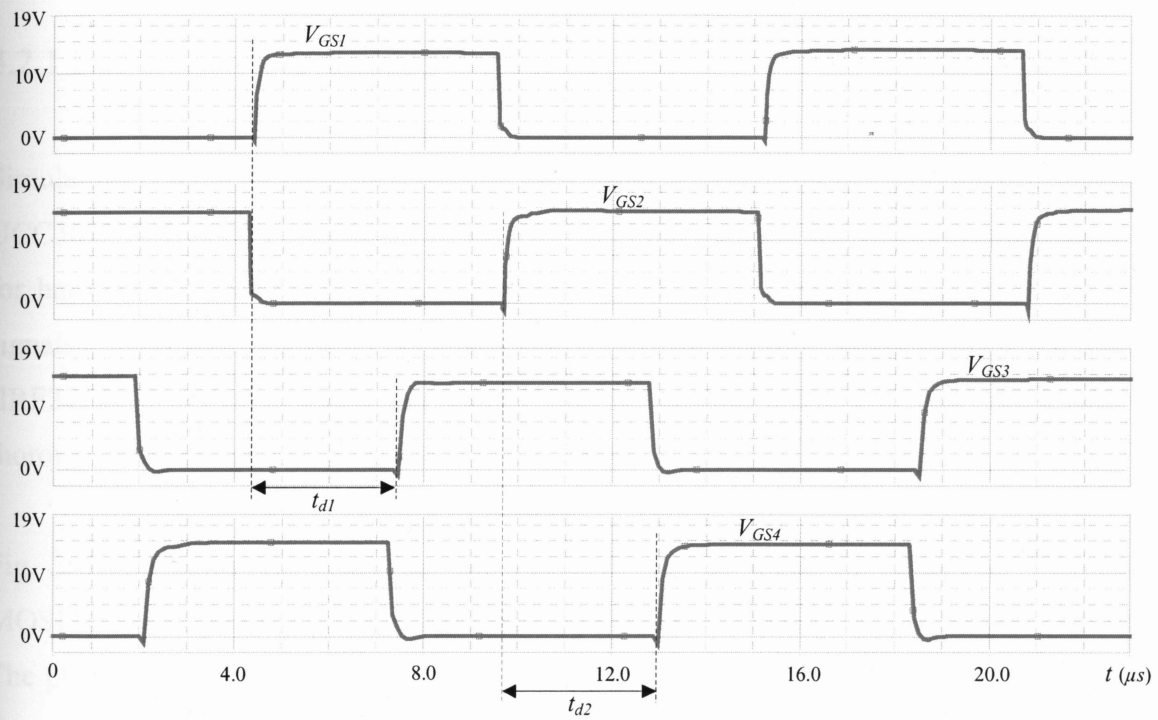


Fig.3-4: Voltage simulation waveforms of MOSFET gate driver using IR2110.

As illustrated in Fig. 3-4, the operation of MOSFET gate driver is verified using IR2110. The voltage waveforms V_{GS1} to V_{GS4} represent the voltages of the gate driver of MOSFETs Q_1 to Q_4, respectively. V_{GS1} is complementary to V_{GS2} and V_{GS3} is complementary to V_{GS4}. V_{GS1}

(respectively V_{GS2}) on the left leg is leading V_{GS3} (respectively V_{GS4}) on the right leg of the full-bridge by time delay t_{d1} (respectively t_{d2}).

3.2 Simulations for Key Component Selection

Simulation waveforms of some of the major components were captured to assure correct operation of the whole system and to verify the design of proposed PIPS. The simulation is run at different input voltages and load conditions to investigate the performance of phase-shifting operation, and to select cost-effective devices for hardware implantation based on current/voltage rating obtained from simulation. In all the simulation tests, the load is instantiated by a resistive load that could be adjusted by using on and off switches.

3.2.1 Simulation Waveforms for Phase-Shift Operation Using UCC3895

Simulation is indispensable to verify the performance of the phase-shift operation and controller UCC3895 in Converter 1. The UCC3895 in the simulation model resembles the actual one used for hardware implementation. The controller IC, UCC3895, generates the appropriate turn on signals for all four MOSFET switches (IRFP250) of the full-bridge through the gate drivers (IRF2110). The design guides on using UCC3895 for the phase-shift full-bridge converter are thoroughly explained in the datasheet of UCC3895.

Fig. 3-5 illustrates the phase shifting operation at the input dc voltage of 80V where the MOSFET gate voltage V_{GS1} lags V_{GS4}, and V_{FB} denotes the voltage across the two legs of PS-FB. The phase-shift operation is clearly observed that when the two voltages V_{GS1} and V_{GS3} overlap, the transformer voltage is zero. When the two switches, V_{GS1} and V_{GS4} of the phase-shift full-bridge are conducting, the power will transfer to the secondary side in the positive half cycle. On the other hand, when V_{GS2} and V_{GS3} of the phase shift full-bridge are conducting, the power will transfer to the secondary side in the negative half cycle. I_{P1}-I_{P6} are the primary currents of the six parallel transformers, and I_P is the sum of these primary currents passing through the output of phase-shift full-bridge shown in the simulation model in Fig. 3-1.

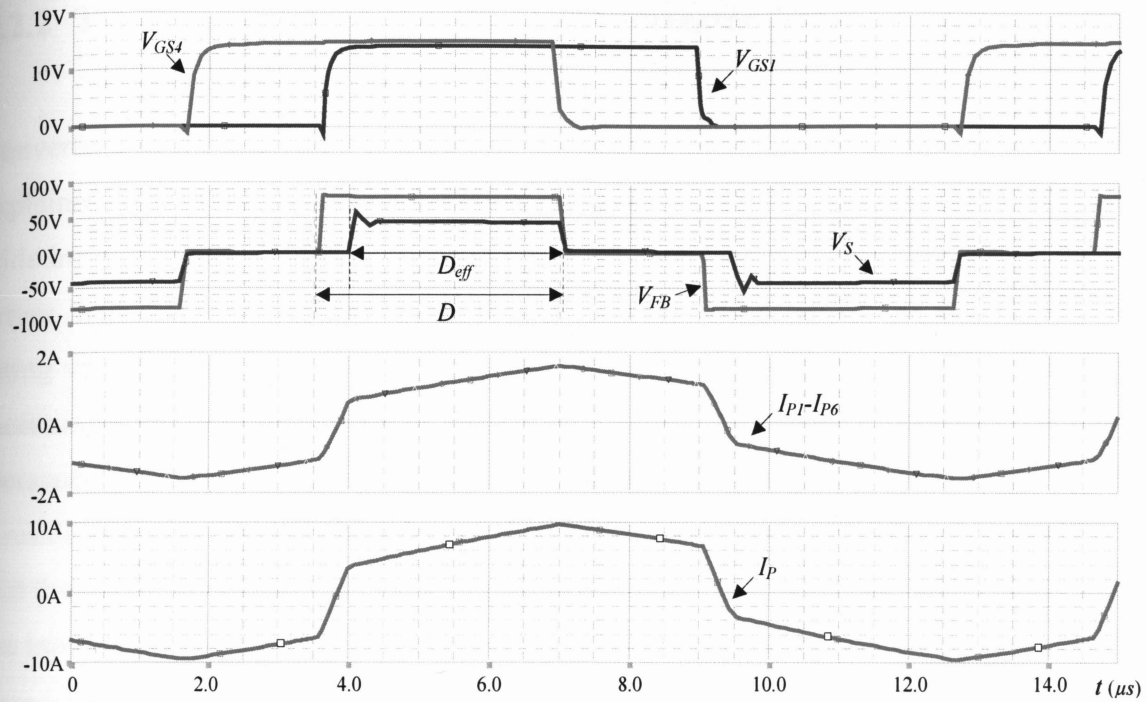


Fig. 3-5: Simulation waveforms for phase-shifting operation.

Note that the duty cycle of V_{FB} equals that of V_{P1}-V_{P6}, the primary voltages of the six parallel transformers. Since the leakage inductance of the transformers is utilized for resonance transition, the need for any external inductance is eliminated.

As a result, there is no duty cycle loss between the primary voltage of the transformers, and the voltage between the two legs of the full-bridge, V_{FB}. However, the secondary duty cycle, D_{eff} is eroded due to the leakage inductance of transformers. The minimum primary duty cycle D and the secondary duty cycle D_{eff} is 63% and 54.5%, respectively, at the maximum input dc voltage as shown in Fig. 3-5. The maximum primary and secondary duty cycle is 98% and 88%, respectively, at the minimum input dc voltage. The maximum duty cycle loss for this design is less than 10% which takes place at the minimum input dc voltage and the maximum output power of $360W$.

3.2.2 The Maximum Input Voltage of Converter 2 at No-Load

Converter 2 is constituted by DC/DC step-down converters, the merits and features of which are explained in detail in Section 2.2.5. One of the specifications of this converter is to operate under wide input dc voltage range 23.6V-36V, while regulating out voltage at 20V dc for the GCT gate driver. It is therefore important that the input voltage of DC/DC never exceeds the maximum rating value of 36V. The output voltage of each isolated power supply of Converter 1 tends to increase to the peak of the secondary voltage of the transformer at no-load condition. This is worsened when Converter 1 operates at the maximum input dc voltage of 80V and at no-load. As a result, a dummy load of 0.2% is added to the output of each isolated power supply, to ensure that the output voltage of each isolated power supply never exceeds the rated voltage required for the input of the DC/DC step-down converters employed in Converter 2.

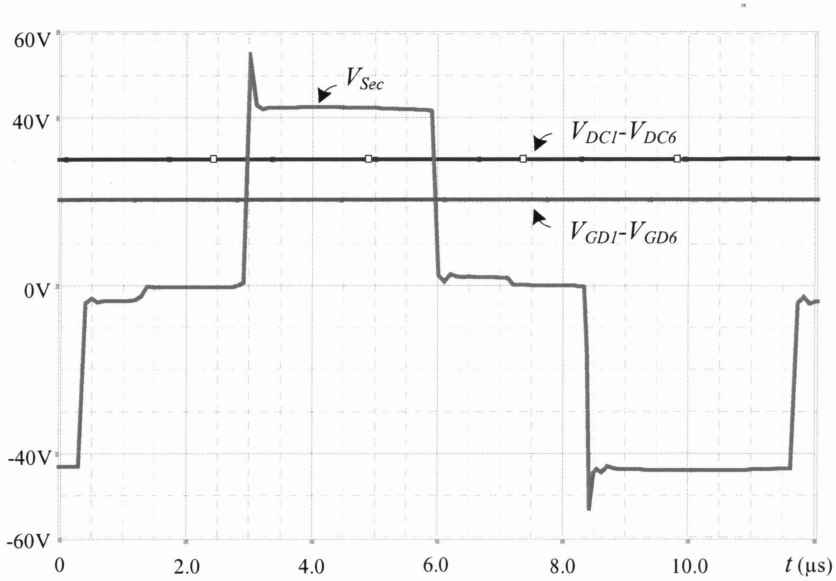


Fig. 3-6: Simulation waveforms for maximum input voltage of DC/DC converter.

Fig. 3-6 displays the output voltage V_{DC1}-V_{DC6} of Converter 1, which stays below 32V at the maximum input dc voltage of 80V and the minimum duty cycle. The output voltage V_{GD1}-V_{GD6} of Converter 2 is regulated at 20V dc from no load to full-load.

3.2.3 Simulation for Key Output Diode and Power MOSFET Selection

The simulation verifies the calculation of power components selection (such as diodes and MOSFETs) for Converter 1 in the proposed PIPS. The voltage rating of the output rectifier diodes and full-bridge MOSFETs shown in Fig. 3-1 is selected based on the worst case simulation scenario, where the input voltage dc supply to the phase-shift full-bridge is at the maximum of $80V$. The current rating of diodes and MOSFETs is chosen also according to the worst case simulation scenario, where the full-bridge input voltage dc is $50V$ and the maximum current of $10A$ is drawn by the full-bridge. The RCD snubber was originally added to the output rectifier diodes of each isolated power supply, which reduced the efficiency of the PIPS. Consequently, all the simulation results obtained here exclude the employment of the snubbers.

1. Output diode selection

When the input dc voltage of the full-bridge is $80V$, the secondary winding voltage is, $80V$ divided by turns ratio, which equals $46V$. Therefore, the peak voltage of a rectifier diode is $46V$. A safety margin should be considered due to the ringing phenomenon at the secondary winding of the high frequency transformer as shown in Fig. 3-7.

The peak overshoot voltage is around $67V$ in the worst case when Converter 1 operates under maximum input dc voltage and full load. As a result, the voltage rating of the diode is determined to be $100V$. A Schottky diode is chosen to lower the switching loss due to the high switching frequency operation. With Schottky diode, forward voltage drop and reverse recovery loss are reduced significantly.

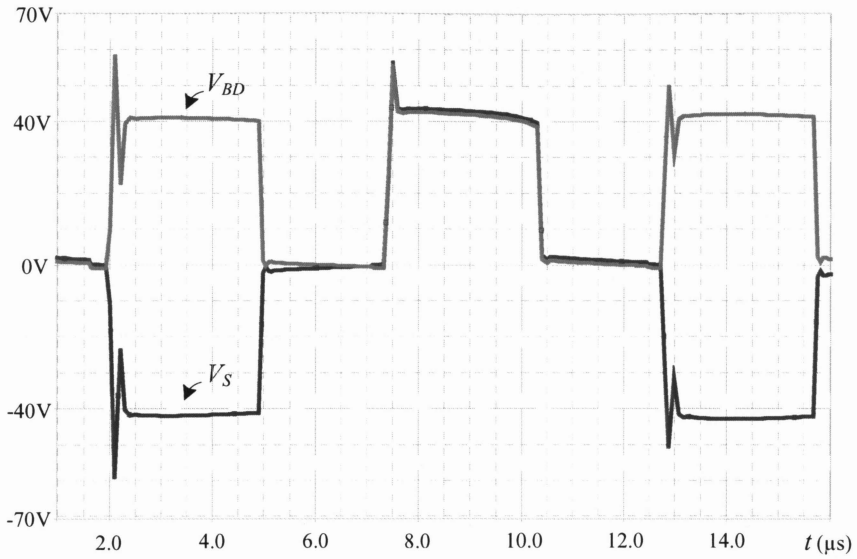


Fig. 3-7: Simulation waveforms for maximum voltage rating of output diodes.

This will improve the efficiency at high switching frequency. The peak current of the diode is identical to the peak current of the inductor.

2. Power MOSFET selection

Power MOSFETs Q_1-Q_4 were selected as switching devices for the PS-FB converter in Fig. 3-1. The peak voltage of a MOSFET is $80V$ as shown in Fig. 3-2(b) which is the maximum input voltage. Considering a safety margin due to small voltage spikes originated from the leakage inductance of the high frequency transformers, the device voltage rating over $150V$ should be acceptable.

Fig. 3-4 illustrates the current I_{LL} passing through the left leg switches (Q_1 and Q_2), and I_{RL} passing though the right leg switches (Q_3 and Q_4). As is shown, the peak current I_{LL} and I_{RL} is around $10A$. Taking safety margins into account, MOSFETs IRFP250, with ratings $200V$ and $30A$ were selected from the manufacture, International Rectifier.

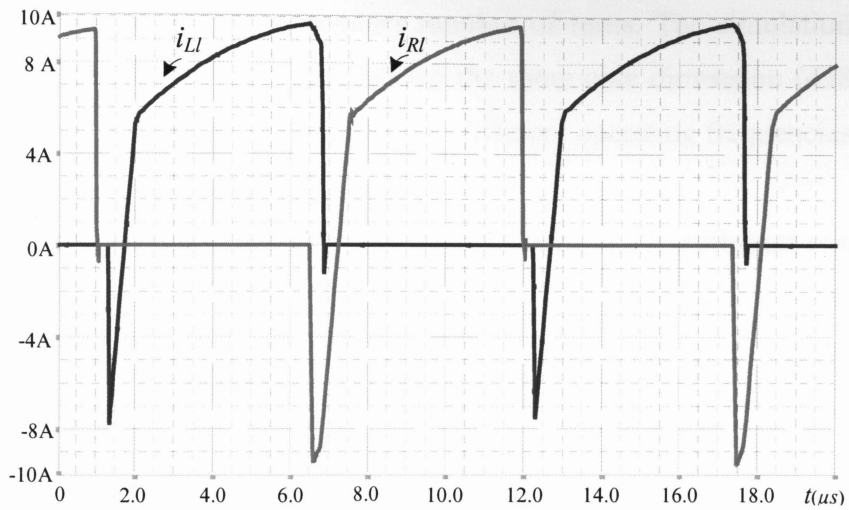


Fig. 3-8: Simulation waveforms for maximum current rating of power MOSFETs.

The reason for selecting MOSFET switches with this high current rating for phase shifted full-bridge PS-FB converter is that, it is desirable to provide some degree of adaptability for future applications. For instance, if later on we need more power handling capabilities, say, 12 isolated power supplies with a total of $720W$, the MOSFET switches must be able to withstand the resulting high current rating.

3.3 Simulation for Maximum Efficiency Fulfillment with Optimized Transformers

The proposed PIPS must deliver the maximum output power for all 6 GCT gate drivers at high efficiency, in order to reduce the cost and size on components such as heat sinks and high voltage isolation transformers. This target can be achieved by means of simulations. The simulation results verify the theoretical calculation of the optimized transformers as well as the performance of these optimized transformers on the overall efficiency of the proposed PIPS.

Table 3-2 demonstrates the simulation results under three different cases to compare the performance of three different optimized transformers on the overall efficiency of Converter 1. Note that the result obtained by simulation is the same as the theoretical calculation in Chapter 2,

for the transformer primary and secondary number of turns. The simulation is repeated in each case with the six toroidal transformers having the same core dimension (43825TC) and different numbers of primary and secondary turns, under different operating frequencies.

Based on the results recorded in Table 3-2, by increasing the transformer operating frequency the number of primary and secondary winding turns of transformer can be reduce and achieve the lowest number of turns desired 7/4, 5/3 and 3/2. Therefore, the switching frequency selection of converter 1 is extremely critical in fulfilling low number of turns, low power losses, and a high efficiency of 91.2%.

Table 3-2: The total power losses breakdown at different operating frequencies.

Component Losses	Case 1		Case 2		Case 3	
	f_{TR}=95kHz	N_p/N_s = 7/4	f_{TR}=125kHz	N_p/N_s = 5/3	f_{TR}=165kHz	N_p/N_s = 3/2
S1-S4	6.7		8.4		10.8	
DB1-DB6	6x2.4=14.4		6x2.6=15.6		6x2.9=17.4	
TR1-TR6	6x1.3=7.8		6x1.8=10.8		6x2.5=15	
Other Losses	6		6		6	
Total Losses	34.9		40.8		49.2	
Efficiency	91.2		89.8		87.9	

3.3.1 Loss Analysis of Converter 1 Operating at 3 Different Frequencies

Fig. 3-9 depicts the percentage ratio of the loss of each component in Table. 3-1 to the maximum output power, $P_{c\text{-}loss}$ / $P_{o,max}$, with respect to three different optimal operating frequencies 95*kHz*, 125*kHz* and 165*kHz*. The Pspice tool is used to calculate the conduction and switching losses (Q_1-Q_4) and the output rectifier diodes (D_{B1}-D_{B6}) which consist of 24 Schottky diodes. Pspice is also leveraged to calculate the transformer losses (TR_1-TR_6) and other losses, such as dummy loads and controller losses for each operating frequency.

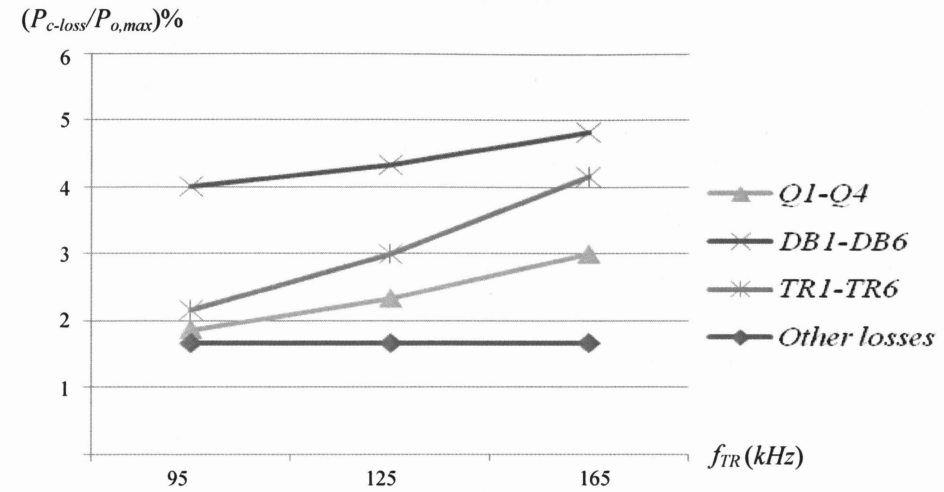


Fig. 3-9: Ratio of component loss to maximum output power vs. operating frequency.

Increased switching frequency should not cause significant losses in the ferrite transformers, which are designed for high frequency operations. However, operating at high switching frequency will degrade the efficiency of Converter 1 and induce EMI for practical implementation. As a result, the maximum operating clock frequency, f_{sw}, is set to $330kHz$ as a reasonable and practical tradeoff between minimizing switching losses and optimizing the transformers. In the full-bridge topology, the core flux swings at half the clock frequency, and thus the maximum transformer operating frequency f_{TR} in this design is $165kHz$.

The major losses in Converter 1, between 4% and 5% of the maximum output power, are caused by the output diode rectifiers (DB_1-DB_6). These losses do not increase significantly at higher operating frequency as shown in Fig. 3-9.

The transformer losses (TR_1-TR_6) will slightly increase when the operating frequency increments from $95kHz$ to $125kHz$, while the operating flux density remains the same for the transformers with turn ratio of 7/4 and 5/3. For the transformer operating at the maximum frequency of $165kHz$ and with minimum number of turns 3/2, the loss (TR1-TR6) is almost 1.5 times that of the transformer operating at $125kHz$, and twice that of the transformer operating at $95kHz$. The reason for the increased losses is due to the fact that the minimum number of winding turn (i.e.,

3/2) is to be achieved at the maximum operating frequency (i.e., 165*kHz*) of Converter 1, causing the flux density to increase as stated in Eq. (2-4).

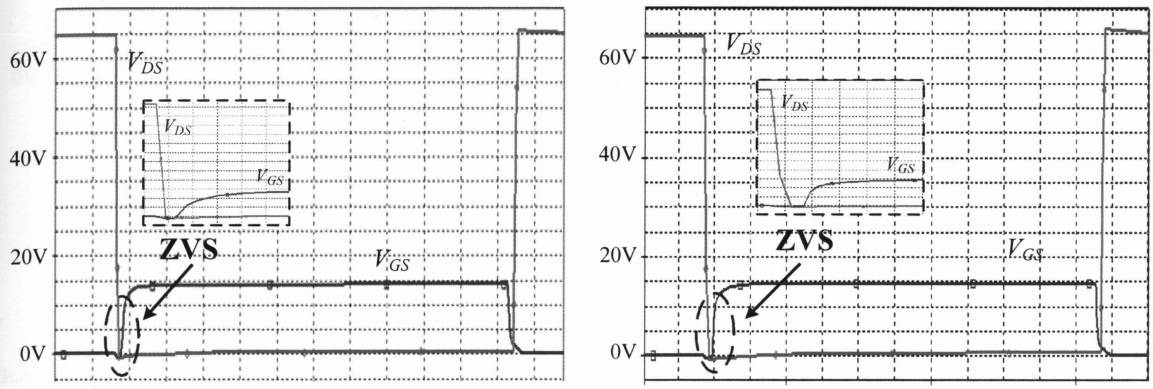
The switching losses of (Q_1-Q_4) at full-load are negligible. In addition, ZVS provides no turn-on losses. The fast turn-off of the devices, together with the large value of output capacitance, minimizes the current and voltage overlap during the turn-off. Even when the ZVS is lost, the total loss associated with each switch is always less than the loss at full-load. The main source of switching losses of (Q_1-Q_4) is the voltage drop in the channel resistance of the MOSFETs. The losses induced by the controller circuitry and the output dummy loads are referred to as other losses, which are below 2% and invariable with respect to the different operating frequencies, as observed in Fig. 3-9.

3.3.2 State of ZVS for Switching Loss Reduction

It is crucial to observe the ZVS operation in MOSFET switches of Converter 1, since the ZVS operation is an indicator for switching loss reduction. The simulation results indicate that the switching losses are decreased when Converter 1 operates at ZVS, giving rise to increased efficiency. In addition, the turn-off losses can be reduced by faster gate turn-off. Hence, the heat sinks for the four MOSFETs and the PCB can be predicted to take on smaller size. As mentioned in Chapter 2, the ZVS operation is different for the lagging leg and leading leg of the full-bridge. It persists for the lagging leg even if under light load condition, but is lost for the leading leg in such condition. Specifically, the ZVS operation is lost under light load, i.e., at 25% of full-load, for leading leg switches, Q_1 and Q_2, causing switching losses. However, these losses are small and will not degrade the efficiency significantly. Heat sinks are selected for the worst case power dissipation at full load, and there is plenty of margin at light loads in spite of the lossy transition. To better demonstrate the state of ZVS in Converter 1, we place one switch on the leading leg and one on the lagging leg, thereby showing the ZVS of all four switches.

1. ZVS at full load condition

Fig. 3-10(a) illustrates the impact of ZVS operation on the output voltage V_{DS1} and the gate voltage V_{GS1} of Q_1, one of the leading leg MOSFET switches.



(a) leading leg (b) lagging leg

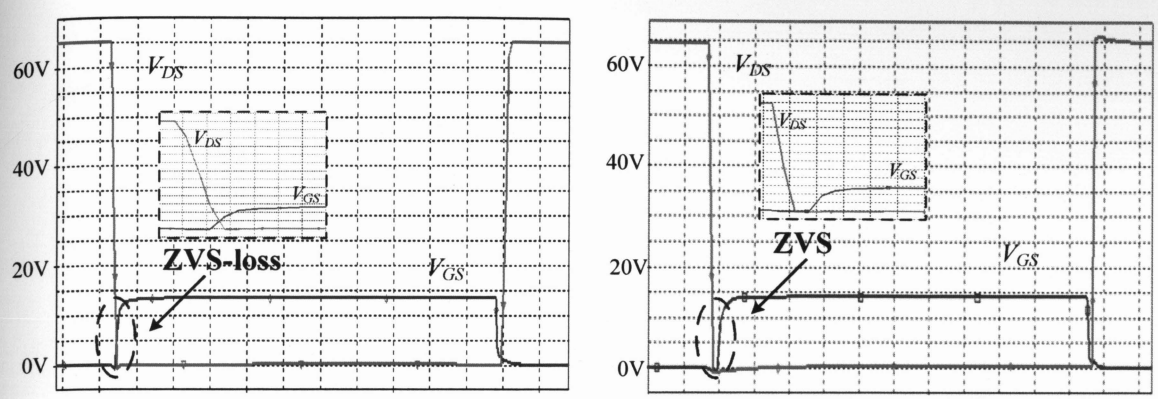
Fig. 3-10: ZVS operation at full-load for (a) leading leg (b) lagging leg.

Similarly, Fig. 3-10(b) illustrates the impact of ZVS operation on the output voltage V_{DS3} and the gate voltage V_{GS3} of S_3, one of the lagging leg MOSFET switches, at the maximum output power of $360W$.

Note that in Fig. 3-10, the voltage across MOSFET V_{DS1} and V_{DS3} tends to zero before the MOSFET gate voltage V_{GS1} and V_{GS3} becomes high, which indicates that the body diode is on before the turn-on of the switch.

2. ZVS at light load condition

Fig. 3-11(a) illustrates the ZVS loss for the leading leg MOSFETs at 25% of full-load. As can be observed, V_{DS1} is non-zero when V_{GS1} turns on, which is the main reason for the ZVS loss. The ZVS for Q_1 and Q_2 is dependent on the load of the converter.



(a) leading leg (b) lagging leg

Fig. 3-11: ZVS operation at 25% of full-load for (a) leading leg (b) lagging leg.

Under light loads, the current through L_{LK} may not be sufficient to charge/discharge the output capacitance of the MOSFETs (Q_1 and Q_2) or to turn on the antiparallel diode (D_1 or D_2). In other words, the ZVS loss incurred here is due to the fact that the energy stored in the leakage inductance is insufficient to charge/discharge the output parasitic capacitances of MOSFETs. On the other hand, Fig. 3-11(b) shows that ZVS is achieved for lagging leg switches Q_3 and Q_4 even under light load condition, the reason being that the energy of the large filter inductor in the secondary is leveraged to achieve ZVS in this case.

3. Efficiency curve of Converter 1

The efficiency curve of Converter 1 operating at $95kHz$ under different loads is displayed in Fig. 3-12. For loads above $275W$, the efficiency of Converter 1 remains above 91% or more.

The peak efficiency is over 91.8% with loads in between $400W$ and $490W$. An overall efficiency of higher than 91% can be attained at the maximum power of $360W$ which is required to supply six GCT devices.

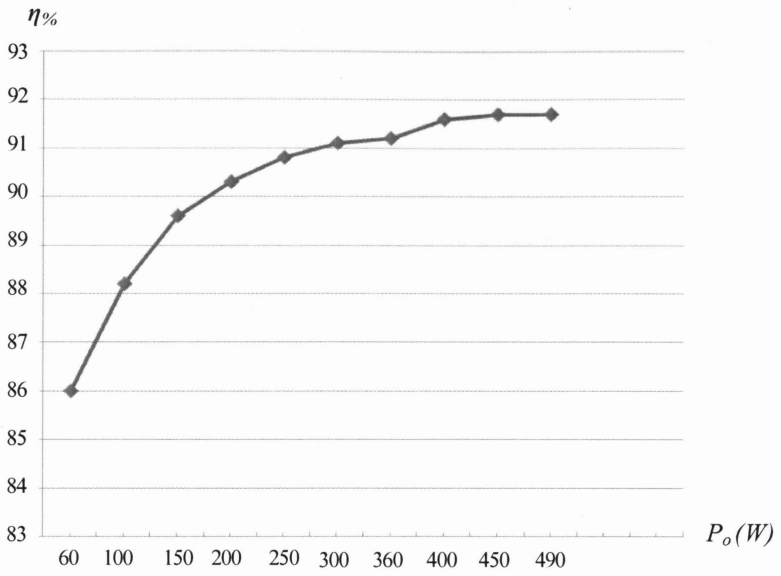


Fig. 3-12: Efficiency curve of Converter 1 (f_{TR}=95kHz).

Based on the efficiency values obtained from the simulation, the power density of the proposed power supply is estimated to be very high, indicating that the heat sinks for all four MOSFET switches can be of less volume and a smaller sized output filter can be selected since the converter operates at high frequency. As a result, one of the major goals of the proposed design, the fulfillment of compact sized power supply with high switching frequency and high efficiency, is assured in that the six power supplies for the GCT gate drivers can be integrated in one PCB unit.

3.4 Summary

In this chapter, the simulation model for parallel isolated power supplies (PIPS) is developed. The performance of the proposed PIPS is investigated leveraging this model. Simulation serves as verification for the suitability of the phase-shift zero voltage switching technique in the proposed design. The successful utilization of this technique attributes to fixed frequency conversion, lossless switching transitions, and high efficiency operations. The voltage/current rating of the selected key devices is determined by the simulation results, which also confirm the theoretical calculation for the optimized transformers and the performance of these transformers

that impacts the overall efficiency of the proposed PIPS. A maximum efficiency of 91.2% is achieved with the optimized transformers at the maximum output power of $360W$ for the six GCT gate drivers. Each isolated channel of the proposed PIPS can provide an output power of more than $60W$, satisfying the requirement of most commercial GCT devices.

CHAPTER 4: HARDWARE IMPLEMENTATION AND VERIFICATION

This chapter focuses on the descriptions of the PIPS prototype, and detailed demonstration and explanations with regard to the experiments conducted on the optimized transformer to achieve high voltage isolation level for the GCT gate driver at low cost. The experiment tasks are to verify the performance of PIPS which provides the voltage regulation, voltage isolation level, and efficiency required for the GCT gate driver. The ZVS design steps for Converter 1 are discussed, with the experimental waveforms for ZVS operations elaborated. Since Converter 1 is operating at high frequency, it is imperative to reduce the switching losses in order to attain the increased efficiency. Finally, the main topic of this chapter is recapped and summarized.

4.1 PIPS Prototype

Fig. 4-1 depicts the DC/DC converter laboratory prototype, which consists of two print circuit boards (PCBs), the first comprising the phase-shift inverter, controller, and 6 parallel toroidal transformers, and the second being the step-down dc/dc converter. The prototype is built based on the circuit shown in Fig. 2-2.

Integrating the two converters into one board renders the optimization easier. The drivers' circuit is on the power stage board to ensure that they are as close to the MOSFETs as possible to eliminate the effects of noise and parasitic inductance. The optimization of PCB routing shortens the routing distance between high power components such as MOSFET switches and the power transformers. The controller UCC3895 and related components are not placed near the power component. The clock frequency of more than $500kHz$ has been attempted on this PCB at power rating of $430W$, and no significant EMI/RFI is observed.

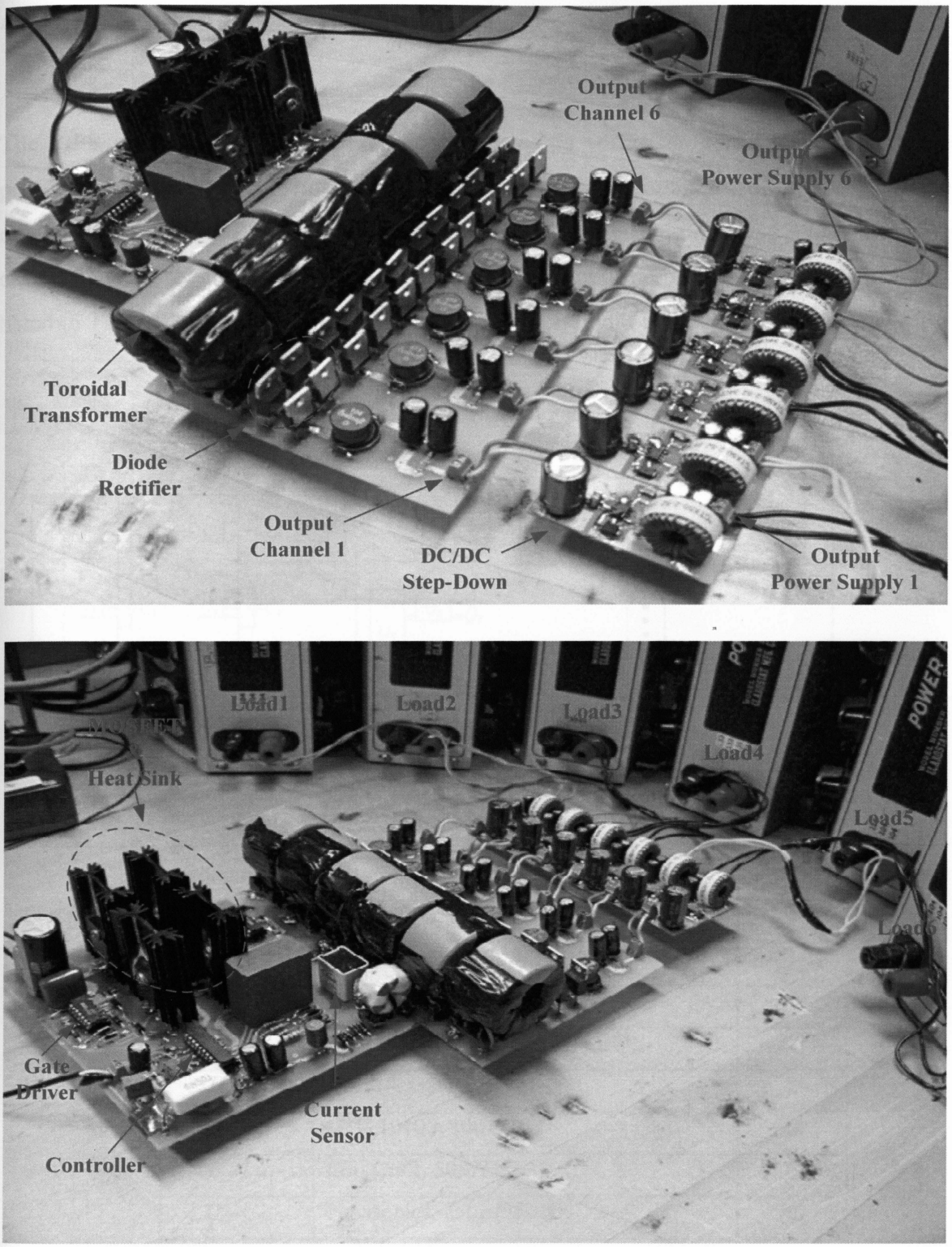


Fig. 4-1: Prototype of Parallel Isolated Power Supply (PIPS).

4.2 Experiments on PIPS

The PIPS prototype shown in Fig. 4-1 was tested to verify the performance of the proposed power supply. The experiments were conducted using a dc voltage rectifier, and V_{in} is the input dc supply for the PIPS. The output loads of PIPS are adjustable resistive loads. The simplified circuit diagram for the prototype is drawn in Fig. 4-2, and the parameters of the PIPS board are listed in Tables 4-1 and 4-2. The schematic of the PCB board is given in Appendix.

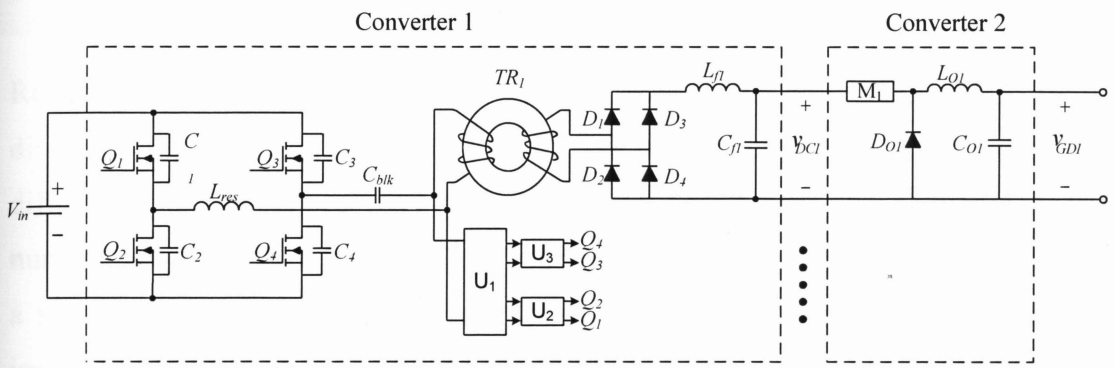


Fig. 4-2: Simplified PIPS circuit diagram.

Table 4-1: Parameters of Converter 1.

Component	Definition	Number
Q_1-Q_4	IRFP250, $250V/23A$	4
C_{blk}	Pulse capacitor, $8\mu F/250V$	1
TR_1-TR_6	43825TC, Magnetic Inc, 7/4	6
U_1	UCC3895, Phase-shift PWM	1
U_2-U_1	IR2110, Gate Driver	2
D_1-D_{24}	MBR10100, $100V/10A$	24
L_{f1}-L_{f6}	Coil Craft, $50\mu H$	6
C_{f1}-C_{f6}	Panasonics, $250\mu F/50V$	6

Table 4-2: Parameters of Converter 2.

Component	Definition	Number
M_1-M_6	TPS5430, DC/DC Buck Converter $3A$	6
D_{O1}-D_{O6}	CZSH5-40, $40V/5A$	6
L_{O1}-L_{O6}	Coil Craft, $50\mu H$	6
C_{f1}-C_{f6}	Panasonics, $68\mu F/35V$	6

4.2.1 Experimental Verification of Transformer Optimization

Results obtained from the experiments for the transformer optimization are illustrated and discussed in this section. We have conducted experiments on toroidal transformers with three different core dimensions (Appendix A). The results verify that 43825TC requires the lowest number of turns since it bears a bigger core cross section area compared to the other two cores. As a result, the voltage isolation level between primary and secondary of the transformer can be improved. Further experiments are carried out to lower the number of turns on 43825TC at different operating frequencies with the desirable B_m (not increasing core loss).

Table 4-3 lists the experimental results for optimized transformer with core dimension 43825TC under three different operating frequencies, at rated output power of 360W and input dc voltage of $52V$. Under all three cases, hereafter referred to as f_{TR}-95, f_{TR}-125, and f_{TR}-165 (distinguished by the operating frequency), the number of primary and secondary turns can be reduced in the operating switching frequency range of $95kHz$ to $165kHz$. However, the tradeoff for achieving the lowest number of turns is the higher switching frequency, resulting in slight degradation of the overall efficiency of the converter. Based on the results recorded in Table 4-3, by increasing the transformer operating frequency f_{TR}, the number of primary and secondary winding turns of the transformer can be reduced, and the lowest number of turns can be obtained as 7/4, 5/3, and 3/2 for the three cases. Therefore, the switching frequency selection of Converter 1 is extremely critical in fulfilling low number of turns, low power losses, low temperature rise, low EMI, and high efficiency of 89.5% that is very close to the Pspice simulation result. Higher switching frequency around $250kHz$ was attempted which nevertheless, reduced the efficiency of Converter 1 to below

81%. We conclude that the optimal switching frequency should be chosen in the rang of $95kHz$ to $165kHz$.

Table 4-3: Experimental results for transformer optimization.

Case	Part #	A_e $[mm^2]$	f_{TR} $[kHz]$	ΔT_{Rise} $[^\circ C]$	N_p/N_s	L_{eq} (μH)	L_{meq} (μH)	% η
1	43825C	231	95	19.6	7/4	1.4	650	89.5
2	43825C	231	125	28.1	5/3	0.87	420	87.4
3	43825C	231	165	36.3	3/2	0.45	215	84.3

4.2.2 High Pot and Corona Testing on Optimized Transformers

The Hi Pot and Corona testing are conducted on the optimized transformers to assure the high voltage isolation level requried for the MV drive application at Rockwell Automation Canada. In the Hi Pot test on the optimized transformers, the primary and secondary winding are shorted. We apply $37kV/60Hz$ between the primary and secondary windings as shown in Fig. 4-3. The leakage current is measured at less than $3mA$ which satisfies the Hi Pot test requried for the MV drive application (i.e., leakage current less that $5mA$ at $37kV/60Hz$).

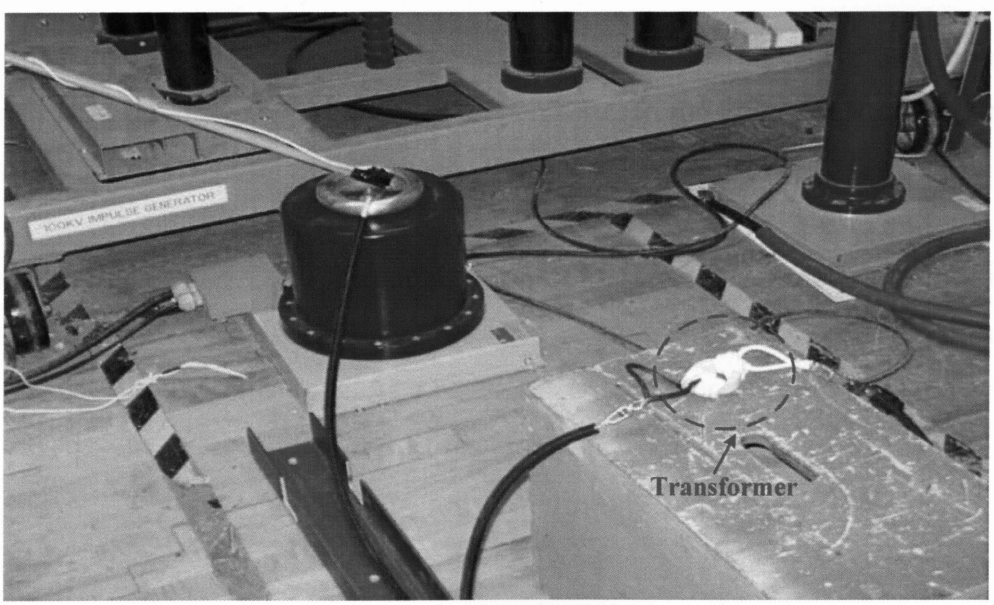


Fig. 4-3: Hi Pot testing on optimized transformers at $37kV/60Hz$.

In Corona test on the optimized transformers, the primary and secondary windings are shorted as illustrated in Fig. 4-4. The voltage is raised to more than $9kV$ rms for a minute between the primary and secondary. The partial discharge is measured at less than $4pC$ which satisfies the Corona test required for the MV drive application (i.e., partial discharge less than $10pC$ at $9kV/60Hz$).

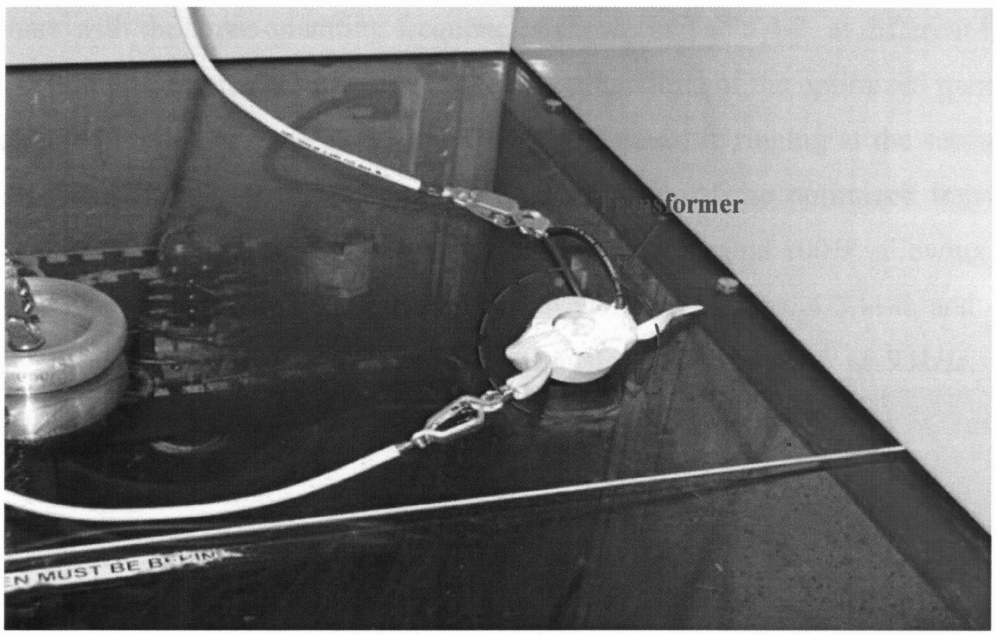


Fig. 4-4: Corona testing on optimized transformers at $12kV/60Hz$.

The greatest improvement was made when a special insulating spray was applied on the transformer to reduce the amount of air entrapped between the primary and secondary windings. In this case, the Corona inception voltage increases up to $12kV$.

Based on the Hi Pot and Corona testing on the optimized transformers, we conclude that the optimized transformers can satisfy the voltage isolation level (for both Hi Pot and Corona) required for MV drive applications. As a result, the transformer need not be potted which greatly reduces the cost due to the potting of the transformers.

4.2.3 Overall Performance of Optimized Transformers on Converter 1

It is important to examine the performance of the optimized transformers on the overall system. The effects of parasitic elements of the transformer on the operation of the system, such as leakage inductance and parasitic capacitance of the windings, are analyzed in this section from the experimental waveforms of the transformer. The experiments are conducted on the optimized transformers with the three operating frequencies shown in Table 4-3, at different input voltage and load conditions, in order to investigate the power handling of the optimized transformers and the duty cycle loss due to the leakage inductance and parasitic ringing at the secondary side of the transformers. Based on the experimental results, each of the optimized transformers can operate at more than 150% of the rated maximum power at around $100W$, allowing ample room for higher power applications. The experimental waveforms of Figs. 4-5, 4-6, and 4-7 illustrate the voltage and current characteristics of the transformers operating at $95kHz$, $125kHz$ and $165kHz$, respectively, under the same fixed input voltage and output load.

1. Transformer operating at 95kHz

Fig. 4-5 depicts the voltage and current waveforms of the transformer operating at $95kHz$, the primary voltage v_P of the six parallel transformers, the secondary voltage v_S of one of the six parallel transformers, and the total primary current I_P passing through the output of PS-FB.

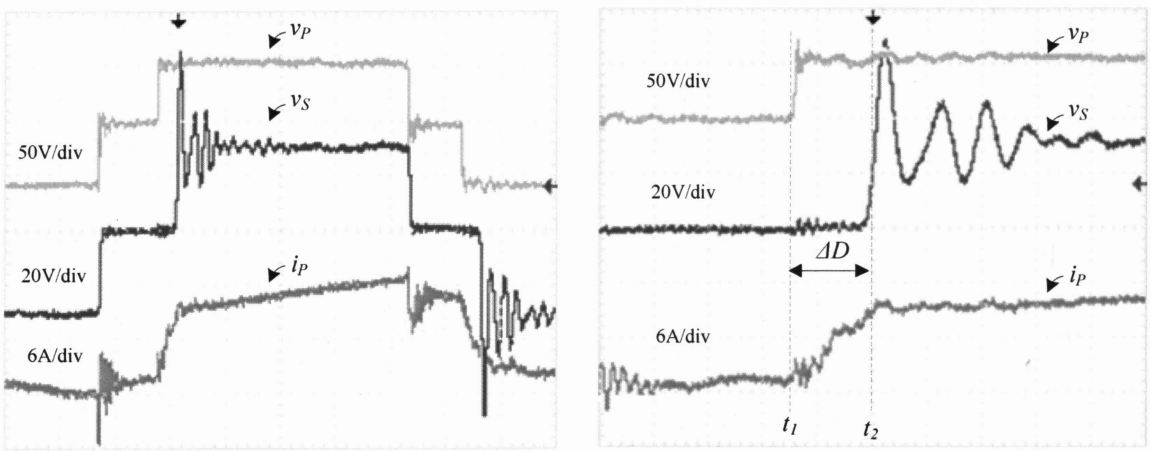


Fig. 4-5: Voltage and current waveforms of optimized transformer operating at $95kHz$.

The parasitic ringing across the secondary side of the transformer is caused by the leakage inductance of the transformer, and the winding capacitance and the junction capacitances of rectifier diodes [17]. The frequency of this ringing is proportional to the turns ratio, and reversely proportional to the value of a) leakage inductance, b) winding capacitance of the transformer, and c) junction capacitance of the output rectifier diodes. The magnitude of overshoot voltage depends on the rate of the current decay and also on the inductance [37]. The approximation of this ringing frequency measured from the secondary side of experimental waveform is $2MHz$. From the waveform, ΔD is the duty cycle loss at the secondary which is around 8% of the duty cycle loss. This ΔD is caused by the finite time (t_1-t_2) necessary for changing the direction of primary current I_P due to the presence of the leakage inductance. I_P is the sum of the primary current of the six parallel transformers.

2. Transformer operating at 125kHz

The voltage and current waveforms of the transformer operating at $125kHz$ are illustrated in Fig. 4-6, with the same parameters v_P, v_S, and I_P defined previously.

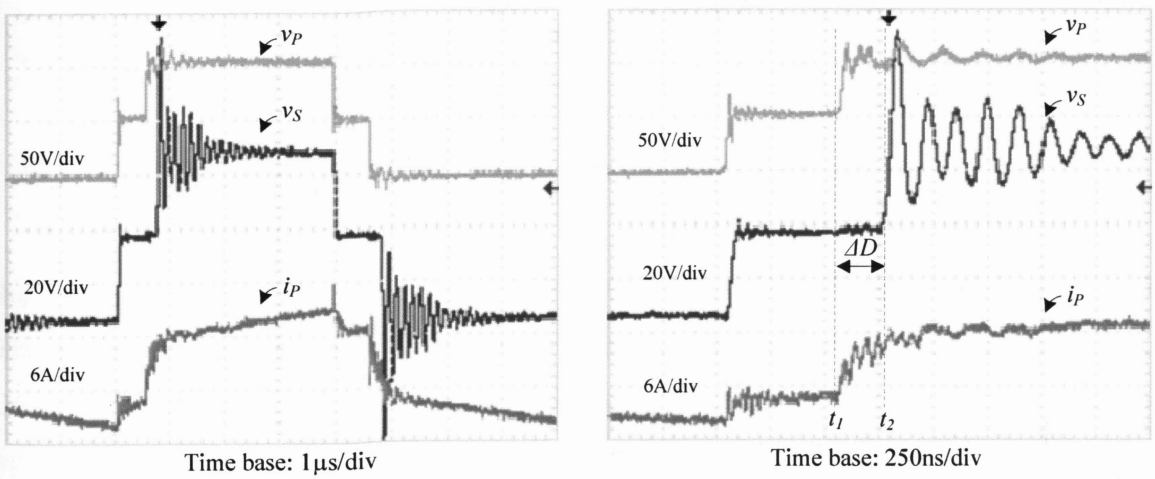


Fig. 4-6: Voltage and current waveforms of optimized transformer operating at $125kHz$.

The parasitic ringing frequency across the secondary side of the transformer is $4MHz$, derived from the waveform. The ringing frequency doubles in the case of f_{TR}-125 compared to f_{TR}-95

since the value of L_{eq} and winding capacitance are lower than those of f_{TR}-95. The magnitude of the overshoot voltage increases in comparison to f_{TR}-95 even though with a smaller value of L_{eq}, caused by the increased switching frequency in the case of f_{TR}-125. The duty cycle loss ΔD at the secondary of f_{TR}-125 is around 6.25% which is slightly lower than that of f_{TR}-95, attributed to the smaller L_{eq} in the former case. Due to the smaller turns ratio, the primary current I_P of the six parallel transformers slightly increases in the case of f_{TR}-125.

3. **Transformer operating at 165kHz**

Fig. 4-7 shows the voltage and current waveforms of the transformer operating at 165*kHz*, where v_P, v_S, and I_P are defined analogously to those for f_{TR}-95 and f_{TR}-125.

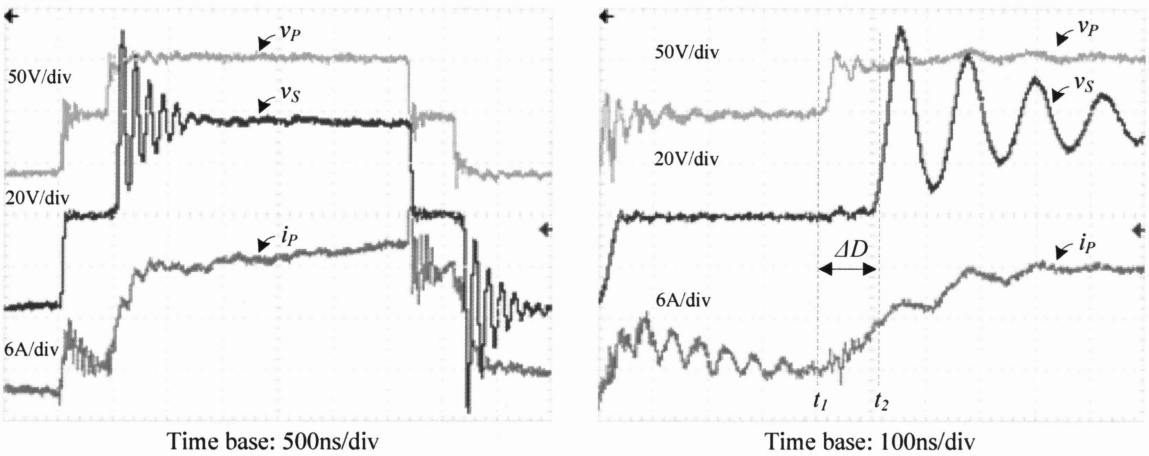


Fig. 4-7: Voltage and current waveforms of optimized transformer operating at 165*kHz*.

The parasitic ringing frequency across the secondary side of the transformer is 6.66*MHz*, measured from the waveform. The ringing frequency in the case of f_{TR}-165 is twice that of f_{TR}-125 and triples as compared with f_{TR}-95, again because of the smaller L_{eq} and winding capacitance than in both the latter cases. The magnitude of the overshoot voltage ringing (2^{nd}, 3^{rd}, etc.) is higher than that of f_{TR}-125 and f_{TR}-95 for a similar reason explained in the case above where the transformer operates at 125*kHz*. It is observed that the duty cycle loss ΔD at the secondary is around 3.8%, smaller than both previous cases due to the decrease in L_{eq}. It resembles Case 2 that I_P increases as a result of the reduced turns ratio of the transformer.

since the value of L_{eq} and winding capacitance are lower than those of f_{TR}-95. The magnitude of the overshoot voltage increases in comparison to f_{TR}-95 even though with a smaller value of L_{eq}, caused by the increased switching frequency in the case of f_{TR}-125. The duty cycle loss ΔD at the secondary of f_{TR}-125 is around 6.25% which is slightly lower than that of f_{TR}-95, attributed to the smaller L_{eq} in the former case. Due to the smaller turns ratio, the primary current I_P of the six parallel transformers slightly increases in the case of f_{TR}-125.

3. **Transformer operating at 165kHz**

Fig. 4-7 shows the voltage and current waveforms of the transformer operating at 165kHz, where v_P, v_S, and I_P are defined analogously to those for f_{TR}-95 and f_{TR}-125.

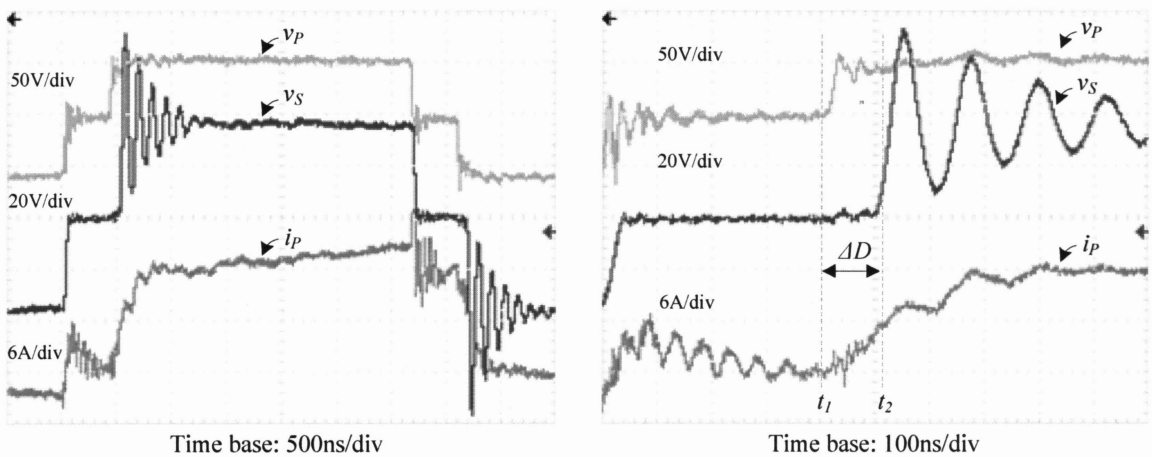


Fig. 4-7: Voltage and current waveforms of optimized transformer operating at 165kHz.

The parasitic ringing frequency across the secondary side of the transformer is 6.66MHz, measured from the waveform. The ringing frequency in the case of f_{TR}-165 is twice that of f_{TR}-125 and triples as compared with f_{TR}-95, again because of the smaller L_{eq} and winding capacitance than in both the latter cases. The magnitude of the overshoot voltage ringing (2^{nd}, 3^{rd}, etc.) is higher than that of f_{TR}-125 and f_{TR}-95 for a similar reason explained in the case above where the transformer operates at 125kHz. It is observed that the duty cycle loss ΔD at the secondary is around 3.8%, smaller than both previous cases due to the decrease in L_{eq}. It resembles Case 2 that I_P increases as a result of the reduced turns ratio of the transformer.

4.2.4 Output Voltage Regulation with Different Load Conditions

For the experiments discussed in this section, the output power of each power supply is varied from 0 to $60W$ by changing the load resistance (R_{L1}-R_{L6}), as shown in Fig. 4-8. In addition, the PIPS input voltage, V_{in}, is set to $60V$ which is supplied by the rectifier diode.

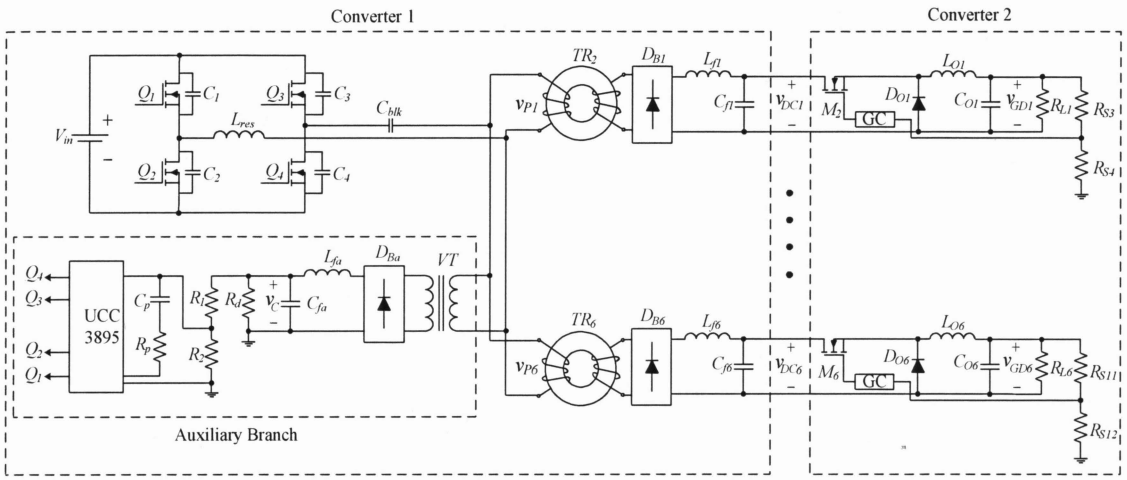
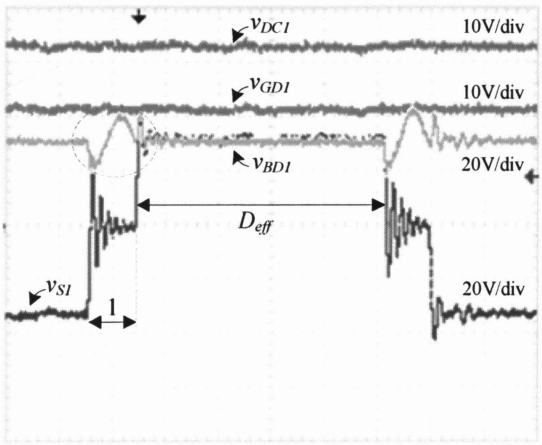


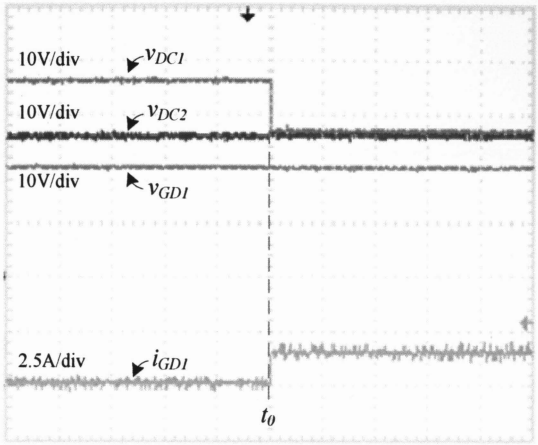
Fig. 4-8: Circuit diagram of PIPS for GCT gate drivers.

1. No-load to 50% of full-load

Fig. 4-9(a) depicts the voltage waveforms of one of the six isolated power supplies, where v_{S1}, v_{BD1}, v_{DC1}, and v_{GD1} denote voltage of the secondary side, the output recifier diode, the output of Converter 1, and the output of DC/DC Step-Down in Converter 2 in no load condition, respectively. Under no-load to 50% of full-load condition, only a small amount of energy is deliverd to the secondary side of the transformer, which is dissipated by the components on the PIPS board. The oscillation across the output rectifier diode during the interval is caused by the LC resonant circuit, which is formed by the leakage inductance of the transformer, the junction capacitance of the diode, and the output filter.



(a)



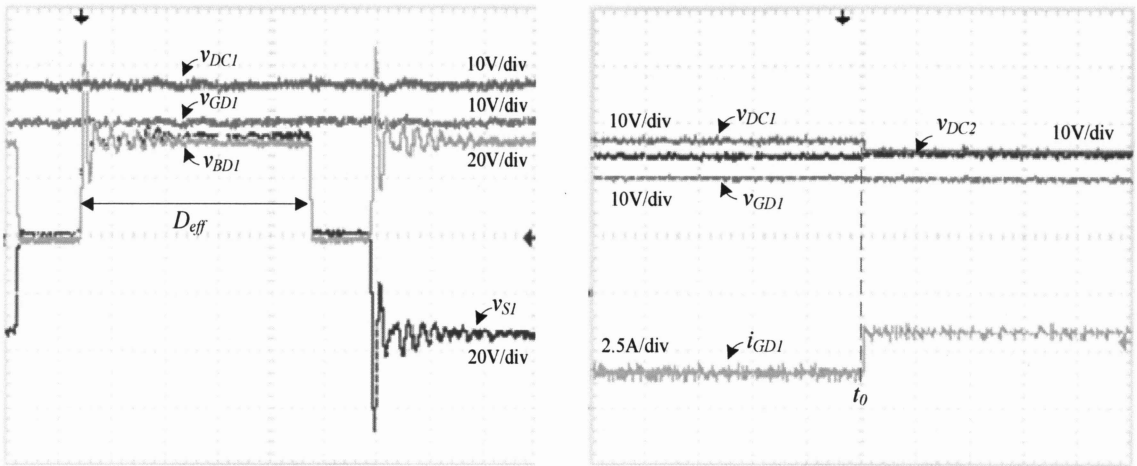
(b)

Fig. 4-9: Waveforms of PIPS (a) at no load; (b) at no load to 50% of full-load.

As observed in Fig. 4-9 (b), the load current i_{GD1}, one of the the six output currents, changes at t_0 from no load to 50% of full load, while the output voltage v_{GD1} of this power supply is regulated at 20V as the other output voltage (v_{GD2}-v_{GD6}). The load change of this power supply only affects the output voltage v_{DC1} of channel 1 in Converter 1 since there is no output voltage feedback. In no load condition, v_{DC1} is $35V$. At 50% of full-load, v_{DC1} steps down to $27V$, the same level as the output voltage v_{DC2} of channel 2 which is equivalent to the other output voltage (v_{DC3}-v_{DC6}).

2. 50% of full-load to rated-load

The output voltage waveforms of v_{S1}, v_{BD1}, v_{DC1} and v_{GD1} are displayed in Fig. 4-10 (a) at 50% of full-load. The ringing across the rectifier is affected by the leakage inductance of the transfomrer, the winding capacitance and the rectifier diode characteristics. This ringing occurs when the voltage rises in the secondary of the transfomrer. In a full-bridge rectifier, when the voltage is applied to the secondary, two of the rectifier diodes are reverse biased, and the leakage of the transfomrer rings with the diode capacitance and winding capacitances [17].



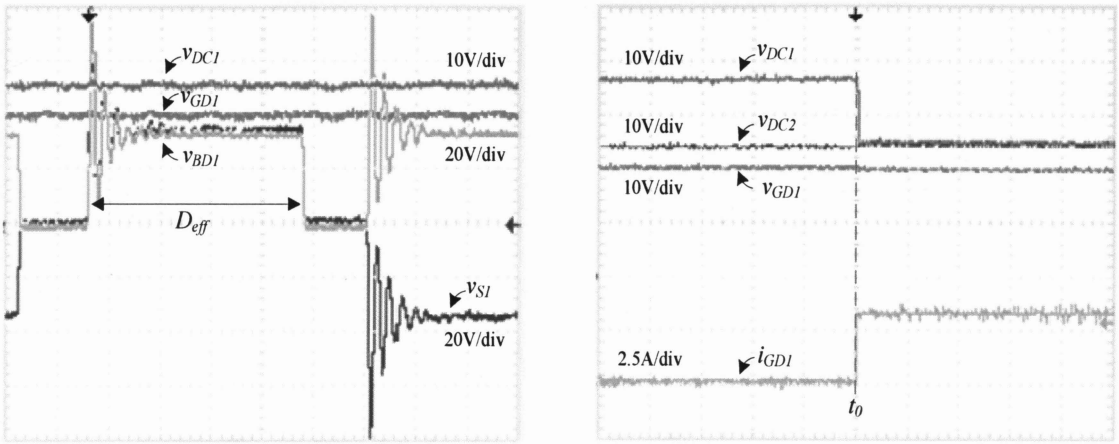
(a) (b)

Fig. 4-10: Waveforms of PIPS (a) at 50% of full-load; (b) at no load to 50% of full-load.

Fig. 4-10 (b) demonstrates that the load current changes from 50% to full-load at t_0 while the voltage (v_{GD1}-v_{GD6}) is regulated at $20V$. Before t_0, v_{DC1} is $27V$, which steps down to $25V$ after t_0, to the same level as the other voltage (v_{DC2}-v_{DC6}). The small step-up vlotage of around $0.6V$ on v_{DC2}-v_{DC6} at t_0 results from the small increase in the effective duty cycle on the secondary side of the transformer. However, the output voltage change on Converter 1 will not affect the output voltage of Converter 2 since the DC/DC Step-Down in Converter 2 will regulate the output voltage tightly.

3. No-load to rated-load

The output voltage waveforms of v_{S1}, v_{BD1}, v_{DC1} and v_{GD1} at full-load are depicted in Fig. 4-11 (a). The ringing and overshoot voltage across the secondary side and the rectifier are more severe at full-load compared to the two cases described above. This could potentially cause high voltage stress on the output rectifier diodes, and thus the fast recovery schottky diodes with voltage rating of more than twice the overshoot voltage were selected for this application. The ringing should not be snubbed since applying the six RCD snubbers degraded the efficiency by 2.4%. In addition, it resulted in heat dissipation, more number of components implying the need for a bigger PCB, and the extra cost on components. The RCD snubbers were therefore removed.



(a) (b)

Fig. 4-11: Waveforms of PIPS (a) at full load; (b) at no load to full-load.

As is obvious in Fig. 4-11 (b), the step load of i_{GD1} changes at t_0, while the output voltage of all six power supplies is regulated at $20V$. As a result, only v_{DC1} substantially reduces from $35V$ to $25V$ since there is no output feed back with respect to the load change at the output of Converter 1. The other output voltage (v_{DC2}-v_{DC6}) in Converter 1 is increased by $0.9V$ due to the same cause as explained above for the small step-up voltage.

4. Discussion

Based on the above observations, the load change of any one of the six parallel power supplies results in a large voltage step change on its own output voltage channel (v_{DC1}-v_{DC6}) in Converter 1, while causing a very small voltage change on other ouput voltage. In addition, the obtained experimental waveforms indicate that the output voltage of Converter 1 is unable to regulate a stable voltage from no-load to full-load because of the lack of output voltage feedback at Converter 1. In what follows, we demonstrate the importance of DC/DC Step-Down in Converter 2 for regulating the output voltage of each power supply, which would otherwise be poor and unacceptable, at very low cost. Under all load conditions and all given input voltage ($50V$ to $80V$ dc), PIPS can yield satisfactory voltage regulation of $20V$ dc for GCT gate drivers.

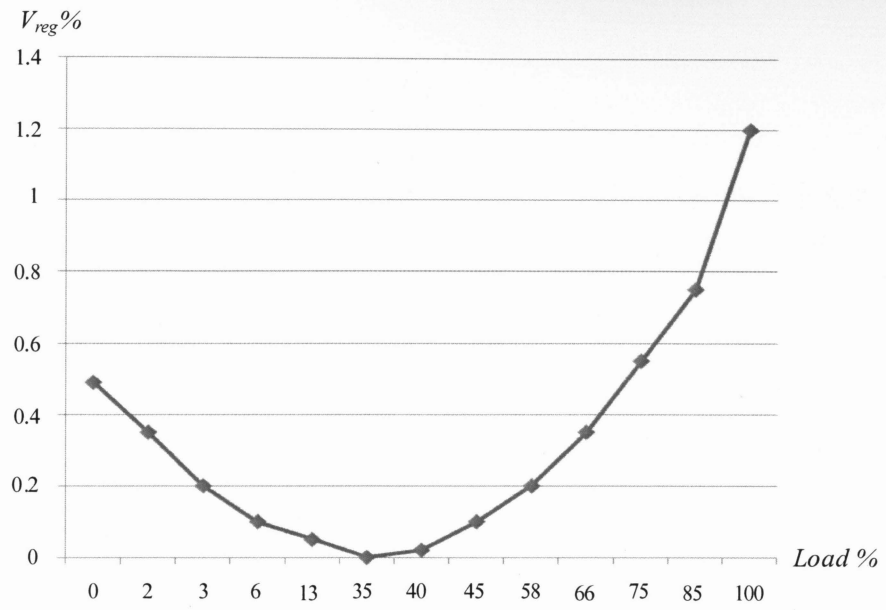


Fig. 4-12: Experimental voltage regulation of PIPS.

The voltage regulation graph of one of the six power supplies is illustrated in Fig. 4-10, under fixed input voltage of $55V$ dc and varying load (from no-load to full-load). Note that all six power supplies produce the same voltage regulation graph, and the voltage regulation of one power supply will not affect the others, regardless of load condition. At the full load of $60W$ (maximum output power of one DC/DC Step-Down), the output voltage of the DC/DC Step-Down converter slightly decreases by $0.25V$ due to the internal design of the TPS5430 and its operation at the maximum output power. It can thus be concluded that the voltage regulation discussed in this section is highly satisfactory for powering up the GCT gate driver.

4.3 Overall efficiency of PIPS

In this section, the ZVS design in the implemented system for all four MOSFET switches of the full-bridge converter is presented based on the design considerations discussed in Chapter 2. High efficiency of Converter 1 is indicated in the experimental results, which is due to the reduction of switching losses of the full-bridge converter contributed by the ZVS operation of MOSFET switches.

4.3.1 ZVS Design

The ZVS-PWM converter provides ZVS for the switches by using the leakage inductance of the transformer and the output capacitance of the switches. No extra component is required to realize ZVS. Now that the transformer has been designed, it is imperative to determine the ZVS transition times. This will allow the turn on delays to be set properly for ZVS to function. Therefore, the total equivalence leakage inductance reflected at the primary side of all six parallel transformers can be leveraged as resonance inductance to charge and discharge the capacitance of the MOSFET switches, during the ZVS operation for all four switches of the full-bridge converter. The total equivalence leakage inductance from the primary side of all six parallel transformers can be measured, based on the known leakage inductance of each transformer as describe below.

1. The resonant component selection

It is unnecessary to reduce the leakage inductance in the optimization of the transformer design, since the leakage inductance can facilitate ZVS operation. After completing the winding of the transformer, the primary equivalence leakage inductance of each transformer, equaling L_{eq1}, is measured which is around $8.5\mu H$ with ±2% error difference between the transformers. The total equivalence leakage inductance L_{eq} of all 6 parallel transformers is hence around $1.4\mu H$ ($L_{eq} = \frac{L_{eq1}}{6}$). This leakage inductance is enough to achieve ZVS operation for all 4 MOSFET switches in the phase-shift full-bridge converter without extra external inductance.

The MOSFET must be selected carefully, especially for MOSFET with low output capacitance (C_{OSS}), in order to reduce the total energy storage required in the leakage inductance to charge/discharge the output capacitance of the MOSFET and to ensure ZVS, as is presented in Eq. (2-4). In addition, the ON-resistance of the MOSFETs should be as low as possible to obtain high efficiency. After cautious comparison of many different MOSFETs for the given maximum current/voltage, the IRFP250 is chosen which has low ON-resistance and output capacitance

C_{OSS}. The IRFP250 has $R_{DS(on)} = 0.075\Omega$ and $C_{OSS} \leq 300pF$ at $V_{DS} = 50V$, derived from the datasheet.

2. ZVS design in the implemented Converter 1

In the implemented power supply, IRFP250 MOSFETs are used as the switching element in the phase-shift full bridge (PS-FB) of Converter 1. The turns ratio for the transformer is 1.75. The equivalence leakage inductance of the transformer is $1.4\mu H$, where the equivalence capacitance of the transformer is assumed to be at the worst case of its value of $120pF$. The equalities given in Chapter 2 can be simplified and leveraged for determining the ZVS design in this section. Some specifications are listed as follows:

$$
\begin{aligned}
&V_{in(\max)} = 80V \\
&C_{OSS} = 300pF \\
&C_{TR} = 60pF \\
&N = 1.75 \\
&L_{LK} = 1.4\mu H
\end{aligned}
\qquad (4\text{-}1)
$$

The resonant capacitance can be calculated by:

$$C_{eq} = \left[\left(\frac{8}{3}C_{OSS}\right) + C_{TR}\right] = \left[\left(\frac{8}{3}\times 300\times 10^{-12}\right) + 120\times 10^{-12}\right] = 707pF \qquad (4\text{-}2)$$

It is more important to maintain ZVS at higher loads for two reasons. The first and apparent reason is that the switching losses are greatly reduced. The other reason is the minimum free-wheel time during full-load. Consequently, the circulation of the reflected load current during the free-wheel time is shortened thereby reducing the $R_{DS(on)}I^2$ losses in free-wheel circulation path [33]. In lighter load conditions, the power dissipation in the MOSFET switches should be trivial if the switching losses appear due to the smaller primary currents during lighter loads.

Recall that the design goal was to maintain ZVS operation down to one fourth of the maximum output power ($90W$). The minimum primary current required for the phase shifted application can be determined by applying Eq. (4-3) to the values given in Eqs. (4-1) and (4-2).

$$I_{P(\min)} = \sqrt{\frac{C_{eq} \times V_{in}^{\ 2}}{L_{LK}}} = \sqrt{\frac{707 \times 10^{-12} \times 80^2}{1.4 \times 10^{-6}}} = 1.8A \qquad (4\text{-}3)$$

The minimum primary current for maintaining the ZVS switching is 1.8A. The following calculation is performed in terms of the output power:

$$I_{o(Critical)} = \frac{N_P}{N_S} \times 1.8 = 3.15A$$

$$P_{o(Critical)} = 3.15 \times 20 = 63W$$

The power at which the supply stops zero-voltage-switching is $63W$, well below one fourth of $P_{o(max)}$, satisfying the design requirements.

The left leg transition can be calculated using Eq. (4-4) by substituting the values derived from Eqs. (4-1) and (4-2) as follows:

$$t_{LL} = \frac{\pi}{2}\sqrt{L_{LK} C_{eq}} = 50nS \qquad (4\text{-}4)$$

Now that the resonant inductor and left leg transition time have been selected, the right leg transition time needs to be determined. It turns out that the maximum right leg transition time occurs during the maximum input voltage and at a load boundary called the ZVS operational limit. The ZVS opeationtional limit refers to the point at which the power supply no longer maintains zero voltage switching.

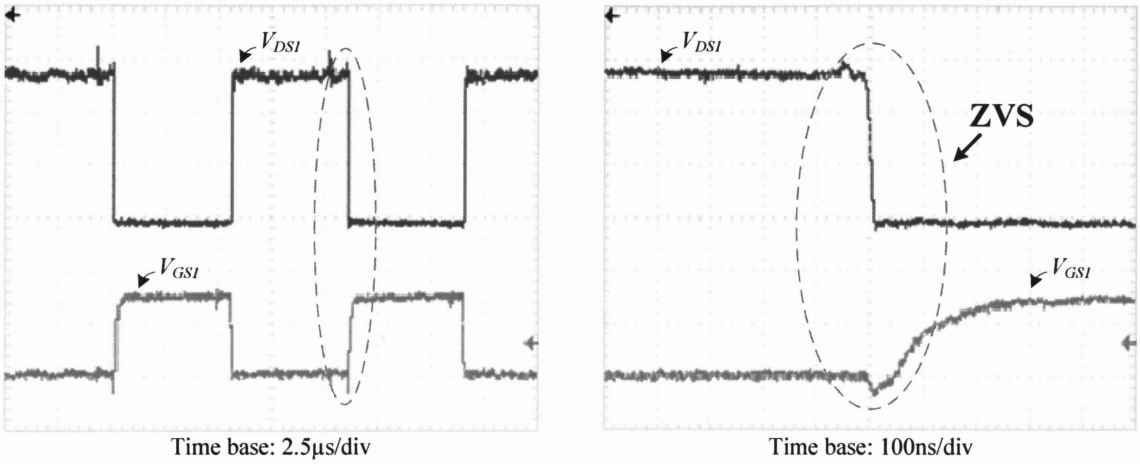
The right leg transition is determined by subsitiuting the values from Eqs. (4-1), (4-2), and (4-3) in Eq. (4-5) as:

$$t_{RL} = \frac{C_{eq} V_{in}}{I_{P(critcal)}} = 18nS \qquad (4\text{-}5)$$

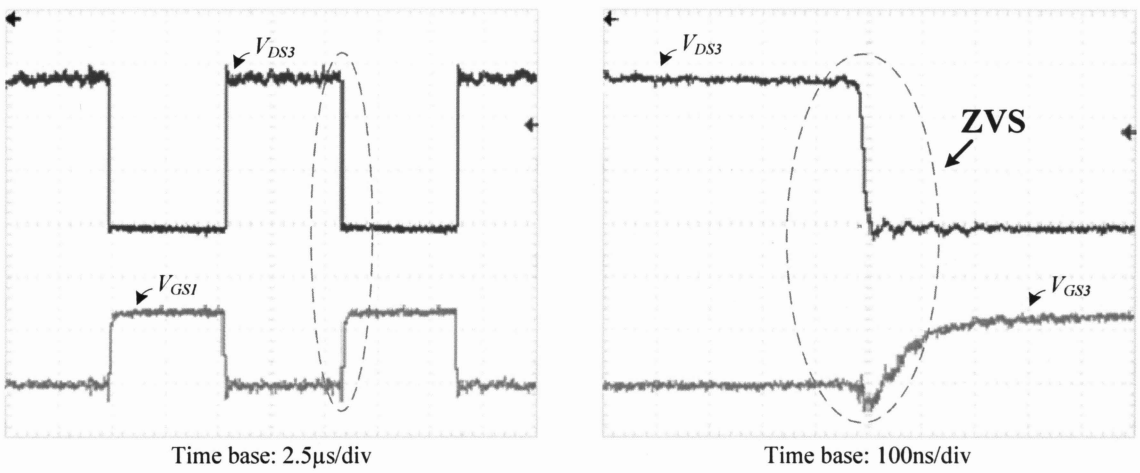
The left-leg and right-leg transition takes $50nS$ and $18nS$, respectively. These values are programmed as the turn on delay via the left-leg delay (R_{DELAB}) and right-leg delay (R_{DELCD}) resistor values on the UCC3895. The MOSFET turn-on and turn-off delays can be found from its datasheet.

3. Verification of switching loss reduction

It is crucial to observe the ZVS operation in the MOSFET switches of Converter 1, since the ZVS operation is an indicator of switching loss reduction. To demonstrate the state of ZVS for Converter1, we place one switch on the leading-leg and one on the lagging-leg, thereby showing the ZVS of all four switches. Fig. 4-11 (a) illustrates the output voltage V_{DS1}, and the gate voltage V_{GS1}, of switch Q_1 on the leading-leg. Similarly, Fig. 4-11 (b) depicts V_{DS3} and V_{GS3} of Q_3 on the lagging-leg at $360W$ maximum output power. Note that in Figs. 4-9(a) and 4-9(b), V_{DS} tends to zero before V_{GS} approaches high, which indicates that the body diode is on before the turn-on of the switch. All the switches are turned on under "soft switching", or zero voltage switching, where V_{DS} tends to zero before V_{GS} goes high. The experimental results show that the ZVS operation can be maintained from full-load to almost one fourth of full-load.



(a)



(b)

Fig. 4-13: Experimental waveforms of ZVS (a) leading-leg; (b) lagging-leg.

The converter can thus work with higher switching frequency and higher efficiency. Due to the ZVS operation, the primary side waveforms are free from high switching noise and no snubber is required.

4. Discussions on efficiency

The experimental results manifest the fact that the switching losses are decreased when Converter 1 is operating at ZVS, giving rise to increased efficiency. It indicates that ZVS

successfully combines the benefits of lossless switching transitions and high efficiency operation.

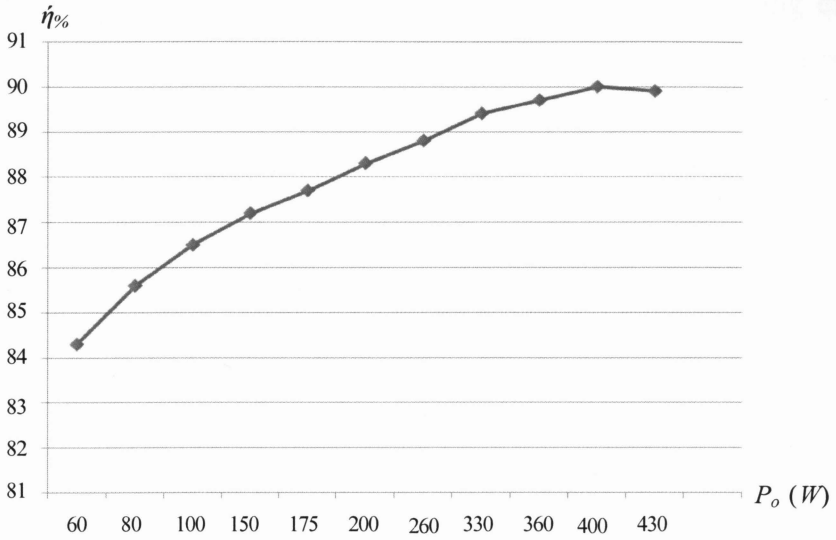


Fig. 4-14: Efficiency curve of Converter 1.

The efficiency curve of Converter 1 under different load operations is displayed in Fig. 4-12. For loads above $300W$, the efficiency of Converter 1 remains above 89% or more. The peak efficiency is over 90.1% with loads in between $400W$ and $415W$. After the peak, a sign of tailing-off at the upper end of the efficiency graph for loads above $420W$ can be observed. This is due to the increases in the conduction losses of the MOSFET and output rectifier diode at higher current.

4.4 Summary and Discussion

A laboratory prototype of the proposed parallel isolated power supply (PIPS) at power rating of $360W$ is designed and built. Various experiments were carried out for the proposed PIPS operating under different input/load conditions, to verify the performance of PIPS for the GCT gate driver. The optimization of the toroidal transformer turns ratio is incorporated to reduce the amount of wiring, which would assist in increasing the possibility of meeting the Corona requirements (voltage isolation more than $9kV$ for GCT gate drives in MV applications). The

resultant efficiency of the main dc/dc converter, Converter 1 in PIPS, is above 89.5% at $360W$, the required power to supply six GCT gate drivers. It can be concluded that the proposed PIPS can satisfactorily operate under the rated and no-load conditions, while regulating $20V$ dc for GCT gate drivers, and a majority of the intended goals are met including efficiency, power density, line and load regulation. Moreover, PIPS features low manufacturing cost, high voltage isolation level, high output power ($360W$), and small physical size, which are the key considerations for industrial adoption.

CHAPTER 5: CONCLUSION

As the concluding chapter, Chapter 5 summarizes and highlights the main contributions and important results of this thesis, with future work also pointed out.

5.1 Summary

The commercial dc power supply for the GCT gate driver must be able to withstand a few thousand volts between the input and output, rendering the power supply an expensive device resulting in low cost efficiency. In addition, the high-voltage isolation transformer normally employed to provide an electrical insulation between the power supply and system ground, is high in cost and physical volume. To enhance the cost and volume efficiency, a novel parallel isolated power supply (PIPS) is proposed in this thesis for powering up six GCT gate drivers in one module, where six is the minimum number of GCT devices in medium voltage (MV) applications. PIPS is supplied from the input dc rectifier at $50V$ to $80V$. Each power supply of PIPS can provide a regulated 20V dc for GCT gate drivers with high electrical isolation levels of up to several kilo-volts. The PIPS design features a general power supply which can be used (by slightly changing the output specification of PIPS) for powering up the gate drivers of all types of GCT devices (symmetrical and asymmetrical) in all MV applications (CSR, CSI, etc.).

The transformer with high voltage isolation level for the GCT gate driver is the most expensive item. The cost of the transformer can be reduced by the optimization procedure that is elaborated in Chapters 2-4. The optimization procedure for the high voltage isolation level transformer is imperative because the transformer must provide an isolation level of up to several kilovolts for GCT devices, at low cost and small size. It is shown through the descriptions of the optimization procedure that the potting of the toroidal transformer can be eliminated, and the costs on both potting and the expensive/bulky commercial power supply are substantially saved.

The main challenge to design the proposed power supply for GCT gate drivers stems from the design of Converter 1 integrating the phase-shift full bridge (PS-FB) and six parallel

transformers. In order to optimize a low-cost and compact sized transformer with high voltage isolation level required for GCT gate drivers, the transformer must operate at both high frequency and efficiency. Therefore, it is indispensable for the phase-shift full-bridge (PS-FB) to employ zero voltage switching (ZVS) for all four MOSFET switches to operate at high frequency of $165kHz$. The adoption of ZVS also delivers a maximum output power of 360W for the six GCT devices at an efficiency of 89.5%, rendering the optimized transformer a feasible solution for high voltage isolation levels of more than $9kV$.

5.2 Contributions

The development of a simple, robust, and cost effective power supply for GCT gate drivers represents the key contribution of this thesis, which can be specified as follows:

1. **A novel parallel isolated power supply (PIPS) for all types of GCT gate diver is designed and developed.** The propsed design achieves a general power supply with high efficiency, in terms of cost, size, and functional operations, for powering the gate drivers of all types of GCT devices (symmetrical and asymmetrical) used in different converter topologies where high voltage insulation level is required, e.g., Medium Voltage Neutral Point Clamped to PWM CSI converters.

2. **A low-cost and compact-sized transformer with optimized design for the GCT device and high voltage isolation of more than several kilovolts.** The most important part in the development of the proposed power supply is the transformer design, where the optimization is imperative because the transformer must produce an isolation level of up to several kilovolts for GCT gate drivers, at low cost and small size. Specifically, the optimization of the high voltage isolation level transformer is carried out to reduce the number of primary and secondary winding turns, and to provide large distance gap between the primary and secondary winding, satisfying the Corona requirements (e.g., voltage isolation level higher than 9KV). The key benefit from obtaining the optimized transformer, is the elimination of the high voltage isolation transformer commonly used in commercial GCT gate driver power supplies, giving rise to remarkable reduction in both manufacturing cost and physical size.

3. **The maximum power requirement for the six GCT gate drivers is fulfilled with high efficiency.** The proposed PIPS can provide an output power of up to $360W$ for six GCT devices while operating at a switching frequency of $165kHz$. This has been made possible by employing zero voltage switching (ZVS) for the main converter within the power supply. When PIPS operates in ZVS, the switching losses are suppressed and hence the efficiency of higher than 89.5% can be attained for the proposed converter.

4. **Simulation models and the prototype of the proposed PIPS are developed.** The performance of the proposed PIPS is investigated leveraging the simulations. To verify the feasibility and efficiency of the proposed PIPS, a laboratory prototype has been implemented and tested. The comprehensive experimental results manifest that the proposed PIPS can satisfactorily meet the technical requirements for GCT gate drivers.

In summary, due to the higher efficiency of our design in terms of cost, size, design complexity, and functional operations of the proposed PIPS, it is reasonable and practical to consider our power supply as a substitute for the more complex, higher cost, and larger sized high voltage isolation transformer, which requires an additional DC/DC converter for its input voltage but is currently prevailing in the industrial applications.

5.3 Future Work

This thesis focuses on the development of six parallel isolated power supplies on one module to power up the minimum six GCT devices employed in an MV application. Nevertheless, there are possibilities of adding another six parallel isolated power supplies to the PS-FB in Converter 1 of PIPS. As mentioned in Chapters 2, the front-end DC/DC converter PS-FB in Converter 1 has the power handling capability more than $1kW$, enabling one module of the power supply to provide the power required for 12 GCT devices in MV applications. This a major advantage of the design discussed in the thesis, where the minimum number of components can supply an additional six GCT devices, contributing to 12 GCTs in total. The implementation and testing of the 12 GCT devices in one module constitute our future work, where special considerations on high voltage

isolation PCB design for GCT gate drivers must be taken, the reason being that in such design, the PCB must be developed with cautions in order to meet the electrical isolation requirement for GCT gate drivers for more than $9kV$.

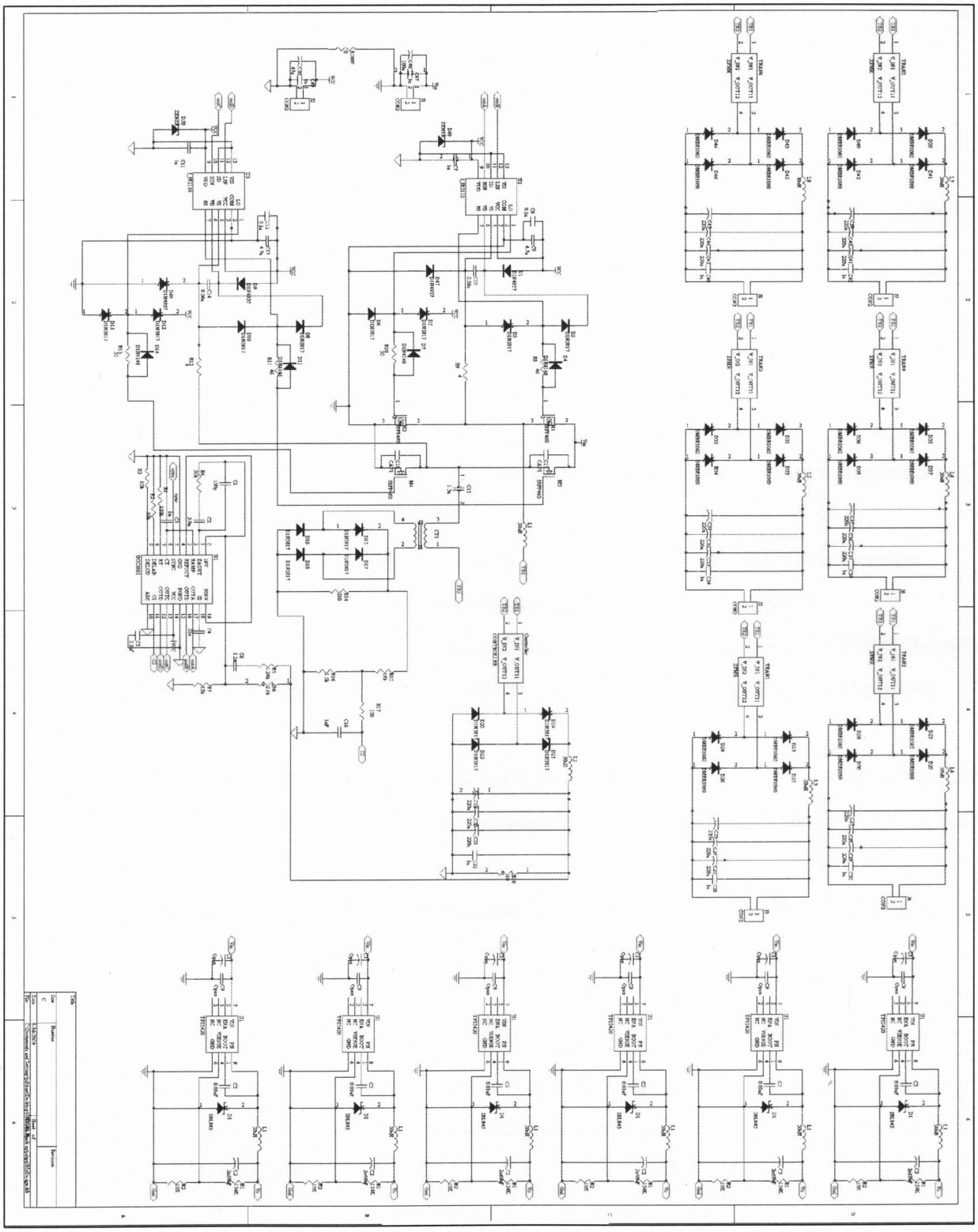
APPENDIX

A. Experimental Results on Toroidal Transformer

Item #	Part #	$A_e\,[mm^2]$	$f_{TR}\,[kHz]$	$B_m\,[mT]$	$P_{fe}\,[W]$	$\Delta T_{Rise}\,[^\circ C]$	N_p/N_s
1	43610TC	62.6	75	200	1.44	37.5	14/7
2	43610TC	62.6	100	200	2.47	57.2	10/5
3	43615TC	95.9	75	200	2.17	53.5	9/5
4	43615TC	95.9	100	200	3.71	64.2	7/4
5	43825TC	231	75	100	0.82	13.1	8/4
6	43825TC	231	95	120	1.37	19.6	7/4
7	43825TC	231	110	120	1.52	21.3	6/3
8	43825TC	231	125	120	2.5	26.4	5/3
9	43825TC	231	135	120	2.9	28.7	4/2
10	43825TC	231	165	130	4.1	36.3	3/2

B. Schematic of the Parallel Isolated Power Supply Prototype

Fig. B-1 Schematic of the parallel isolated power supply prototype.



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