

FIVE-LEVEL NPC INVERTER FED BY DUAL 18-PULSE RECTIFIER FOR HIGH-POWER DRIVES

by

Zhongyuan Cheng

Bachelor of Engineering, Xi'an Jiaotong University, China

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Five-Level NPC Inverter Fed by Dual 18-Pulse Rectifier
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ABSTRACT

This thesis focuses on the topology of multi-pulse rectifiers and the modulation technique of multilevel inverters for high-power medium voltage drives. A dual 18-pulses rectifier topology is proposed. The topology achieves harmonic performance of 36-pulse rectifiers by using relatively simple 18-pulse transformers. It can also neutralize the 5th and 7th harmonics caused by unbalanced secondary windings. Moreover, a novel space vector modulation (SVM) algorithm with flexible three-segment switching sequence is proposed for multilevel inverters. It features: 1) minimized device switching frequency, 2) lower weighted total harmonic distortion due to the increase of the inverter sampling frequency, and 3) easy implementation thanks to the simplified sequence design. The algorithm is applicable to various multilevel inverter topologies.

Theoretical analyses and computer simulations are carried out for the proposed topology and algorithm. The harmonic performance is verified by experiments on a 10kVA 5-level NPC/H-bridge inverter fed by a dual 18-pulse rectifier.

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NOMENCLATURE

Generic Variable Usage Conventions

Variable Format	Meaning
F	CAPITALS: peak AC, rms AC or average DC value
f	LOWER CASE: instantaneous value
[., ., .]	SQUARE BRACKETS: switching states
(., ., .)	PARENTHESES: coordinate triple, 3-phase instantaneous values
AB	BOLD CAPITALS: vector with tail A and tip B
f	BOLD LOWER CASE: vector

Specific Variable Definitions

Variable	Meaning
a, b, c, o	inverter output terminals; transformer secondary terminals
(a, b, c)	three phase variables
A, B, C	transformer primary terminals
C	DC link capacitance
D_A, D_B, D_C, D_D	duty cycles
E, E_1, E_2, E_3	step voltage; isolated DC voltages
f_1	fundamental frequency
f_{extra}	extra switching frequency
f_{inv_sp}	inverter sampling frequency (the center frequency of the 1 st sideband in spectra of line-to-line voltage)
f_{sp}	sampling frequency of space vector modulation algorithms
f_{sw_actual}	actual average device switching frequency
f_{sw_ideal}	ideal average device switching frequency
(g, h)	hexangular coordinates
(g_0, h_0)	hexangular coordinates of the base vertex
h	harmonic order
i_1, i_2	currents of different secondary windings of PSTs
i'_1, i'_2	induced currents of i_1, i_2
i_A, i_B, i_C	3-phase currents at the primary side
i_a, i_b, i_c	3-phase currents at the secondary side
$i_{aY} (i_{a\Delta})$	instantaneous current of Y (Δ) windings
$i'_{aY} (i'_{a\Delta})$	instantaneous current of Y (Δ) windings referred to the primary side
I_{ces}	collector-emitter cut-off current of IGBTs

i_r, i_s, i_t	secondary coil currents of zigzag transformers
i_X, i_Y, i_Z	primary coil currents of zigzag transformers
k_v	primary to secondary voltage ratio
L_s	total mains-side inductance
(m, n)	local coordinates in the vector plot
m_a	amplitude modulation index
m_f	normalized sampling frequency of SVM
$N_1, N_2, N_p, N_{p\Delta}, N_{pY}, N_{s1}, N_{s2}$	number of turns
p	number of pulses
R_s	total mains-side resistance
S	state value; switching function; power capacity
$[S_a, S_b, S_c]$	3-phase switching states
S_{ao}, S_{no}	switching states of NPC arms
T_a, T_b, T_0	dwell times
THD	total harmonic distortion
T_s	sampling period ($T_s = 1/f_{sp}$)
u, v	unit vectors
V_1, V_2, \dots, V_7	stationary vectors of 2-level inverters
$V_{1rms}(V_{hrms})$	rms value of the fundamental (h^{th} harmonic)
V_{1rms_max}	maximum rms value of the fundamental
(v_a, v_b, v_c)	3-phase voltages
v_{ab}	line-to-line voltage
v_{an}	phase A voltage with respect to the 3-phase neutral n
$v_{ao}(v_{no})$	voltage of NPC arm with respect to the DC neutral
V_d	DC link voltage; rectifier output voltage
V_{ref}	reference vector
V_{ref}	magnitude of the reference vector
(v_α, v_β)	coordinates of (α, β) plane
w	number of secondary windings
$WTHD$	weighted THD
ΔS	total state value change
δ	phase shift angle
δS	phase state value change
γ	arbitrary angle
θ	argument of the reference vector
ω	angular frequency

CHAPTER 1 INTRODUCTION

1.1 Overview

High-power medium voltage (MV) motor drives have been used increasingly in industry and there is still much room for the growth because only 3% of the currently installed MV motors are controlled by drives^[1].

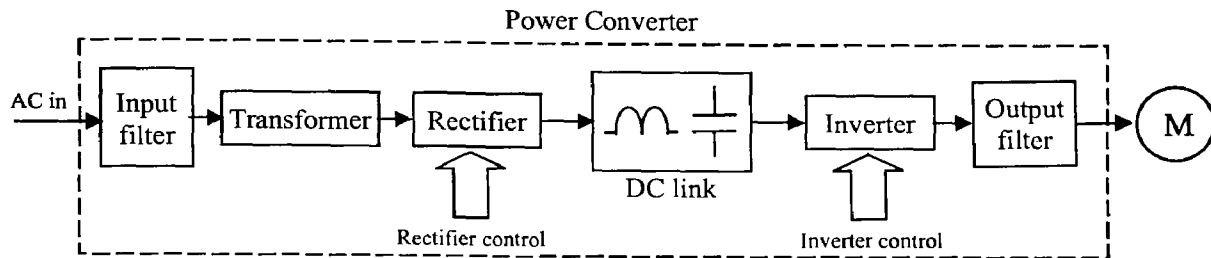


Fig.1-1 General topology of MV motor drives.

Fig.1-1 shows the block diagram of an MV motor drive. The AC power drawn from the utility is converted by the power converter and supplies the motor in whatever voltage, current and frequency necessary to achieve the desired mechanical performance. The converter includes the optional input/output filters, the transformer, the rectifier, the DC link and the inverter. The DC link may be a group of capacitors if the inverter is voltage source based, or reactor if it is current source based. The transformer normally has multiple phase-shifted secondary windings and accounts for a significant part of the drive cost. Depending on whether it is an active or passive rectifier, the converter may or may not have the rectifier control, but it always has the inverter control. The inverter control is important for the drive to generate desirable waveforms for the motor.

The technical requirements and challenges of MV drives mainly come from the following origins^[1]: the power quality requirements of the utility, the inverter design and control, the requirements of the interface with the motor, and system requirements of the drives.

To meet the utility-side power quality requirements, phase-shifting transformers (PSTs) and multi-pulse rectifiers are used more and more often to limit the line current distortion and

improve the power factor^{[1]-[7]}. At the inverter stage, the multilevel topology provides good opportunities to generate high-quality waveforms and to increase the inverter voltage to MV level (up to 6kV) with limited device voltage ratings^{[1][5][9]-[18]}.

While taking advantage of the harmonic cancellation, the better-shaped output waveforms, and the higher inverter voltage brought by multi-pulse rectifiers and the multilevel inverters, one should keep in mind that high-pulse PSTs are expensive and the control of multilevel inverters are very complex.

The thesis focuses on the simplification of the front-end topology and the improvement of the modulation techniques of multilevel inverters.

1.2 Multi-Pulse Rectifiers

The term ‘multi-pulse’ probably comes from the multiple humps per fundamental cycle in the rectifier output. For a conventional 3-phase rectifier there are 6 humps thus it is in fact a 6-pulse rectifier. Similarly we have other multi-pulse rectifiers, such as 12-, 18- and 24-pulse rectifiers. For convenience, the PST powering a p -pulse rectifier is called a **p -pulse transformer** or **p -pulse PST** in the thesis.

The motivation of the adoption of multi-pulse rectifiers is to meet the harmonic regulations set by IEEE Standard 519-1992^[8] and its European counterpart IEC 1000. For example, the current distortion limit set by IEEE 519-1992 for power converters is 5% of the maximum demand load current (15- or 30-minute demand), which can not be achieved by 6-pulse rectifiers.

The simplest multi-pulse rectifier for harmonic cancellation is the 12-pulse rectifier shown in Fig.1-2. There are two 6-pulse diode rectifiers whose DC outputs are connected in series. The rectifiers are powered by the two secondary windings of a 12-pulse PST. One of the secondaries is in Y-connection, the other in Δ . If the phase angle of the primary line-to-line voltage is used as the reference, the phase-shifting angle of the Y-secondary is $\delta=0^\circ$ and that

of the Δ -secondary is $\delta=30^\circ$. The secondary terminal currents, i_{aY} and $i_{a\Delta}$, are referred to the primary as i'_{aY} and $i'_{a\Delta}$, the sum of which is the primary current i_A .

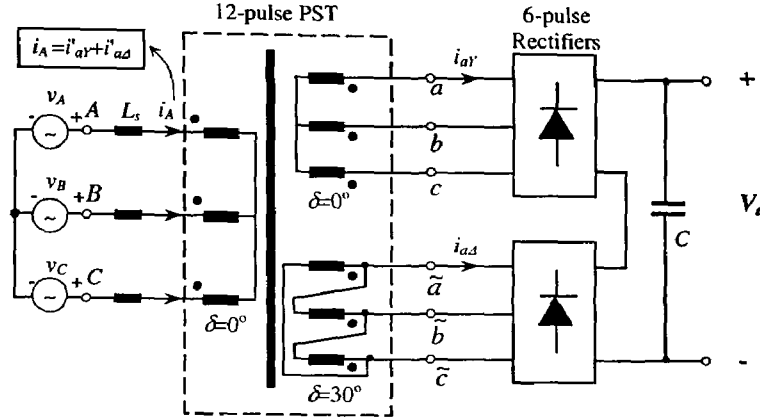


Fig.1-2 Topology of 12-pulse rectifier

Some of the harmonics in i'_{aY} can neutralize those of $i'_{a\Delta}$, leading to lower THD of i_A . Fig.1-3(a) shows the waveforms of i'_{aY} , $i'_{a\Delta}$ and i_A when the DC load is 0.5p.u., the total supply-side inductance $L_s=0.15$ p.u. The waveform of i_A is more sinusoidal than both of i'_{aY} and $i'_{a\Delta}$. Fig.1-3(b) shows the spectra of the currents. Currents i'_{aY} and $i'_{a\Delta}$ have the same spectra, but some of the harmonic contents are 180° out of phase and cancel each other. As a result, these harmonics, such as 5th, 7th, 17th and 19th, disappear in the spectra of i_A . The THD of i_A is about 9%, compared to 25% of i'_{aY} and $i'_{a\Delta}$.

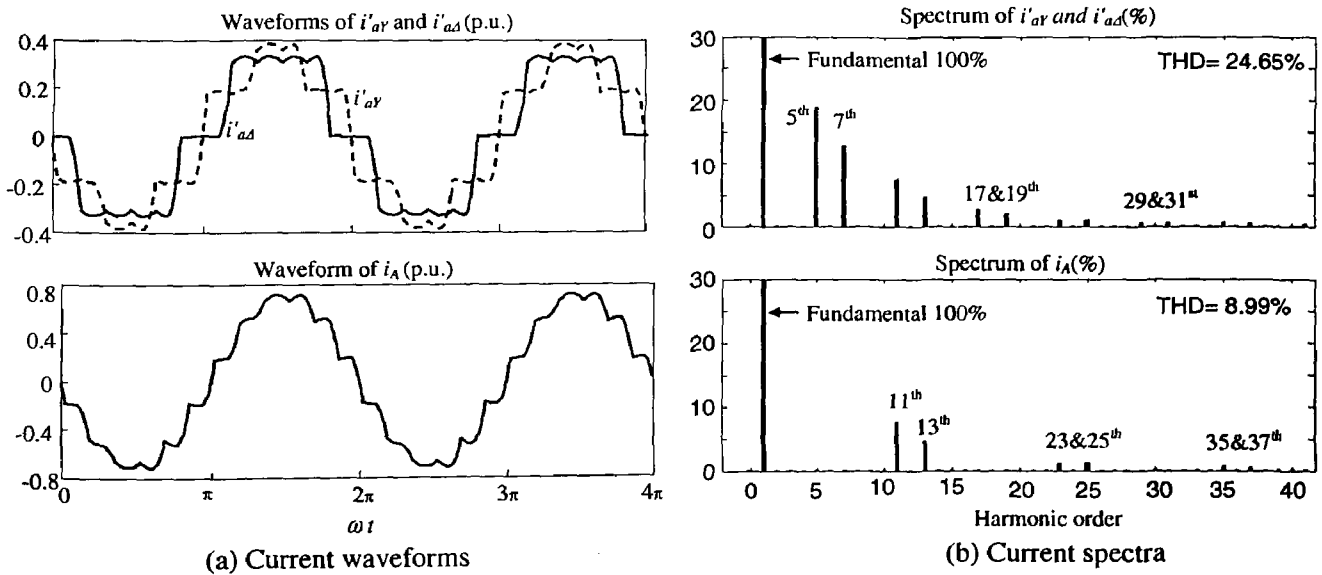


Fig.1-3 Current waveforms and spectra of 12-pulse rectifier

Harmonic cancellation can be further enhanced by PSTs with higher number of pulses. Fig.1-4 shows the typical topology of an 18-pulse rectifier. There are 3 identical 6-pulse rectifiers power by a PST with 3 secondaries. The secondaries of the PST are connected in Δ or extended- Δ , producing phase-shifting angles of 20° , 0° and -20° respectively. Similar to the case of 12-pulse rectifier, some harmonic contents are absent in the spectrum of primary current and the lowest order harmonic is now the 17th.

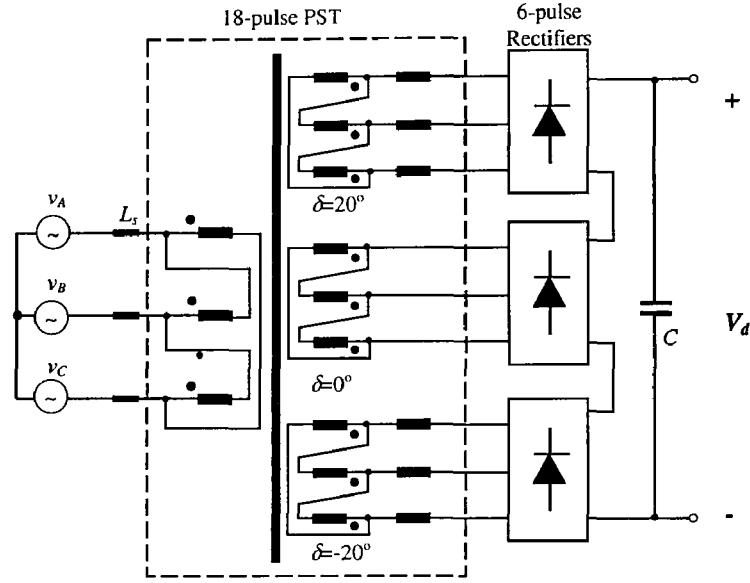


Fig.1-4 Topology of 18-pulse rectifier

Table 1.1 Harmonic cancellation patterns of multi-pulse rectifiers

$\begin{matrix} h \\ p \end{matrix}$	5 th	7 th	11 th	13 th	17 th	19 th	23 rd	25 th	29 th	31 st	35 th	37 th	41 st	43 rd	47 th	49 th
12	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled
18	cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled
24	cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled	not cancelled	cancelled
30	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled
36	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled	Cancelled

Note: h : the harmonic order

Generally, for a p -pulse rectifier, the harmonics lower than $(p-1)^{\text{st}}$ order can be cancelled. Table 1.1 summarizes the cancellation patterns^[1]. Larger p results in better cancellation. For rectifier with 5% per unit (p.u.) supply-side inductance and 0.80 p.u. load current, the input current THD is about 35% for 6-pulse rectifiers, 9% for 12-pulse, 3.8% for 18 pulse and 1.7% for 24-pulse^{[1][2]}. It can be expected that higher-pulse rectifiers have even better performance.

Multi-pulse rectifiers are commonly used in high-power converters, especially for multilevel converters, which is to be introduced in the next section.

1.3 Multilevel Inverters

Multilevel inverters are used to meet the requirements coming from the motor side. As mentioned before, one of the major advantages of multilevel inverters is the high inverter voltage they can achieve. The inverter voltage is decided by the voltage ratings of the switching devices. The majority of the MV drives from 1MW to 4MW work at 3.3kV to 6.6kV voltage levels. However, the voltage ratings of the switching devices are often limited. For MV drives they are often rated at 6kV for GTO/GCT, 1.7kV, 2.5kV, 3.3kV, 4.5kV or 6.5kV for IGBTs.

There are generally three methods for higher inverter voltage: connecting devices in series, using switching devices with higher voltage rating, or adopting multilevel topology. The first method can be used only when the problem of dynamic voltage sharing has been efficiently solved. Otherwise it should be avoided. The choice of the second and third methods is really a complicated compromise of the cost, reliability and availability. Given limited device voltage ratings, the most effective solution to higher inverter voltage is multilevel topologies.

Other benefits coming with multilevel topology include lower output THD, lower dV/dt which is beneficial to the motor and increased EMC. However these features are not in the scope of the thesis and will not be discussed in detail.

1.3.1 NPC Inverters

Among the other multilevel topologies, the 3-level neutral point clamped (NPC) topology, which was first proposed by Nabae et al^{[12][14]}, has been widely used.

Fig.1-5 shows the topology of the NPC inverter, where only one DC source V_d is needed. Two capacitors are used to split the DC voltage and provide a neutral point o . Each phase

contains 4 active switches, S_{k1} to S_{k4} , and 2 clamping diodes D_{k1} and D_{k2} , $k=a, b$ or c . The 4 switches are controlled as two complementary pairs. For example, switches S_{a1} and S_{a3} , S_{a2} and S_{a4} are complementary pairs. Each phase can be connected to three potentials: $+V_d/2$, 0 or $-V_d/2$.

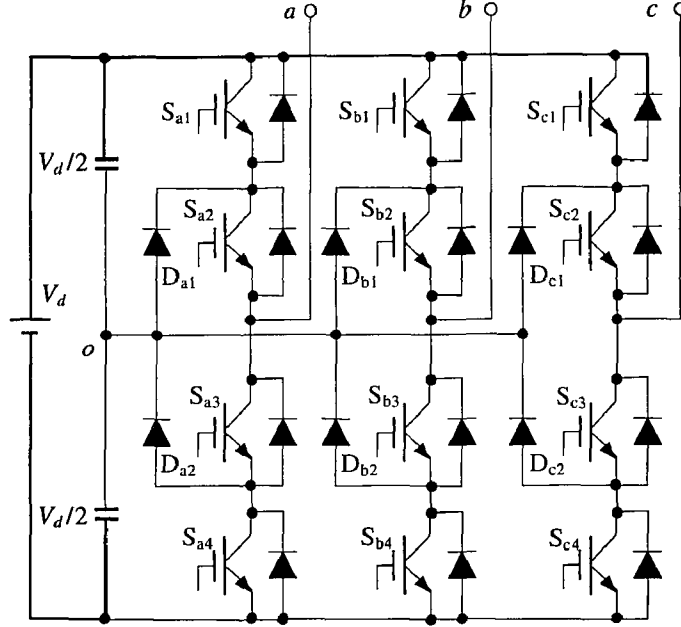


Fig.1-5 Three-level NPC inverter

The maximum *rms* value of the fundamental of the line-to-line voltage V_{1rms_max} is the same as that of the 2-level inverters. For SPWM modulation, it is

$$V_{1rms_max} = 0.5 \frac{\sqrt{3}}{\sqrt{2}} V_d = 0.61 V_d. \quad (1.1)$$

Compared to 2-level inverters, the main feature of NPC inverter is that it can achieve higher inverter voltage. This is because the maximum voltage for each device in the NPC topology is $V_d/2$, while it is V_d in a 2-level topology. For example, if the motor voltage is 2.3kV, the DC link voltage can be calculated to be around 3.3kV. For 2-level topology it requires switching devices rated at around 6.6kV, which hits the 6.5kV upper limit of device voltage ratings (for IGBT) in the market place. If the 3-level NPC topology is used, each switching device blocks only 1700V. Less expensive 3.3kV devices can be used without series connection.

For 3.3kV IGBTs, the highest inverter voltage of the NPC topology can achieve is 2.3kV. If the inverter voltage is more than 2.3kV, for example 3.3kV, the device voltage rating should be more than 5.4kV in the NPC topology. However the voltage of the MV drives is often higher than 2.3kV, with most of them being at 4.16kV level. For the inverters with 4.16kV output voltage, the device rating will be more than 6.8kV for the NPC topology. In other words, if the motor voltage exceeds 2.3kV, the 3.3kV IGBT-base NPC topology can not be used.

1.3.2 NPC/H-Bridge Inverters

NPC/H-bridge inverters is designed for inverter voltage higher than 2.3kV. It can achieve up to 4.16kV inverter voltage with 3.3kV IGBTs.

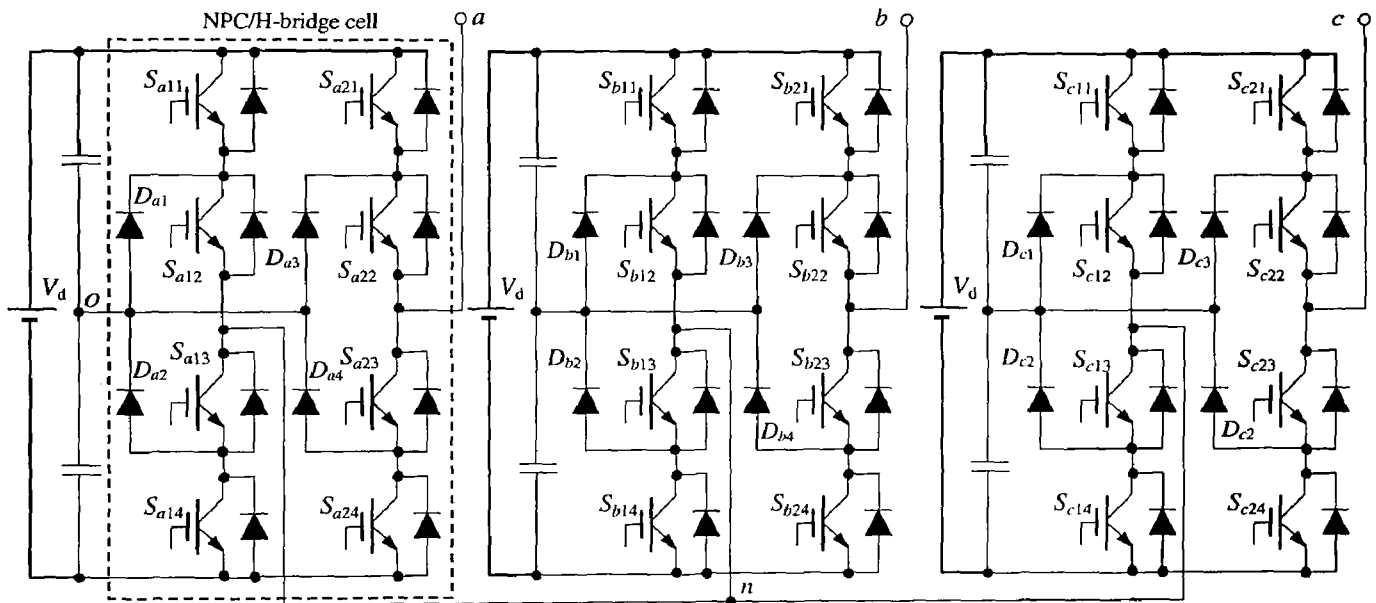


Fig.1-6 Five-level NPC/H-bridge inverter.

Fig.1-6 shows the topology of an NPC/H-bridge inverter. Each phase is an NPC/H-bridge cell composed by two NPC arms. The 4 switches of each NPC arm operate similarly to the NPC inverters. Every phase is powered by an isolated DC source, which is split into halves by capacitors. The NPC arms are 3-level and the difference of the two arms, which is the phase voltage, has five voltage levels: V_d , $V_d/2$, 0, $-V_d/2$ and $-V_d$.

Each active switching devices must block $V_d/2$ forward voltage, the same as that of NPC inverters. However the output voltage is doubled in comparison with 3-level NPC topology. For NPC/H-bridge inverters with SPWM modulation, the maximum *rms* value of the fundamental V_{1rms_max} is:

$$V_{1rms_max} = \frac{\sqrt{3}}{\sqrt{2}} V_d = 1.22 V_d . \quad (1.2)$$

Let's consider the 4.16kV inverter with the NPC/H-bridge topology. The required DC link voltage is now 3.4kV and the device voltage will be of the same level. Thus 3.3kV IGBTs can be used without devices in series.

Another feature of the NPC/H-bridge topology is that it potentially needs only three isolated DC sources. However this feature is not exploited in MV drives because the PSTs used for multi-pulse rectifiers also provide multiple isolated DC sources, leading to fixed neutral potential and avoiding neutral voltage deviation.

The five-level NPC/H-bridge inverters were studied by some researchers and marketed by manufactures. The NPC/H-bridge topology was reported to be used as single phase inverter by C. M. Wu et. al. in 1999^[19] and was first granted patent to a manufacturer in 2000^[20]. The topology was then used in high-power drives at 3.3kV and 4.2kV levels^[6].

To summarize, Table 2.1 compares the NPC and NPC/H-bridge topologies. It can be concluded that if 3.3kV IGBTs are used, the NPC topology is for drives up to 2.3kV and the NPC/H-bridge topology is for drives up to 4.16kV.

Table 1.2 Comparison of NPC and NPC/H-bridge inverters

Topology \ Item	Voltage levels	Max device voltage	Max gain (V_{1rms_max}/V_d)	# of IGBTs	# of clamping diodes	# of isolated DC source	Max inverter voltage with 3.3kV IGBT
NPC	3	$V_d/2$	0.61	12	6	1	2.3kV
NPC/H-bridge	5	$V_d/2$	1.22	24	12	3	4.16kV

1.4 High-Power MV Drives

As was mentioned in Section 1.1, the high-power MV drives must meet the challenges and requirement coming from both the utility side and the motor side. According the requirements from the utility side, drives should draw less harmonic current and operate at near unit power factor^[1]. On the other hand, the motor side requires waveforms with desired amplitude and frequency with lower harmonics and lower dV/dt . To satisfy the motor's requirements, high-power MV drives are often fed by multilevel inverters, which are powered by multi-pulse rectifiers at the front-end.

Fig.1-7 shows the topology of a drive system fed by a 5-level cascaded H-bridge (CHB) inverter^[21]. Each phase contains two H-bridge cells (shown in the dashed circle) in series. Each H-bridge cell is powered by a 6-pulse rectifier. The two rectifiers of the same phase are powered by two secondary windings with 30° phase shift from each other, forming a 12-pulse rectifier. The PST has altogether 6 secondary windings, supplying three 12-pulse rectifiers.

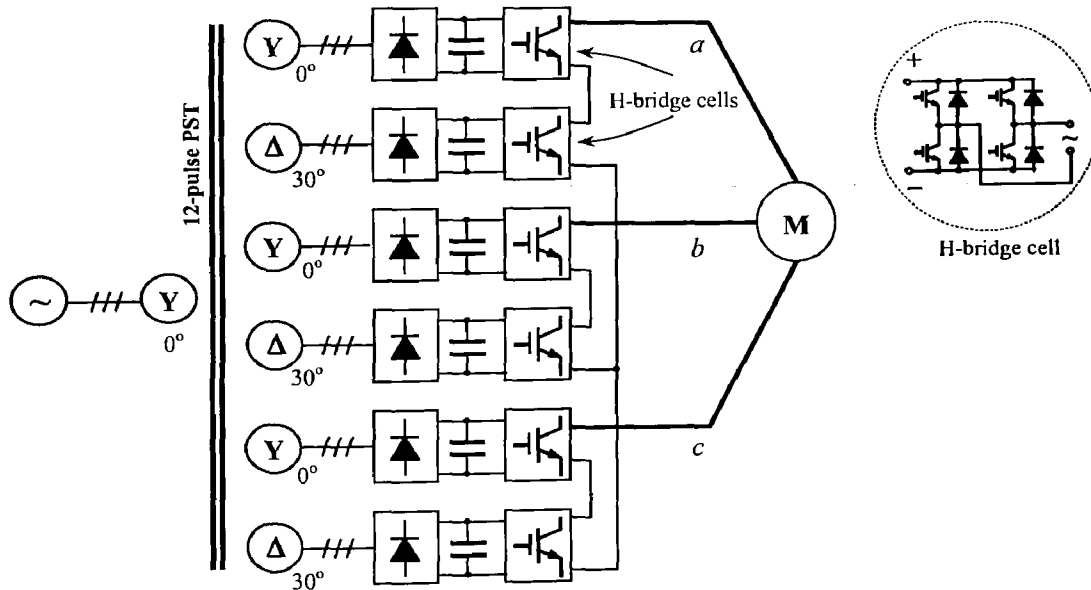


Fig.1-7 Topology of MV drives fed by 5-level CHB inverter

To achieve even lower current THD and higher the drive voltage, more complicated topologies are used in industry. Fig.1-8 shows the topology of an MV drive fed by 7-level CHB inverter^[5]. Each phase contains three H-bridge cells, which are connected to three 6-

pulse rectifiers powered by the secondary windings with 20° phase shift from each other, forming 18-pulse rectification. The PST has altogether 9 secondary windings.

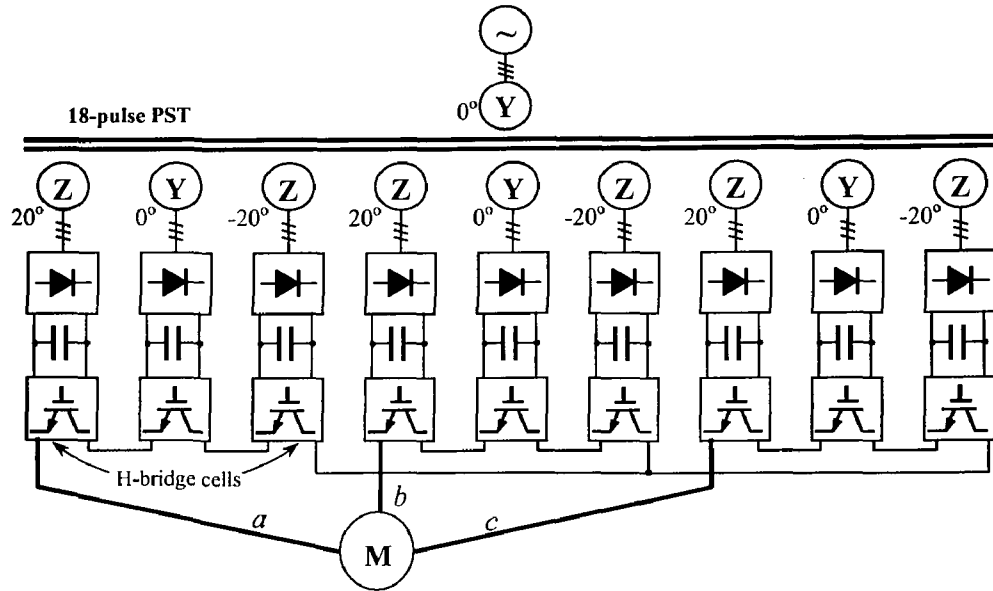


Fig.1-8 Topology of 7-level CHB inverter MV fed drives

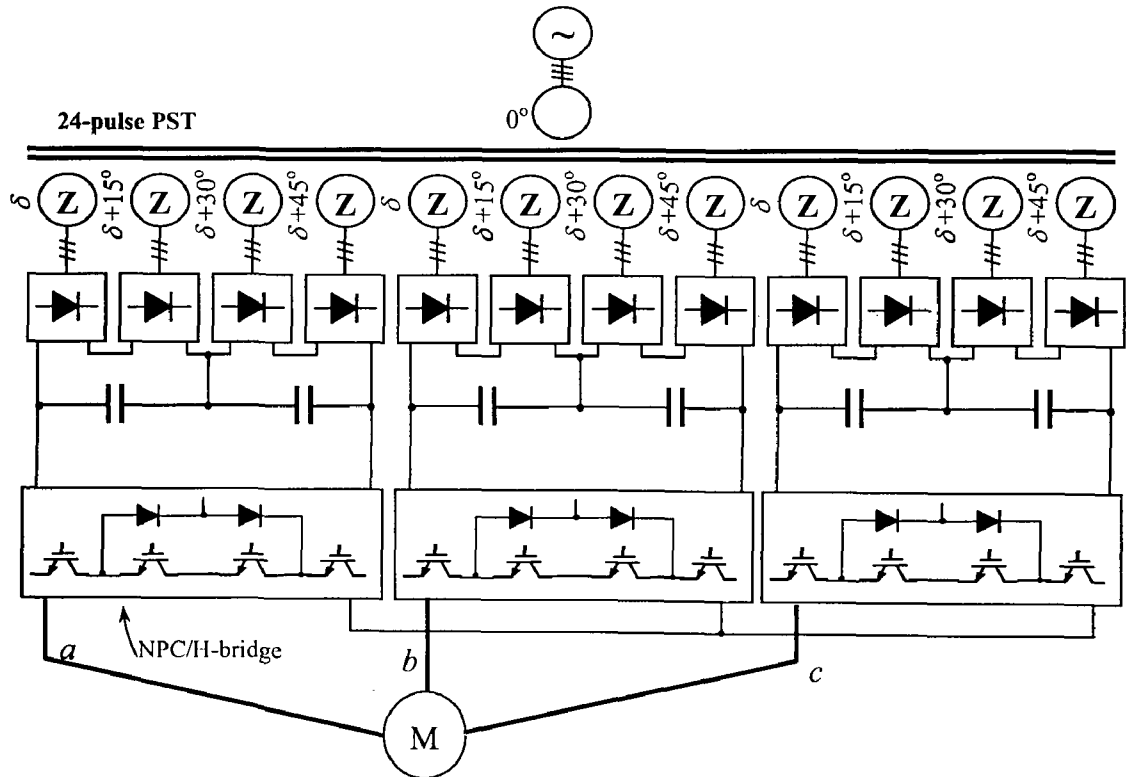


Fig.1-9 Topology of 5-level NPC/H-bridge inverter fed MV drive

Fig.1-9 shows the topology of an MV drive fed by 5-level neutral point clamped (NPC) H-bridge inverter^[6]. Each bridge is power by a 24-pulse rectifier, which is used to achieve less

than 3% input current THD. The PST now has 12 secondary windings, every four of which are combined to power the 24-pulse rectifier. There are altogether 12 rectifiers and 6 groups of DC links capacitors. Table 1.3 is the number of the major parts used by the topology.

Table 1.3 Parts count table of the 5-level NPC/H-bridge drive powered by 24-pulse rectifier

Items	secondary windings	3-phase diode rectifiers	DC-link capacitors	Active switches	Clamping diodes
Parts count	12	12	6	24	12

The choice of the number of pulse and the number of voltage levels depends on the numerous factors under the economic constraints, such as the input current THD requirements, the rated voltage of the drive, the topology of the inverter and the voltage rating of the devices. The more pulses, the higher number of secondary windings. The higher number of voltage levels, the more complicated control for the inverter.

1.5 Space Vector Modulation of Multilevel Inverters

The control of the multilevel inverter is one of major challenges for MV motor drives. The modulation scheme developed in two lines: sinusoidal PWM (SPWM) and space vector modulation (SVM). SVM has been studied extensively studies since its birth in the mid 1980s. Researches have shown that SVM is equivalent in everyway to the more traditional SPWM^{[22]-[24]}. Adjusting one parameter in SVM is equivalent to adjusting other parameter in SPWM. For example, adjusting the modulation index or the carrier frequency in SPWM is equivalent to adjusting the modulus of the reference vector or sampling frequency in SVM. The major benefit of SVM is the explicit identification of pulse placement as an additional degree of freedom that can be exploited to achieve harmonic performance and inverter gains^[24]. Furthermore SVM is commonly recognized as a favourable PWM scheme for digital implementation^{[1][10][24]}.

1.5.1 SVM for Two-Level Inverters

The principle of space vector modulation will be briefly introduced using a 2-level

inverter as an example^[1]. Fig.1-10 shows the circuit diagram and the vector plot of a 2-level inverter. In Fig.1-10(a) there are 6 switches, S_1 to S_6 , producing 8 switching combinations. For example, if switches S_1 , S_2 and S_3 are turned on, the three phase voltages with reference to the negative DC bus will be $v_a=V_d$, $v_b=V_d$ and $v_c=0$, i.e. $(v_a, v_b, v_c)=V_d*(1,1,0)$. We use the triple $[1,1,0]$, which is called **switching state**, to represent this situation. Similarly the switching states can be found for the other 7 combinations, as listed in Table 1.4.

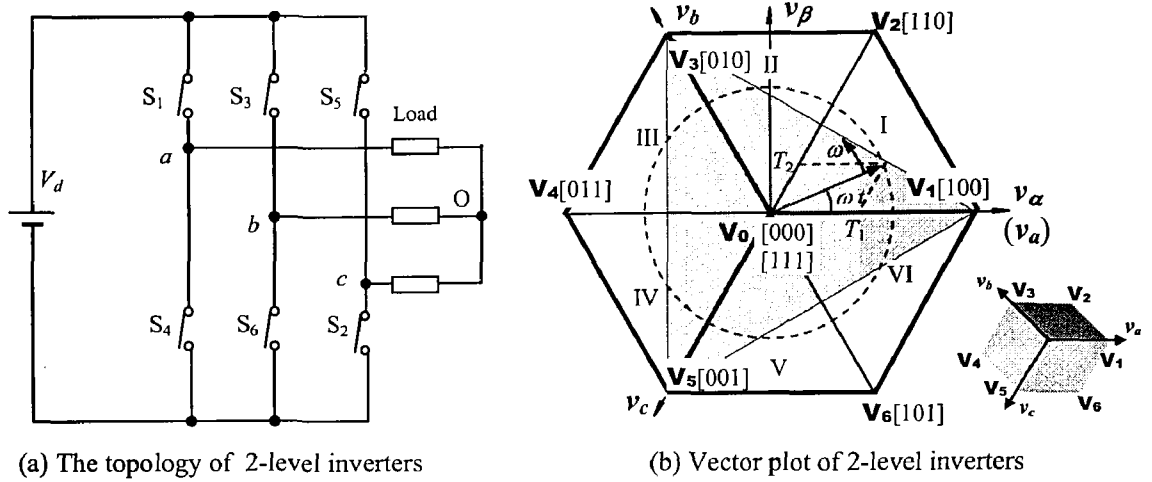


Fig.1-10 Circuit diagram and vector plot of a 2-level inverter.

Now set up a Cartesian 3-D space in Fig.1-10(b) with three axes v_a , v_b and v_c perpendicular to each other and draw all the 8 points representing the switching states shown in Table 1.4. The small cubic block in the diagram is for better comprehension of the 3-dimensional vector plot. If the vector plot is viewed as 3-D, the switching states are in fact the coordinates. The 8 points represent the 8 **space vectors** V_0 to V_7 .

Table 1.4 Space vector, switching states and on-state switches

On state Switches	S_1, S_3, S_5	S_2, S_4, S_6	S_1, S_2, S_6	S_1, S_2, S_3	S_2, S_3, S_4	S_3, S_4, S_5	S_4, S_5, S_6	S_1, S_5, S_6
Switching State	$[1,1,1]$	$[0,0,0]$	$[1,0,0]$	$[1,1,0]$	$[0,1,0]$	$[0,1,1]$	$[0,0,1]$	$[1,0,1]$
Space Vector	V_0	V_7	V_1	V_2	V_3	V_4	V_5	V_6

The space vectors is then projected on a plane. For three-phase balanced system, we have the constraint:

$$v_a + v_b + v_c = 0. \quad (1.3)$$

which is in fact the equation of plane through the origin and with a normal direction (1,1,1), i.e. the plane parallel to the shaded triangle and thru the origin in Fig.1-10(b). The plane is called **vector plane**. By projection, the images of the three axes are 120° away from each other. The images of the 8 space vectors are called **stationary vectors**. Vectors V_0 and V_7 have the same image, the origin, thus are called **zero vectors**. The switching states representing the same image are **redundant switching states**. The images of V_1 to V_6 are located at the vertices of a hexagon, which can be divided into 6 sectors. The vector plane can be meshed by the triangles using the tips of stationary vectors as vertices.

On the other hand, we need only two axes to form the basis of a plane, which means the three-phase voltage can be represented by a two-phase vector. The *Forward Clarke Transformation* can be used for such a purpose^[1]:

$$\vec{V}(t) = v_a(t) + jv_b(t) = \frac{2}{3}[v_a(t)e^{j0} + v_b(t)e^{j2\pi/3} + v_c(t)e^{j4\pi/3}]. \quad (1.4)$$

By using the transformation, the stationary vector can be calculated for each switching state. For example, for the switching state [1,1,0], the three phase voltages with respect to the negative DC bus are: $v_a(t)=V_d$, $v_b(t)=V_d$ and $v_c(t)=0$. Using Eq.(1.4), we have the vector:

$$\vec{V}(t) = \frac{2}{3}[v_a(t)e^{j0} + v_b(t)e^{j2\pi/3} + v_c(t)e^{j4\pi/3}] = \frac{2}{3}V_d e^{j\pi/3}. \quad (1.5)$$

If we normalize it by $2V_d/3$, it is exactly V_2 .

While the stationary vectors represent the switching combinations, the three-phase voltage can be represented by a rotating vector, whose magnitude stands for the amplitude of the phase voltage and the angular speed stands for the frequency. The rotating vector is called as **reference vector** (V_{ref}). Once the plane is meshed by stationary vectors, the reference vector can be approximated by the stationary vectors. If the reference stays at a location for a period of T_s , we can use adjacent stationary vectors, generally the nearest three-vectors (NTVs), to produce the same amount average. In Fig.1-10(b) the reference vector is located in Sector I,

the sampling period T_s can be split among $V_0(V_7)$, V_1 and V_2 based on the so-called volt-second balance:

$$T_1 = T_s m_a \sin(-\theta + \pi/3), \quad (1.6)$$

$$T_2 = T_s m_a \sin \theta, \quad (1.7)$$

$$T_0 = T_s - T_1 - T_2. \quad (1.8)$$

where m_a is the amplitude modulation index, $m_a = \sqrt{3}V_{ref}/V_d$, T_1 , T_2 and T_0 are the time segment assigned to V_1 , V_2 and $V_0(V_7)$ respectively, which are called **dwell times**.

The general procedure of implementing SVM is:

- (a) calculate the switching states of the stationary vectors and mesh the vector plane;
- (b) define the switching sequences for each triangle;
- (c) identify the NTVs;
- (d) calculate the dwell times;
- (e) generate gating signal by decoding the switching states in the timed switching sequence.

1.5.2 The Application of SVM for Multilevel Inverters

The application of SVM for multilevel inverters is much more complicated than for 2- or 3-level inverters. The main reason is that there are large number of redundant switching states and stationary vectors for multilevel inverters^{[1][25][26][27]}. Almost every step in the procedure of using SVM such as identification of the NTVs, the calculation of the dwell times, and the design of the switching sequences becomes computation-intensive and troublesome. Fortunately, the computational burden for the identification of NTVs and calculation of the dwell times is significantly lessened thanks to the contributions of many researchers. One of these is the application of hexangular coordinate system^[25].

However, there are still some other problems to be solved related to switching sequence design. The problems can be divided into the selection of redundant switching states and the

optimization of the schedule of the sequence, both of which are tedious and tough work for multilevel inverters. Earlier studies showed that it is reasonable to constrain the choice of redundant states to the ‘middle states’, which limits the number of switching states to 4 or 5 for each triangle^{[26][27]}. Even with this simplification, the switching sequence design is still a major concern for optimal performance: better THD profile and lower switching loss^[1].

Harmonic reduction is the first concern of switching sequence design. For high-power MV motor drives, the switching frequency is often relatively low (about 500Hz) in the consideration of the switching loss^[1]. The lower device switching frequency brings negative side-effects to the spectrum of the output voltage. If the first sideband of the spectrum is too close to the fundamental frequency, lower order harmonics such as 5th and 7th, will be great headaches. It is desirable if the switching sequence can be properly designed so that the centre of the first sideband is shifted to higher frequency.

The second concern is the reduction of the switching loss. For multilevel inverters, the complexity of the vector plot often makes extra switchings inevitable. Extra switchings are the switchings that don’t contribute to the inverter sampling frequency, which is defined as the centre of the 1st sideband in the spectrum of the line-to-line voltage. Because high-power converters often work at lower switching frequencies, extra switching is a painful waste.

Other concerns include easy implementation. For multilevel inverters, the switching sequence design must be done for each case (triangle), which results in a complex look-up table. This case-study-based design can be improved by a rule-based design, where the selection of the switching state and the arrangement of switching sequence are implemented in real time according to some simple rules.

Moreover, waveform symmetry should also be taken into account. Although it seems that half-wave symmetry is not a big issue for MV motor in most cases, it is critical for rectifiers because the even order harmonics are strictly regulated by IEEE 519-1992, which set the limits of even harmonic to a quarter of those of odd harmonics.

1.6 Motivation and Objective

As mentioned earlier, there are numerous technical challenges and requirements for MV high-power motor drives. Two of them will be addressed in the thesis.

The first challenge is how to simplify the topology of the rectifier and to achieve friendlier converter-to-utility interface. As introduced in Section 1.2, multi-pulse rectifiers are often the solution to the reduction of the current THD. However, the more pulses of the rectifier, the more complicated the PST. This is why rectifiers of more than 30-pulse are not used in practice.

The second challenge is how to effectively apply SVM to multilevel inverters with desirable THD profile at relatively lower switching frequency. The key issue here is how to efficiently design the switching sequence. Conventionally, switching sequence design is done by predefining the sequence for each triangle in the vector plot. This is a manual job and is really a tedious one for multilevel converter.

In brief, the effort devoted to the rectifiers for high-power drives is targeted to:

(1) the simplification of the PST. The topology shown in Fig.1-9 is used as the starting point of the simplification. The standard 18-pulse PST will be used in place of the complex 24-pulse PST. Meanwhile the number of secondary windings is reduced by half, thus the number of DC links and rectifiers can be reduced by half accordingly.

(2) the improvement of harmonic cancellation. The topology in Fig.1-9 features 24-pulse harmonic cancellation. It will be improved to 36-pulse cancellation with reduced secondary windings. The principle can also be used for harmonic cancellation between two different drives or for extra opportunities for harmonic cancellation when the PSTs are non-ideal.

The work on the switching sequence of SVM is intended to achieve the following objectives:

(3) the improvement of THD profile by increasing the inverter sampling frequency.

(4) the decrease of the device switching frequency by reducing the extra switchings.

(5) easy sequence design and implementation by rule-based design and mechanism of sequence reproduction. The rule-based design makes the algorithm is applicable to other multilevel inverters.

(6) Waveform symmetry which enables the algorithm to be used for active rectifiers.

1.7 Thesis Organization

The work of the thesis is organized into 5 chapters.

Following the introduction of Chapter 1, Chapter 2 deals with the front-end of the MV motor drives, i.e. multi-pulse rectifiers, for which the dual 18-pulse rectifier is proposed. The dual 18-pulse rectifier features 36-pulse harmonic cancellation with simple 18-pulse PSTs, fewer secondary windings, rectifier bridges and DC capacitors, compared with the 24-pulse rectification shown in Fig.1-9. Theoretical analysis and computer simulation was given to verify the above features.

For the inverter stage, emphasis of Chapter 3 is laid on the control of the multilevel inverters, i.e. the space vector modulation algorithms, for which a flexible 3-segment SVM algorithm is put forward. Compared to conventional 7-segment SVM schemes, the proposed algorithm achieves higher inverter sampling frequency, lower device switching frequency, easy sequence design and digital implementation. The algorithm is also applicable for other high-level inverters or active rectifiers which require half-wave symmetry. The performance of the algorithm is verified by extensive computer simulations in comparison with the 7-segment SVM.

The experimental verification is given in Chapter 4, in which the experimental setup is introduced and experimental results are discussed in association with the simulations.

Chapter 5 is the conclusions which can be drawn from the research in the thesis.

Other supporting materials and more detailed waveforms are attached in the appendices.

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19. The nineteenth is that the system is not a simple one.

20. The twentieth is that the system is not a simple one.

21. The twenty-first is that the system is not a simple one.

22. The twenty-second is that the system is not a simple one.

23. The twenty-third is that the system is not a simple one.

24. The twenty-fourth is that the system is not a simple one.

25. The twenty-fifth is that the system is not a simple one.

CHAPTER 2 DUAL 18-PULSE RECTIFIER

Multi-pulse rectification is used extensively by manufacturers to reduce the harmonics drawn from the utility. Phase-shifting transformers (PSTs) are the key to the harmonic reduction. Because multilevel rectifiers for high-power drives often require multiple isolated DC sources, thus PSTs with multi secondary windings are frequently found in the literatures. However PSTs with higher pulse numbers are too complicated to be manufactured due to the large number of secondary windings which must be wound with precise phase-shift angles. The highest number of pulses ever seen in practice is 30-pulse. The chapter discusses the possibility to reduce the number of secondary windings and to enhance the harmonic cancellation. A dual 18-pulse rectifier, which utilizes simple 18-pulse PSTs to achieve 36-pulse harmonic cancellation, is proposed for high power MV drives^[13].

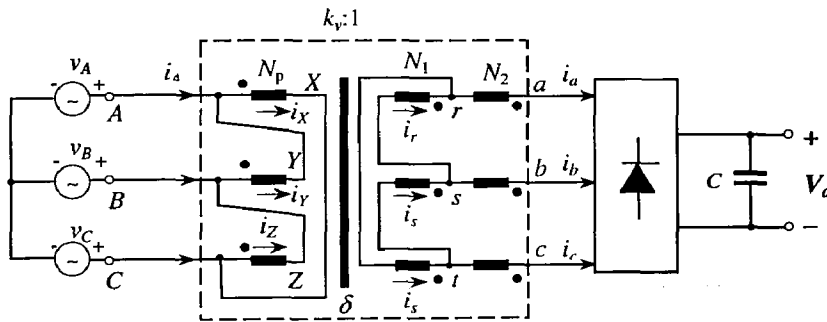


Fig.2-1 Circuit model of a 6-pulse rectifier fed by a PST.

2.1 Principle of Harmonic Cancellation

First look at a general case: a six pulse rectifier shown in Fig.2-1, where the rectifier is fed by a phase-shifting transformer. The primary winding is connected in Δ and the secondary in extended- Δ , producing a phase shift angle δ :

$$\delta = \angle v_{ab} - \angle v_{AB} \quad (2.1)$$

Assume the primary to secondary voltage ratio is k_v , and N_p , N_1 and N_2 are the numbers of turns as shown in Fig.2-1. To achieve the phase shift angle δ , the turns ratios should be^[1]:

$$\begin{cases} \frac{N_p}{N_1} = \frac{k_v \sin 120^\circ}{\sin \delta} \\ \frac{N_p}{N_1 + N_2} = \frac{k_v \sin 120^\circ}{\sin(120^\circ + \delta)} \end{cases} \quad (2.2)$$

Assume the secondary terminal currents are:

$$\begin{cases} i_a = \sum_{h=1,5,7,\dots}^{\infty} \hat{I}_h \sin h\omega t \\ i_a = \sum_{h=1,5,7,\dots}^{\infty} \hat{I}_h \sin h(\omega t - 120^\circ) \\ i_a = \sum_{h=1,5,7,\dots}^{\infty} \hat{I}_h \sin h(\omega t + 120^\circ) \end{cases} \quad (2.3)$$

where \hat{I}_h is the magnitude of the h^{th} harmonic, and ω is the fundamental angular frequency.

These terminal currents flow through the extended coils (N_2). The currents through the secondary Δ -coils (N_1) are i_r , i_s and i_t as shown in the figure. All these six currents will be induced in the primary winding inversely proportional to the turns ratios. Thus the coil currents of the primary are

$$\begin{cases} i_X = \frac{N_1}{N_p} i_r + \frac{N_2}{N_p} i_a \\ i_Y = \frac{N_1}{N_p} i_s + \frac{N_2}{N_p} i_b \\ i_Z = \frac{N_1}{N_p} i_t + \frac{N_2}{N_p} i_c \end{cases} \quad (2.4)$$

Specifically the primary terminal current of phase A is:

$$i_A = i_X - i_Y \quad (2.5)$$

Substituting Eq.(2.4) into Eq.(2.5) yields:

$$i_A = \frac{N_1 + N_1}{N_p} i_a - \frac{N_2}{N_p} i_c. \quad (2.6)$$

Applying Eqs.(2.2) and (2.3) to Eq. (2.6), we have:

$$\begin{aligned}
i_A &= \frac{1}{k_v \sin 120^\circ} \sum_{h=1,5,7,\dots}^{\infty} \hat{I}_h [\sin h\omega t \sin(120^\circ + \delta) - \sin h(\omega t + 120^\circ) \sin \delta] \\
&= \frac{1}{k_v \sin 120^\circ} \sum_{h=1,5,7,\dots}^{\infty} \hat{I}_h [\sin((h+1) \cdot 60^\circ) \sin(h\omega t + (h-1) \cdot 60^\circ - \delta) \\
&\quad - \sin((h-1) \cdot 60^\circ) \sin(h\omega t + (h+1) \cdot 60^\circ + \delta)] \\
&= \frac{1}{k_v} \sum_{\substack{h=6k+1 \\ k=0,1,2,\dots}}^{\infty} \hat{I}_h \sin(h\omega t - \delta) + \frac{1}{k_v} \sum_{\substack{h=6k-1 \\ k=1,2,3,\dots}}^{\infty} \hat{I}_h \sin(h\omega t + \delta)
\end{aligned} \tag{2.7}$$

A general conclusion can be drawn from Eq.(2.7): when the secondary voltage is shifted by δ with respect to the primary, the secondary terminal current can be referred to the primary terminal in a way such that:

- (1) The positive-sequence harmonics are phase-shifted by $-\delta$;
- (2) The negative-sequence harmonics are phase shifted by δ ;
- (3) The magnitudes are scaled by the same ratio.

Table 2.1 The phase angles of the harmonic of 24-pulse PST

h current		1 st	5 th	7 th	11 th	13 th	17 th	19 th	23 rd	25 th	29 th	31 st	35 th	37 th
Original (°)	i_1	0	0	0	0	0	0	0	0	0	0	0	0	0
	i_2	-15	-75	-105	-165	-195	-255	-285	-345	-15	-75	-105	-165	-195
	i_3	-30	-150	-210	-330	-30	-150	-210	-330	-30	-150	-210	-330	-30
	i_4	-45	-225	-315	-135	-225	-45	-135	-315	-45	-225	-315	-135	-225
Referred (°)	i'_1	-22.5	22.5	-22.5	22.5	-22.5	22.5	-22.5	22.5	-22.5	22.5	-22.5	22.5	-22.5
	i'_2	-22.5	-67.5	-112.5	-157.5	-202.5	-247.5	-292.5	22.5	-22.5	-67.5	-112.5	-157.5	-202.5
	i'_3	-22.5	-157.5	-202.5	-337.5	-22.5	-157.5	-202.5	22.5	-22.5	-157.5	-202.5	-337.5	-22.5
	i'_4	-22.5	-247.5	-292.5	-157.5	-202.5	-67.5	-112.5	22.5	-22.5	-247.5	-292.5	-157.5	-202.5
Cancelled?		no	yes						no		Yes			
i_1 : the current in the 22.5° secondary; i_2 : the current in the 7.5° secondary; i_3 : the current in the -7.5° secondary; i_4 : the current in the -22.5° secondary;														

The above conclusions can be used to analyze the harmonic cancellation pattern of multi-pulse rectifiers. Let's take the 24-pulse rectifier as an example. Assume the 4 secondary windings are phase-shifted by 22.5°, 7.5°, -7.5° and -22.5° with respect to the primary. Using the above results we can quickly figure out the phase angles of the referred currents of each harmonic. For instance, the phase angles of the 5th harmonic at the secondaries are 0°, 5*(-15°), 5*(-30°) and 5*(-45°) respectively. When they are referred to the primary, the phase

angles are: $0^\circ+22.5^\circ$, $-75^\circ+7.5^\circ$, $-150^\circ-7.5^\circ$, $-225^\circ-22.5^\circ$, i.e. 22.5° , -67.5° , -157.5° and -247.5° . Because they are referred with the same ratio, the referred currents with 22.5° and -157.5° angles are 180° out of phase and cancel each other. It is the same for the other two. The phase angles of all the harmonics in the referred currents are listed until the 37th in Table 2.1, from which we can find the lowest harmonic in the primary current is the 23rd.

2.2 Reduction of Secondary Windings

The performance of harmonic reduction is decided by the number of pulses. From Fig.1-7, Fig.1-8 and Fig.1-9, the number of secondary windings, w , is half of the number of pulses for H-bridge-based multilevel converters. For example, the 12-pulse PST has 6 secondary windings and the 24-pulse PST has 12. Can it be reduced or reconfigured for simplicity and better performance?

Now, because each secondary produces 6-humps per fundamental cycle in the DC output, theoretically, for a p -pulse PST, the ideal number of secondary windings w is

$$w=p/6 \quad (2.8)$$

For MV motor drives, the choice of the pulse number p depends on: 1) the input current harmonic requirements and, 2) the number of DC supplies needed by the inverter.

Obviously the actual number of secondaries in Fig.1-7, Fig.1-8 or Fig.1-9 is three times the number predicted by Eq.(2.8). The number of secondaries in Fig.1-7 and Fig.1-8 cannot be reduced because of the number of isolated DC sources required by the inverter. However, it could be reduced for the topology of Fig.1-9 where the number of secondaries is more than the number of required DC sources. It should be noted that even though the secondaries in Fig.1-7 and Fig.1-8 can not be reduced, according to Eq.(2.8), the number of pulses can be expected to be tripled for better harmonic cancellation. For example, the PST in Fig.1-7 has 6 secondary windings, thus 36-pulse harmonic cancellation can be achieved theoretically.

Now let's focus on Fig.1-9. We have two alternatives to reconfigure the rectifier: to triple

the pulse number or to reduce the secondary number. With 12 secondaries, 72-pulse harmonic cancellation could be expected. However 72-pulse harmonic cancellation is not practical from both the viewing points of the PST manufacturing and IEEE 519-1992 harmonic requirements. Because only 6 DC sources are needed for fixed neutral point potential, the number of secondaries can be halved, leading to a 36-pulse configuration (Fig.2-2), where the secondaries are shifted by 10° from each other and γ is any angle that is practically meaningful.

Table 2.2 compares the major features of the 36-pulse rectifier and 24-pulse rectifiers in Fig.1-9. Obviously the topology of Fig.2-2 achieves better harmonic cancellation and uses fewer secondary windings although the ripple in the DC may be larger than that of Fig.1-9.

Now the problem is that 36-pulse PSTs are too complex for manufacturing. The problem can be solved by the proposed dual 18-pulse rectification.

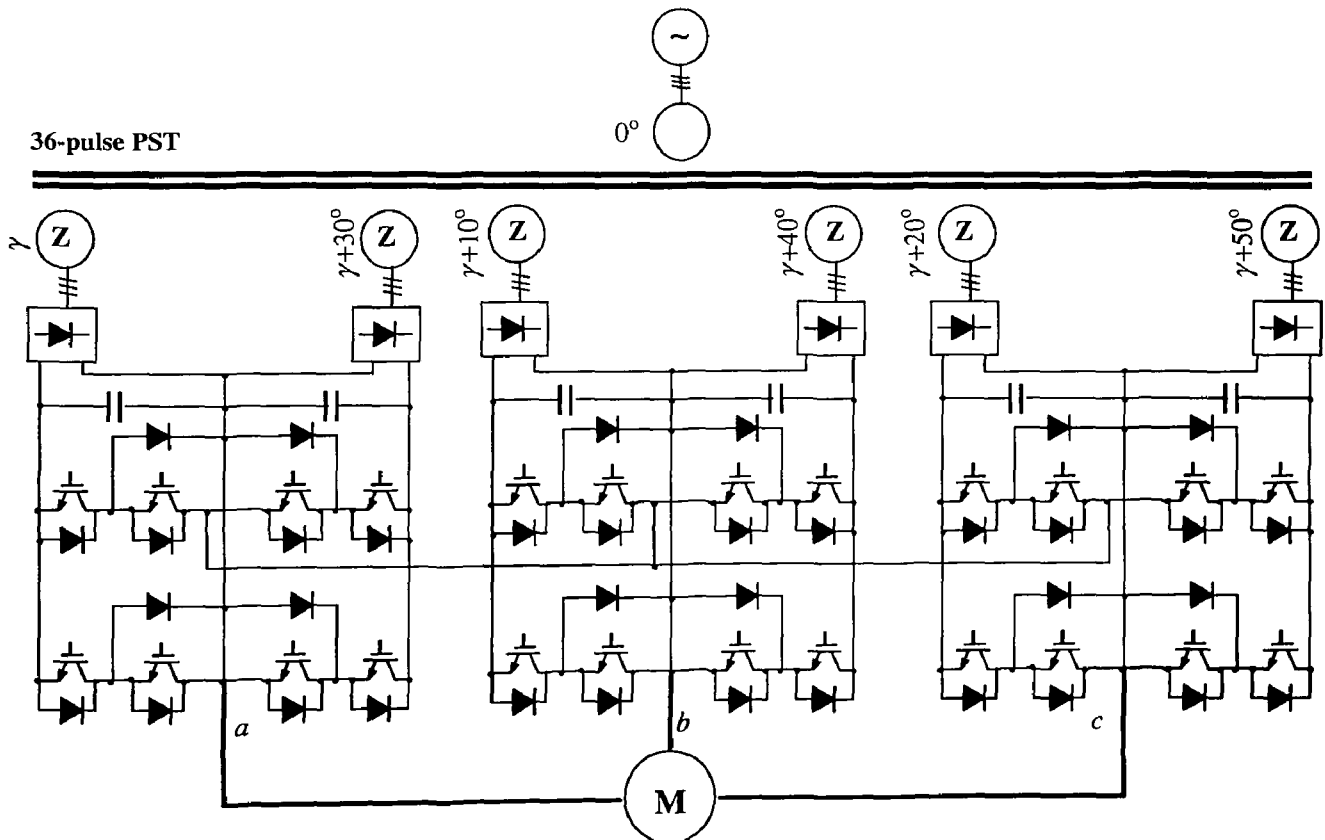


Fig.2-2 Topology of 36-pulse 5-level NPC/H-bridge inverter fed drive.

Table 2.2 Comparison of the rectifiers in Fig.1-9 and Fig.2-2

Topology \ Item	# of secondaries	# of rectifiers and caps	Lowest dominant harmonic	# of ripples in DC per cycle
24-pulse (Fig.1-9)	12	12	23	24
36-pulse (Fig.2-2)	6	6	35	12

2.3 Dual-18 Pulse Rectification

2.3.1 Topology

The topology of the dual 18-pulse rectifier is shown in Fig.2-3, where two 18-pulse PSTs are used in stead of a bulk 36-pulse PST. The top PST, xmfr 1, is of Y-primary and the secondaries are phase-shifted by γ , $\gamma-20^\circ$ and $\gamma-40^\circ$, where γ is any angle which is practical. The bottom PST, xmfr 2, is of Δ -primary, which makes its secondaries shifted by additional $\pm 30^\circ$ from those of the top PST. The six DC outputs DC1 to DC6 can be used to power the multilevel inverters.

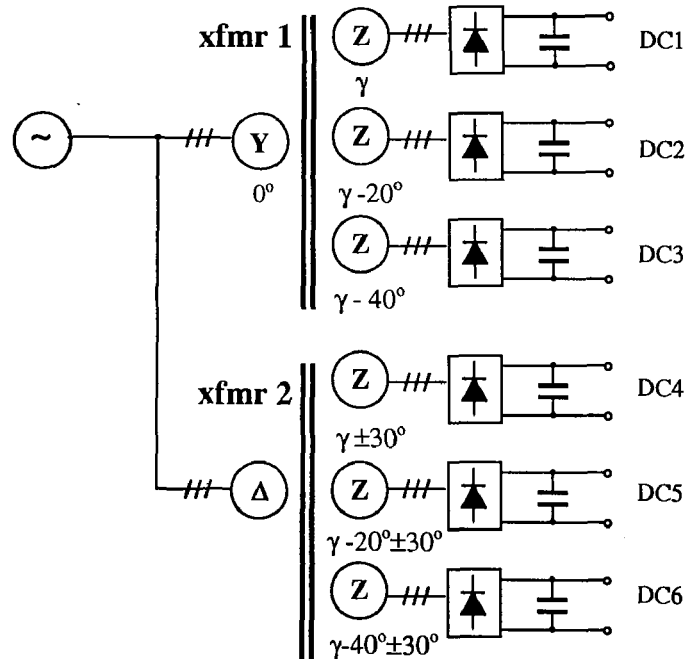


Fig.2-3 Topology of dual 18-pulse rectifier.

According to the winding arrangements, PSTs can be of Y/Z or Δ /Z configurations: the primary may be in Y- or Δ -connection and the secondary in zigzag (Z). The Y/Z or Δ /Z configuration makes no difference to the effect of harmonic cancellation if the PST is used alone. However, if two PST are combined, extra benefit can be achieved.

2.3.2 Harmonic Cancellation

According the theory of Section 2.1, if the line current of a secondary of a zigzag PST is

$$i_1 = \sum_{h=1}^{\infty} \hat{I}_h \sin h\omega t, \quad (2.9)$$

the referred current at primary terminal is:

$$i_1' = \frac{1}{k_v} \sum_{h=1,7,13,\dots}^{\infty} \hat{I}_h \sin(h\omega t - \delta) + \frac{1}{k_v} \sum_{h=5,11,17,\dots}^{\infty} \hat{I}_h \sin(h\omega t + \delta) \quad (2.10)$$

where δ is the phase shift angle. Consider another secondary with phase angle δ with respect to i_1 , i.e.:

$$i_2 = \sum_{h=1}^{\infty} \hat{I}_h \sin h(\omega t + \delta). \quad (2.11)$$

When it is reflected in the primary, it becomes

$$\begin{aligned} i_2' &= \frac{1}{k_v} \sum_{h=1,7,13,\dots}^{\infty} \hat{I}_h \sin[h(\omega t + \delta) - \delta] + \frac{1}{k_v} \sum_{h=5,11,17,\dots}^{\infty} \hat{I}_h \sin[h(\omega t + \delta) + \delta] \\ &= \frac{1}{k_v} \sum_{h=1,7,13,\dots}^{\infty} \hat{I}_h \sin[h\omega t + (h-1)\delta] + \frac{1}{k_v} \sum_{h=5,11,17,\dots}^{\infty} \hat{I}_h \sin[h\omega t + (h+1)\delta] \end{aligned} \quad (2.12)$$

where k_v is the primary to secondary voltage ratio. From Eq.(2.12), it can be concluded that: if the initial angle of a secondary current is δ , the harmonic current referred to the primary is shifted by $(h-1)\delta$ for positive-sequence harmonics, and by $(h+1)\delta$ for negative-sequences.

Now use the above conclusions for two 18-pulse transformers: the first transformer, xfmr 1, has three secondaries at -20° , 0° and 20° . The second, xfmr 2, is shifted by α with respect to xfmr1, with the secondary angles $-20^\circ + \alpha$, $0^\circ + \alpha$ and $20^\circ + \alpha$. The phase shift angle of the harmonics are calculated and listed in Table 2.3.

Table 2.3 Phase angles of the referred harmonics and cancellation patterns of dual 18-pulse rectifiers

	$\delta \begin{smallmatrix} h \\ \end{smallmatrix}$	1	5	7	11	13	17	19	23	25	29	31	35	37	41	43	47	49	53	55	59	61
xfmr1	-20	0	-120	-120	120	120	0	0	-120	-120	120	120	0	0	-120	-120	120	120	0	0	-120	-120
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	20	0	120	120	-120	-120	0	0	120	120	-120	-120	0	0	120	120	-120	-120	0	0	120	120
xfmr2	-20+ α	0	-120 +6 α	-120 +6 α	120 +12 α	120 +12 α	18 α	18 α	-120 +24 α	-120 +24 α	120 +30 α	120 +30 α	36 α	36 α	-120 +42 α	-120 +42 α	120 +48 α	120 +48 α	54 α	54 α	-120 +60 α	-120 +60 α
	α	0	6 α	6 α	12 α	12 α	18 α	18 α	24 α	24 α	30 α	30 α	36 α	36 α	42 α	42 α	48 α	48 α	54 α	54 α	60 α	60 α
	20+ α	0	120 +6 α	120 +6 α	-120 +12 α	-120 +12 α	18 α	18 α	120 +24 α	120 +24 α	-120 +30 α	-120 +30 α	36 α	36 α	120 +42 α	120 +42 α	-120 +48 α	-120 +48 α	54 α	54 α	120 +60 α	120 +60 α
Pattern 1	no	yes		yes		no		yes		yes		no		yes		yes		no		yes		
Pattern 2	no	yes		no		yes		no		yes		no		yes		no		yes		no		
Pattern 3	no	no		no		yes		no		no		no		no		no		yes		no		
Note: Pattern 1: harmonic cancellation within transformers; Pattern 2: inter-transformer cancellation when $\alpha = \pm 30^\circ$; Pattern 3: inter-transformer cancellation when $\alpha = \pm 10^\circ$.																						
											yes: cancellation pattern is effective; no: cancellation patter is ineffective.											

Table 2.3 shows 3 patterns for harmonic cancellation:

Pattern 1: harmonics are cancelled within the transformers. It is in fact the cancellation pattern of standard 18-pulse rectifiers.

Pattern 2: inter-transformer harmonic cancellation in addition to Pattern 1 when $\alpha = \pm 30^\circ$. The 5th, 7th, 17th, 19th ... harmonics are cancelled.

Pattern 3: inter-transformer harmonic cancellation in addition to Pattern 1 when $\alpha = \pm 10^\circ$. The 17th, 19th, 53rd, 55th ... harmonics are cancelled.

For a standard 36-pulse rectifier, $\alpha = \pm 10^\circ$. Patterns 1 and 3 are effective. It is clear from Table 2.3 that the lowest harmonic order is the 35th. For the proposed dual 18-pulse rectifier, Patterns 1 and 2 are effective. The lowest order harmonic is also the 35th.

To compare the dual 18-pulse rectifier and standard 36-pulse rectifier, it is interesting to consider the following two situations:

(1) Ideal PSTs. Ideal means the phase errors are negligible and the windings are well balanced. It is easy to conclude that there is no substantial difference in terms of harmonic profile between standard 36-pulse rectifiers and dual 18-pulse rectifiers.

(2) Non-ideal PSTs with either remarkable phase-shifting error or winding balancing problem. No doubt that certain amount of lower order harmonics will appear, depending on

how serious the problem is. However, it seems that the performance of dual 18-pulse rectifiers will be superior to that of standard 36-pulse rectifiers. The reason is that Pattern 2 provides more additional opportunities for harmonic cancellation than Pattern 3, especially for the nastiest 5th and 7th.

By the way, there are some other harmonic cancellation patterns when α takes the other values. For example when $\alpha=5^\circ$, the 35th and 37th harmonic can be neutralized. However these patterns are of little practical meaning.

When $\alpha=\pm 30^\circ$, the two transformers differ in Y- or Δ -connection, which is good for manufacturing.

2.4 Applications

2.4.1 Configuration of the DC Output

The DC outputs of the 18-pulse rectifier can be configured differently to fit the inverter topologies. Here are three application cases.

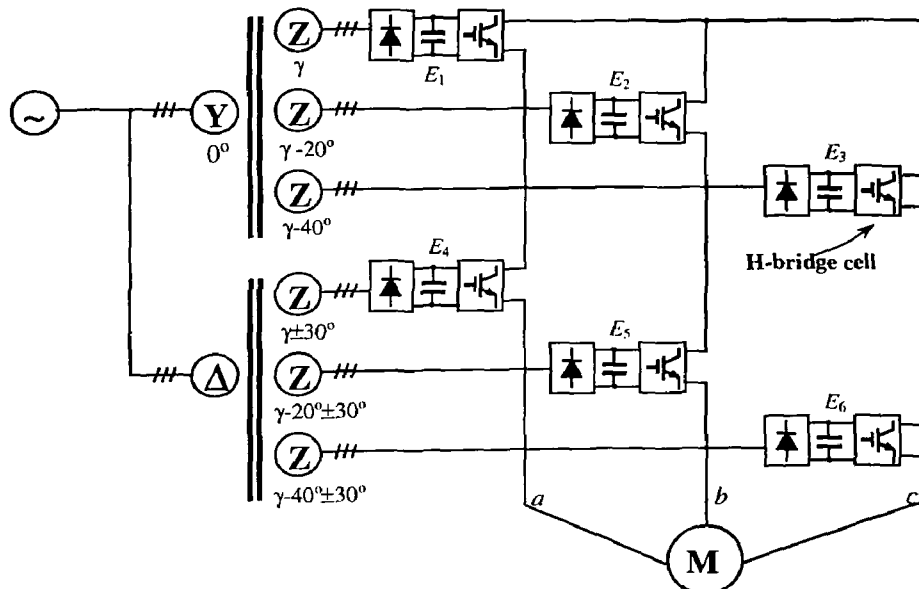


Fig.2-4 DC connection of Application Case 1: for 5-level CHB inverters.

Application case 1: for cascaded H-bridge (CHB) inverters

The DC outputs are connected as isolated sources E_1 - E_6 to supply the six H-bridges of a 5-

level CHB inverter (Fig.2-4). The waveform of one of the isolated DC output, E_1 , is shown in Fig.2-5 for a fundamental period. It is the typical voltage waveform of a 6-pulse rectifier.

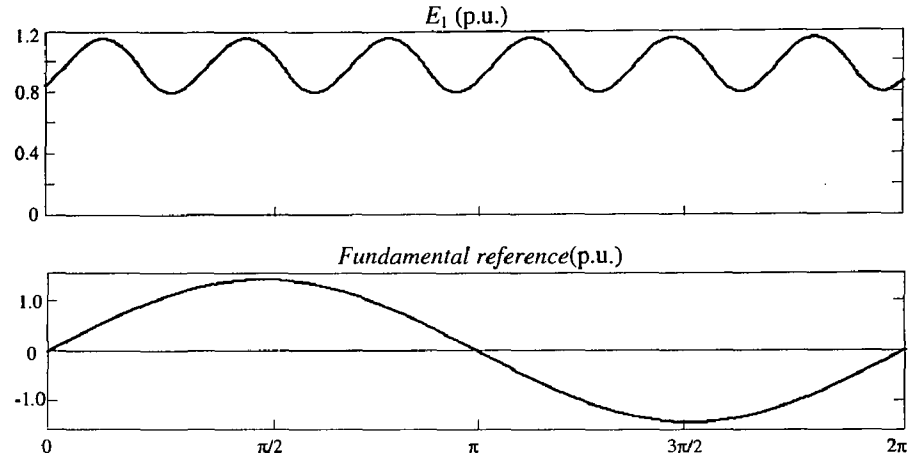
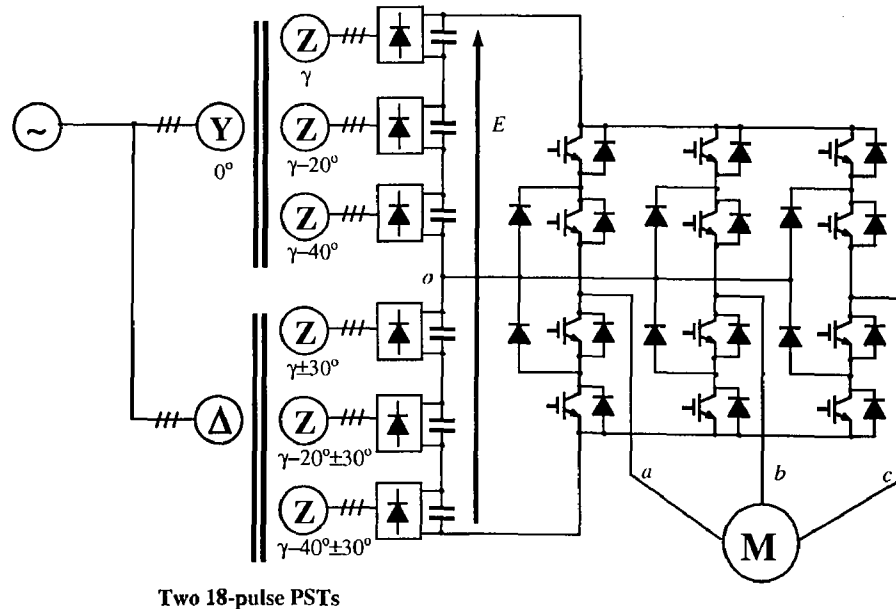


Fig.2-5 Simulated DC output of Application Case 1

Application case 2: for 3-level NPC inverters

The DC outputs are used as a 36-pulse DC source E with a neutral o . It is ideal for conventional 3-level NPC inverters (Fig.2-6), where the neutral point of the inverter is connected to the point o with fixed potential. Thus the problem of capacitor voltage deviation is avoided. The waveform of E is shown in Fig.2-7, which is the typical output of 36-pulse rectifiers and contains very little ripple.



Two 18-pulse PSTs

Fig.2-6 DC connection of Application Case 2: for 3-level NPC inverters.

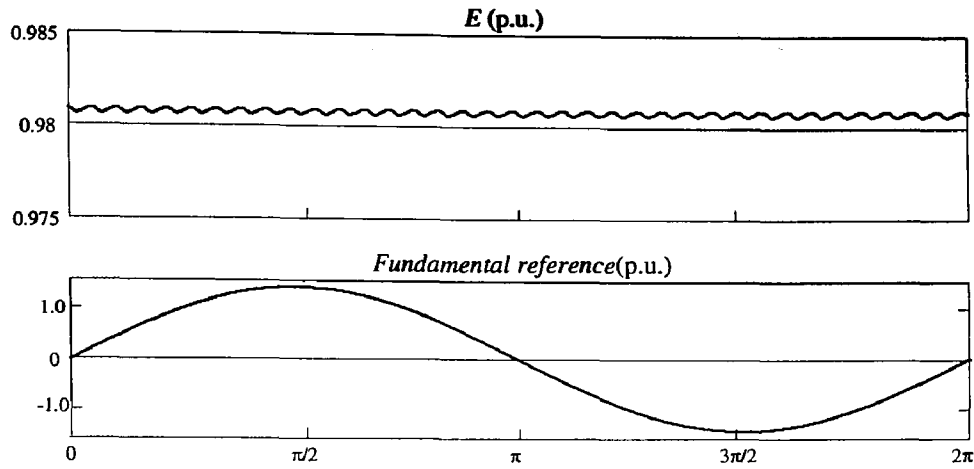


Fig.2-7 Simulated DC output of Application Case 2

Application case 3: for 5-level NPC/H-bridge inverters

The DC outputs are grouped into three pairs, E_1 to E_3 (Fig.2-8) for the three bridge cells of a 5-level NPC/H-bridge inverter. The secondary windings feeding the rectifiers of each pair are of 30° phase shift. The DC voltage waveform of E_1 is shown in Fig.2-9, which is the typical output of 12-pulse rectifiers.

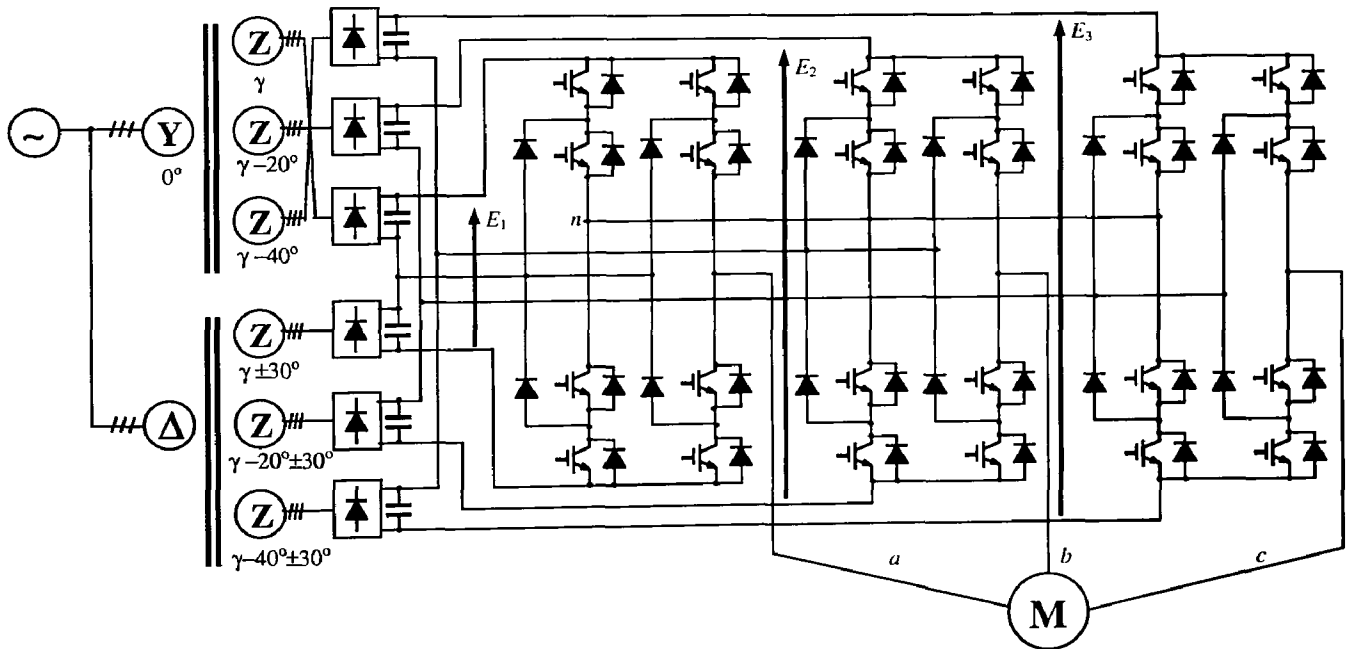


Fig.2-8 DC connection of Application Case 3: for 5-level NPC/H-bridge inverters.

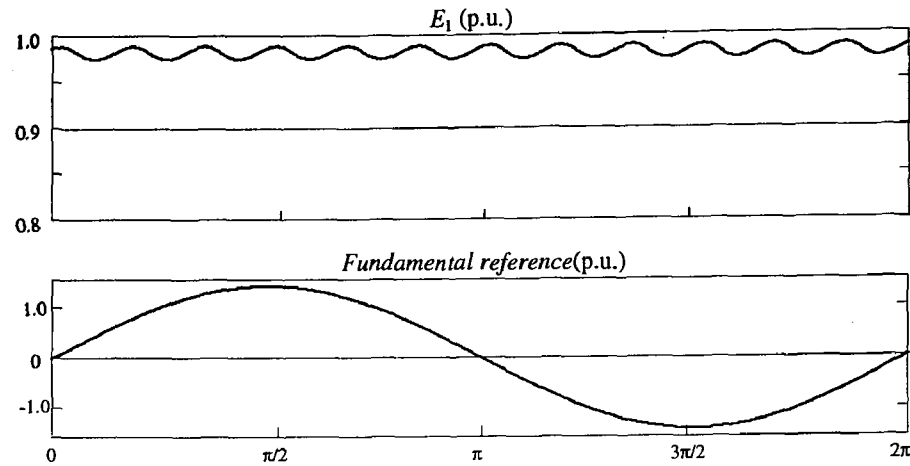


Fig.2-9 Simulated DC output of Application Case 3

2.4.2 Harmonic Neutralization Between Two Drives

The principle of dual 18-pulse rectifiers can also be used to achieve harmonic cancellation between two drives. Fig.2-10 shows such as example, where two 18-pulse converters are matched to cancel the balanced portion of the harmonics, leading to better current waveforms at the up-streaming point of common coupling.

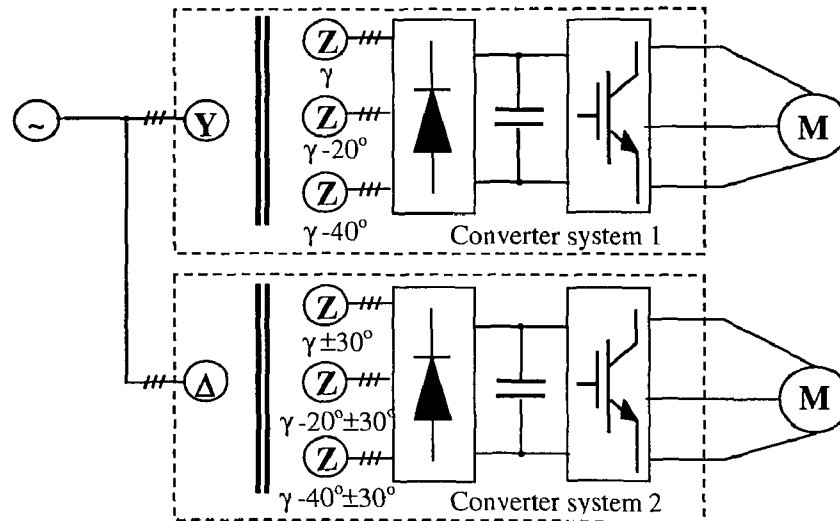


Fig.2-10 Matching two 18-pulse drives for harmonic cancellation.

Another important conclusion drawn from Table 2.3 is that the dual 18-pulse rectification provides additional opportunity for the cancellation of the 5th and 7th harmonics, which are the most troublesome contents. This is especially meaningful for some drives with non-ideal or defective secondaries. For example if phase error occurs, the 5th and 7th harmonics can not be

neutralized within the PSTs, but the balanced portion can be cancelled inter-transformer.

2.4.3 Other Application Concerns

It should also be mentioned that one of the shortcomings of dual 18-pulse rectification is that two transformers are needed. It would be certainly better to use 36-pulse PSTs if someday they could be manufactured at reasonable cost because one bulky transformer will be better in terms of core efficiency and converter size.

Another price paid by 18-pulse rectifiers is the higher voltage ripples in the DC output compared to the conventional 24-pulse rectifiers. Depending on the tolerance, larger the DC link capacitance may be needed, which is also helpful to decouple the inverter with the rectifier so that non-characteristic harmonics are blocked from entering the mains-side. However, with the 5-level topology, the tolerance of ripples should be higher than lower-level inverters.

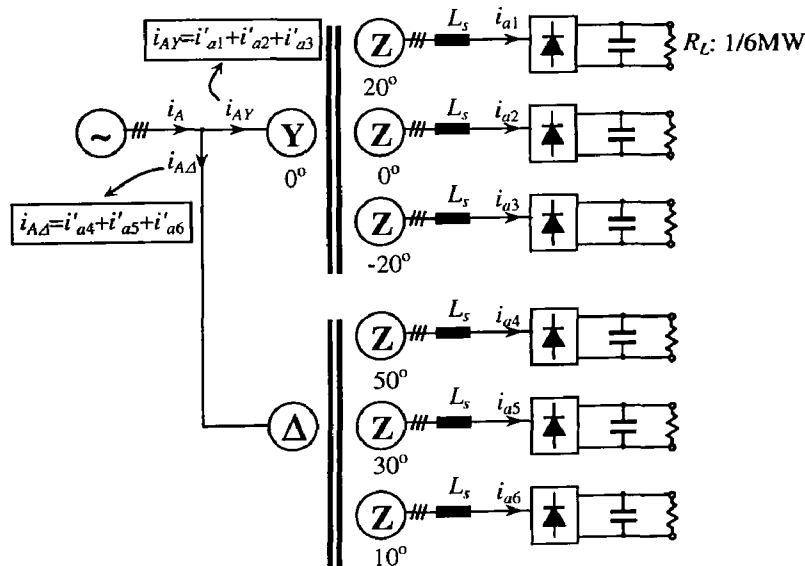


Fig.2-11 Circuit diagram of dual 18-pulse rectifiers for simulation.

2.5 Simulation: Waveforms and Spectra

The circuit used for the simulation is shown in Fig.2-11. In Fig.2-11 and the following discussions, subscript 'A' stands for Phase A of the primary, 'Y' for the Y/Z PST and 'Δ' for

Δ/Z PST. All currents are line currents.

The total mains-side line current is

$$i_A = i_{AY} + i_{A\Delta}, \quad (2.13)$$

where i_{AY} and $i_{A\Delta}$ are the primary currents.

When the secondary line currents, i_{a1} to i_{a6} , are referred to the primary, the reflected currents are i'_{a1} to i'_{a6} , satisfying:

$$i_{AY} = i'_{a1} + i'_{a2} + i'_{a3} \quad (2.14)$$

$$i_{A\Delta} = i'_{a4} + i'_{a5} + i'_{a6} \quad (2.15)$$

Other circuit parameters include:

Rated Load: 1MW; Rated primary voltage: 4160V; Voltage ratio k_v : 4160:1260; Capacitance: 100 μ F per rectifier; Mains-side inductance L_s : 5%, 10% and 15%p.u. (including the line inductance and the leakage inductance); Mains side total resistance R_s : 0.5% p.u.;

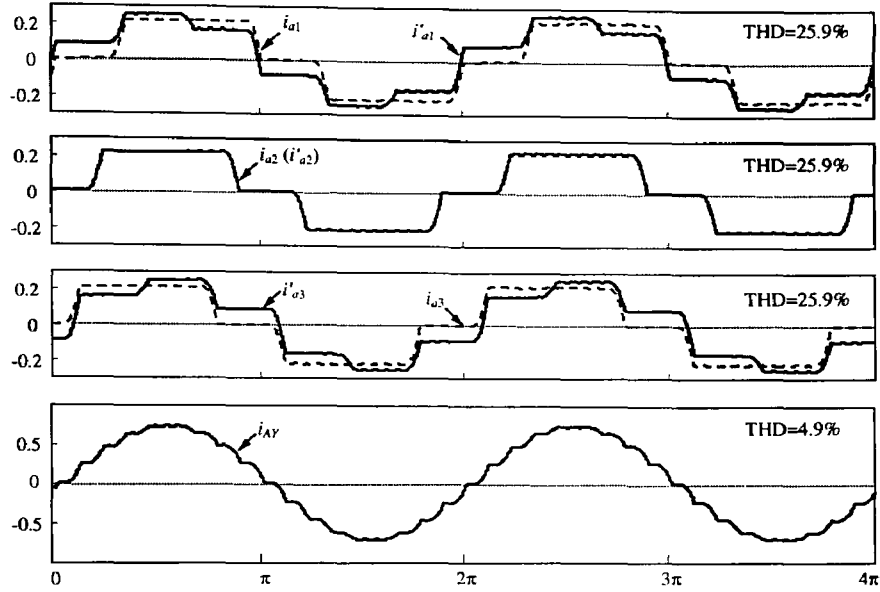
The DC connection in Fig.2-11 adopts Application Case 1 (Section 2.4.1). If other DC connection schemes are to be simulated, the connections and the load resistance should be adjusted accordingly.

2.5.1 Ideal Transformers

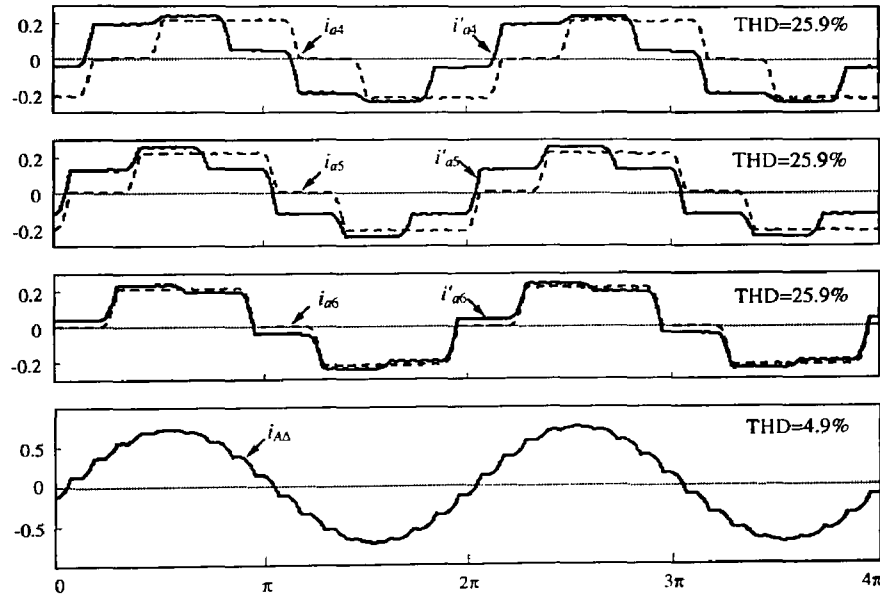
Assume the 18-pulse transformers are ideal: the phase-shifting angles are accurate and the leakage inductances of all the secondary windings are balanced.

Fig.2-12 shows the simulated current waveforms when $L_s=0.15$ p.u. and the load $P=1$ p.u. All the currents labelled in Fig.2-11 for the PST with Y-primary are shown in Fig.2-12(a). It can be seen that the shape of the reflected currents are different from the primary currents. This is because the PST changes the phase angle of the harmonics. As a result, the primary current i_{AY} is much more sinusoidal. It is also interesting that the THD of the referred currents are the same as the corresponding secondary currents. Similarly the currents of the PST with D-primary are shown in Fig.2-12(b). Again all the secondary currents and the reflected currents have the same THD and the primary current $i_{A\Delta}$ is more sinusoidal. The total current

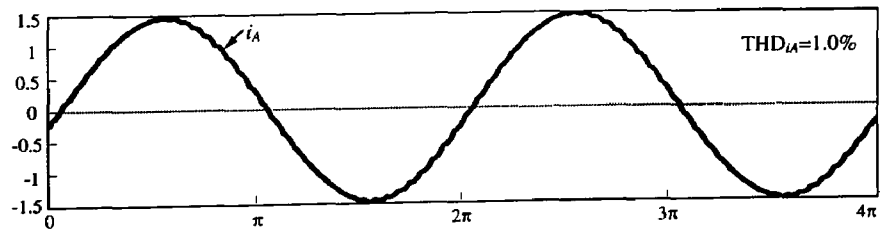
of the dual 18-pulse rectifier is shown in Fig.2-12(c), from which it can be seen that the shape of the total current i_A is better than both i_{AY} and $i_{A\Delta}$.



(a) currents in PST with Y-primary(in p.u.)



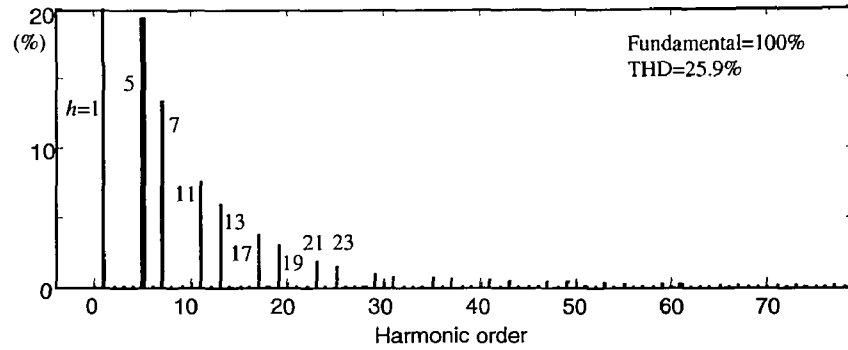
(b) currents in the PST with Δ -primary (in p.u.)



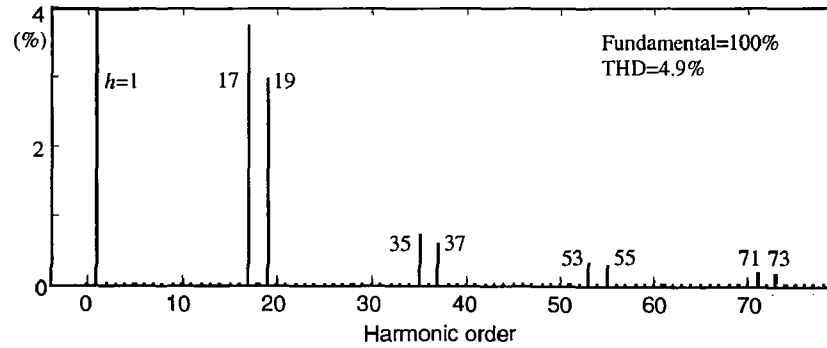
(c) the total current(in p.u.)

Fig.2-12 Simulated current waveforms
($L_s=0.15$ p.u. and 1p.u. load)

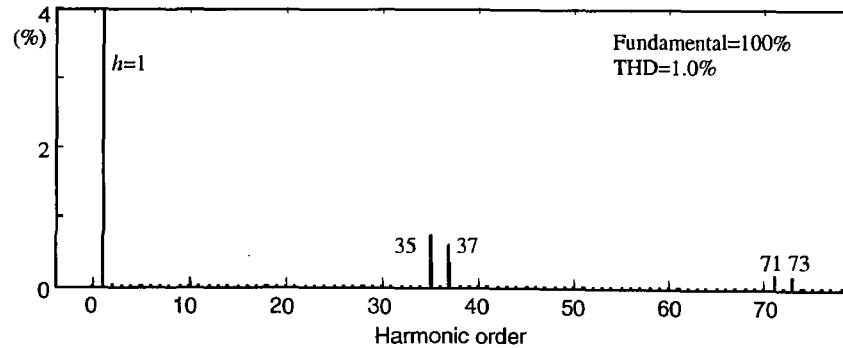
The spectra of the currents are shown in Fig.2-13. All the secondary currents and the reflected currents have the same spectrum, which is shown in Fig.2-13(a) and contains all sorts of non-triplen odd harmonics with a THD of 25.9%. The spectra of the primary currents i_{AY} and i_{AD} are the same as shown in Fig.2-13(b). The lowest order is the 17th and the THD decreases to 4.9%. The spectrum is typical of 18-pulse rectifiers. The spectrum of i_A is shown in Fig.2-13(c), where the lowest order harmonic is the 35th and the THD is 1%.



(a) Spectrum of i_{a1} - i_{a6} and i'_{a1} - i'_{a6} currents



(b) Spectrum of i_{AY} and i_{AD}



(c) Spectrum of i_A

Fig.2-13 Simulated spectra of the currents

The THD of the input current versus the load is shown in Fig.2-14 with L_s as a parameter. The THD decreases with the increasing load and inductance. As a conceptual fact, the THD of

the dual 18-pulse rectifier is about (1~3)% when the mains-side total inductance is 0.05 to 0.15 p.u. at rated load.

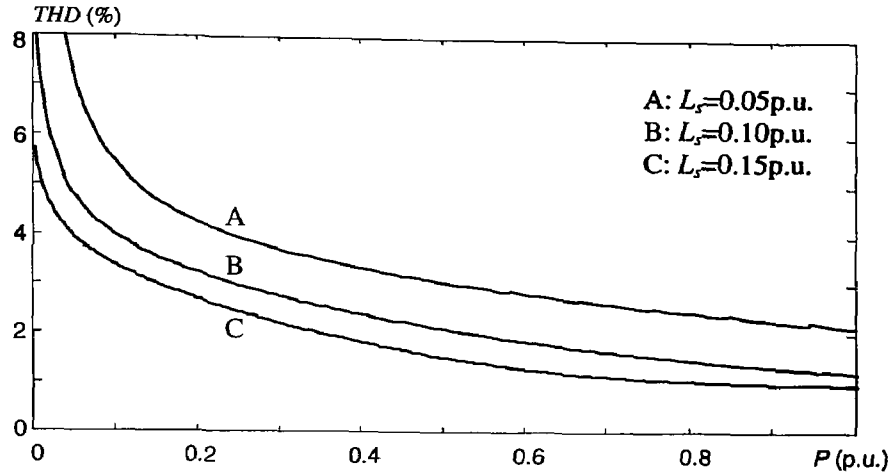
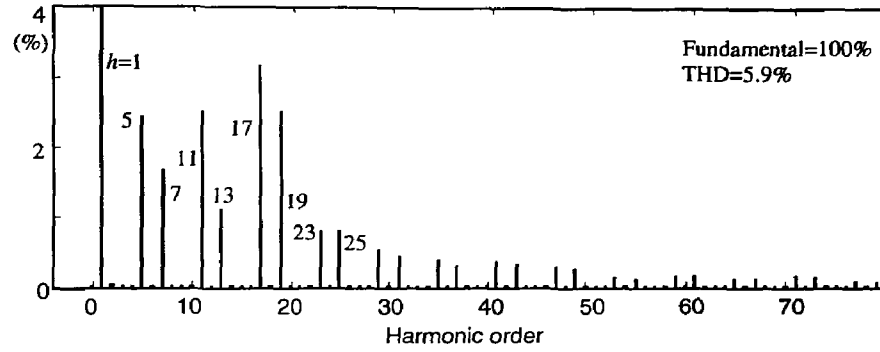
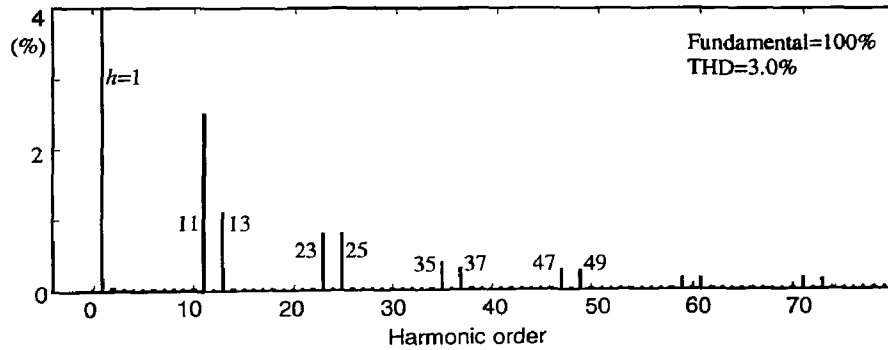


Fig.2-14 Simulated THD of the input current versus load



(a) Spectrum of i_{AY} and i_{aA}



(b) Spectrum of i_A

Fig.2-15 Simulated spectra of the currents of non-ideal PSTs

2.5.2 Non-Ideal Transformers

If the PSTs are non-ideal, i.e. with either phase shifting errors or unbalanced leakage inductances, certain amount of lower order harmonics will appear in the spectra of i_{AY} and i_{aA} .

To simulate this case, assume each transformer has a defective secondary whose phase shifting angle has a -3.7° error while the load condition and inductance are kept unchanged, i.e. at rated load with $L_s=15\%$ p.u. The simulated spectra of i_{AY} (i_{AD}) and i_A are shown in Fig.2-15. Lower order harmonics appear in the spectra of i_{AY} and i_{AD} (Fig.2-15(a)), leading to a THD of 5.9%. However, the spectrum of i_A contains fewer harmonics (Fig.2-15(b)). The harmonics such as 5th, 7th, 17th and 19th, are all cancelled. The THD of i_A decreases to 3.0%. This is consistent with the theoretical expectation of Table 2.3: Pattern 2 results in the extra harmonic cancellations.

2.6 Summary

This chapter introduces the dual 18-pulse PST based rectifiers. Compared to the 24-pulse rectifiers or 30-pulse rectifiers which are used in practice, the proposed topology has the following features:

(1) Simpler transformer and reduced secondary windings. Standard 18-pulse PSTs are used instead of more complicated 24-pulse or 30-pulse PSTs. The total number of windings is decreased to 8, in comparison with 13 windings of the 24-pulse rectifiers.

(2) Improved harmonic cancellation. The dual 18-pulse rectifiers can achieve 36-pulse cancellation for ideal PSTs. When the PSTs are non-ideal, extra harmonic cancellation is available for some important harmonics, such as the 5th and 7th.

(3) The principle of dual 18-pulse rectifiers can also be used to achieve inter-transformer harmonic neutralization for two drives.

(4) The topology can be used to power different multilevel inverters, including 3-level NPC inverters, 5-level H-bridge inverters and 5-level NPC/H-bridge inverters.

The main drawback of the suggested rectification is that it needs two transformers, and in some cases larger DC link capacitors are needed to suppress voltage ripples and to achieve better decoupling effect.

CHAPTER 3 SPACE VECTOR MODULATION

The main challenges of the space vector modulation algorithms for multilevel inverters are originated from the large number of redundant switching states and stationary vectors. The simplification of the switching sequence design, the reduction of device switching frequencies and the optimization of harmonic profile are all the major concerns. This chapter will focus on these concerns. The switching sequence design will be simplified by a ‘sequence reproduction’ mechanism and rule-based sequence design. Then it will be applied to the conventional 7-segment SVM for the control of 5-level NPC/H-bridge inverters. A novel SVM scheme with flexible 3-segment sequence will be proposed for multilevel inverters. The proposed SVM reduces the device switching frequencies, achieves better harmonic performance, and is convenient for digital implementation.

3.1 Simplification of Switching Sequence Design

The switching sequence design is to be simplified in two ways. First, a **sequence reproduction mechanism** is used to obtain the switching sequence for any sampling period by ‘copying’ the sequence which was used 1/6 fundamental period (60°) ago. The 60° angle in the sequence reproduction mechanism coincides with the 60° sector span of the vector plot and is convenient to be integrated into the SVM algorithm. Second, the sequence design is based on triangle types rather than specific triangles. Once the rule is designed for several triangle types, the switching sequence can be generated for the numerous triangles in real time.

3.1.1 Switching Sequence Reproduction

It happens frequently that the resultant waveform of SVM contains unwanted triplen harmonics or even-order harmonics. The reason of these harmonics is the lack of three-phase (TP) symmetry or half-wave (HW) symmetry. The best way to ensure waveform symmetry is to reproduce the switching sequence in a symmetrical way. It will be shown later that the

'sequence reproduction' mechanism introduced in this section also brings significant simplification to the sequence design.

The necessary and sufficient condition for half-wave symmetry of SVM requires that if we use switching state $[S_a, S_b, S_c]$ at certain moment ① in sector n ($n=1,2,3$), then after 180° at moment ② in sector $n+3$, the complementary state $-[S_a, S_b, S_c]$ should be used (Fig.3-1(a)).

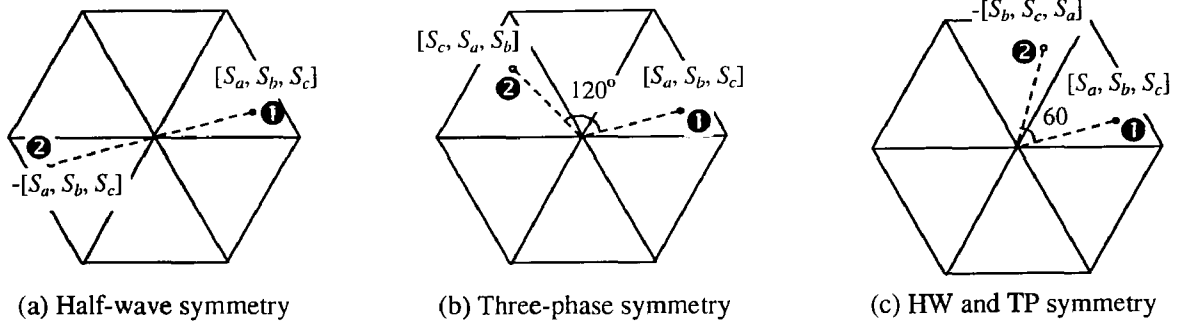


Fig.3-1 Waveform symmetry represented by switching states.

Similarly, the necessary and sufficient condition for three-phase (TP) symmetry requires that if we use switching state $[S_a, S_b, S_c]$ at certain moment ①, then after 120° at moment ②, the switching state should be $[S_c, S_a, S_b]$ (Fig.3-1(b)).

The above two symmetries can be expressed as a uniform 60° -symmetry, i.e. if at certain moment ①, the switching state is $[S_a, S_b, S_c]$, then after 60° at sampling point ②, the switching state should be $-[S_b, S_c, S_a]$ (Fig.3-1(c)).

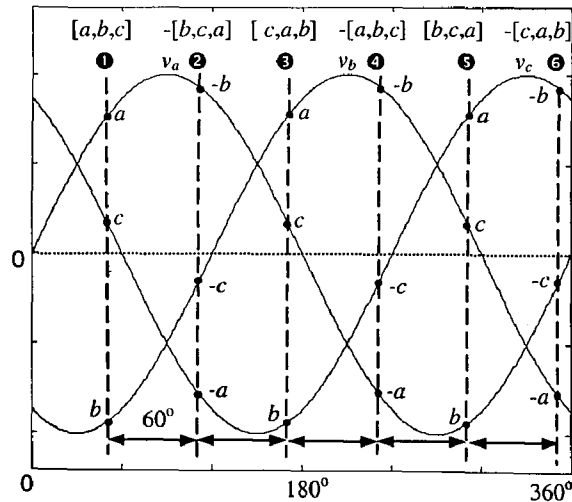


Fig.3-2 Waveform presentation of the 60° symmetry

It is much easier to understand the 60° -symmetry by waveform presentation in Fig.3-2, where the 3-phase voltages are marked on the waveforms every 60° . The voltages for the two adjacent moments are of 60° -symmetry, for example, the voltage at the moment ③ is $[c, a, b]$, and it is $-[a, b, c]$ at the moment ④.

The 60° -symmetry can be exploited for switching sequence design: After we finished sequence design in Sector I, the switching sequences for the other sectors can be obtained by 'negative rotation', i.e. rotate the switching state of phase B to phase A, C and to B and A to C, then change the sign of result. For example, if a 7-segment sequence, $[1,1,0] \rightarrow [1,0,0] \rightarrow [1,0,-1] \rightarrow [0,0,-1] \rightarrow [1,0,-1] \rightarrow [1,0,0] \rightarrow [1,1,0]$ is used for a triangle in Sector I of a 5-level inverter, then the switching sequence for the corresponding triangle in Sector II can be easily obtained as $[-1,0,-1] \rightarrow [0,0,-1] \rightarrow [0,1,-1] \rightarrow [0,1,0] \rightarrow [0,1,-1] \rightarrow [0,0,-1] \rightarrow [-1,0,-1]$ by 'negative rotation'. This process remarkably simplifies the switching sequence design.

3.1.2 Sequence Design by Triangle Types

For high-level inverters, it is a tedious task to design switching sequence even just for Sector I. Fortunately the triangles can be classified^[26].

Using the method introduced in Appendix 1, the vector plot of the 5-level NPC/H-bridge inverter can be drawn in Fig.3-3, which utilized hexangular g - h coordinate system. The vector plot contains 125 switching states, which belong to 61 stationary vectors. The switching states are represented by the integral triples in square brackets. The stationary vectors are located on the peripheral of 4 concentric hexagons, which are divided into 6 sectors and partitioned by 64 small regular triangles. The triangles can be categorized into 4 types, T_1 to T_4 . T_1 and T_3 represent triangles containing odd number of switching states while T_2 and T_4 have even number of switching states. T_1 and T_2 are standing upright and T_3 and T_4 up-side-down. The classification is made because the number of switching states in a triangle and its orientation

affect the sequence design.

In the following discussions, the switching sequence design will be based on the triangle types, rather than specific triangles.

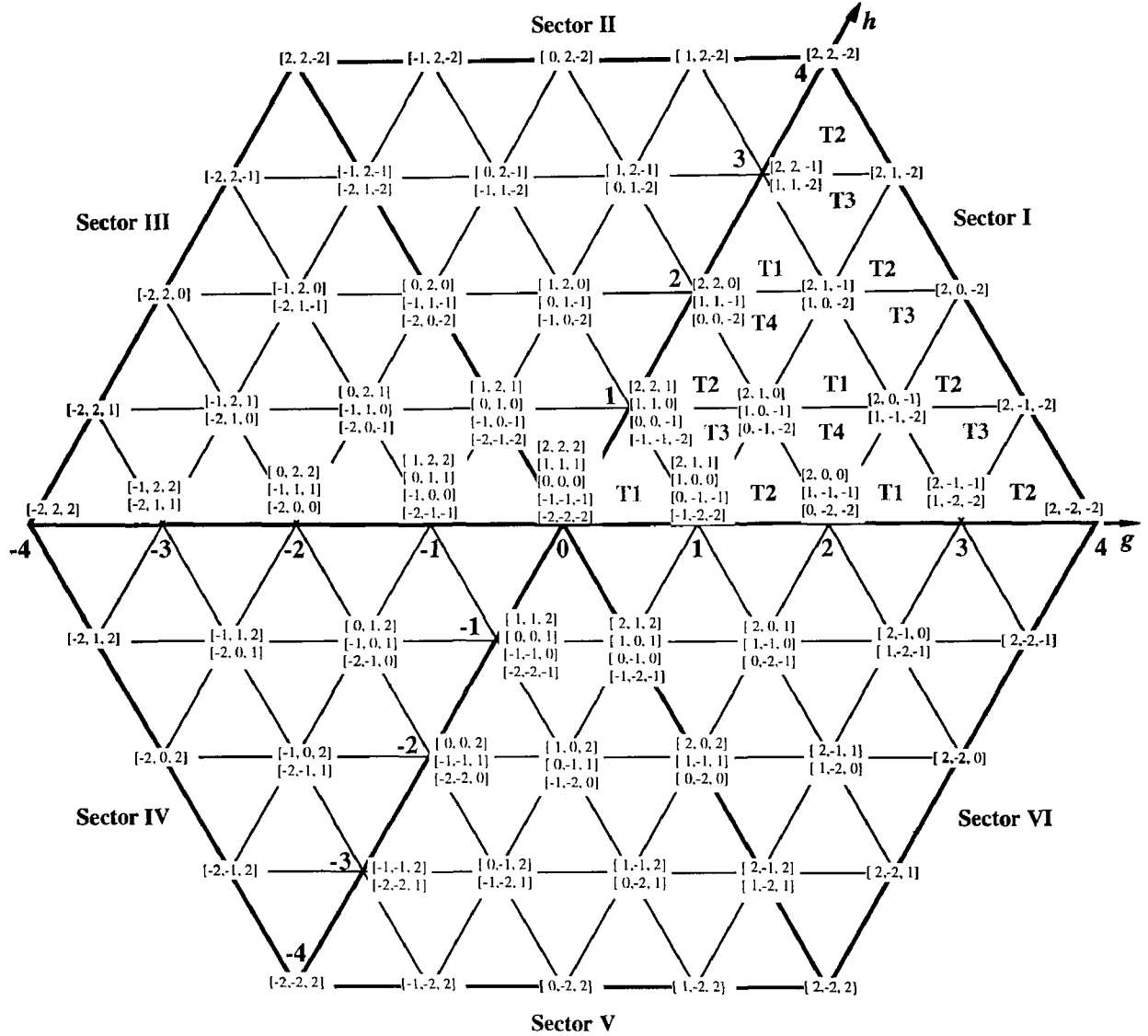


Fig.3-3 The vector plot of 5-level inverters

3.2 Seven-Segment SVM for NPC/H-Bridge Inverters

Depending on how many pieces the sampling cycle T_s is divided into, the switching sequence can be named differently. Fig.3-4 shows an example of the 7-segment switching sequence for NPC/H-bridge inverters. The reference vector \mathbf{V}_{ref} is located in ΔABC and five of its redundant switching states are shown in Fig.3-4(a). The dwell times of the three vertices

are T_A , T_B and T_C . The waveform of three-phase switching states S_a , S_b and S_c are shown in Fig.3-4(b). The whole sampling period T_s is divided into 7-segments. During each piece of time segment, different switching states are used: state $[2,1,-1]$ of vertex C is used in the first time segment, $[2,0,-1]$ of B for the second segment and so on. The switching sequence can be represented by a train of switching states: $[2,1,-1] \rightarrow [2,0,-1] \rightarrow [1,0,-1] \rightarrow [1,0,-2] \rightarrow [1,0,-1] \rightarrow [2,0,-1] \rightarrow [2,1,-1]$. Here the switching state of the first time segment is called the **leading state** of the sequence while the switching state of the last time segment is called the **ending state**. For the 7-segment sequence, the leading state is same as the ending state.

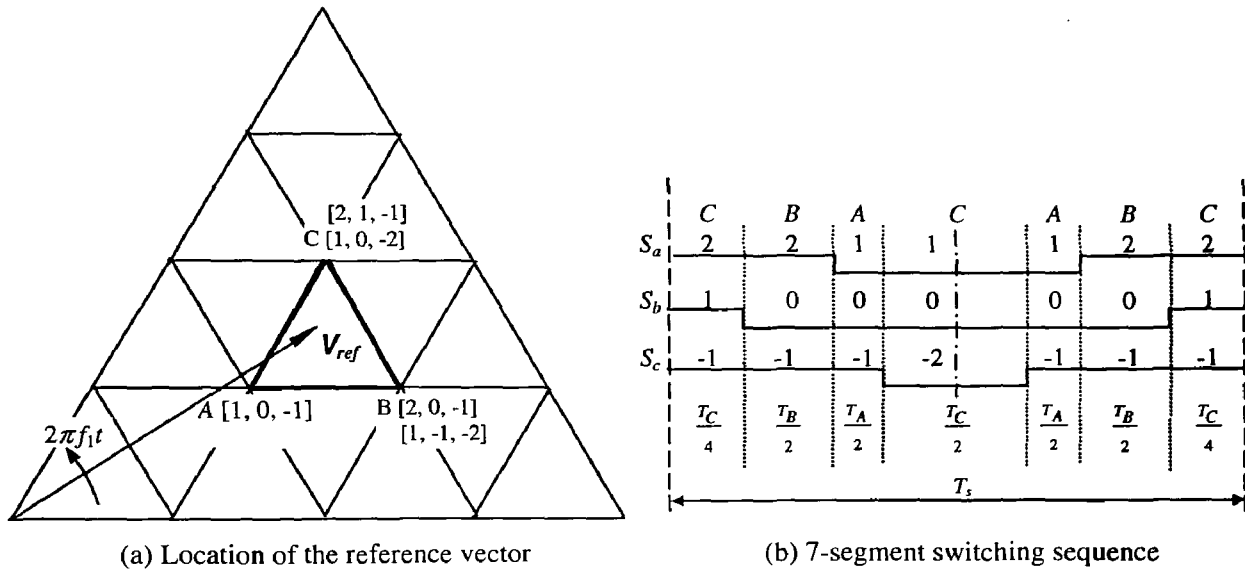


Fig.3-4 The 7-segment switching sequence

The 7-segment sequence features the following^[1]:

- (1) Each phase has 2-switching transitions per sampling period;
- (2) Each transition involves only 1 voltage step, indicating there are only two switching devices operating at each transition.
- (3) The whole sequence involves 4 switching states, two of them are redundant switching states of the same vertex of the triangle; the sequence must start from and end with the same redundant switching state.
- (4) The sequence is symmetrical about $T_s/2$.

It can also be deduced that when the 7-segment SVM is applied to the NPC/H-bridge

inverter, the ideal average device switching frequency for is

$$f_{sw-ideal} = f_{sp}/4 \quad (3.1)$$

The inverter sampling frequency is:

$$f_{inv-sp} = f_{sp} = 4f_{sw-ideal} \quad (3.2)$$

Before designing the 7-segment sequences for multilevel inverters, we must decide how to select redundant switching states.

3.2.1 Selection of the Redundant Switching States

For convenience, let's first index the switching states. Define state value of a switching state $[S_a, S_b, S_c]$ as:

$$S = \sum_{i=a,b,c} S_i \quad (3.3)$$

which actually reflects the level of common mode voltage.

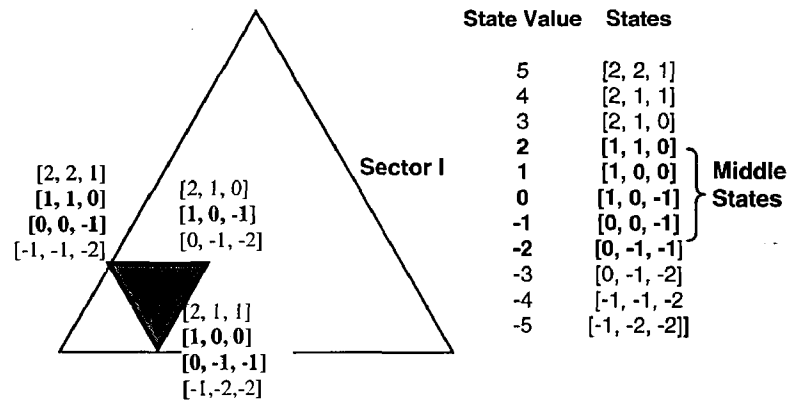


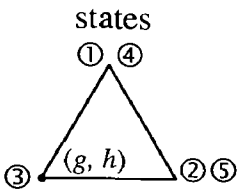
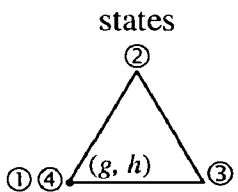
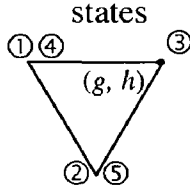
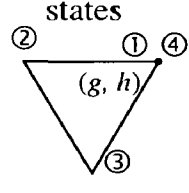
Fig.3-5 Middle switching states

The switching states can be indexed by S . Fig.3-5 shows a triangle of the vector plot of a 5-level inverter. There are altogether 11 switching states which are listed at the right side by descending state values. It can be seen that the state values are an arithmetic sequence. The switching states corresponding to the 5 state values in the middle of the arithmetic sequence are called middle states. In fact the middle states on the list are also the middle states of the corresponding vertex. The vertex with odd number of redundant states has one middle state

otherwise it has two. If a vertex has two middle states, the one with larger state value is called **large state**, the other is called **small state**^[26].

Triangles of T_1 and T_3 types have 5 middle states and Triangles of T_2 and T_4 types have 4. The middle states are also the states with the least common mode voltage.

Table 3.1 The middle switching states for T_1 to T_4

T_1			T_2		
					
#	Middle State	S	#	Middle State	S
①	$[h+g+2, h-g+2, -h-g]/2$	$0.5(h-g)+2$	①	$[h+g+1, h-g+1, -h-g+1]/2$	$0.5(h-g)+1.5$
②	①-[0,1,0]	$0.5(h-g)+1$	②	①-[0,0,1]	$0.5(h-g)+0.5$
③	①-[1,1,0]	$0.5(h-g)$	③	①-[0,1,1]	$0.5(h-g)-0.5$
④	①-[1,1,1]	$0.5(h-g)-1$	④	①-[1,1,1]	$0.5(h-g)-1.5$
⑤	①-[1,2,1]	$0.5(h-g)-2$			
T_3			T_4		
					
#	Middle State	S	#	Middle State	S
①	$[h+g, h-g+2, -h-g+2]/2$	$0.5(h-g)+2$	①	$[h+g+1, h-g+1, -h-g+1]/2$	$0.5(h-g)+1.5$
②	①-[0,1,0]	$0.5(h-g)+1$	②	①-[1,0,0]	$0.5(h-g)+0.5$
③	①-[0,1,1]	$0.5(h-g)$	③	①-[1,1,0]	$0.5(h-g)-0.5$
④	①-[1,1,1]	$0.5(h-g)-1$	④	①-[1,1,1]	$0.5(h-g)-1.5$
⑤	①-[1,2,1]	$0.5(h-g)-2$			

For a given triangle with a base vertex (g, h) (see Appendix 1 for 'base vertex'), the middle states and the corresponding state values can be calculated according to Table 3.1, where the middle states are numbered as ① to ⑤ according to the state value for easy programming. State ① has the largest state value.

The sequence design involves only the middle states in this thesis mainly for two reasons: better THD profiles and smoother transition from one triangle to the other as reported by other researchers^{[24][26][27]}, in addition to the awareness of common mode voltage indication.

Now the focus can be set to Sector I with only middle states, which is shown in Fig.3-6 and is a part of Fig.3-3. The triangles are now numbered from 1 to 16 for convenient citation. The switching sequence for the other sectors can be reproduced by negative rotation.

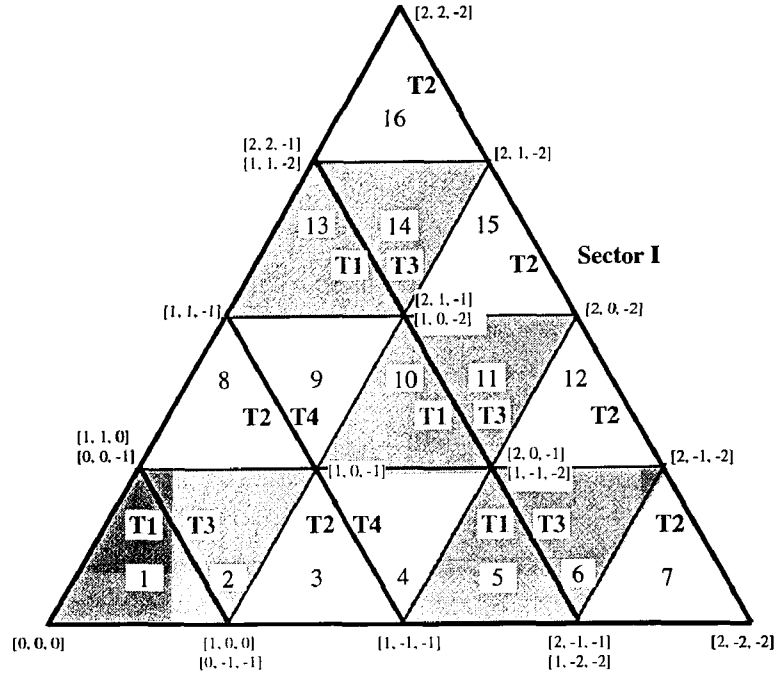
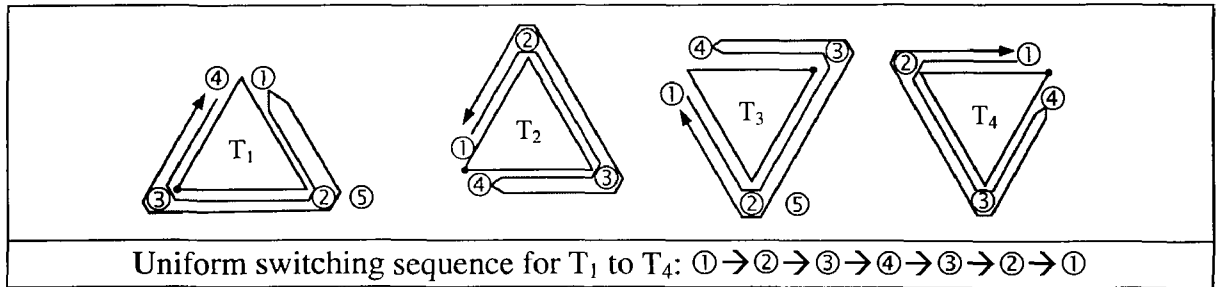


Fig.3-6 Sector I with only middle states

Table 3.2 Seven-segment switching sequences for T_1 to T_4



3.2.2 Design of Seven-Segment Switching Sequence

The sequence-design rule of the 4 types of triangles are shown in Table 3.2, where 4-types of triangles have the uniform switching sequence: ①→②→③→④→③→②→①. Because the 7-segment switching sequence can only start from the vertices with even redundant switching states, there are two possible switching sequences for T_1 or T_3 . Since the space vector rotates counter-clockwisely, the upper vertex is preferred to be used at the beginning and the end of

the sequences for smoother transition between triangles. Thus another possible switching sequence involving state ⑤ is not used. For T_2 or T_4 , there is only one switching sequence.

The fact that the 7-segment sequence must finally switch back to the leading state is actually a rigid constraint for sequence design. It can be eased by the more flexible 3-segment sequence which is to be discussed in Section 3.3.

Applying the uniform sequence to Sector I, we have the switching sequence for each triangle listed in Table 3.3. The sequences for the other sectors can be obtained by the 'negative rotation' described in Section 3.1.1.

Table 3.3 The switching sequence for Sector I

Triangle	Sequence
1	$[1,1,0] \rightarrow [1,0,0] \rightarrow [0,0,0] \rightarrow [0,0,-1] \rightarrow [0,0,0] \rightarrow [1,0,0] \rightarrow [1,1,0]$
2	$[1,1,0] \rightarrow [1,0,0] \rightarrow [1,0,-1] \rightarrow [0,0,-1] \rightarrow [1,0,-1] \rightarrow [1,0,0] \rightarrow [1,1,0]$
3	$[1,0,0] \rightarrow [1,0,-1] \rightarrow [1,-1,-1] \rightarrow [0,0,-1] \rightarrow [1,-1,-1] \rightarrow [1,0,-1] \rightarrow [1,0,0]$
4	$[2,0,-1] \rightarrow [1,0,-1] \rightarrow [1,-1,-1] \rightarrow [1,-1,-2] \rightarrow [1,-1,-1] \rightarrow [1,0,-1] \rightarrow [2,0,-1]$
5	$[2,0,-1] \rightarrow [2,-1,-1] \rightarrow [1,-1,-1] \rightarrow [1,-1,-2] \rightarrow [1,-1,-1] \rightarrow [2,-1,-1] \rightarrow [2,0,-1]$
6	$[2,0,-1] \rightarrow [2,-1,-1] \rightarrow [2,-1,-2] \rightarrow [1,-1,-2] \rightarrow [2,-1,-2] \rightarrow [2,-1,-1] \rightarrow [2,0,-1]$
7	$[2,-1,-1] \rightarrow [2,-1,-2] \rightarrow [2,-2,-2] \rightarrow [1,-2,-2] \rightarrow [2,-2,-2] \rightarrow [2,-1,-2] \rightarrow [2,-1,-1]$
8	$[1,1,0] \rightarrow [1,1,-1] \rightarrow [1,0,-1] \rightarrow [0,0,-1] \rightarrow [1,0,-1] \rightarrow [1,1,-1] \rightarrow [1,1,0]$
9	$[2,1,-1] \rightarrow [1,1,-1] \rightarrow [1,0,-1] \rightarrow [1,0,-2] \rightarrow [1,0,-1] \rightarrow [1,1,-1] \rightarrow [2,1,-1]$
10	$[2,1,-1] \rightarrow [2,0,-1] \rightarrow [1,0,-1] \rightarrow [1,0,-2] \rightarrow [1,0,-1] \rightarrow [2,0,-1] \rightarrow [2,1,-1]$
11	$[2,1,-1] \rightarrow [2,0,-1] \rightarrow [2,0,-2] \rightarrow [1,0,-2] \rightarrow [2,0,-2] \rightarrow [2,0,-1] \rightarrow [2,1,-1]$
12	$[2,0,-1] \rightarrow [2,0,-2] \rightarrow [2,-1,-2] \rightarrow [1,-1,-2] \rightarrow [2,-1,-2] \rightarrow [2,0,-2] \rightarrow [2,0,-1]$
13	$[2,2,-1] \rightarrow [2,1,-1] \rightarrow [1,1,-1] \rightarrow [1,1,-2] \rightarrow [1,-1,-1] \rightarrow [2,1,-1] \rightarrow [2,2,-1]$
14	$[2,2,-1] \rightarrow [2,1,-1] \rightarrow [2,1,-2] \rightarrow [1,1,-2] \rightarrow [2,1,-2] \rightarrow [2,1,-1] \rightarrow [2,2,-1]$
15	$[2,1,-1] \rightarrow [2,1,-2] \rightarrow [2,0,-2] \rightarrow [1,0,-2] \rightarrow [2,0,-2] \rightarrow [2,1,-2] \rightarrow [2,1,-1]$
16	$[2,2,-1] \rightarrow [2,2,-2] \rightarrow [2,1,-2] \rightarrow [1,1,-2] \rightarrow [2,1,-2] \rightarrow [2,2,-2] \rightarrow [2,2,-1]$

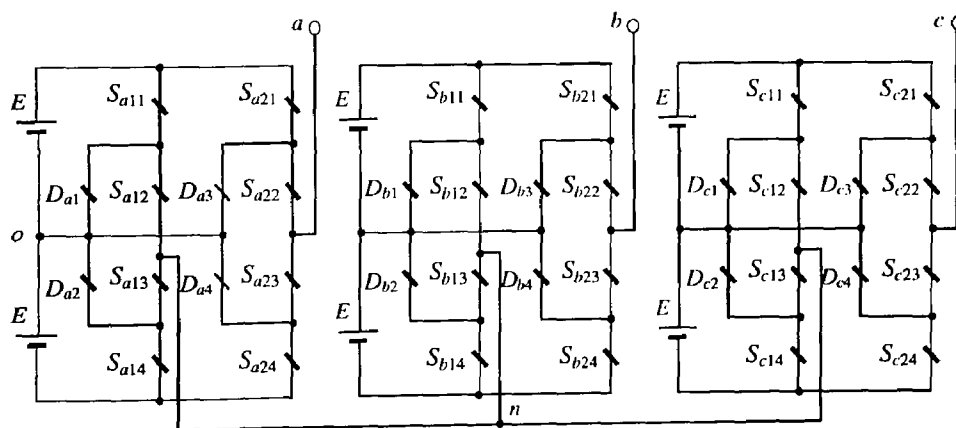


Fig.3-7 Sketch topology of the NPC/H-bridge inverter with isolated DC sources

3.2.3 Typical Waveforms

The performance of the 7-segment SVM has been simulated by modulating the 5-level NPC/H-bridge inverter. The topology is re-sketched in Fig.3-7 for convenient viewing, where each bridge is powered by two isolated DC source with equal voltage E .

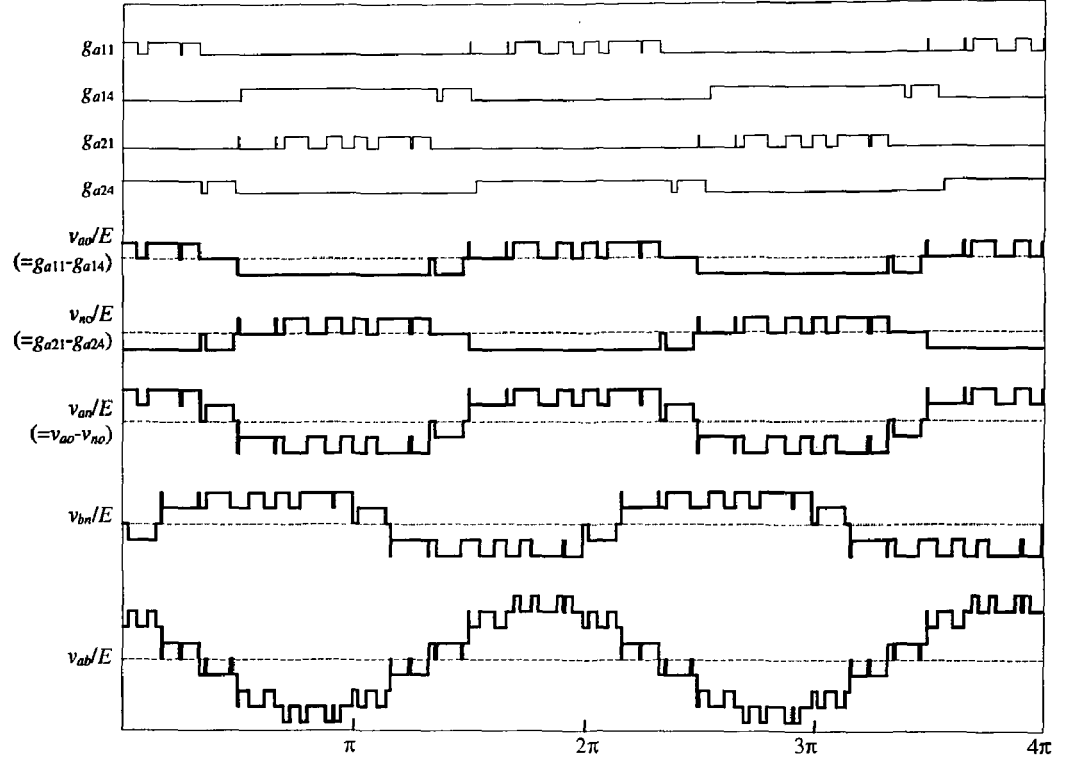


Fig.3-8 Typical waveforms of NPC/H-bridge inverter with 7-segment SVM

($m_a=0.87, f_{sp}=720\text{Hz}$)

Fig.3-8 shows a set of typical waveforms. The gating signals for switches S_{a11} , S_{a14} , S_{a21} and S_{a24} are shown in the top 4 traces. The normalized voltages, v_{a0}/E , v_{n0}/E , v_{an}/E , v_{bn}/E , v_{ab}/E are shown in the other traces. It can be seen the voltage of each arm (v_{a0}/E or v_{n0}/E) is 3-level, the phase voltage (v_{an}/E or v_{bn}/E) is 5-level and the line voltage is 9-level.

The normalized *rms* value of the fundamental line voltage versus m_a or V_{ref} is shown in Fig.3-9, where V_{ref} is modulus of the reference vector normalized by $2E/3$. For 5-level inverters, m_a is

$$m_a = \frac{V_{ref}}{2\sqrt{3}} \quad (3.4)$$

From Fig.3-9 we can conclude:

$$V_{1rms} = 2\sqrt{2}m_a E = \sqrt{\frac{2}{3}}V_{ref} E \quad (3.5)$$

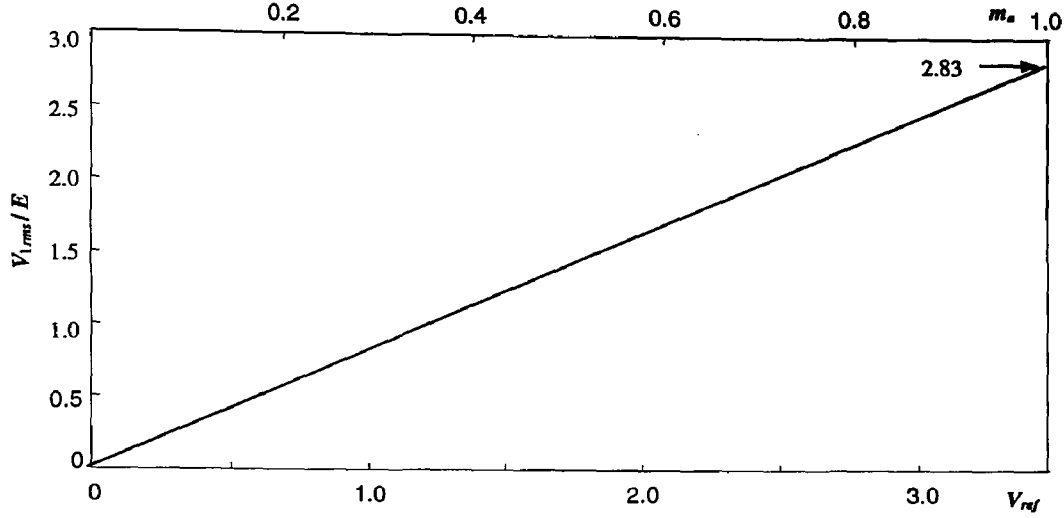


Fig.3-9 Simulated fundamental voltage versus m_a (7-segment SVM)

To take the frequency response into account when the choppy voltage is imposed on inductive loads, weighted THD (WTHD) is used to evaluate the quality of waveforms^[24]:

$$WTHD = \frac{1}{V_{1rms}} \sqrt{\sum_{h=2}^{\infty} \left(\frac{V_{hrms}}{h} \right)^2} \quad (3.6)$$

where h is the harmonic order, V_{hrms} is the rms value of the h^{th} harmonic ($h=1,2,3\dots$).

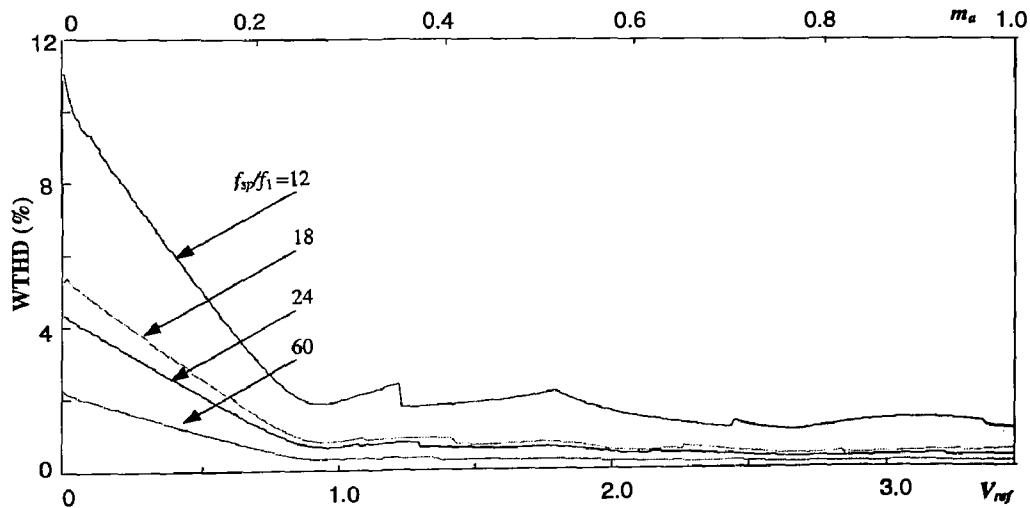


Fig.3-10 Simulated WTHD versus m_a (7-segment SVM)

Fig.3-10 shows the WTHD of the line voltage versus V_{ref} with f_{sp}/f_1 as a parameter. It can

be seen that higher sampling frequency results in lower WTHD. However, the improvement is limited at large modulation index ($V_{ref} > 1$) when f_{sp}/f_1 increases to more than 24. More simulation results will be given in Section 3.4.

3.3 SVM with Flexible Three-Segment Sequence

The major motives of the 3-segment SVM are to minimize the device switching frequency and to increase the inverter sampling frequency. The flexibility of the algorithm comes from the adaptive 3-segment sequence design, compared to the predefined switching patterns used in 7-segment SVM.

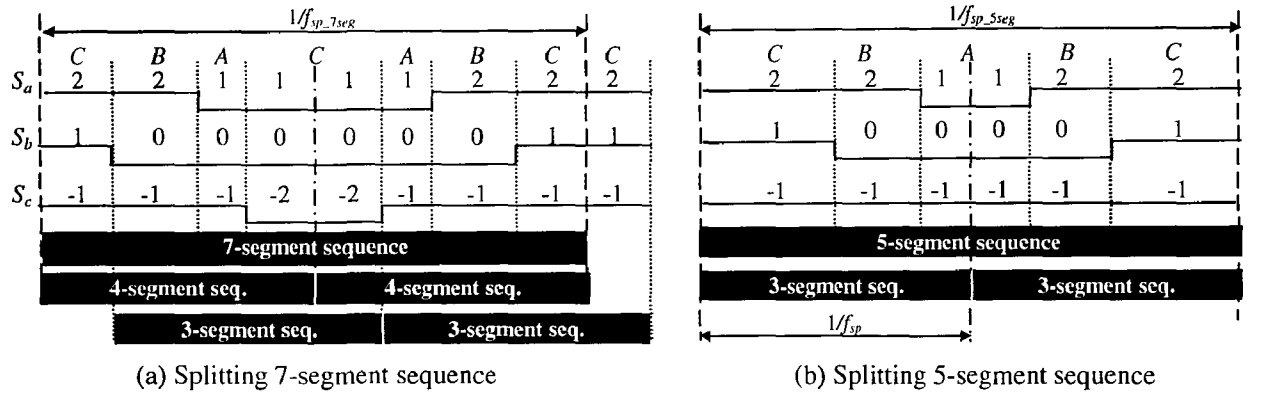


Fig.3-11 Splitting switching sequences

3.3.1 Split Sequence and Inverter Sampling Frequency

As was shown in the last section, there are 6 switching transitions bound in each sampling period of a 7-segment sequence. The 6 switching transitions are scheduled based on the dwell times calculated at the beginning of the sampling period. In fact, the dwell times can also be updated at any moment within the sampling period. If they are updated at the centre of the sampling period, the 7-segment sequence is split into two 4-segment sequences, which are in fact equivalent to asymmetrical 7-segment scheme. It has been proven by other researchers that asymmetrical PWM is superior over symmetrical PWM because symmetrical PWM causes additional sideband harmonic components^[24].

Actually the sequence can be split in different ways. For the reference vector shown in

Fig.3-4(a), the conventional switching sequences, such as the 7-segment and 5-segment sequences, can be split as shown in Fig.3-11. The 7-segment switching sequence can be split as two 4-segment sequences as mentioned earlier, or as two 3-segment sequences as shown in Fig.3-11(a). The 4-segment sequence involves 4 switching states, and it must start at the vertex with even redundant switching states. This constraint will cause extra switchings, just like the 7-segment sequences. The two 3-segment sequences are different sequences and complicated to use because they must be applied alternatively.

Fig.3-11(b) shows the splitting of 5-segment SVM. Two 3-segment sequences are obtained and one is the reversal of the other. The whole sampling period($1/f_{sp_5seg}$) is equally divided into two sampling periods ($1/f_{sp}$). Because the 3-segment sequences involve only 3 switching states and are able to start with any switching states of any vertex, they are more flexible. The three-segment sequences shown in Fig.3-11(b) will be adopted to modulate the NPC/H-bridge inverter. The ideal average device switching frequency for the NPC/H-bridge is now

$$f_{sw-ideal} = f_{sp}/12 \quad (3.7)$$

The inverter sampling frequency, or the centre frequency of the 1st sideband, is:

$$f_{inv-sp} = f_{sp}/2 = 6f_{sw-ideal} \quad (3.8)$$

Comparing Eqs. (3.1) and (3.2) we can expect that for the same ideal average device switching frequency, the 3-segment SVM achieves higher inverter sampling frequency.

3.3.2 Extra Switchings

The 7-segment switching pattern discussed in Section 3.2 is a kind of SVM schemes using predefined switching patterns: the switching sequence doesn't change for the same triangle no matter what modulation indices or sampling frequencies are used. This may cause extra switchings. Extra switchings happen when the leading state is not same as the ending state of the last sequence. Now let's analyze the extra switchings caused by the 7-segment SVM.

Fig.3-12 shows the distribution of the reference vectors when $f_{sp}/f_1=18$ where the reference vector stops at three sampling points A , B and C when it revolves across Sector I. When m_a changes, the sampling points move along the sampling lines OX , OY and OZ , involving different triangles. For example, when $V_{ref} < oy_1$, the sampling points are located within the innermost circle and only Triangle 1 is involved. If $oy_1 < V_{ref} < ox_1$, the sampling points are within the first innermost circular band, which involves Triangles 1 and 2.

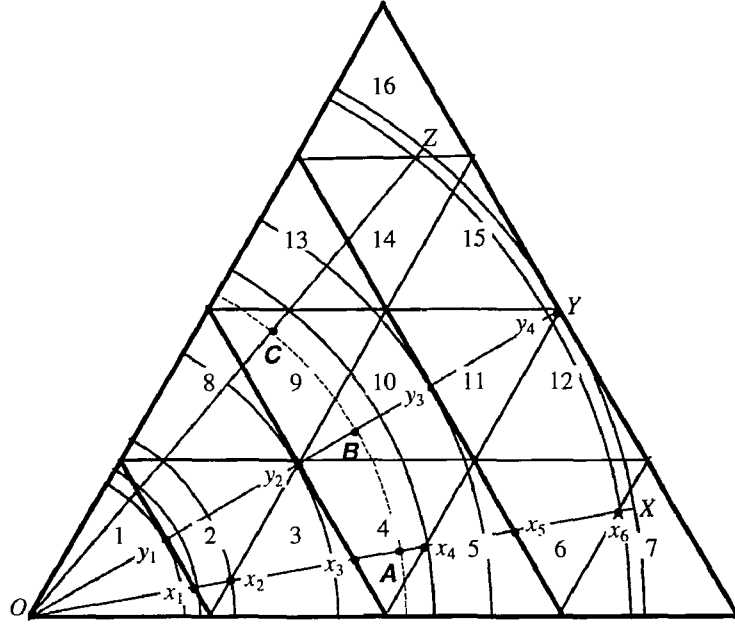


Fig.3-12 Boundaries of extra switching patterns of 7-segment SVM ($f_{sp}/f_1=18$)

Obviously there will be different transition patterns when different triangles are involved. Some transitions may cause extra switchings. Table 3.4 summarizes the switching transitions and maximum voltage change. According to the range of V_{ref} listed in the first column, the sampling points A , B and C may be located in different triangles, which are listed in the second column. In the second column, the triangle numbers with a prime, such as $\Delta 1'$, is the triangle in sector II in which the reference vector will be landed. The leading and ending states of the sequences are listed in the third column. Extra switching can be calculated by counting the variation of the switching states in this column. Column 4 lists the maximum voltage change occurred in the transitions. From the table it can be concluded that extra switching varies from f_1 to $2f_1$ and the maximum voltage transition is 2 voltage levels.

Table 3.4 Sequence transition from triangle to triangle ($f_{sp}/f_1=18$)

V_{ref}	Triangles involved				Sequence transition				Voltage transition	f_{extra}/f_1	f_{sw_actual}/f_1
	A	B	C	Sector II	A	B	C	Sector II			
$V_{ref} \leq oy_1$	$\Delta 1 \rightarrow \Delta 1 \rightarrow \Delta 1 \rightarrow \Delta 1'$				$[1,1,0] \rightarrow [1,1,0] \rightarrow [1,1,0] \rightarrow [-1,0,-1]$				2 steps	1	5.5
$oy_1 \leq V_{ref} \leq ox_1$	$\Delta 1 \rightarrow \Delta 2 \rightarrow \Delta 1 \rightarrow \Delta 1'$				$[1,1,0] \rightarrow [1,1,0] \rightarrow [1,1,0] \rightarrow [-1,0,-1]$				2 steps	1	5.5
$ox_1 \leq V_{ref} \leq ox_2$	$\Delta 2 \rightarrow \Delta 2 \rightarrow \Delta 2 \rightarrow \Delta 2'$				$[1,1,0] \rightarrow [1,1,0] \rightarrow [1,1,0] \rightarrow [-1,0,-1]$				2 steps	1	5.5
$ox_2 \leq V_{ref} \leq oy_2$	$\Delta 3 \rightarrow \Delta 2 \rightarrow \Delta 8 \rightarrow \Delta 3'$				$[1,0,0] \rightarrow [1,1,0] \rightarrow [1,1,0] \rightarrow [0,0,-1]$				1 step	1	5.5
$oy_2 \leq V_{ref} \leq ox_3$	$\Delta 3 \rightarrow \Delta 10 \rightarrow \Delta 8 \rightarrow \Delta 3'$				$[1,0,0] \rightarrow [2,1,-1] \rightarrow [1,1,0] \rightarrow [0,0,-1]$				1 step	2	6.5
$ox_3 \leq V_{ref} \leq ox_4$	$\Delta 4 \rightarrow \Delta 10 \rightarrow \Delta 9 \rightarrow \Delta 4'$				$[2,0,-1] \rightarrow [2,1,-1] \rightarrow [2,1,-1] \rightarrow [0,1,-2]$				2 steps	2	6.5
$ox_4 \leq V_{ref} \leq oy_3$	$\Delta 5 \rightarrow \Delta 10 \rightarrow \Delta 13 \rightarrow \Delta 5'$				$[2,0,-1] \rightarrow [2,1,-1] \rightarrow [2,2,-1] \rightarrow [0,1,-2]$				2 steps	1.5	6
$oy_3 \leq V_{ref} \leq ox_5$	$\Delta 5 \rightarrow \Delta 11 \rightarrow \Delta 13 \rightarrow \Delta 5'$				$[2,0,-1] \rightarrow [2,1,-1] \rightarrow [2,2,-1] \rightarrow [0,1,-2]$				2 steps	1.5	6
$ox_5 \leq V_{ref} \leq ox_6$	$\Delta 6 \rightarrow \Delta 11 \rightarrow \Delta 14 \rightarrow \Delta 6'$				$[2,0,-1] \rightarrow [2,1,-1] \rightarrow [2,2,-1] \rightarrow [0,1,-2]$				2 steps	1.5	6
$ox_6 \leq V_{ref} \leq oy_4$	$\Delta 7 \rightarrow \Delta 11 \rightarrow \Delta 16 \rightarrow \Delta 7'$				$[2,-1,-1] \rightarrow [2,1,-1] \rightarrow [2,2,-1] \rightarrow [1,1,-2]$				2 steps	1.5	6

It is easy to understand that when the sampling frequency changes, extra switching will happen in different ways. However no matter what the sampling frequency is, it can be generally concluded that extra switchings of $1.5f_1$ to $2f_1$ are inevitable and the maximum phase voltage change during the transitions is 2 voltage levels. These conclusions are also true for other SVM with predefined switching sequence, such as 5-segment SVM.

The actual average switching frequency is

$$f_{sw_actual} = f_{sw_ideal} + f_{extra} \quad (3.9)$$

Extra switching transition makes no contribution to the inverter sampling frequency and increases switching loss. For high power converters which work at relatively low switching frequency, extra switching is especially undesirable.

3.3.3 Design of Three-Segment Switching Sequence

3.3.3.1 Principle of Minimization of Device Switching Frequency

Extra switchings are decided by the difference between the present leading state and the last ending state. If the two sequences are for the same triangles, we can always make the

difference zero. Otherwise we can only minimize the difference and achieve minimized extra switchings. The most important part of the design of the 3-segment sequence is to select the leading state which has the least difference from the last ending state.

Consider the transition between two sampling periods where the ending state of the first period is $[S_a, S_b, S_c]$ and the leading state of the 2nd period is $[S_{a0}, S_{b0}, S_{c0}]$. Define two parameters for the transition: **total state value change** ΔS and **phase state value change** δS :

$$\Delta S = \sum_{i=a,b,c} |S_i - S_{i0}|, \quad (3.10)$$

$$\delta S = \max_{i=a,b,c} (|S_i - S_{i0}|). \quad (3.11)$$

The leading state of a switching sequence can be selected in three steps:

- (1) Find the subset of switching states with minimal ΔS . This criterion effectively minimizes extra switchings. If there is more than one state in the subset, then
- (2) Choose the states with minimum δS from the subset in (1). This criterion is to limit the voltage change during the transition and avoid unreasonable voltage jumps. Generally the leading state can be singled out by these two steps. If there is still more than one state, then
- (3) Select the state with least state value S for the completeness of the algorithm.

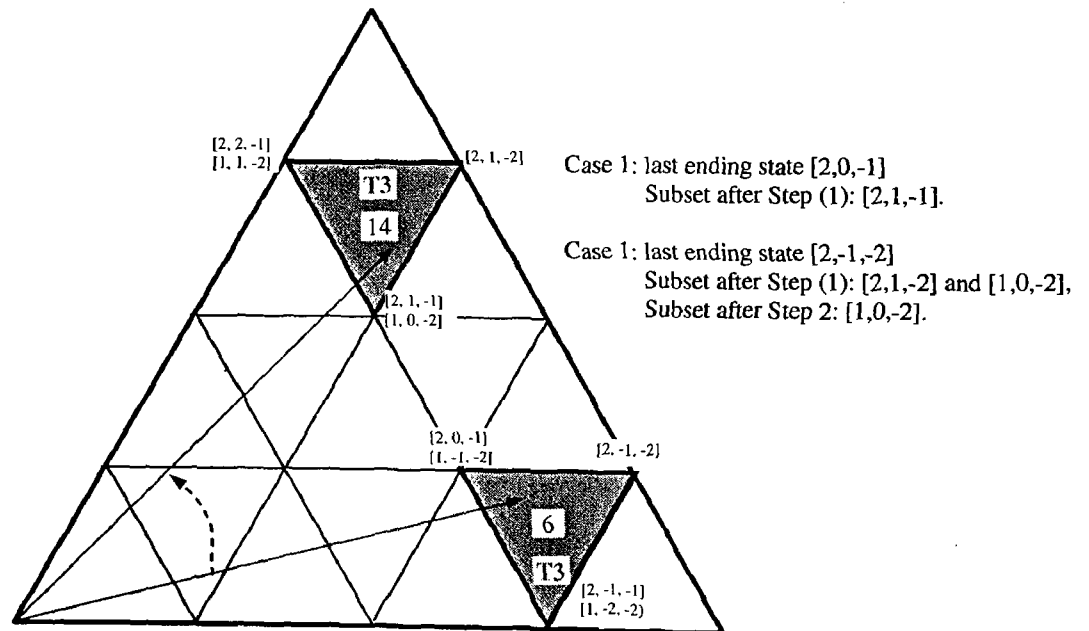


Fig.3-13 Example of the selection of leading state

For instance, let's consider the selection of the leading states for Triangle 14 shown in Fig.3-13. The previous sampling point was located in Triangle 6. The candidate states of Triangle 14 are $[2,2,-1]$, $[2,1,-1]$, $[2,1,-2]$, $[1,1,-2]$ and $[1,0,-2]$. If the previous sequence in Triangle 6 ended up with $[2,0,-1]$, the state $[2,1,-1]$ will be selected after Step (1). If the ending state was $[2,-1,-2]$, then $[2,1,-2]$ and $[1,0,-2]$ will be the subset after Step (1). After Step (2), $[1,0,-2]$ will be singled out and the transition is limited to 1 voltage level.

3.3.3.2 Arrangement of Switching Sequence

The switching sequence is constrained among the middle states as introduced in Section 3.2. The switching pattern can then be designed in a flexible way to adapt to the leading state.

Table 3.5 Three-segment switching sequences for T_1 to T_4

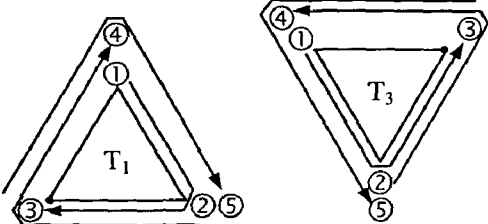
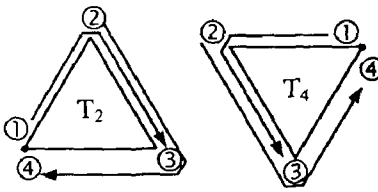
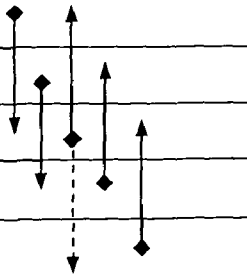
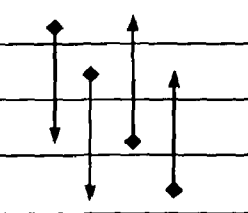
T1&T3			T2&T4		
					
States		Sequences	States		Sequences
①	state value decreasing ↓		①	state value decreasing ↓	
②			②		
③			③		
④			④		
⑤					

Table 3.5 shows the 3-segment switching sequences for T_1 to T_4 . For T_1 and T_3 , there are five middle states which are all possible to be the leading state. In the second row of the table, the switching sequences are sketched for different triangles. Note that reversal switching sequences, such as the sequences $① \rightarrow ② \rightarrow ③$ and $③ \rightarrow ② \rightarrow ①$, are drawn only once. All the possible switching sequences are illustrated by arrows in the bottom rows. For example, if the

leading states is ①, the sequence must be ①→②→③. However, when the leading state is ③, the sequence can be designed in two ways: to use the states with higher or lower state value S . Simulation reveals that it make no significant difference to the performance and the two methods can be used arbitrarily. Thus there are 5 kinds of switching sequences for T_1 and T_3 , and 4 kinds for T_2 and T_4 .

It is obvious from Table 3.5 that the 3-segment sequences can start at any switching states of any vertex, which brings the flexibility for the minimization of extra switchings.

3.3.3.3 Selection of the First Leading State

If the switching sequences (S_1, S_2, S_3, \dots) are placed on the time axis, it is in fact a train of switching states (Fig.3-17). Each cart of the train represents a sampling cycle and is loaded by of 3 switching states. The leading switching states (S_4, S_7, \dots , etc.) of each carriage except the first one, can be selected as per the discussion in Section 3.3.3.1. The switching states (S_5 and S_6, S_8 and S_9 , etc.) following the leading states can be selected according to the sequence arrangement in Section 3.3.3.2. The switching states for the following sectors can be reproduced by the negative rotation discussed in Section 3.1. There is still one problem to be solved, i.e. to select S_1 , the first leading state, which is the leading state of the first switching sequence in Sector I.

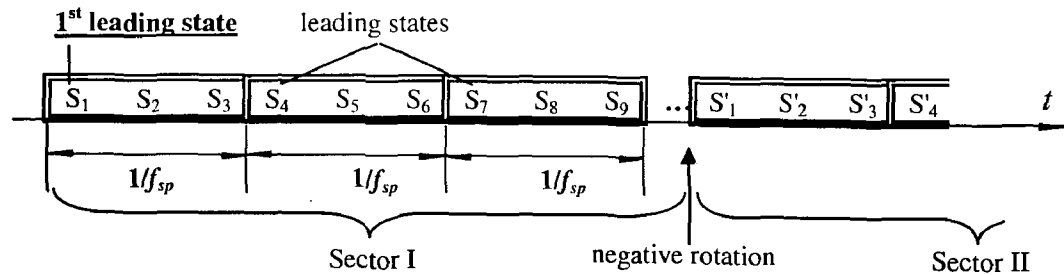
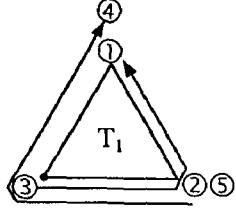
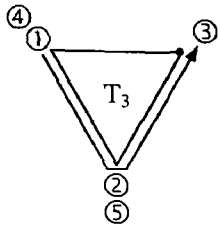
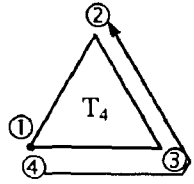
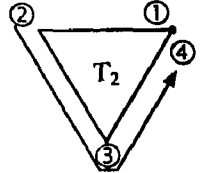


Fig.3-14 The train of switching states and the 1st leading state

Because the reference vector rotates counter-clockwisely, it is preferable to let the first switching sequence end at the uppermost vertex so that it is ready for the next triangle. Table

3.6 shows the preferable ‘first leading state’ for the four kinds of triangles.

Table 3.6 The first leading states

	T1	T3	T2	T4
				
Sequence 1	③ → ② → ①	① → ② → ③	④ → ③ → ②	② → ③ → ④
Sequence 2	② → ③ → ④			
1 st leading states	③ for sequence 1 ② for sequence 2	①	④	②

It should be noted that the sequences in Table 3.6 are ‘preferable’ to initiate the SVM is meaningful in the context that the next sampling point is located in the other triangle, which may not always be case in reality. However simulation reveals that the sequence listed in Table 3.6 yields better performance in most cases. The two preferable sequences for T_1 provides different performance when $V_{ref} < 1$: when $V_{ref} > 1$ the WTHD performances are almost the same but the Sequence 1 results lower device switching frequency; when $V_{ref} < 1$, they produce almost the same device switching frequency but Sequence 2 provides better THD. Thus if $V_{ref} < 1$, Sequence 2 is used, otherwise Sequence 1 is used.

3.3.3.4 Examples of Three-Segment Sequence

Example 1: $f_{sp}/f_i=18$, $V_{ref}=3$. The distribution of the sampling points A to C is shown in Fig.3-15(a). Triangles 6, 11 and 14 are involved. The switching states selected for the 3-segment sequences are circled and threaded by dashed line according to the order of usage.

The switching sequences are listed as follows:

Switching sequence at Point A: $[2, -1, -2] \rightarrow [2, -1, -1] \rightarrow [2, 0, -1]$,
Switching sequence at Point B: $[2, 0, -1] \rightarrow [2, 0, -2] \rightarrow [1, 0, -2]$,
Switching sequence at Point C: $[1, 0, -2] \rightarrow [1, 1, -2] \rightarrow [2, 1, -2]$.

There are no extra switchings in this case. Each transition involves only one voltage step.

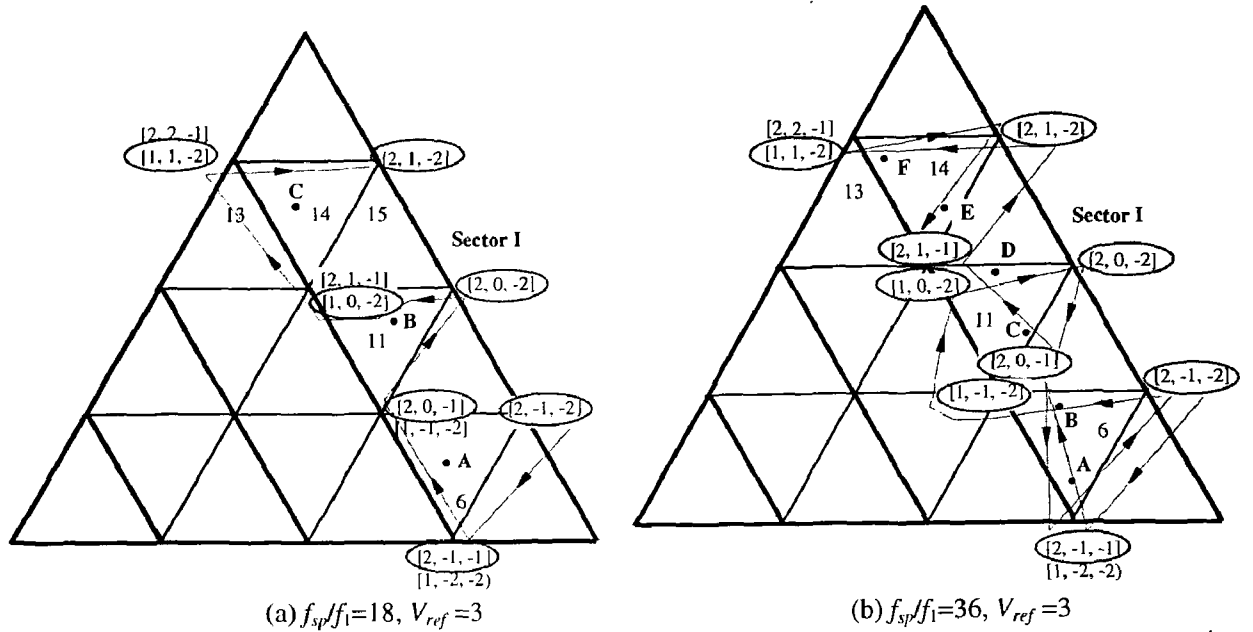


Fig.3-15 Examples of 3-segment sequence

Example 2: $f_{sp}/f_i=36, V_{ref}=3$. The distribution of the sampling points A to F is shown in Fig.3-15(b). Triangles 6, 11 and 14 are involved. The switching states selected for 3-segment sequences are circled. The switching sequences are listed as follows:

Switching sequence at Point A: $[2, -1, -2] \rightarrow [2, -1, -1] \rightarrow [2, 0, -1]$,
 Switching sequence at Point B: $[2, 0, -1] \rightarrow [2, -1, -1] \rightarrow [2, -1, -2]$,
 Switching sequence at Point C: $[1, -1, -2] \rightarrow [1, 0, -2] \rightarrow [2, 0, -2]$,
 Switching sequence at Point D: $[2, 0, -2] \rightarrow [2, 0, -1] \rightarrow [2, 1, -1]$,
 Switching sequence at Point E: $[2, 1, -1] \rightarrow [2, 1, -2] \rightarrow [1, 1, -2]$,
 Switching sequence at Point F: $[1, 1, -2] \rightarrow [2, 1, -2] \rightarrow [2, 1, -1]$.

There is only one extra switching transition which occurs between sampling point B and C. Again, only 1 voltage step is involved for each transition.

3.3.4 Simulation

The performance of the 3-segment SVM has been simulated by modulating the 5-level NPC/H-bridge inverter (Fig.3-7).

Fig.3-16 shows a set of typical waveforms. The gating signals for switches S_{a11} , S_{a14} , S_{a21} and S_{a24} are in the top 4 traces. The normalized voltages, v_{ao}/E , v_{no}/E , v_{an}/E , v_{bn}/E , v_{ab}/E are shown by the other traces. It can be seen the voltage of each arm (v_{ao}/E or v_{no}/E) is 3-level, the phase voltage (v_{an}/E or v_{bn}/E) is 5-level and the line voltage is 9-level.

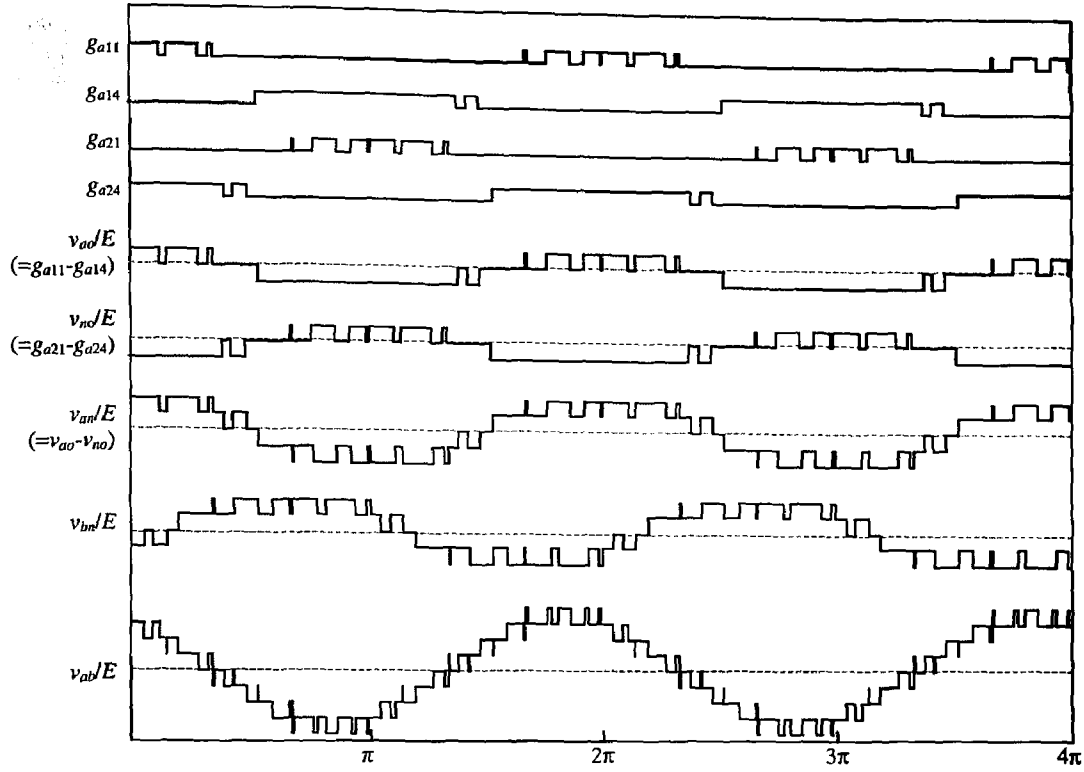


Fig.3-16 Typical waveforms of NPC/H-bridge inverter with 3-segment SVM

$$(m_a=0.87, f_{sp}=2160\text{Hz})$$

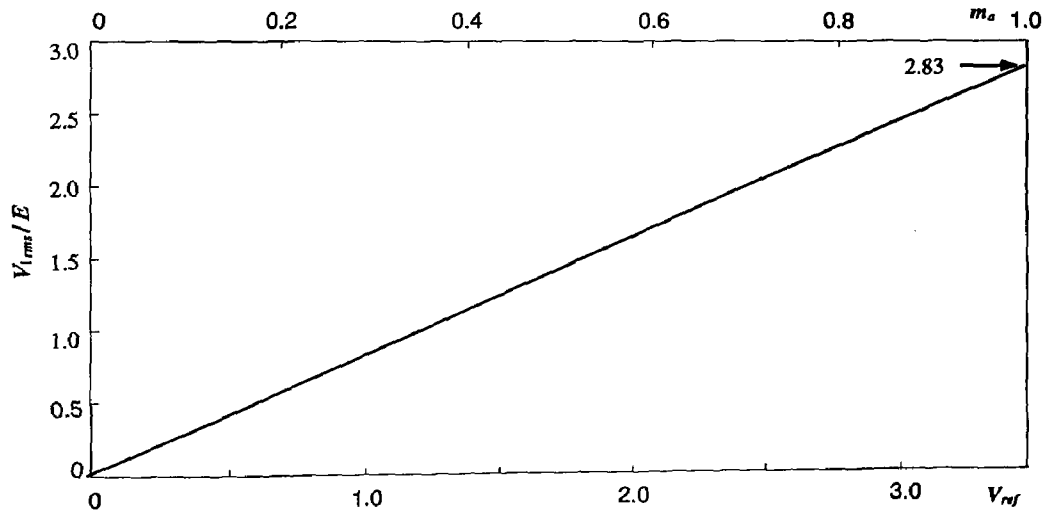


Fig.3-17 Simulated fundamental voltage versus m_a (3-segment SVM)

The *rms* value of the fundamental voltage (normalized by the step voltage E) is shown in Fig.3-17. It follows the same relationship defined by Eq.(3.4). Fig.3-18 shows the WTHD of the line-to-line voltage versus V_{ref} with f_{sp}/f_1 as a parameter. It can be seen higher sampling frequency results in lower WTHD. More simulation results will be given in the next section.

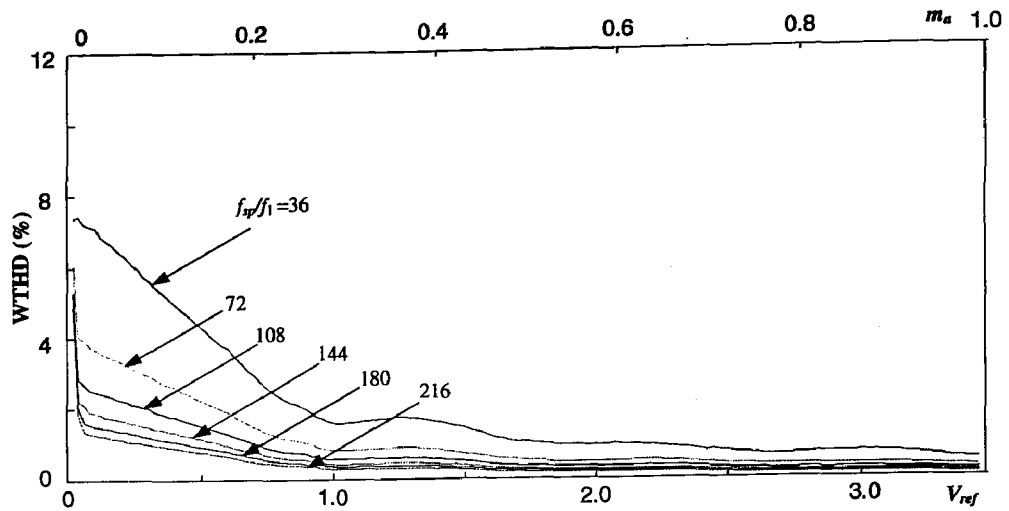


Fig.3-18 Simulated WTHD versus m_a (3-segment SVM)

3.4 Comparative Study

3.4.1 Simulation Conditions

In all simulations, the sampling frequency f_{sp} is limited to be a multiple of 6, which are listed in Table 3.7. It should be noted that some sampling frequencies workable for 3-segment SVM can not be used for 7-segment SVM. The comparisons will be made for the frequencies in the shaded rows, where the two schemes have the same ideal average device switching frequency f_{sw_ideal} .

Table 3.7 Comparison of sampling frequency

f_{sp}/f_1		f_{sw_ideal}/f_1	f_{sp}/f_1		f_{sw_ideal}/f_1
3-segment SVM	7-segment SVM		3-segment SVM	7-segment SVM	
12	-	1	120	-	10
18	6	1.5	126	42	10.5
24	-	2	132	-	11
30	-	2.5	138	-	11.5
36	12	3	144	48	12
42	-	3.5	150	-	12.5
48	-	4	156	-	13
54	18	4.5	162	54	13.5
60	-	5	168	-	14
66	-	5.5	174	-	14.5
72	24	6	180	60	15
78	-	6.5	186	-	15.5
84	-	7	192	-	16
90	30	7.5	198	66	16.5
96	-	8	204	-	17

102	-	8.5	210	-	17.5
108	36	9	216	72	18
114	-	9.5			

For each sampling frequency, the simulations were done for V_{ref} from 0.01 to 3.46 with 0.01 increment, or equivalent m_a from 2.9×10^{-3} to 1.0 with 2.9×10^{-3} increment. The inverter topology is shown in Fig.3-7. The detailed block diagrams and initialization functions are attached in Appendix 2.

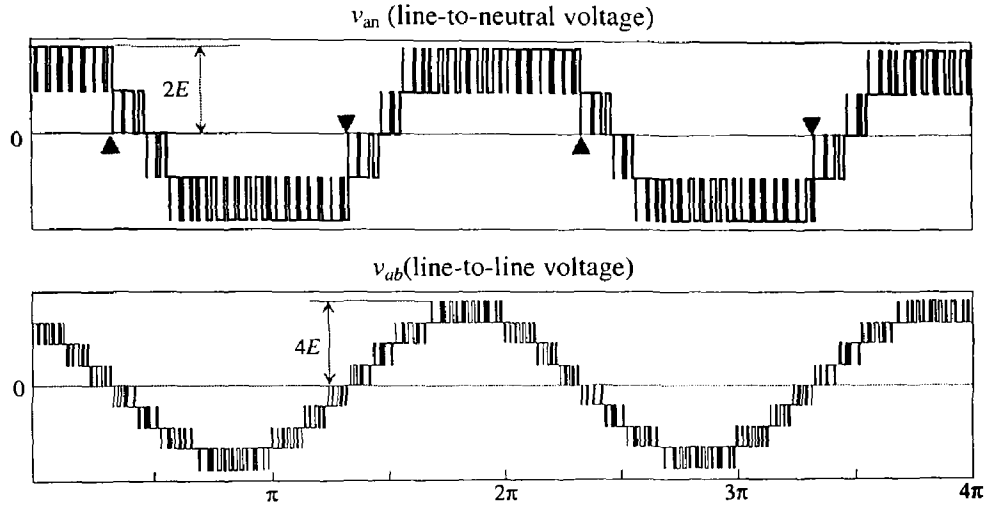


Fig.3-19 Simulated voltage waveforms of NPC/H-bridge inverter with 7-segment SVM
 $(m_a=0.87, f_1=60\text{Hz}, f_{sp}/f_1=42, f_{sw_ideal}=630\text{Hz})$

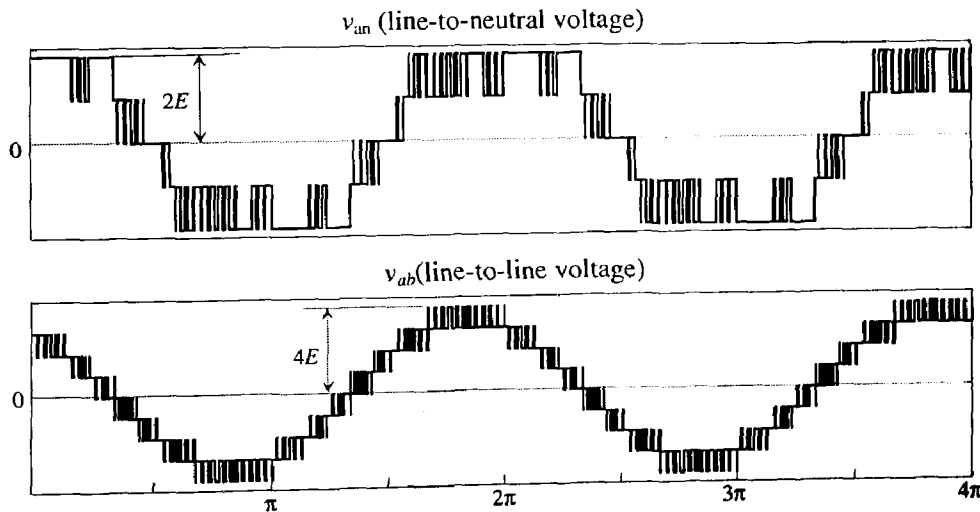


Fig.3-20 Simulated voltage waveforms of NPC/H-bridge inverter with 3-segment SVM
 $(m_a=0.87, f_1=60\text{Hz}, f_{sp}/f_1=126, f_{sw_ideal}=630\text{Hz})$

3.4.2 Waveforms

While the shapes of the line-to-neutral voltages are different, the line-to-line voltage waveforms are quite similar. Fig.3-19 and Fig.3-20 shows the waveforms. For both schemes the line-to-neutral voltages have 5 voltage levels and the line-to-line voltage is 9-level.

It should be noted that there are two transitions with 2-voltage-level jumps each fundamental period in Fig.3-19(a) for the 7-segment SVM, which are pointed out by triangular marks. In contrast the transitions in Fig.3-20(a) are always limited to 1 voltage level for the 3-segment SVM. This is true for all other modulation index and sampling frequencies.

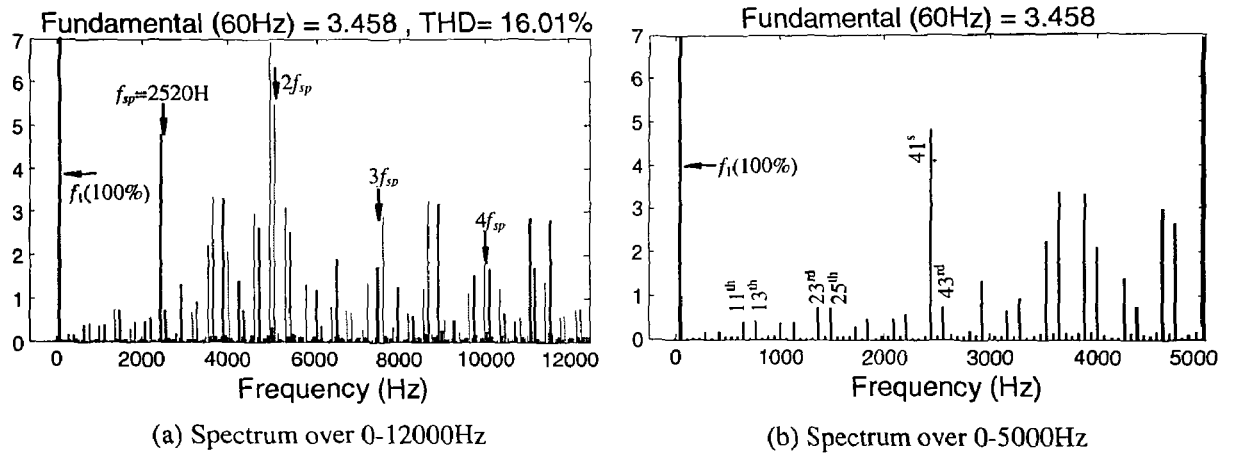


Fig.3-21 Simulated spectra of line voltage of NPC/H-bridge inverter with 7-segment SVM

($m_a=0.87$, $f_i=60Hz$, $f_{sp}/f_i=42$, $f_{sw_ideal}=630Hz$)

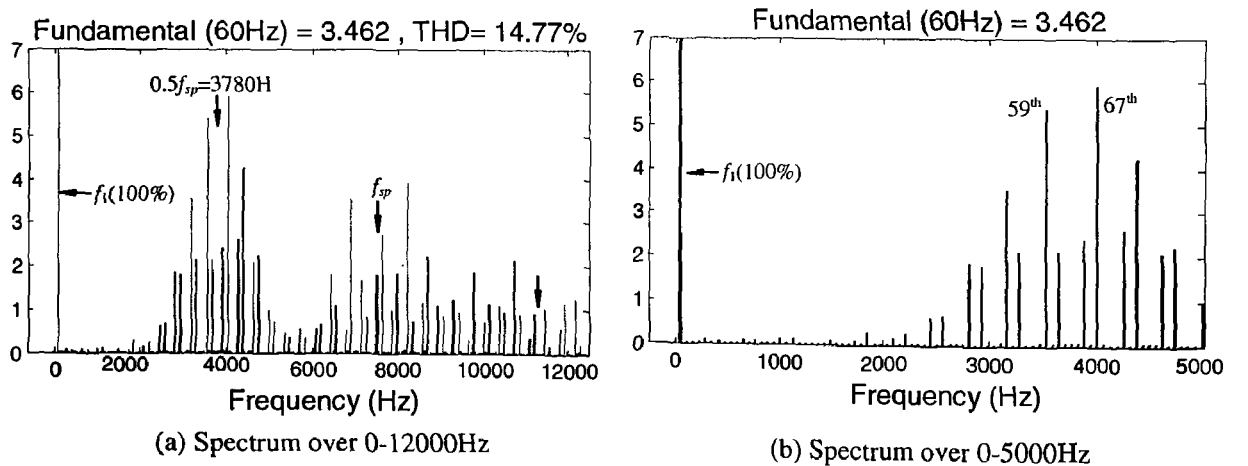


Fig.3-22 Simulated spectra of line voltage of NPC/H-bridge inverter with 3-segment SVM

($m_a=0.87$, $f_i=60Hz$, $f_{sp}/f_i=126$, $f_{sw_ideal}=630Hz$)

3.4.3 Spectra, THD and WTHD

The centre of the first sideband in the spectra of the output voltages is at higher frequency for the 3-segment SVM, as shown in Fig.3-21 and Fig.3-22. Fig.3-21(a) and Fig.3-22(a) are the spectra over a wider frequency range up to 12000Hz, i.e. 200th harmonics. The first sideband in Fig.3-21 (a) is centred at 2520Hz, which is the same as the sampling frequency for the 7-segment SVM while it is 3780Hz in Fig.3-22(a), which is half of the sampling frequency of the 3-segment SVM. The centre of the first side band of the 3-segment SVM is 1.5 times that of the 7-segment SVM, which is consistent with Eqs.(3.2) and (3.8).

For the above reason, the 7-segment SVM produces more lower-order harmonics as shown in the zoomed spectra in Fig.3-21(b) and Fig.3-22(b). Thus it is reasonable to expect that 3-segment SVM can achieve lower WTHD.

It should also be mentioned that both algorithms produces no even harmonics.

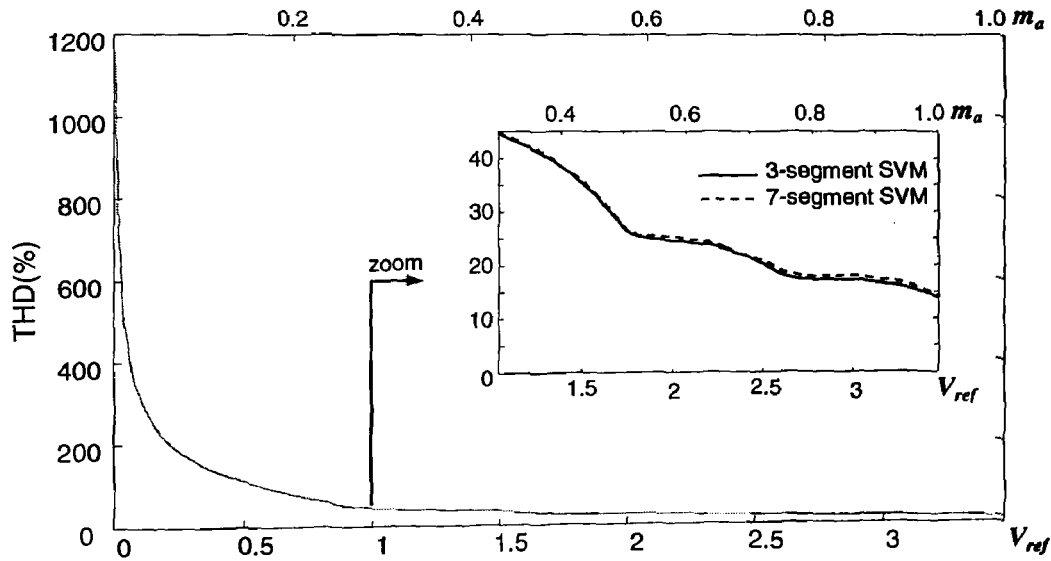


Fig.3-23 Comparison of THD versus m_a

($f_1=60\text{Hz}$, $f_{sw_ideal}=630\text{Hz}$)

The above observations about the spectra can also be found for other modulation indices. Fig.3-23 and Fig.3-24 shows the THD and WTHD versus V_{ref} . While the THD is very close to each other, the WTHD of the 3-segment SVM is better except when V_{ref} is between 0.8-1.0 or

1.4-1.6. The superiority of 3-segment in terms of WTHD is true for other sampling frequencies, especially at lower sampling frequencies. For more comparative results. see Appendix 3.

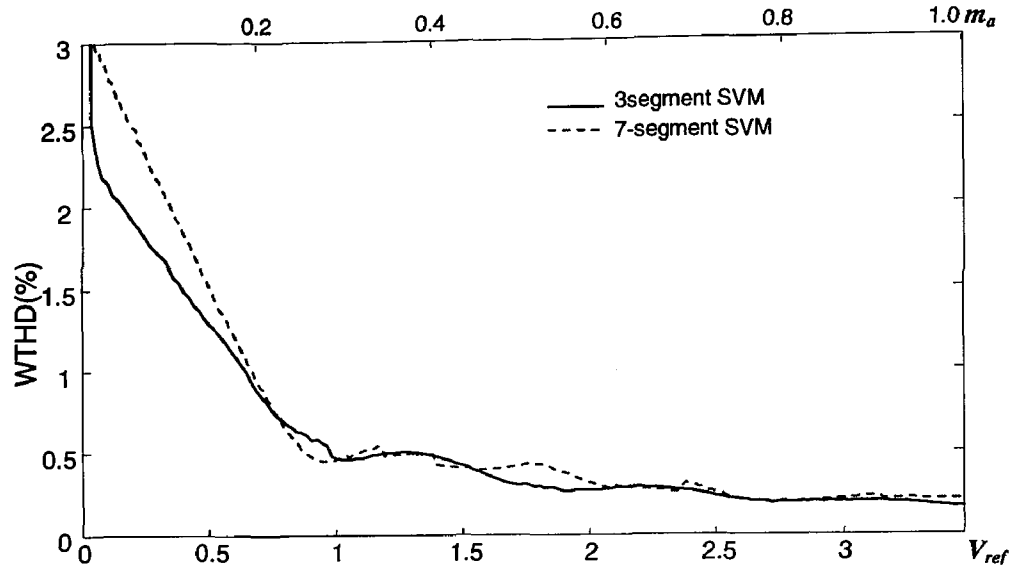


Fig.3-24 Comparison of WTHD versus m_a

($f_1=60\text{Hz}$, $f_{sw_ideal}=630\text{Hz}$)

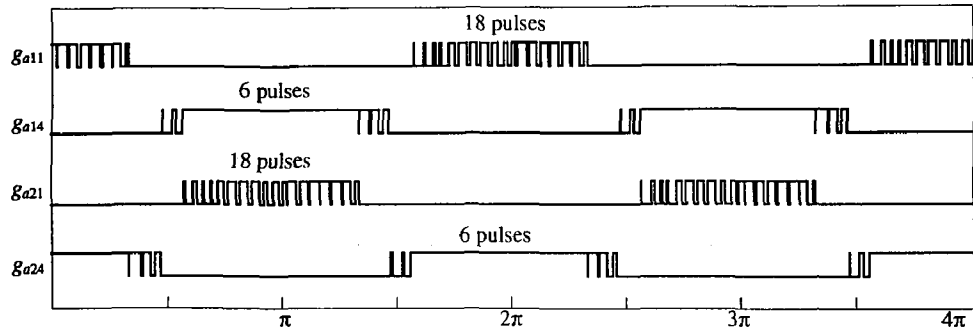


Fig.3-25 Gating pattern of 7-segment SVM

($m_a=0.87$, $f_1=60\text{Hz}$, $f_{sp}/f_1=42$, $f_{sw_ideal}=630\text{Hz}$)

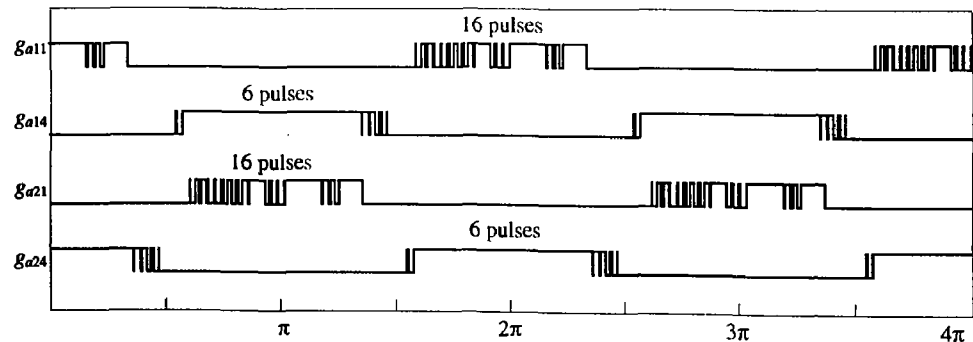


Fig.3-26 Gating pattern of 3-segment SVM

($m_a=0.87$, $f_1=60\text{Hz}$, $f_{sp}/f_1=126$, $f_{sw_ideal}=630\text{Hz}$)

3.4.4 Gating Pattern and Device Switching Frequency

The gating pattern is symmetrical for the left and right arms, but asymmetrical for the top and bottom switches. Fig.3-25 and Fig.3-26 shows the gating signals for the switches S_{a11} , S_{a14} , S_{a21} and S_{a24} . For the 7-segment SVM, the top switches operate at 1080Hz and the bottom ones at 360Hz. The average switching frequency is 270Hz. For the 3-segment SVM the top switches work at 960Hz and the lower ones at 360Hz. The average switching frequency is 660Hz.

The deviation in switching loss caused by asymmetrical switching pattern can be corrected by swapping the coding schemes, which will be depicted in the next Chapter.

The conclusion that 3-segment SVM yields lower actual device switching frequency is general for other modulation indices and sampling frequencies. Fig.3-27 shows the normalized actual average device switching frequency versus V_{ref} when the ideal switching frequency is 630Hz. It can be seen that the device switching frequency of 3-segment SVM is $0.5f_1$ to $1.5f_1$ less than that of 7-segment SVM. More comparative curves for the other sampling frequencies are included in Appendix 3.

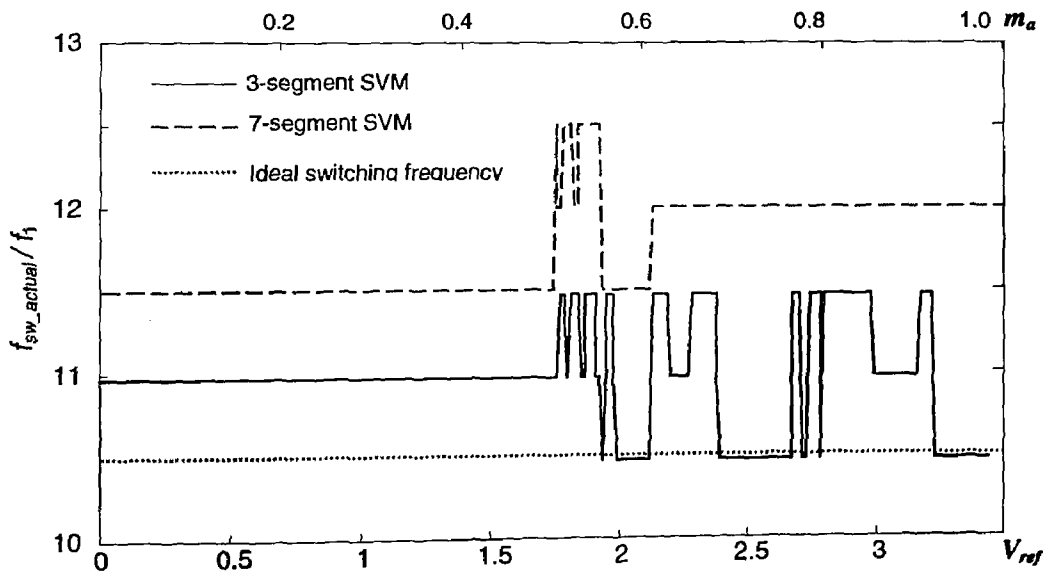


Fig.3-27 Actual average device switching frequency versus m_a ($f_{sw_ideal}=630\text{Hz}$)

3.5 Application of 3-Segment SVM to 9-Level Inverters

The proposed 3-segment SVM is generally applicable to any multilevel topologies. As an example, this section will present the simulation results for a 9-level CHB inverter. Fig.3-28 shows the line-to-neutral and line-to-line voltages for one fundamental cycle. The line-to-neutral voltage contains 9 levels and the line-to-line voltage is of 15 levels. Fig.3-29 shows the spectrum of the line-to-line voltage when the ideal average switching frequency is 630Hz. The inverter sampling frequency is still $0.5f_{sp}$, pushing the centre of the 1st sideband to 7650Hz, which is doubled from 5-level NPC/H-bridge inverters.

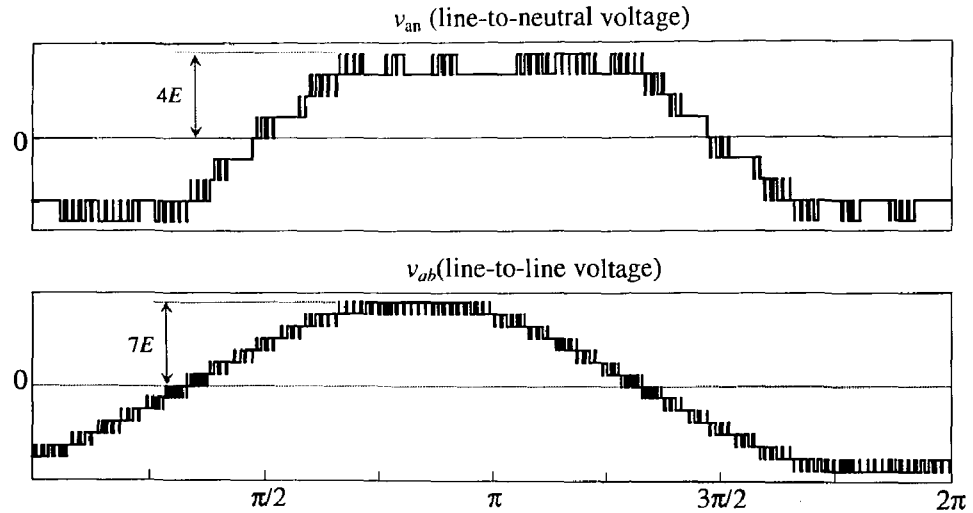


Fig.3-28 Simulated voltage waveforms of 9-level CHB inverter with 3-segment SVM

$$(m_a=0.87, f_1=60\text{Hz}, f_{sp}/f_1=252, f_{sw_ideal}=630\text{Hz})$$

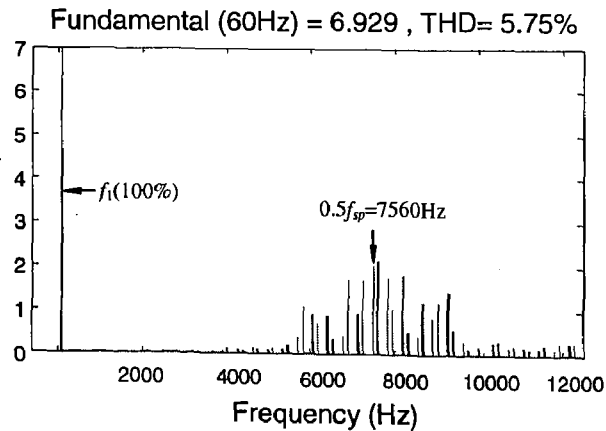


Fig.3-29 Simulated spectra of line voltage of 9-level CHB inverter with 3-segment SVM

3.6 Summary

This chapter presents the simplified sequence design for multilevel inverters. A flexible 3-segment SVM scheme is proposed and compared with conventional 7-segment SVM scheme. The proposed 3-segment SVM features:

- (1) Lower device switching frequency which leads to lower switching losses. Extra switchings caused by the reference vector crossing triangle boundaries are minimized by the flexible 3-segment sequences.
- (2) Higher inverter sampling frequency which leads to lower WTHD. The center frequency of the first sideband of the 3-segment SVM is 50% high than that of 7-segment SVM. This feature is of particular importance for high-power MV drives that operate at lower switching frequencies.
- (3) Easy implementation by rule-based sequence design which can be fulfilled in real time. Because the sequence is generated in real time from the information carried by the previous sequence, there is not need to design sequence table for each triangle.
- (4) General applicability to any multilevel inverters. The algorithm was developed based on the vector plot of multilevel inverters, thus is independent of inverter topology. It can be used for any voltage levels.
- (5) Half-wave symmetry eliminating even harmonics, which enables it to be used for active rectifiers.

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CHAPTER 4 EXPERIMENTS

A prototype converter system has been set up to verify the performance of the proposed dual 18-pulse rectifier and the flexible 3-segment SVM. This chapter will introduce the experiment setup, including the system block diagram, the planning and testing of the 18-pulse transformers and the coding scheme of space vector modulation for the NPC/H-bridge inverter. The experimental results of the harmonic contents of the input current will be discussed in association with the theoretical expectation of Chapter 2. The SVM schemes with 7-segment and flexible 3-segment switching sequences were implemented via dSpace Rapid Control Prototyping system. The experimental output voltage waveforms and the spectra were compared to the simulation results. The principles of the proposed rectifier topology and the performance of the 3-segment SVM scheme were confirmed by the experimental results.

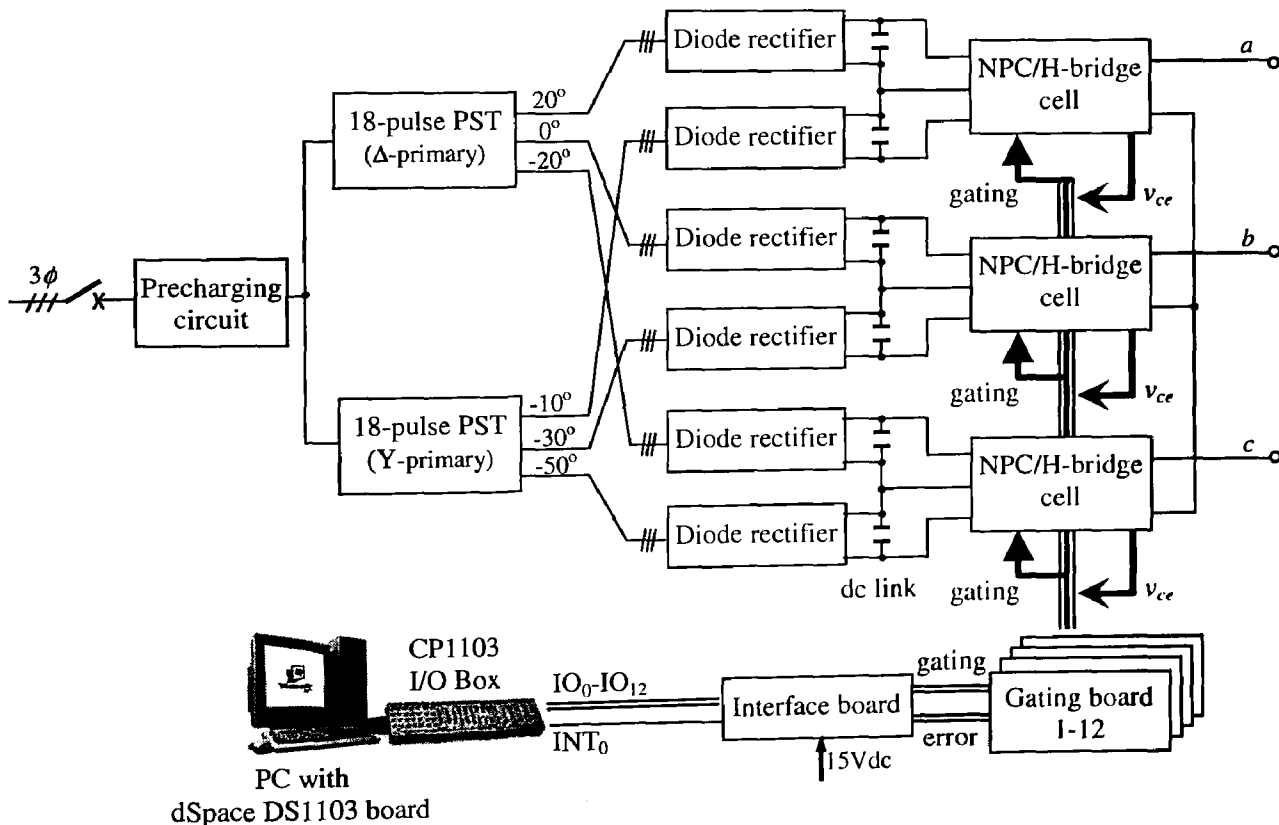


Fig.4-1 System block diagram of the experimental setup

4.1 Experiment Setup

4.1.1 System Configuration

The system block diagram of the experimental setup is shown in Fig.4-1.

The three-phase utility power is connected to the two 18-pulse PSTs through the precharging circuit, which is used to limit the inrush current at the startup. Six 3-phase diode rectifiers are powered by two 18-pulse PSTs and their DC outputs are connected according to the application case 3 shown in Fig.2-8 (Section 2.4). Each inverter phase is an NPC/H-bridge cells (see Fig.1-6).

The control of the inverter is based on dSpace hardware-in-the-loop simulation environment, which allows easy prototyping of controllers with the Simulink/RTI and downloading of these controllers to dedicated Digital Signal Processor (DSP) based systems for implementation. The dSpace main board DS1103 is embedded within the host PC, on which the Simulink/RTI environment is running. Digital I/O bits IO_0 to IO_{11} are used for the gating signals for the top and bottom switches of the NPC arms. These signals are shifted from TTL level to CMOS level by the interface board. Complementary gating signals for the middle switches are generated by the interface board. All these signals are buffered and sent to the gating boards.

The gating signals are reshaped, amplified, isolated and passed to the 12 IGBT modules by 12 gating boards. Semikron SKHI 22B hybrid dual IGBT driver modules are used. The blank-off time is set to $4.3\mu s$ and the short-pulse suppress is 500ns. The gating boards also generate error signals in the case of short-circuit, low supply voltage or all-high gating signals. The error signal is passed to the controller running in DS1103 via INT_0 , provoking service subroutine for fault processing. If an error occurs, all the gating signals at IO_0 to IO_{11} will be cleared and a FORBIDDEN signal is sent to the interface board via IO_{12} , which is then used to block all the complementary gating signals. As a result all the IGBTs will be switched off.

The major parts counts of the experimental setup are listed in Table 4.1.

Table 4.1 Parts Count table of the experiment setup

	Transformer	Winding	Rectifier	Cap	IGBT module	Diode module
Number	2	5	6	6	12	6
Model (parameter)	Rating: 240:120V; 5kVA each; Phase shift: 20°, 0°, -20° (Δ -primary); Phase shift: -10°, -30°, -50° (Y-primary);	Primary: 240V5kVA Secondary: 120V3kVA	Semikron SKD 50/12A3 (1200V50A)	4700 μ F 400V	Semikron SKM 75GB123D (1200V75A)	Semikron SKKD 75F12 (1200V75A) T_{rr} =920ns

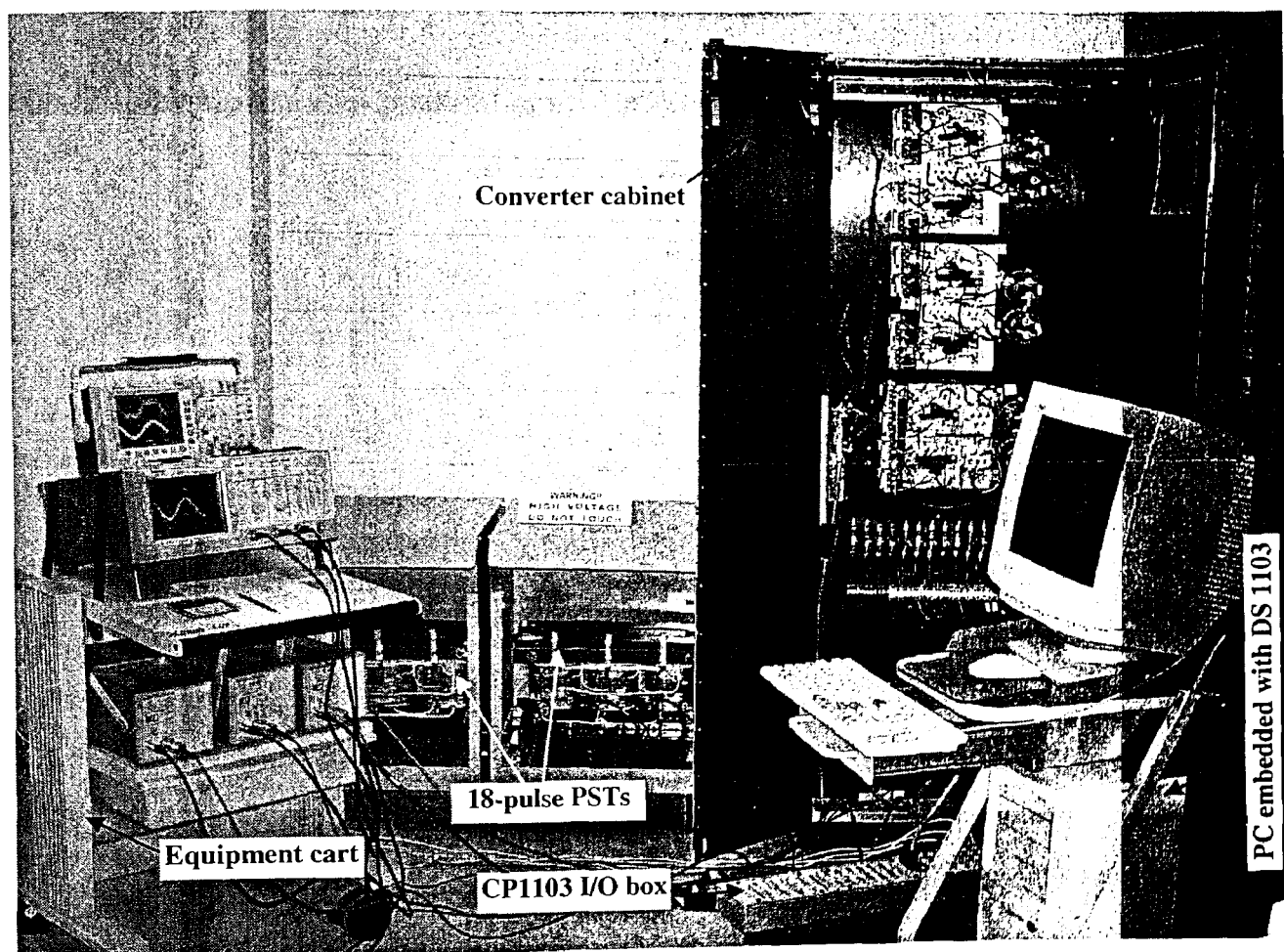


Fig.4-2 Photo of the experiment setup

The picture of the experiment setup is shown in Fig.4-2. The converter cabinet stands at the right. It holds the fuses, rectifiers, DC link capacitors, inverters, interface board, gating board, heat sink and so on. The computer equipped with dSpace main board DS1103 is located in front of the cabinet. It is connected to the interface board through I/O box CP1103. To the left of the cabinet are the two 18-pulse PSTs, which power the dual 18-pulse rectifier.

4.1.2 Planning and Testing of the Transformers

To achieve dual-18-pulse rectification, the two 18-pulse are designed in a way that one transformer is phase-shifted by 30° from the other. The wiring diagram of one PST is shown in Fig.4-3(a), where the primary is in Δ -connection and secondaries are in extended- Δ . The phase shift angles of the secondaries are 20° , 0° and -20° . The wiring of the other PST is shown in Fig.4-3(b), where the primary is in Y-connection, and secondaries are also in extended- Δ to balance the secondary leakage inductance with those of the 1st PST. If the primary voltage of the 1st PST is used as the reference, the phase shift angles are -10° , -30° and -50° .

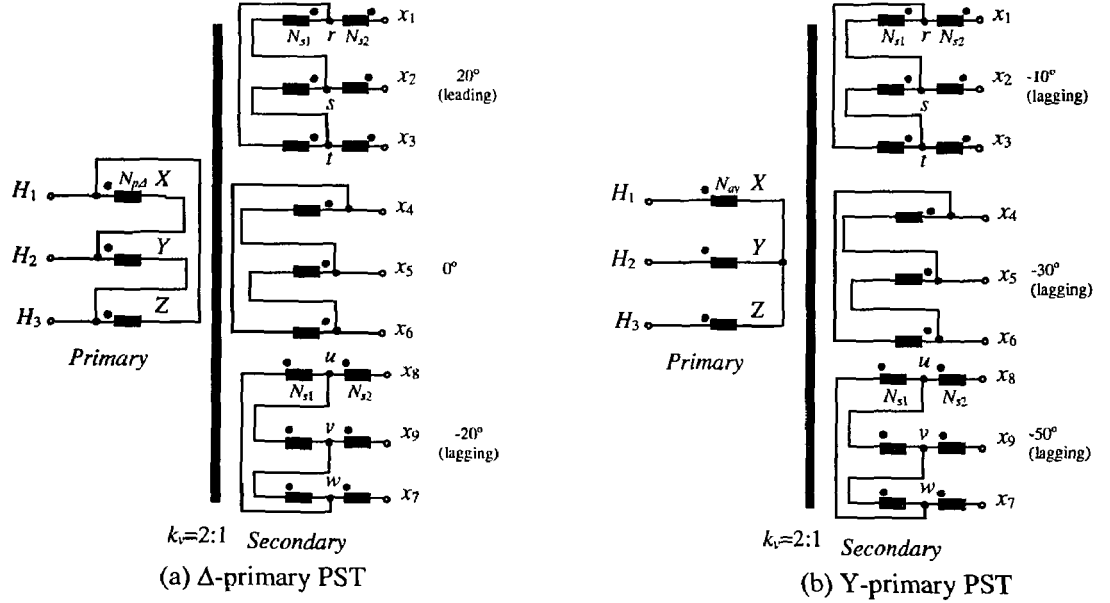


Fig.4-3 Winding diagram of the PSTs

The turns ratios can be calculated from the phasor diagrams of Fig.4-4. Take the PST with Δ -primary as an example. The voltage phasors of the secondary $x_1x_2x_3$ are shown in the dotted circle at the top right corner of Fig.4-4(a). Apply the Law of Sines in Δx_1x_2s :

$$\frac{x_1x_2}{\sin 120^\circ} = \frac{x_2s}{\sin 20^\circ} = \frac{x_1s}{\sin 140^\circ}, \quad (4.1)$$

Thus

$$\frac{N_{p\Delta}}{N_{s2}} = \frac{2x_1x_2}{x_2s} = \frac{2\sin 120^\circ}{\sin 20^\circ} = 5.064, \quad (4.2)$$

$$\frac{N_{p\Delta}}{N_{s1}} = \frac{2x_1x_2}{x_1x_2 - x_2s} = \frac{1}{0.5 - N_{s2}/N_{p\Delta}} = 3.305. \quad (4.3)$$

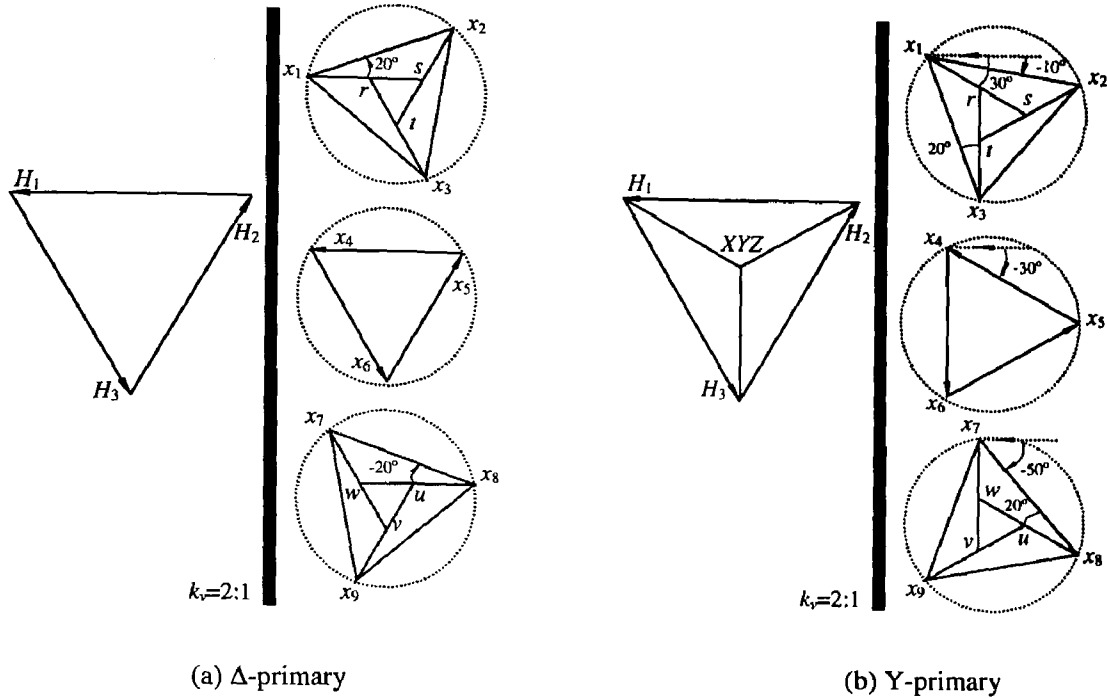


Fig.4-4 Phasor diagram of the PSTs

where $N_{p\Delta}$ is the turns number of the Δ -primary, N_{s1} is the turns number of the Δ -coils of the secondary, and N_{s2} is the turns number of the extended- Δ coil (Fig.4-3(a)).

The turns ratio of the Y-primary PST can be calculated in a similar way.

The actual transformers are tested to obtain parameters of leakage inductance and phase-shifting angles. The results are shown in Table 4.2. The phase-shifting angles and errors are recorded in the 'Phase shift angle' column. It can be seen the PSTs are non-ideal because the maximum phase error is 3.7° . The short circuit test results are shown in the right 6 columns in terms of actual unit and per unit. The average leakage reactance is around 1% p.u. and the average copper resistance is about 3.4% p.u. on the basis of the primary parameters (240V5kVA). The short circuit parameters are slightly unbalanced for the 6 secondaries.

Table 4.2 Phase Test and short circuit test results of the PSTs

		Phase shift angle	Impedance(Z)		Resistance(R)		Reactance(ωL)	
			Ω	p.u. (%)	(Ω)	p.u.(%)	Ω	p.u. (%)
Δ -primary	20° secondary	(17.7°, 16.3°, 17.3°) error: (-2.3, -3.7, -2.7)°	0.42	3.6	0.40	3.5%	0.10	0.87
	0° secondary	(-0.1°, -0.4°, -0.6°) error: (-0.1, -0.4, -0.6)°	0.41	3.6	0.39	3.4	0.13	1.1
	-20° secondary	(-20.5°, 20.5°, -20.5°) error: (-0.5, 0.5, -0.5)°	0.37	3.4	0.37	3.2	0.11	0.92
Y-primary	-10° secondary	(-10.1°, -9.5°, -10.3°) error: (-0.1, 0.5, -0.3)°	0.45	3.9	0.43	3.8	0.13	1.1
	-30° secondary	(-31.1°, -31°, -30.5°) error: (-1.1, -1, -0.5)°	0.42	3.7	0.40	3.5	0.14	1.2
	-50° secondary	(-51.3°, -50.4°, -50.3°) error: (-1.3, -0.4, -0.3)°	0.38	3.3	0.37	3.2	0.085	0.74
Average			0.41	3.58	0.39	2.86	0.12	0.99
Note: The per unit values are based on the primary (240V5kVA); $Z_{base}=V_{base}/I_{base}=V_L^2/S=240*240/5000=11.52\Omega$.								

4.1.3 State Decoder for NPC/H-Bridge

The inverter can be viewed as a coder: the switches are driven to different positions by gating pulses to generate codes (switching states). The modulating process is in fact a decoding process: translating the command voltage into switching sequence which is composed of a train of switching states, then decoding the switching states to obtain the gating pulses. For example, if the code is [2,-2, 2] for the NPC/H-bridge inverter, it should be decoded in a way such that that S_{a11} , S_{a12} , S_{a23} and S_{a24} are turned on, S_{b11} , S_{b12} , S_{b23} and S_{b24} turned off, and S_{c11} , S_{c12} , S_{c23} and S_{c24} turned on (see Fig.1-6). The other switching devices are operated in complementary ways.

Thus the last step of SVM algorithm is to design a decoder which generates gating signals according to the switching states.

However, for 5-level NPC/H-bridge inverter, there are different ways to generate codes '1', '0' and '-1'. To illustrate this situation, phase A of the NPC/H-bridge inverter is redrawn in Fig.4-5. If the switching function of Phase A is S , then

$$v_{an}=SE, \quad (4.4)$$

where $S = \pm 2, \pm 1$ or 0. The switching function can be implemented in different ways listed in Table 4.3, where S_{ao} and S_{no} are the switching functions of the NPC arms. There are 2 ways to decode ' ± 1 ', and 3 ways to decode '0'. Thus there are altogether 12 ways to decode S , which correspond to the 12 decoder shown in Table 4.4

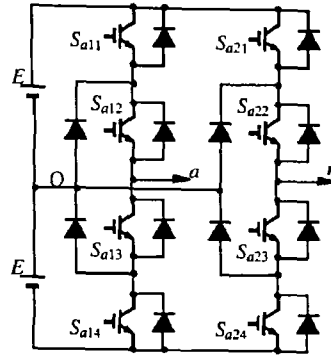


Fig.4-5 Phase A of the NPC/H-bridge inverter.

Table 4.3 Different schemes to synthesize the switching function S

S	-2	-1		0			1		2
S_{ao}	-1	-1	0	-1	0	1	0	1	1
S_{no}	1	0	1	-1	0	1	-1	0	-1

Table 4.4 Different decoding schemes for S and bad transitions

	Decoder 1		Decoder 2		Decoder 3		Decoder 4		Decoder 5		Decoder 6	
S	S_{ao}	S_{no}	S_{ao}	S_{no}	S_{ao}	S_{no}	S_{ao}	S_{no}	S_{ao}	S_{no}	S_{ao}	S_{no}
-2	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1
-1	-1	0	-1	0	-1	0	-1	0	-1	0	-1	0
0	1	1	1	1	0	0	0	0	-1	-1	-1	-1
1	1	0	0	-1	1	0	0	-1	1	0	0	-1
2	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1
	Decoder 7		Decoder 8		Decoder 9		Decoder 10		Decoder 11		Decoder 12	
S	S_{ao}	S_{no}	S_{ao}	S_{no}	S_{ao}	S_{no}	S_{ao}	S_{no}	S_{ao}	S_{no}	S_{ao}	S_{no}
-2	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1
-1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	1	1	1	0	0	0	0	-1	-1	-1	-1
1	1	0	0	-1	1	0	0	-1	1	0	0	-1
2	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1

Note: 1) bad transitions involving 1 voltage step are marked by arrows with solid lines;
2) bad transitions involving 2 voltage steps are marked by arrows with dotted lines.

For NPC/H-bridges, the maximum voltage change of a single NPC arm for every transition should be limited to ONE voltage step, i.e. the transitions of S_{ao} and S_{no} are limited to 1 voltage-step, otherwise there will be voltage sharing problem. For example, if the voltage

change of the left arm in Fig.4-5 is +2 voltage steps, i.e. v_{ao} changes from $-E$ to E , all the four switches in the left arm have to be operated, with S_{a11} and S_{a12} switched to 'off' and S_{a13} and S_{a14} switched to 'on'. In this case dynamic voltage sharing problem will occur, leading to possible device damages. Transitions involving 2-voltage-step change in a single NPC arm are considered to be **bad transitions**.

Analysis of the switching transitions of Table 4.4 shows that

- (1) if S is allowed to have 2-voltage-step jump during the transition, only the 4th and 9th decoder are workable. The other decoders cause bad transitions, which are marked by arrows with dotted line. This is important for 7-segment SVM that causes 2-voltage-step change for S .
- (2) if S is limited to 1-voltage-step jump during the transition, the 3rd, 4th, 6th, 7th, 9th and 10th decoders are workable. Bad transitions in this case are marked by arrows with solid line. This is for flexible 3-segment SVM, which generates transitions with only 1-voltage-step jumps.

It can be concluded that decoder 4 and 9 can be used for both 7-segment and 3-segment SVM schemes. It was mentioned in Section 3.4.4 that the unbalanced switching pattern can be corrected by swapping the decoding schemes. In fact Decoder 4 and 9 can be used alternatively to balance the top and bottom switches. Fig.4-6 shows the gating signals of the top and bottom switches of phase A when swapping happens every 3 fundamental cycles. It is clear that the gating patterns are now balanced.

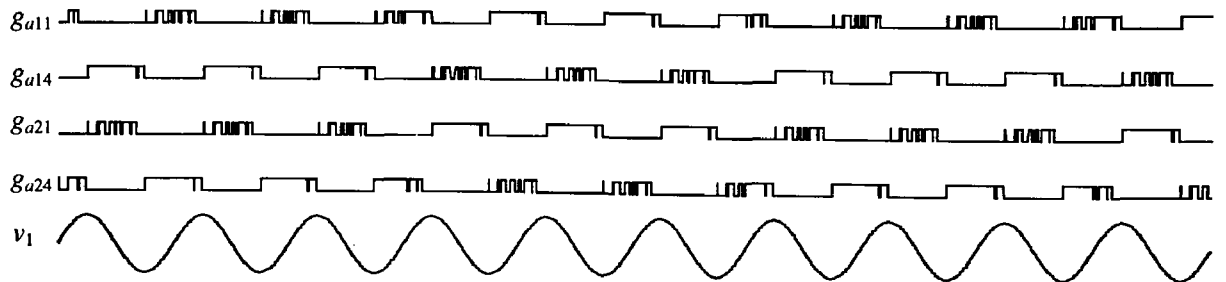


Fig.4-6 Balanced gating signals by swapping decoding schemes.

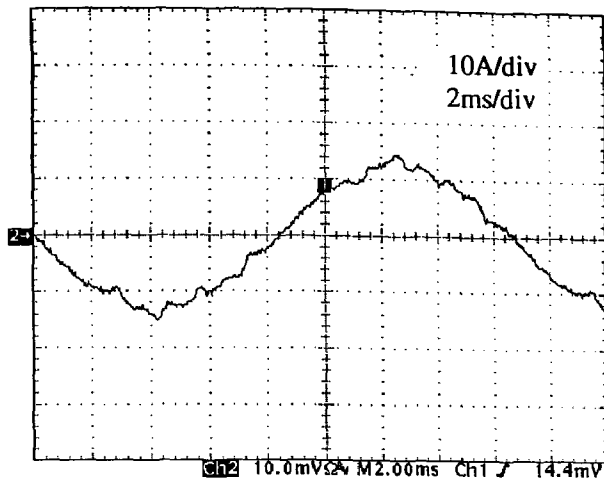
4.1.4 Simulink/RTI Model for the Controller

The Simulink/RTI model for the implementation of the SVM schemes are shown in Fig.4-

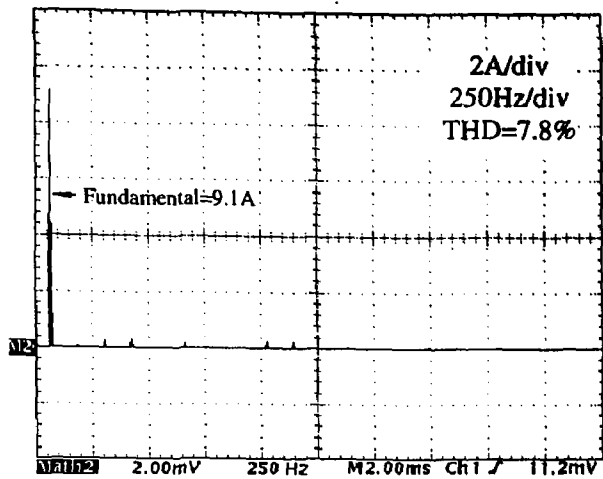
The test was done for 4kW (0.4 p.u.) resistive load. The current waveforms and spectra are shown in Fig.4-8. The input currents of each PST, $i_{A\Delta}$ and $i_{A\gamma}$, and the total current i_A are shown in Fig.4-8(a), (c) and (e) (see Fig.2-11 for the definitions of $i_{A\Delta}$, $i_{A\gamma}$ and i_A). Apparently the total current i_A has better shape. The spectra of the three currents are shown in Fig.4-8(b), (d) and (f), from which the THD can be calculated as 7.8%, 7.7% and 2.7% respectively. Considering that no input filter is applied, the 2.7% overall THD is a good index of performance. In the spectra of i_A and $i_{A\Delta}$, some lower order harmonics can be identified. However most of the lower order harmonics are diminished in the spectrum of i_A .

To compare the details of the current waveforms and the spectra, Fig.4-8(g) displays the current waveform in a single frame and Fig.4-8(h) shows the vertically zoomed spectra. The harmonic cancellation pattern is consistent with theoretical expectation of Table 2.3. Because the non-ideal parameters of the 18-pulse PSTs, non-characteristic harmonics such as the 5th, 7th, 11th, 13th, 23rd, 25th and so on, appear in the spectra of $i_{A\Delta}$ and $i_{A\gamma}$ (the top and middle traces of Fig.4-8(h)). However some of these harmonics, such as the 5th, 7th, 17th, 19th and so on, are neutralized in the spectra of i_A (bottom trace) due to cancellation Pattern 2 (Section 2.3.2), which is consistent with the simulation results of Fig.2-15. The cancellation of the 5th and 7th harmonics is a big relief because these two are the nastiest harmonics.

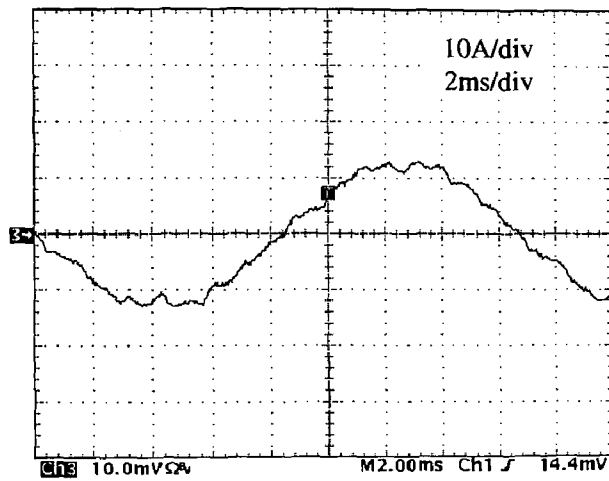
It is reasonable to deduce that if the 18-pulse PSTs were defectiveness, the 11th, 13th, 23rd and 25th harmonics would be neutralized within the PSTs, thus the lowest harmonic should be the 35th. The third harmonic peak is caused by the lack of three phase asymmetry.



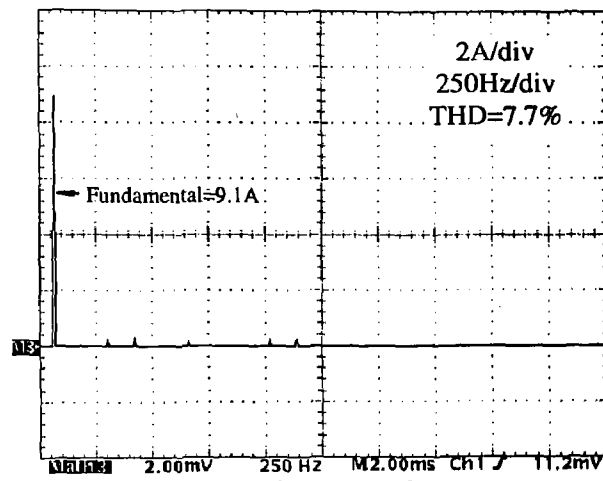
(a) Input Current of PST with Δ -primary ($i_{A\Delta}$)



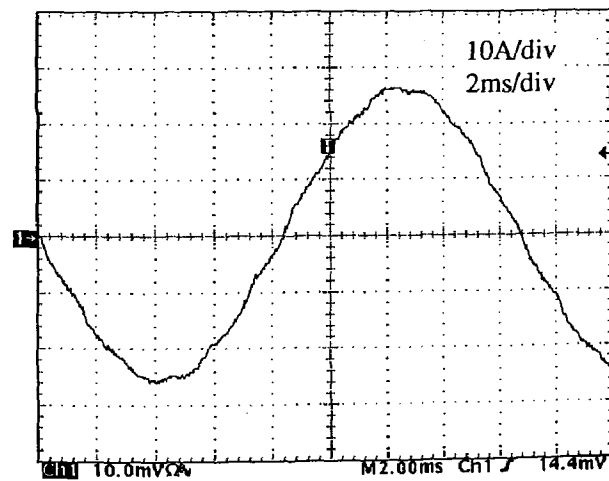
(b) Spectrum of $i_{A\Delta}$



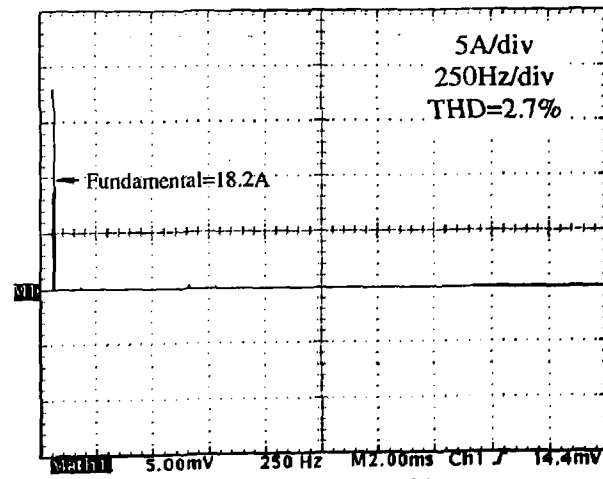
(c) Input Current of PST with Y-primary (i_{AY})



(d) Spectrum of i_{AY}



(e) Total Input Current (i_A)



(f) Spectrum of i_A

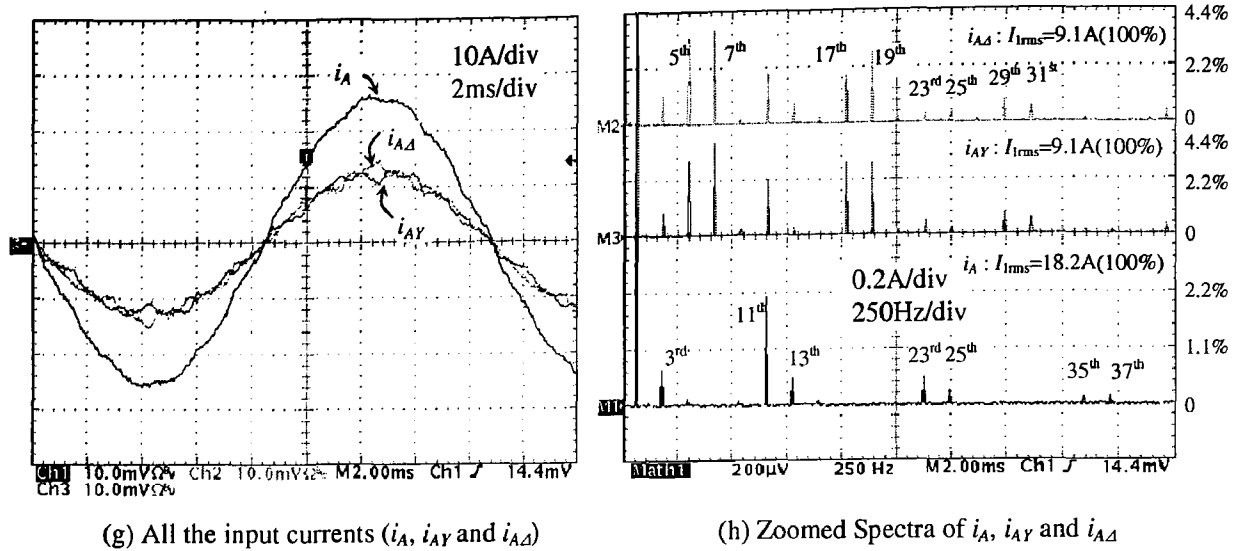


Fig.4-8 Experiment waveforms of the input currents.

4.2.2 Output voltage of the Inverter

The performance of the flexible 3-segment and 7-segment SVM schemes was compared at difference sampling frequencies and fundamental frequencies. The output line-to-line voltage and their spectra are recorded.

Fig.4-9 shows the waveforms and spectra of the output voltages obtained by the 3-segment SVM when the fundamental frequency $f_1=60\text{Hz}$. The line-to-neutral voltage v_{an} and line-to-line voltage v_{ab} are shown in Fig.4-9(a), where v_{an} contains 5 voltage levels and v_{ab} 9 levels. The spectra of the voltages are shown in Fig.4-9(b). To shown relative magnitude of the harmonics, Fig.4-9(c) shows the zoomed spectra, from which the first sideband can be identified. The centre of the first sideband is at 3780Hz, which is $0.5f_{sp}$. Fig.4-9(d) shows more detailed spectra over 0-5kHz, from which it can been seen that v_{an} contains triplen harmonics while v_{ab} contains only non-triplen odd harmonics.

Fig.4-10 shows comparatively the waveforms and spectra obtained by 7-segment SVM when $f_1=60\text{Hz}$. The most distinct difference is the centre of the first sideband is now 2520Hz, which is the same as the sampling frequency for 7-segment SVM. It should be noted that the ideal average device switching frequencies are the same for both SVM schemes. Thus it can

be concluded that the flexible 3-segment SVM can increase the inverter sampling frequency by 50% ($3780/2520=1.5$).

It can also be found that in both case the spectra contain no even harmonics.

The waveforms and spectra are consistent with the simulation results of Fig.3-19, Fig.3-20, Fig.3-21 and Fig.3-22.

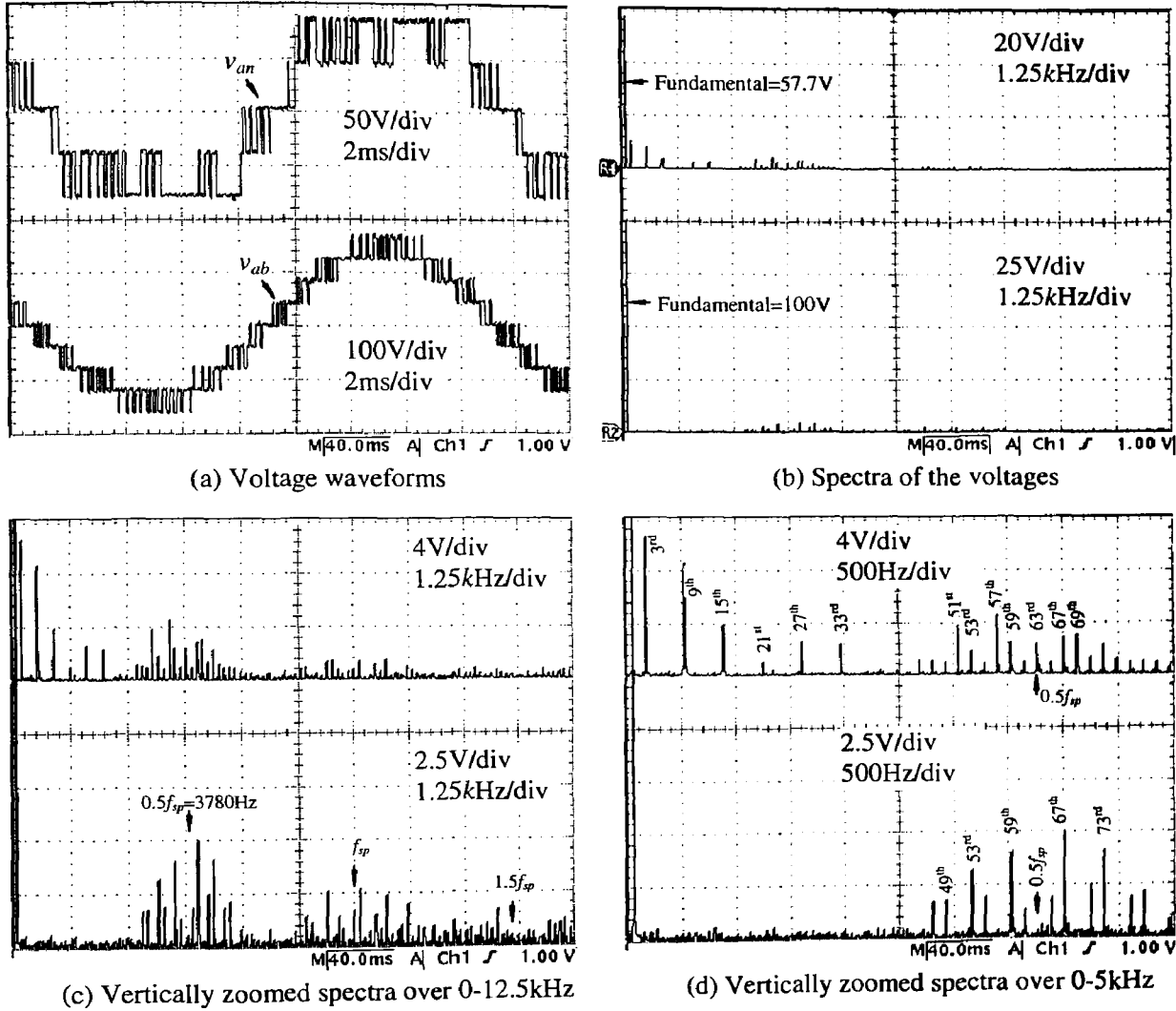
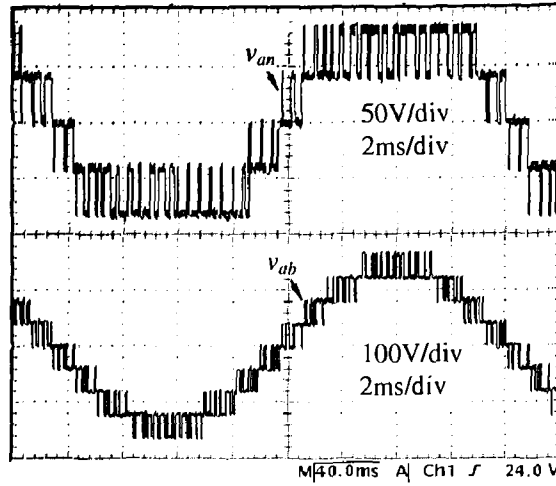
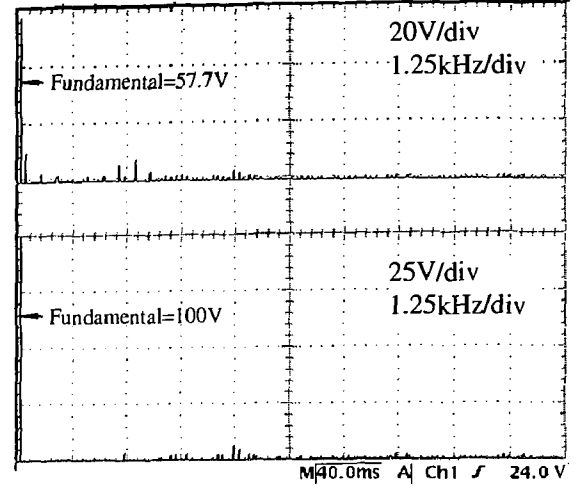


Fig.4-9 Experiment waveforms of inverter output voltage(3-segment SVM, $f_1=60\text{Hz}$).

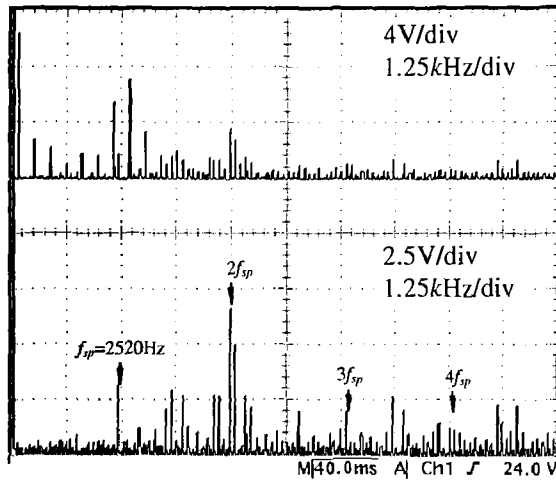
$$(f_{sp}/f_1=126, f_{sw_ideal}=630\text{Hz and } m_a=0.87)$$



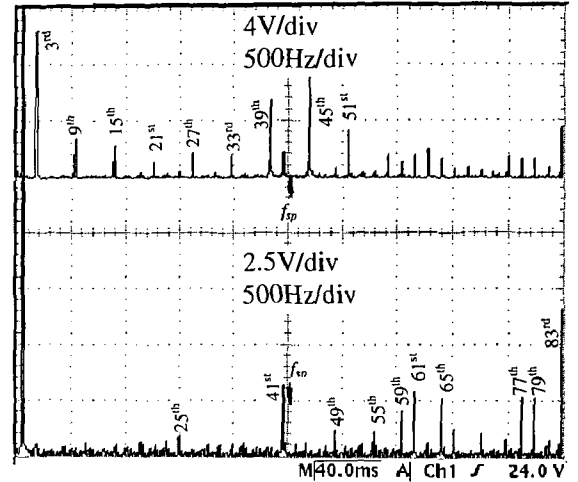
(a) Voltage waveforms



(b) Spectra of the voltages



(c) Vertically zoomed spectra over 0-12.5kHz

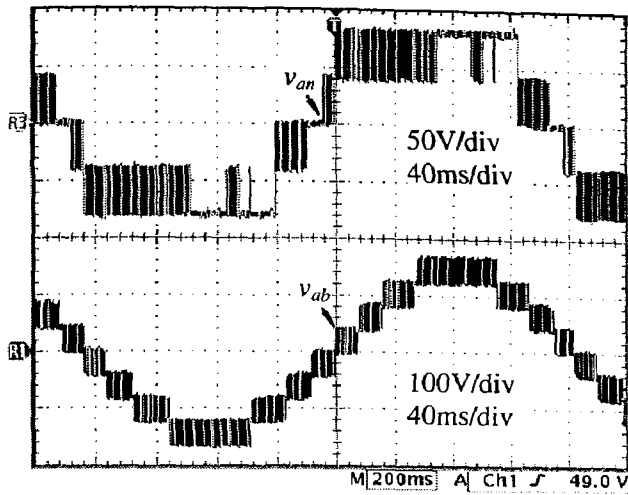


(d) Vertically zoomed spectra over 0-5kHz

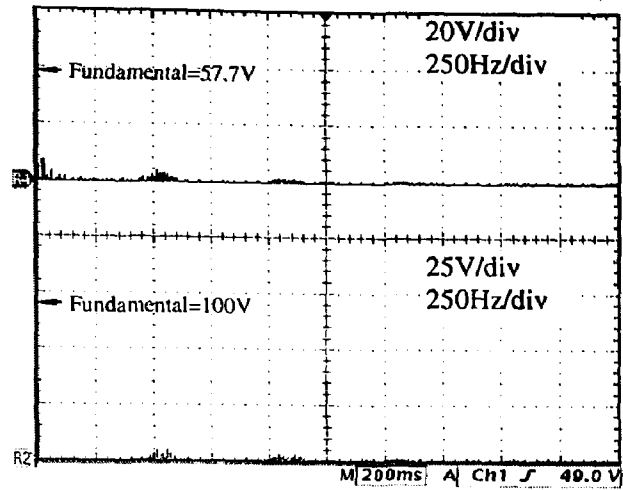
Fig.4-10 Experiment waveforms of inverter output voltage (7-segment SVM, $f_i=60\text{Hz}$).

$$(f_{sp}/f_1=42, f_{sw_ideal}=630\text{Hz and } m_a=0.87)$$

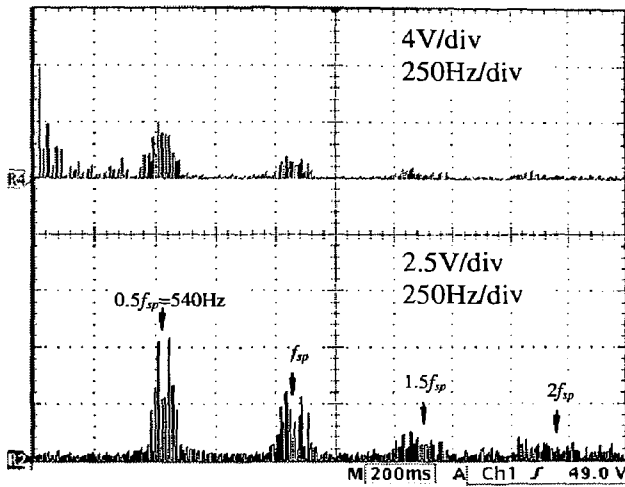
The sidebands are not easy to be recognized in Fig.4-9 and Fig.4-10 because the normalized sampling frequency is relatively low and the sidebands are merged to some extent. Fig.4-11 and Fig.4-12 show the waveforms and spectra of another case: $f_1=3\text{Hz}$ and $f_{sw_ideal}=90\text{Hz}$. The waveforms obtained by 3-segment SVM are shown in Fig.4-11. The sidebands can be clearly identified. The inverter sampling frequency is 540Hz. Fig.4-12 shows the waveforms obtained by conventional 7-segment SVM, the sideband bands can also be clearly identified and the inverter sampling frequency is 360Hz, which is 2/3 of the inverter frequency of the 3-segment SVM.



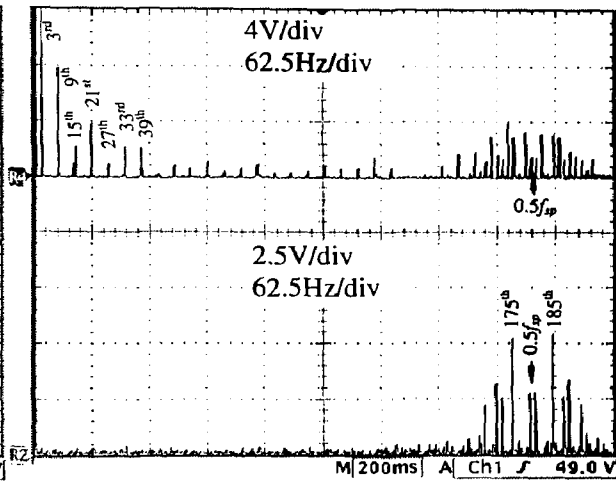
(a) Voltage waveforms



(b) Spectra of the voltages



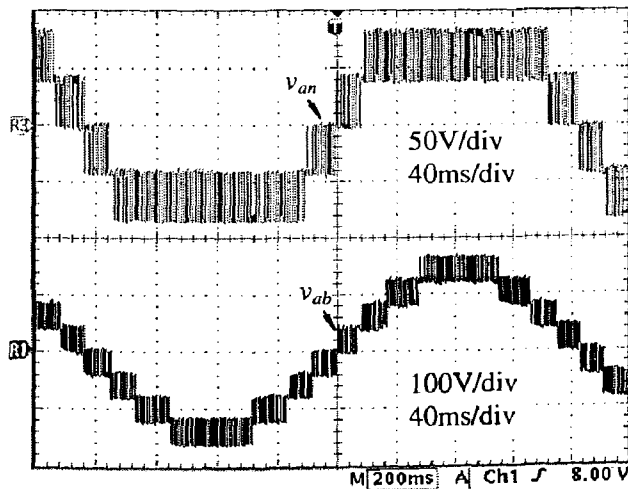
(c) Vertically zoomed spectra over 0-2.5kHz



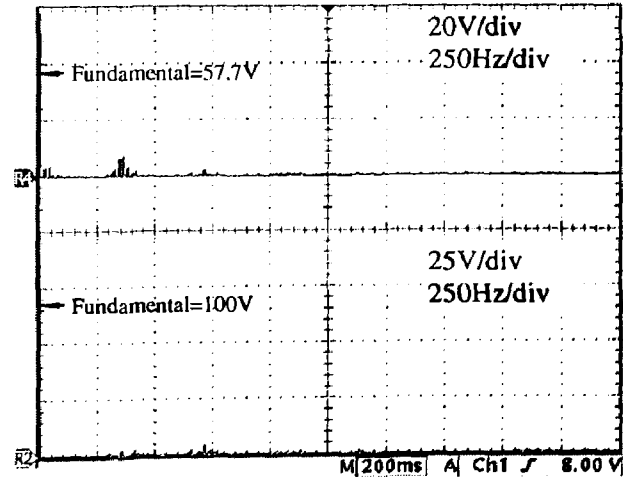
(d) Vertically zoomed spectra over 0-625Hz

Fig.4-11 Experiment waveforms of inverter output voltage (3-segment SVM, $f_1=3\text{Hz}$).

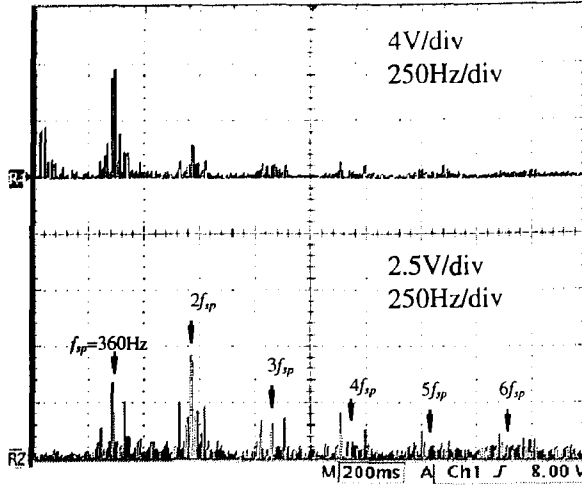
$$(f_{sp}/f_1=360, f_{sw_ideal}=90\text{Hz and } m_a=0.87)$$



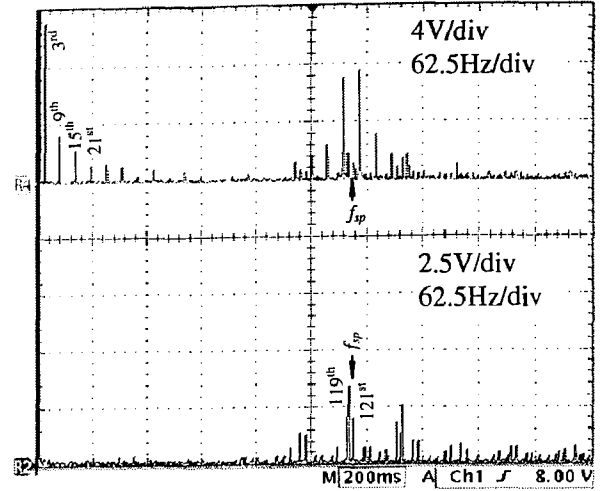
(a) Voltage waveforms



(b) Spectra of the voltages



(c) Vertically zoomed spectra over 0-2.5kHz



(d) Vertically zoomed spectra over 0-625Hz

Fig.4-12 Experiment waveforms of inverter output voltage (7-segment SVM, $f_1=3\text{Hz}$).

($f_{sp}/f_1=120$, $f_{sw_ideal}=90\text{Hz}$ and $m_a=0.87$)

More waveforms and spectra can be found in Appendix 4 for various sampling frequencies.

4.3 Summary

This chapter presents the experimental setup and results. The overall block diagram of the system, the planning and testing of the 18-pulse PSTs, the coding schemes for the NPC/H-bridge inverter and the Simulink/RTI model are introduced in detail. Experiments were carried out to test the dual 18-pulse rectifier and to compare the performance of the conventional 7-segment and flexible 3-segment SVM schemes. It can be concluded from the experiment that:

- (1) The harmonic cancellation pattern of the dual 18-pulse PST based rectifier is consistent with the theoretical expectation.
- (2) The proposed rectifier provides additional opportunity to cancel the 5th and 7th harmonics when the 18-pulse transformers are non-ideal.
- (3) The performance of the proposed 3-segment SVM scheme is verified by the experiment. The inverter sampling frequency is 50% high than that of the 7-segment SVM scheme.

CHAPTER 5 CONCLUSIONS

The thesis is devoted to the development of a multi-pulse rectifier and multilevel inverter for high-power medium voltage (MV) drives. The research can be divided into two parts: the space vector modulation scheme for the multilevel inverter and the topology of the multi-pulse rectifier, both of which involve extensive theoretical analysis, computer simulation and experimental verification.

For the control of multilevel inverters of high-power MV drives, the focus is set on the simplified switching sequence design of space vector modulation. To improve the performance, a flexible 3-segment SVM algorithm is proposed. The design and simulation of the proposed algorithm is introduced in detail. The main contributions are as follows:

(1) The flexible 3-segment SVM algorithm can effectively reduce the actual device switching frequency by $0.5f_1$ to $1.5f_1$, which accounts for a significant percentage of the switching frequency of high-power MV drives. Lower device switching frequency results in lower switching loss. The device switching frequency is reduced because extra switchings at triangle boundaries are minimized.

(2) The inverter can achieve higher sampling frequency by the flexible 3-segment SVM, leading to lower WTHD. The inverter sampling frequency is increased by 50% from that of the 7-segment SVM for the same device switching frequency. This is important for high-power drives because their device switching frequency is usually several hundred Hertz and the inverter sampling frequency is close to the fundamental. Raising the inverter sampling frequency helps to depress the lower order harmonics.

(3) The algorithm is easy for digital implementation because it uses rule-based switching sequence design and a 'sequence reproduction mechanism'. The switching sequence can be generated automatically in real time rather than using look-up-table for all the triangles..

(4) The algorithm is generally applicable to inverters of any voltage levels. Although the

experiment was performed for the 5-level NPC/H-bridge inverters, the flexible 3-segment SVM can be used for the other multilevel topologies.

(5) The algorithm is intrinsically half-wave symmetrical and produces no even harmonics. It can be used for PWM rectifiers where the even-order harmonics are strictly regulated by IEEE Standard 519-1992.

To simplify the multi-pulse rectifier and enhance the harmonic cancellation effect, a dual 18-pulse rectifier topology is proposed for multilevel inverters. Theoretical analyses, simulations and experiments confirm the following features of the dual 18-pulse rectifier.

(1) It uses simpler phase-shifting transformers (PSTs). Compared to 24-pulse or 30-pulse rectifiers for advanced high-power MV drives, the proposed rectifier uses standard 18-pulse transformers rather than more complex higher-pulse transformers.

(2) It enhances harmonic cancellation. The performance is equivalent to that of the 36-pulse rectifier. It also provides additional harmonic cancellation for the 5th and 7th harmonics caused by non-ideal transformers.

For the future work, it is suggested to

(1) further study the modulation schemes which can balance the power flows of different secondary windings of the PSTs;

(2) compare the performance of the dual 18-pulse rectifier with that of the 36-pulse rectifier.

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APPENDIX

1. SVM computation in hexangular coordinates

1.1 Hexangular Coordinates

The hexangular coordinate system can be used to simplify the computation involved in SVM. To set up the hexangular system (goh), the lines $y=0$ and $y=x\tan 60^\circ$ in the rectangular Cartesian system (xoy) are used as the basis for plane, which is shown Fig.A-1.

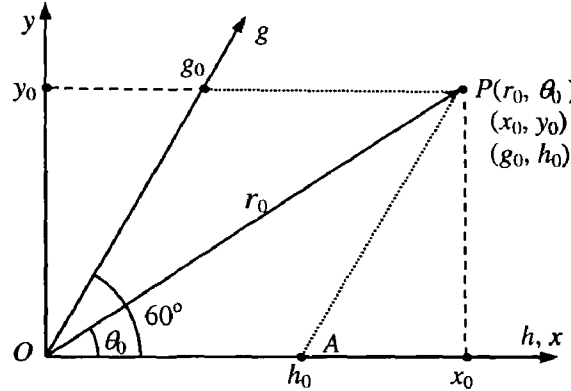


Fig.A-1 Coordinate transformation from rectangular to hexangular system

The coordinate of the point P , (x_0, y_0) in rectangular form, or (r_0, θ_0) in polar form, can be converted into hexangular form by applying the Law of Sines in $\triangle OPA$:

$$\begin{cases} g_0 = r_0 \sin(\theta_0 + 120^\circ) / \sin(120^\circ) = x_0 - \frac{y_0}{\sqrt{3}} \\ h_0 = r_0 \sin \theta_0 / \sin(120^\circ) = \frac{2y_0}{\sqrt{3}} \end{cases} \quad (A1.1)$$

1.2 Computation of the Stationary Vector Plot

Now apply the transformation to the Forward Clarke Transformation of Eq.(1.4). For a given the switching state $[S_a, S_b, S_c]$, the three-phase voltage are $v_{i0} = S_x E$ where $i = a, b$ and c , and E is the step voltage. From Eq.(1.4), the stationary vector is:

$$\begin{cases} v_x = \frac{2}{3} E (S_a - 0.5S_b - 0.5S_c) \\ v_y = \frac{2}{3} E \times \frac{\sqrt{3}}{2} (S_b - S_c) \end{cases} \quad (A1.2)$$

Applying Eq.(A1.1) to Eq.(A1.2) and scaling the result by $\frac{2}{3}E$, we have:

$$\begin{cases} g = S_a - S_b \\ h = S_b - S_c \end{cases}, \quad (\text{A1.3})$$

where (g, h) is the hexangular coordinates of the stationary vector. It is interesting to note that the hexangular coordinates are in fact the normalized line-to-line voltages v_{ab} and v_{bc} .

Consider the following two situations related to stationary vectors of multilevel inverters:

(1) Given the switching state, find the corresponding stationary vector. The solution is quite straightforward from Eq.(A1.3). For example given the switching state $[1, -2, 1]$, we can quickly figure out it belongs to the stationary vector $(3, -3)$.

(2) Given the stationary vector, find all of the redundant switching states.

Rewrite Eq.(A1.3) using S_a as the parameter:

$$\begin{cases} S_b = S_a - g \\ S_c = S_a - g - h \end{cases}. \quad (\text{A1.4})$$

It is clear from Eq.(A1.4) that the solution is not unique because we have three unknowns but only the two equations.

For a $(2n+1)$ -level inverter, S_a , S_b and S_c can be any integers from $-n$ to n . Thus the following constraints are imposed upon Eq. (A1.4):

$$-n \leq S_a, S_b, S_c \leq n. \quad (\text{A1.5})$$

For any given stationary vector (g, h) , we can use Eqs.(A1.4) and Eq.(A1.5) to decide the switching states. First find all the possible values for S_a . Rewrite (A1.5) into three separate inequalities and substitute Eq.(A1.4) for S_b and S_c ,

$$\begin{cases} -n \leq S_a \leq n \\ -n + g \leq S_a \leq n + g \\ -n + g + h \leq S_a \leq n + g + h \end{cases}, \quad (\text{A1.6})$$

or

$$\max(-n, -n + g, -n + g + h) \leq S_a \leq \min(n, n + g, n + g + h). \quad (\text{A1.7})$$

For any given stationary vector (g, h) , we can use Eqs. (A1.4) and (A1.7) to find all the switching states. Table A.1 shows the results for the 6 sectors.

Table A.1 Switching states for stationary vector (g, h)

	Sector I	Sector II	Sector III
	$g \geq 0, h \geq 0$	$g < 0, h \geq 0, g + h \geq 0$	$g < 0, h \geq 0, g + h < 0$
S_a	$n, n-1, \dots, (-n+g+h)$	$(n+g), (n+g)-1, (-n+g+h)$	$(n+g), (n+g)-1, \dots, -n$
(S_a, S_b, S_c)	(S_a, S_a-g, S_a-g-h)	(S_a, S_a-g, S_a-g-h)	(S_a, S_a-g, S_a-g-h)
# of redundancies	$(2n+1)-(g+h)$	$(2n+1)-h$	$(2n+1)+g$
	Sector IV	Sector V	Sector VI
	$g < 0, h < 0$	$g \geq 0, h < 0, g + h < 0$	$g \geq 0, h < 0, g + h \geq 0$
S_a	$(n+g+h), (n+g+h)-1, \dots, -n$	$(n+g+h), (n+g+h)-1, -n+g$	$n, n-1, \dots, -n+g$
(S_a, S_b, S_c)	(S_a, S_a-g, S_a-g-h)	(S_a, S_a-g, S_a-g-h)	(S_a, S_a-g, S_a-g-h)
# of redundancies	$(2n+1)+g+h$	$(2n+1)+h$	$(2n+1)-g$

If the inverter has even number of levels, for example $2n$ levels, S_a, S_b and S_c can be any integers from 0 to $2n$, which is shifted from that of odd number of levels by n . We can analyze the case in a similar way.

Now some general conclusions are:

(1) For a given switching state $[S_a, S_b, S_c]$, the stationary vector is $[S_a-S_b, S_b-S_c]$, the number of redundant switching states is $((2n-1)-(\max(S_i)-\min(S_i)))$, where $i=a, b, c$. E.g.: Given the state $[1, -2, 0]$ of a 5-level inverter, it belongs to the vector $(1-(-2), -2-0)=(3, -2)$ and the number of redundancies for this vector is $5-(1-(-2))=2$.

(2) For a given stationary vector (g, h) , the switching states are $[S_a, S_a-g, S_a-g-h]$, where $\max(-n, -n+g, -n+g+h) \leq S_a \leq \min(n, n+g, n+g+h)$. E.g.: Given the vector $(-1, -2)$ of a 5-level inverter, the switching states are $[-1, 0, 2]$ and $[-2, -1, 1]$.

1.3 Detection of NTVs

In the hexangular system, it is easy to find the nearest three vectors (NTVs) for the reference vector. As an example, Fig.A-2 shows the case when the reference vector **OV** is located in Sector I of a 6-level inverter. The NTVs can be detected by first locating to which parallelogram V belongs then identifying the triangle by which it is inscribed.

In Fig.A-2 the vertex $A(g_0, h_0)$, which is the closest to the origin, can be determined by

$$(g_0, h_0) = \text{fix}((g, h)), \quad (\text{A1.8})$$

where (g, h) is the coordinates of \mathbf{OV} , and function $\text{fix}(x)$ rounds the elements of x to the nearest integers towards zero. The other three vertices are $B(g_0+1, h_0)$, $C(g_0+1, h_0+1)$ and $D(g_0, h_0+1)$

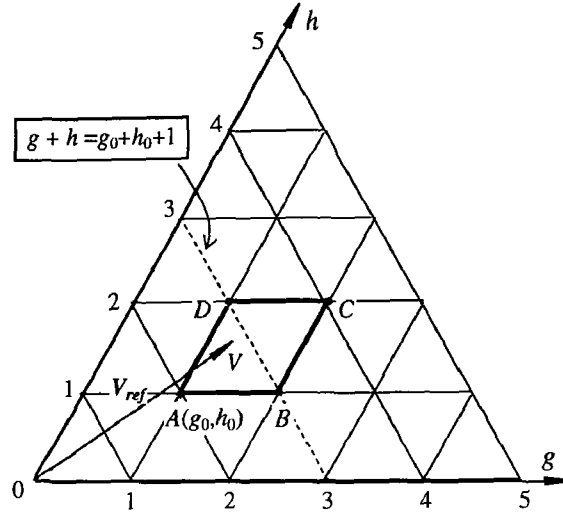


Fig.A-2 Identification of the nearest three vectors.

Now further decide in which triangle V is located. In hexangular system, the equation of line BD is $g+h = g_0+h_0+1$. The points above or on line BD satisfy $g+h \geq g_0+h_0+1$ while points below the line satisfy $g+h < g_0+h_0+1$. Thus if $g+h \geq g_0+h_0+1$, V is in $\triangle BCD$, otherwise it is in $\triangle ABD$. In brief, the NTVs can be found in two steps:

(1) Point V is in parallelogram $ABCD$, whose vertices are $A(g_0, h_0) = \text{fix}((g, h))$, $B(g_0+1, h_0)$, $C(g_0+1, h_0+1)$ and $D(g_0, h_0+1)$.

(2) V is in $\triangle ABD$, if $g+h < g_0+h_0+1$. The NTVs are \mathbf{OA} , \mathbf{OB} and \mathbf{OD} .

V is in $\triangle BCD$, if $g+h \geq g_0+h_0+1$. The NTVs are \mathbf{OC} , \mathbf{OB} and \mathbf{OD} .

1.4 Calculation of Dwell Times

The mathematical merit of SVM to represent \mathbf{OV} by the NTVs. Assume at certain moment the reference vector \mathbf{OV} is located in $\triangle ABD$, which is standing upright (Fig.A-3(a)). Vector \mathbf{OV} can be expressed as a linear combination of \mathbf{OA} , \mathbf{OB} and \mathbf{OD} .

$$\mathbf{OV} = \mathbf{OA} + \mathbf{AV} = \mathbf{OA} + m\mathbf{u} + n\mathbf{v}$$

$$= \mathbf{OA} + m(\mathbf{OB} - \mathbf{OA})/AB + n(\mathbf{OD} - \mathbf{OA})/AD$$

$$= (1 - m/AB - n/AD) \mathbf{OA} + (m/AB) \mathbf{OB} + (n/AD) \mathbf{OD}, \quad (\text{A1.9})$$

where \mathbf{u} and \mathbf{v} are the unit vectors along vectors \mathbf{AB} and \mathbf{AD} , $\mathbf{u} = \mathbf{AB}/AB$ and $\mathbf{v} = \mathbf{AD}/AD$, and $m\mathbf{u}$ and $n\mathbf{v}$ are components of \mathbf{AV} resolved along \mathbf{u} and \mathbf{v} , m and n are two scalars.

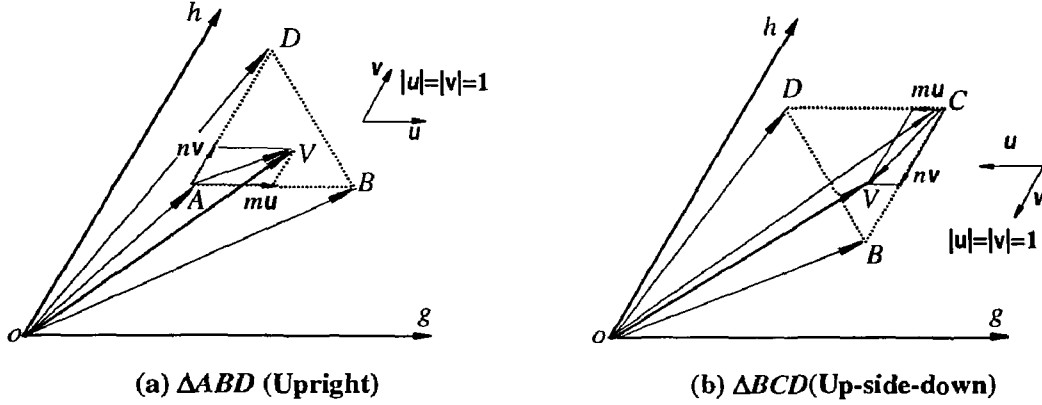


Fig.A-3 Diagram for dwell time calculation.

If we multiply both sides of Eq.(A1.9) by the sampling period T_s , we get the so-called 'volt-second balance' equation with the coefficients being the duty cycles of corresponding vectors. In hexangular coordinate system, $AB=AD=BD=1$. Eq.(A1.9) can be simplified as

$$\mathbf{OV} = (1 - m - n) \mathbf{OA} + m\mathbf{OB} + n\mathbf{OD} \quad (\text{A1.10})$$

Assume the coordinate of V is (g, h) , the coordinate of A is (g_0, h_0) , then $m = g - g_0$, $n = h - h_0$, which are the local coordinates of the point V in the local coordinate system DAB . The duty cycles for \mathbf{OA} , \mathbf{OB} and \mathbf{OD} are:

$$\begin{cases} D_A = 1 - (g - g_0) - (h - h_0) \\ D_B = g - g_0 \\ D_D = h - h_0 \end{cases} \quad (\text{A1.11})$$

Similarly, when \mathbf{OV} is located in up-side-down $\triangle BCD$ (Fig.A-3(b)), the duty cycles for vectors \mathbf{OC} , \mathbf{OB} and \mathbf{OD} are

$$\begin{cases} D_C = 1 - (g_0 - g) - (h_0 - h) \\ D_D = g_0 - g \\ D_B = h_0 - h \end{cases}, \quad (A1.12)$$

where (g_0, h_0) is the coordinates of C .

Eqs.(A1.11) and (A1.12) are very simple compared to the formulas derived in rectangular coordinate system. Because vertices A and C are the origins of the local coordinate system, they are called the base vertices of the triangles.

2. Simulink models of SVM algorithms

2.1 Block diagrams

The Simulink model is shown in Fig.A-4. The subsystem 'Gate Signal' is the main part of the model. The switching sequences and dwell times are calculated in the preload function which initializes the model. The model be used for both 3-segment and 7-segment SVM schemes. However when it used for different SVM schemes, 'Gate Signal' and the preload function must be changed.

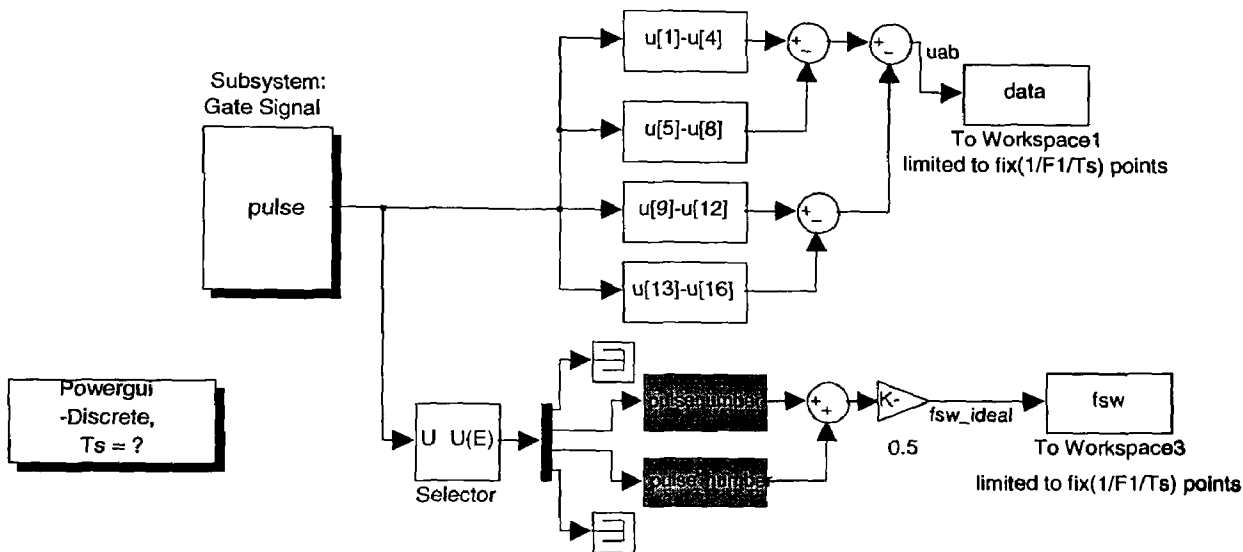
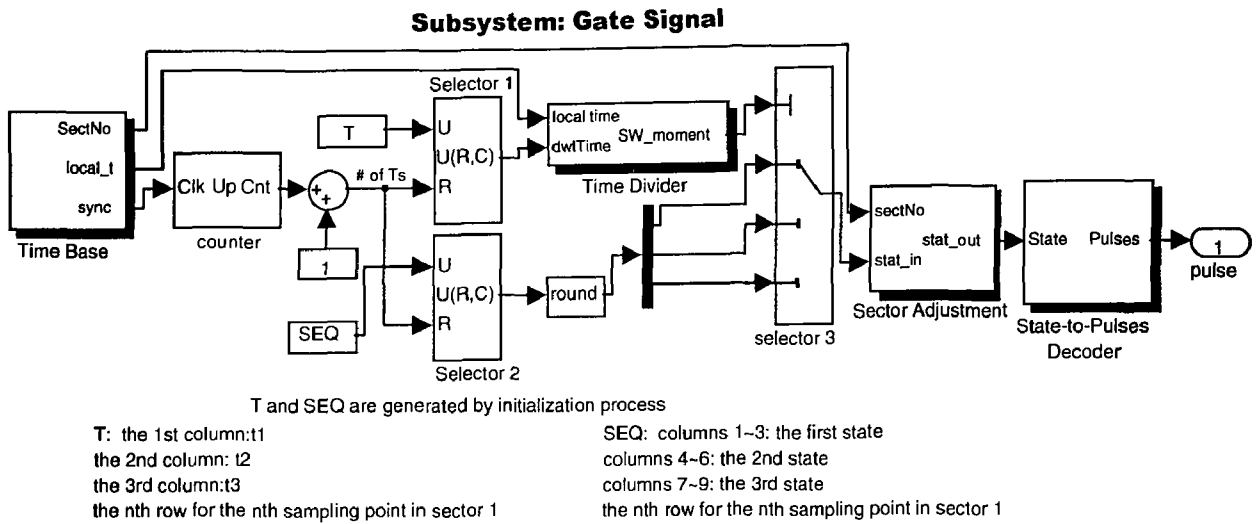


Fig.A-4 Block diagram of the SVM controller for NPC/H-bridge inverter.

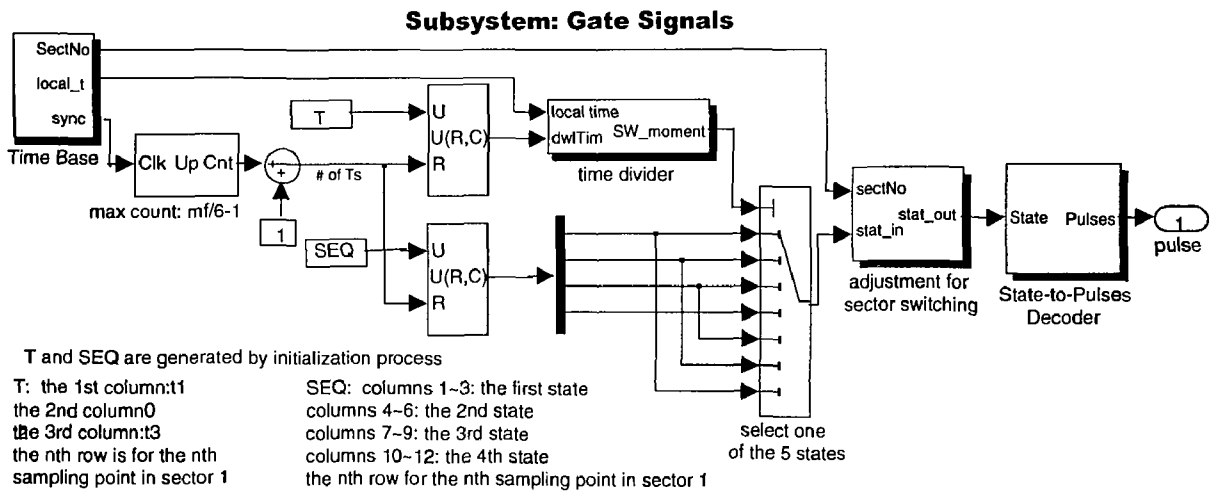
(for 3-segment and 7segment)

The subsystems 'Gate Signal' are shown in Fig.A-5. Fig.A-5 (a) is for the 3-segment SVM. The 'Time Base' subsystem is to calculate the section number (*SectNo*), the real time localized in each sampling period (*local_t*) and the synchronization signal (*sync*) for each sampling period. A counter is used to count the number of the sampling periods, which is used by Selectors 1 and 2 to pick up the corresponding switching sequence and dwell times. A 'Time Divider' subsystem is used to divide the sampling periods into 3 segments and then drive Selector 3 to select one of the three switching states. The subsystem 'Sector Adjustment' is used to reproduce switching sequences for Sectors II to VI. The subsystem 'State-to-Pulse

'Decoder' is used to decode the switching states and generate the gating signals. Similarly the 'Gate Signal' subsystem for 7-segment SVM is shown in Fig.A-5 (b).



(a) 'Gate Signals' for 3-segment SVM



(b) 'Gate Signals' for 7-segment SVM

Fig.A-5 Subsystem 'Gate Signals'

The subsystem 'Time Base' is shown in Fig.A-6, via which the real time is converted into *SectNo* (sector number) signal, *local_t* (local time within each sampling period) and *sync* (synchronization pulses). It can be used for both SVM schemes.

The subsystem 'Time Divider' is shown in Fig.A-7, which splits the sampling period into 3 segments (Fig.A-7(a)) or 7 segments (Fig.A-7(b)) in accordance with to the dwell times. The signal *SW_moment* will be used to decide the moment switching to next state of a sequence.

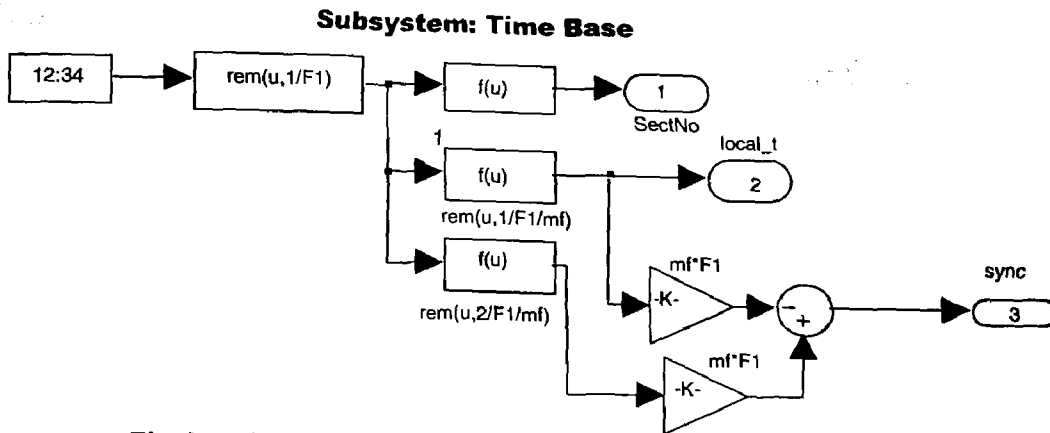
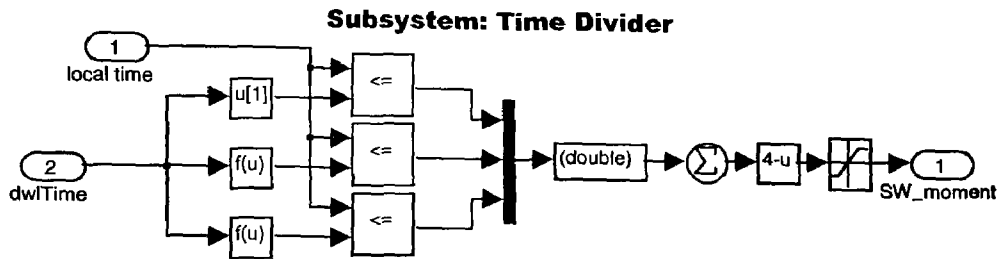
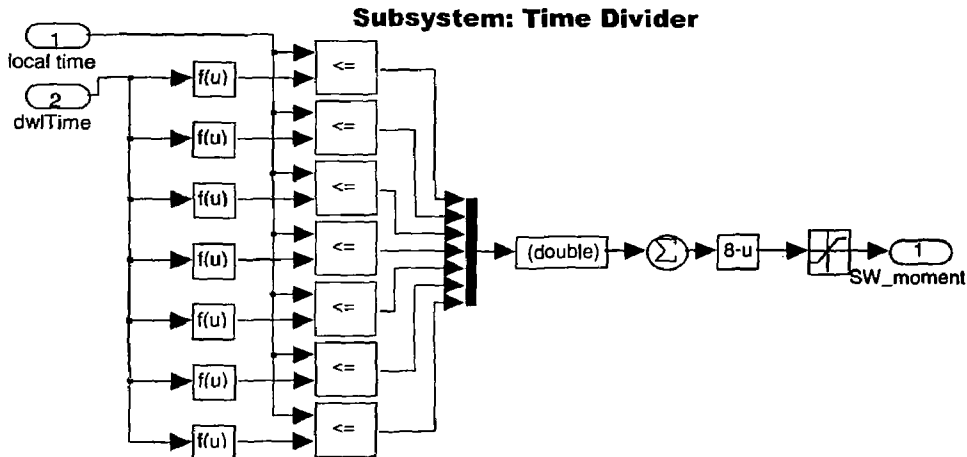


Fig.A-6 Subsystem 'Time Base' (for 3-segment and 7-segment).



(a) 'Time Divider' for 3-segment SVM



(b) 'Time Divider' for 7-segment SVM

Fig.A-7 Subsystem 'Time Divider'.

The subsystem 'Sector Adjustment' is shown in Fig.A-8, which uses the 'negative rotation' to generate switching states for Sectors II to VI. The subsystem can be used for both SVM schemes.

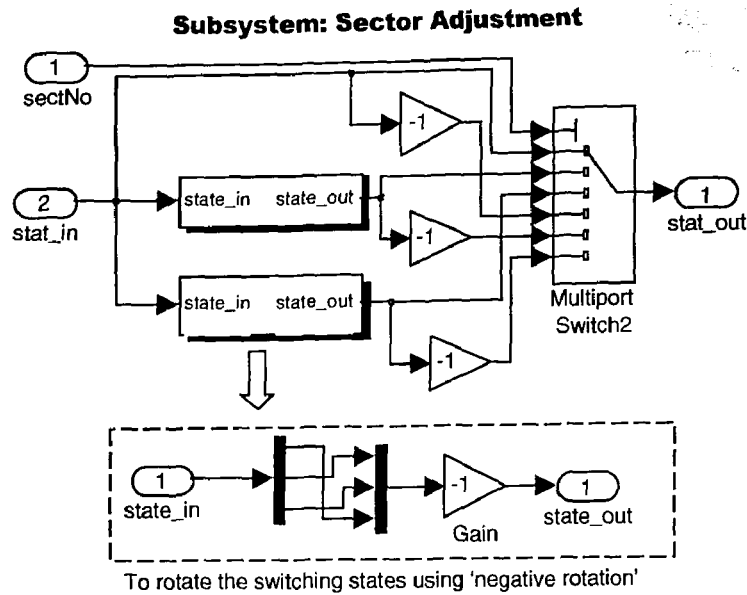


Fig.A-8 Subsystem 'Sector Adjustment' (for 3-segment and 7segment).

The subsystem 'State-to-Pulse Decoder' is shown in Fig.A-9. Two decoding schemes are swapped to balance the gating pattern. The subsystem can be used for both SVM schemes.

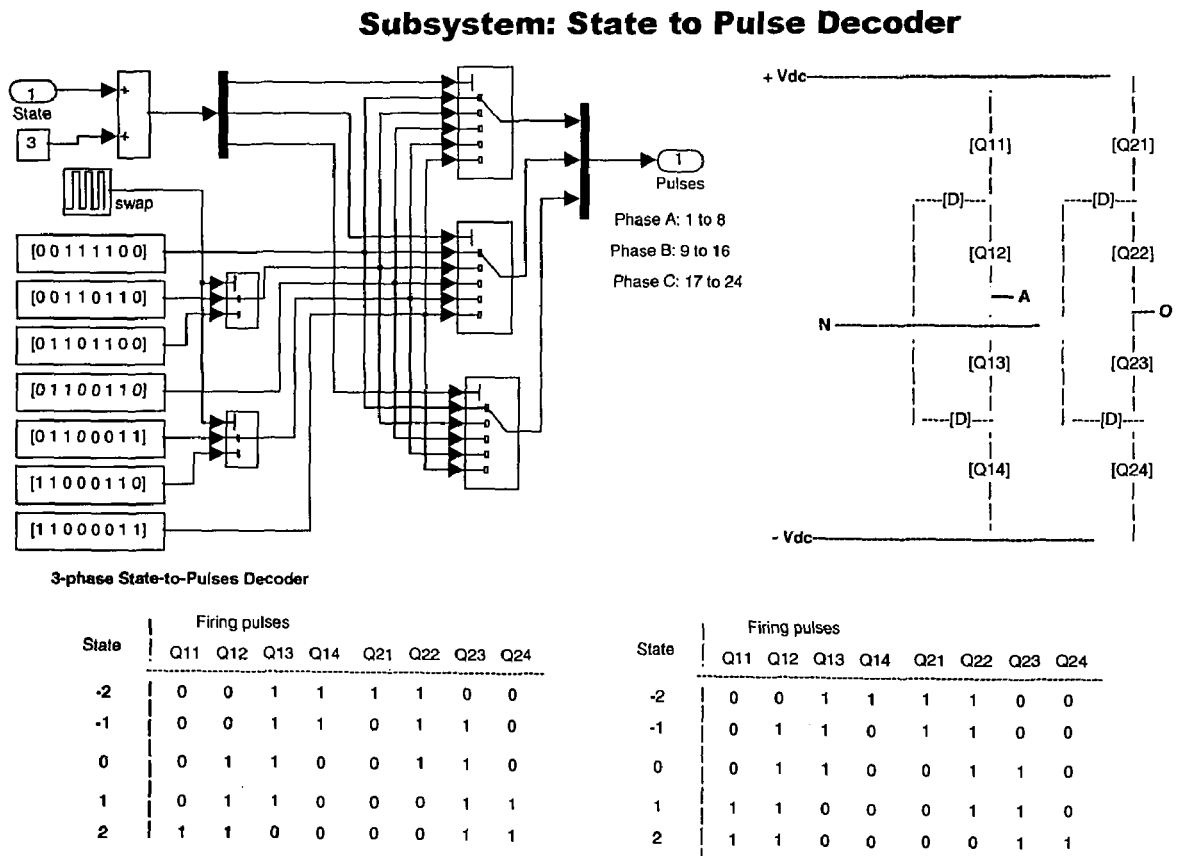


Fig.A-9 Subsystem 'State to Pulse Decoder' (for 3-segment and 7segment).

2.2 Preload function of 3-segment SVM

```
% This program is used to initialize the model
% It is for flexible 3-segment SVM
% Input parameters: f1, mf, Ts, Vstep, Vref
% Output variables (will be used in the model)
% SEQ(n,9): save the 3 states used in a sequence
% T(n,3): dwell time for each state in the sequence
% Intermediate variables:
% STATES(5,3): save all states of a triangle;
% VERTICES(n,6): save NTVs
% in the order A or C then B then D
% VERTEX_ORDER(n,3): vertex order in seq.:
% '1': stands for point A or C, '2' for B, '3' for D
STATES=[];VERTICES=[];VEXTEX_ORDER=[];S
EQ=[];T=[];
```

```
n=mf/6; %number of sampling point each sector
for k=1:n
    alpha=2*pi/mf*(k-0.5); %initial angle 2*pi/mf
    x=sin(pi/3-alpha)/sin(2*pi/3)*Vref;
    y=sin(alpha)/sin(2*pi/3)*Vref;
    xa=floor(x);ya=floor(y); %base vertex
```

```
%%% triangle types %%%
```

```
type=1;
if ((x+y)>(xa+ya+1))&((rem(xa+ya,2)==0))
    type=3; end
if ((x+y)>(xa+ya+1))&~(rem(xa+ya,2)==0))
    type=4; end
if ((x+y)<(xa+ya+1))&~(rem(xa+ya,2)==0))
    type=2; end
```

```
%%% dwell times %%%
```

```
tb=(x-xa)/F1/mf;td=(y-ya)/F1/mf;
if (type==3)|(type==4)
    tb=(ya+1-y)/F1/mf;td=(xa+1-x)/F1/mf; end
tac=1/mf/F1-tb-td;
```

```
clear S;
```

```
switch type %find all available states
```

```
case 1
```

```
S(1,1:3)=[ya+xa+2,ya-xa+2,-ya-xa]/2;
S(2,1:3)=S(1,1:3)-[0,1,0];
S(3,1:3)=S(1,1:3)-[1,1,0];
S(4,1:3)=S(1,1:3)-[1,1,1];
S(5,1:3)=S(1,1:3)-[1,2,1];
```

```
case 2
```

```
S(1,1:3)=[ya+xa+1, ya-xa+1,-ya-xa+1]/2;
S(2,1:3)=S(1,1:3)-[0,0,1];
S(3,1:3)=S(1,1:3)-[0,1,1];
S(4,1:3)=S(1,1:3)-[1,1,1];
```

```
case 3
```

```
S(1,1:3)=[ya+xa+2, ya-xa+2,-ya-xa]/2;
S(2,1:3)=S(1,1:3)-[0,1,0];
```

```
S(3,1:3)=S(1,1:3)-[0,1,1];
S(4,1:3)=S(1,1:3)-[1,1,1];
S(5,1:3)=S(1,1:3)-[1,2,1];
```

```
case 4
```

```
S(1,1:3)=[ya+xa+3, ya-xa+1,-ya-xa-1]/2;
S(2,1:3)=S(1,1:3)-[1,0,0];
S(3,1:3)=S(1,1:3)-[1,1,0];
S(4,1:3)=S(1,1:3)-[1,1,1];
```

```
end
```

```
number_of_states=5; %
```

```
if (type==2)|(type==4)
```

```
    number_of_states=4;end
```

```
%% the 1st state %%
```

```
if k==1
```

```
    if Vref<=0.59
```

```
% if Vref<=sqrt(3)/2*((rem(n,2)==1)+(rem(n,2)==0)*cot(
pi/mf)) % if the point is located in triangle 1, use
scheme 2
```

```
switch type
```

```
case 1
```

```
    first_state=2;
```

```
case 2
```

```
    first_state=4;
```

```
case 3
```

```
    first_state=3;
```

```
case 4
```

```
    first_state=4;
```

```
end
```

```
else
```

```
%otherwise use scheme 4
```

```
switch type
```

```
case 1
```

```
    first_state=3;
```

```
case 2
```

```
    first_state=4;
```

```
case 3
```

```
    first_state=3;
```

```
case 4
```

```
    first_state=4;
```

```
end
```

```
end
```

```
else % search least difference state
```

```
clear State_change Total_change Single_change;
```

```
for k1=1:number_of_states
```

```
    State_change(k1,:)=abs(S(k1,:)-SEQ(k-1,7:9));
```

```
% abs value for each phase; SEQUENCE(k-1,7:9) is
the last state of previous sampling period
```

```
Total_change(k1)=sum(State_change(k1,:));
```

```
% total voltage level change
```

```
Single_change(k1)=max(State_change(k1,:));
```

```

%maximum phase voltage level change
end

Total_change=min(Total_change)==Total_change;
%if a state has min total change, assign '1'
Single_change=(1000-
Single_change).*Total_change; % only keep those
with min total changes

Single_change=max(Single_change)==Single_chang
e;

Single_change=Single_change.*(1:number_of_states
);
first_state=max(Single_change); % pick up the
possible state with least state value as first state;

end

S1=S(first_state,1:3); % pick up the first state;
%% The other two states %%
if first_state < 3
S2=S(first_state+1,:);
S3=S(first_state+2,:);
else
S2=S(first_state-1,:);
S3=S(first_state-2,:);
end

%% set the order of vertex usage %%
switch first_state %for T1 and T3
case 1
vertex_order=[3 2 1];
case 2
vertex_order=[2 1 3];
case 3

```

```

vertex_order=[1 2 3];
case 4
vertex_order=[3 1 2];
case 5
vertex_order=[2 3 1];
end

if rem(type,2)==0
switch first_state
case 1
vertex_order=[1 3 2];
case 2
vertex_order=[3 2 1];
case 3
vertex_order=[2 3 1];
case 4
vertex_order=[1 2 3];
end
end

SEQ(k,1:3)=S1;SEQ(k,4:6)=S2;SEQ(k,7:9)=S3;
%save sequence

for kk=1:3
switch vertex_order(kk)
case 1
T(k,kk)=tac; % T(k,1:3) saves dwell times
case 2
T(k,kk)=tb;
case 3
T(k,kk)=td;
end
end
end

```

2.3 Preload function of 7-segment SVM

```

% This program is used to initialize the model
% Input parameters: fl, mf, Ts, Vstep, Vref
% Output variables (will be used in the model)
% SEQ(n,12): save the 4 states used in a sequence
% T(n,3): dwell time for each state in the sequence
% Intermediate variables:
% STATES(5,3): save all states of a triangle;
% VERTICES(n,6): save NTVs
% in the order A or C then B then D
% VERTEX_ORDER(n,3): vertex order in seq.:
% '1': stands for point A or C, '2' for B, '3' for D
STATES=[];VERTICES=[];VEXTEX_ORDER=[];S
EQ=[];T=[];

```

```

%% hexangular coordinates %%

```

```

n=mf/6; %number of sampling point each sector

for k=1:n
alpha=2*pi/mf*(k-0.5); %angle of sampling point,
theta0=2*pi/mf
x=sin(pi/3-alpha)/sin(2*pi/3)*Vref;
y=sin(alpha)/sin(2*pi/3)*Vref;
xa=floor(x);ya=floor(y); %base vertex

%%% triangle types %%%
if ((x+y)<=(xa+ya+1))&((rem(xa+ya,2)==0))
type=1;
vertex=[xa,ya,xa+1,ya,xa,ya+1];
else if ((x+y)>(xa+ya+1))&((rem(xa+ya,2)==0))
type=3;

```

```

vertex=[xa,ya,xa,ya-1,xa-1,ya];
else if ((x+y)<=(xa+ya+1))&(~(rem(xa+ya,2)==0))
type=2;
vertex=[xa,ya,xa+1,ya,xa,ya+1];
else
type=4;
vertex=[xa,ya,xa,ya-1,xa-1,ya];
end

%%% dwell times %%%
if (type==3)|(type==4)
tb=(ya+1-y)/F1/mf;td=(xa+1-x)/F1/mf;
else
tb=(x-xa)/F1/mf;td=(y-ya)/F1/mf;
end
tac=1/mf/F1-tb-td;

switch type %find all available middle states
case 1
STATES(1,1:3)=[ya+xa+2,ya-xa+2,-ya-xa]/2;
STATES(2,1:3)=STATES(1,1:3)-[0,1,0];
STATES(3,1:3)=STATES(1,1:3)-[1,1,0];
STATES(4,1:3)=STATES(1,1:3)-[1,1,1];
STATES(5,1:3)=STATES(1,1:3)-[1,2,1];
case 2
STATES(1,1:3)=[ya+xa+1, ya-xa+1,-ya-
xa+1]/2;
STATES(2,1:3)=STATES(1,1:3)-[0,0,1];
STATES(3,1:3)=STATES(1,1:3)-[0,1,1];
STATES(4,1:3)=STATES(1,1:3)-[1,1,1];
case 3
STATES(1,1:3)=[ya+xa+2, ya-xa+2,-ya-xa]/2;
STATES(2,1:3)=STATES(1,1:3)-[0,1,0];
STATES(3,1:3)=STATES(1,1:3)-[0,1,1];

```

```

STATES(4,1:3)=STATES(1,1:3)-[1,1,1];
STATES(5,1:3)=STATES(1,1:3)-[1,2,1];
case 4
STATES(1,1:3)=[ya+xa+3, ya-xa+1,-ya-xa-
1]/2;
STATES(2,1:3)=STATES(1,1:3)-[1,0,0];
STATES(3,1:3)=STATES(1,1:3)-[1,1,0];
STATES(4,1:3)=STATES(1,1:3)-[1,1,1];
end

if (type==2)|(type==4)
order=[1 3 2]; %for T2 and T4
else
order=[3 2 1]; % for T1 and T3
end

%save sequence
SEQ(k,1:3)=STATES(1,:);
SEQ(k,4:6)=STATES(2,:);
SEQ(k,7:9)=STATES(3,:);
SEQ(k,10:12)=STATES(4,:);

for kk=1:3
switch order(kk)
case 1
T(k,kk)=tac; % T(k,1:3) saves dwell times
case 2
T(k,kk)=tb;
case 3
T(k,kk)=td;
end
end
VERTICES(k,:)=vertex;
VERTEX_ORDER(k,:)=order;
end

```

2.4 Mat lab program for automatic simulation

```

% Program to run automatic simulation
% the results are saved as .txt file in the current
directory
% important note: make sure the variable name is not
the same as that in the
% initialization preload function

clc;clear all;
for mf=12:6:216
assignin('base','F1',[60]);
assignin('base','Vstep',[1]);

%% select a simulation step Ts~1us
factor=100;
while 1/F1/mf/60/factor<1e-6
factor=factor-1;
if factor==1

```

```

break;
end
end
Ts=1/F1/mf/60/factor;

k_index=1;
for Vref=0.01:0.01:3.46
clear S data OUT;
sim Fix_Seven_segment_fast_run_ver2.mdl;
%the model saves vab data and fsw arrays to
workspace; change the file name for 3-segment SVM

%get the switching frequency
n=length(fsw);
FSW(k_index,1)=fsw(n); %record the last data

% to calculate the thd(%),wthd(%),V1rms

```

% The file name of the input is data, which is generated by To-workspace block

% For fixed step model, if the sampling time is Ts, fundamental is F1 (Hz),

% the number of points in data should be fix(1/F1/Ts), i.e. one cycle

% the dc and rms value of each harmonic are stored in OUT

N=length(data);NN=ceil(N/2);S=2*fft(data)/N;

OUT(1)=S(1)/2;OUT(2:NN)=S(2:NN);OUT(2:NN)=abs(OUT(2:NN)).*(abs(OUT(2:NN))>1e-6)/sqrt(2);

OUT=OUT*Vstep;

thd=sqrt(OUT(1)^2+sum(abs(OUT(3:NN).^2)))/OUT(2)*100;

wthd=sqrt(sum(abs(OUT(3:NN)).^2)/(3:NN).^2)/OUT(2)*100;

%save thd, wthd and all harmonic rms arrays

THD(k_index,1)=thd;

WTHD(k_index,1)=wthd;

V1RMS(k_index,1)=OUT(2);

V5RMS(k_index,1)=OUT(6);

V7RMS(k_index,1)=OUT(8);

V11RMS(k_index,1)=OUT(12);

V13RMS(k_index,1)=OUT(14);

V17RMS(k_index,1)=OUT(18);

V19RMS(k_index,1)=OUT(20);

V23RMS(k_index,1)=OUT(24);

V25RMS(k_index,1)=OUT(26);

V29RMS(k_index,1)=OUT(30);

V31RMS(k_index,1)=OUT(32);

V35RMS(k_index,1)=OUT(36);

V37RMS(k_index,1)=OUT(38);

k_index=k_index+1;

end

assignin('base',strcat('THD_mf,num2str(mf)'),THD);

save(strcat('THD_mf,num2str(mf),'_7seg_ver2.txt'),'THD','-ascii');

assignin('base',strcat('WTHD_mf,num2str(mf)'),WTHD);

save(strcat('WTHD_mf,num2str(mf),'_7seg_ver2.txt'),'WTHD','-ascii');

assignin('base',strcat('V1RMS_mf,num2str(mf)'),V1RMS);

save(strcat('V1RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V1RMS','-ascii');

save(strcat('V5RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V5RMS','-ascii');

save(strcat('V7RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V7RMS','-ascii');

save(strcat('V11RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V11RMS','-ascii');

save(strcat('V13RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V13RMS','-ascii');

save(strcat('V17RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V17RMS','-ascii');

save(strcat('V19RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V19RMS','-ascii');

save(strcat('V23RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V23RMS','-ascii');

save(strcat('V25RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V25RMS','-ascii');

save(strcat('V29RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V29RMS','-ascii');

save(strcat('V31RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V31RMS','-ascii');

save(strcat('V35RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V35RMS','-ascii');

save(strcat('V37RMS_mf,num2str(mf),'_7seg_ver2.txt'),'V37RMS','-ascii');

assignin('base',strcat('FSW_mf,num2str(mf)'),FSW);

save(strcat('FSW_mf,num2str(mf),'_7seg_ver2.txt'),'FSW','-ascii');

end

assignin('base','Vref',[0.01:0.01:3.46]);

save(strcat('Vref','_7seg_ver2.txt'),'Vref','-ascii');

disp('\$ Finished \$')

3. Performance comparison for various m_a and f_{sp}

The simulated curves presented here are to compare the performance of the flexible 3-segment and 7-segment SVM schemes for various sampling frequencies f_{sp} and modulation indices m_a . There are 6 scenarios for the comparison, covering ideal average switching frequency from 180Hz to 630Hz. For each scenario, the THD, WTHD, f_{sw_actual}/f_1 (normalized average actual switching frequency) and V_{1rms}/E (normalized fundamental voltage) versus m_a or V_{ref} (magnitude of reference) are compared. The topology of the inverter is 5-level NPC/H-bridge based and the fundamental frequency $f_1 = 60\text{Hz}$.

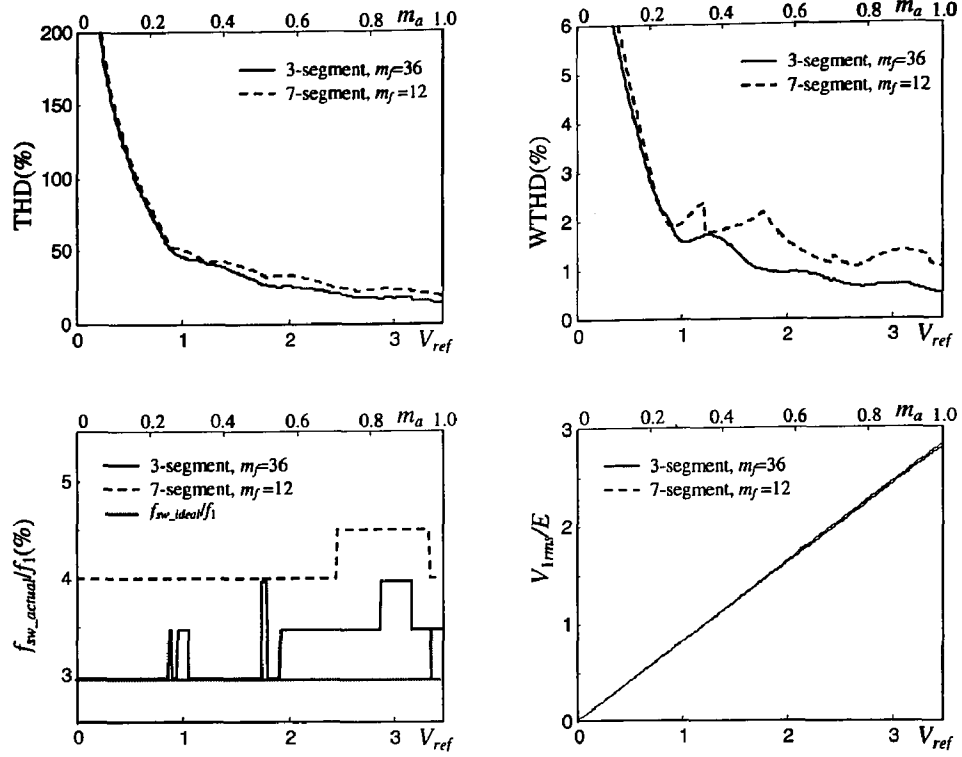
$$V_{ref} = 2 m_a \sqrt{3};$$

$$m_f = f_{sp}/f_1$$

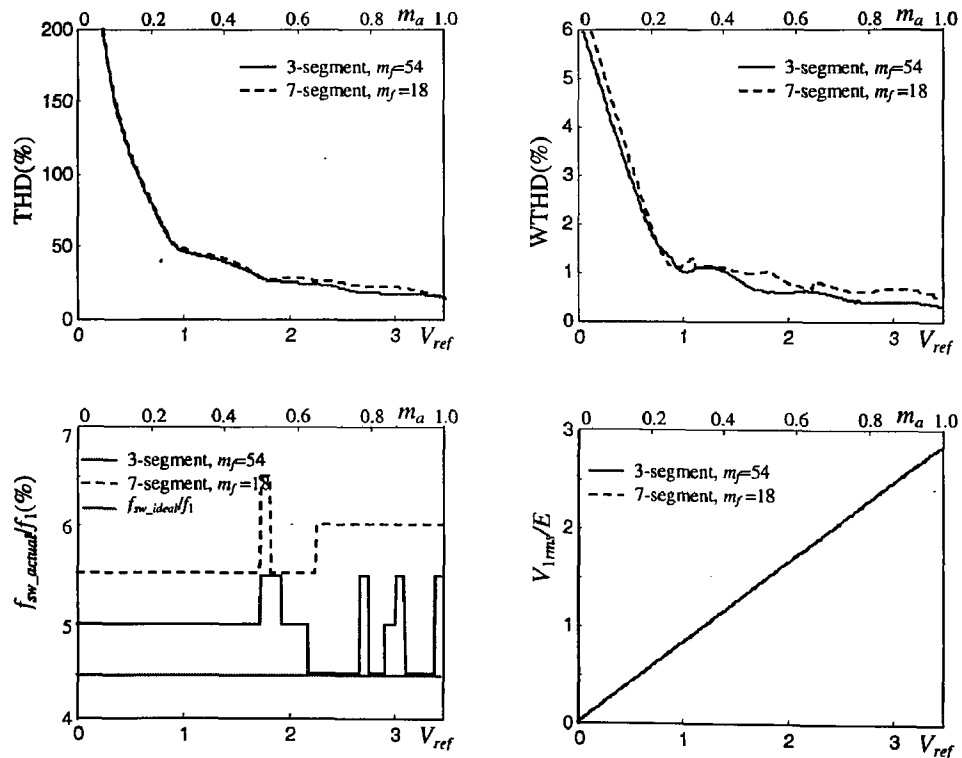
Lay out of the curves:

THD versus V_{ref}	WTHD versus V_{ref}
f_{sw_actual} versus V_{ref}	V_{1rms} versus V_{ref}

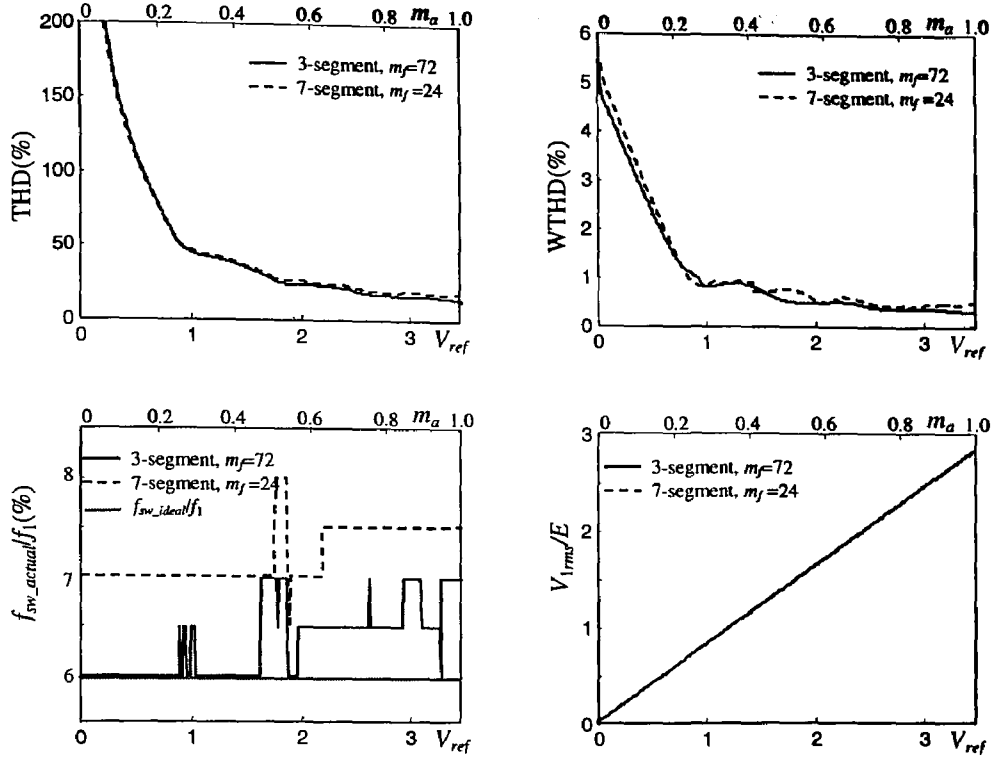
(1) $f_{sw_ideal}=180\text{Hz}$



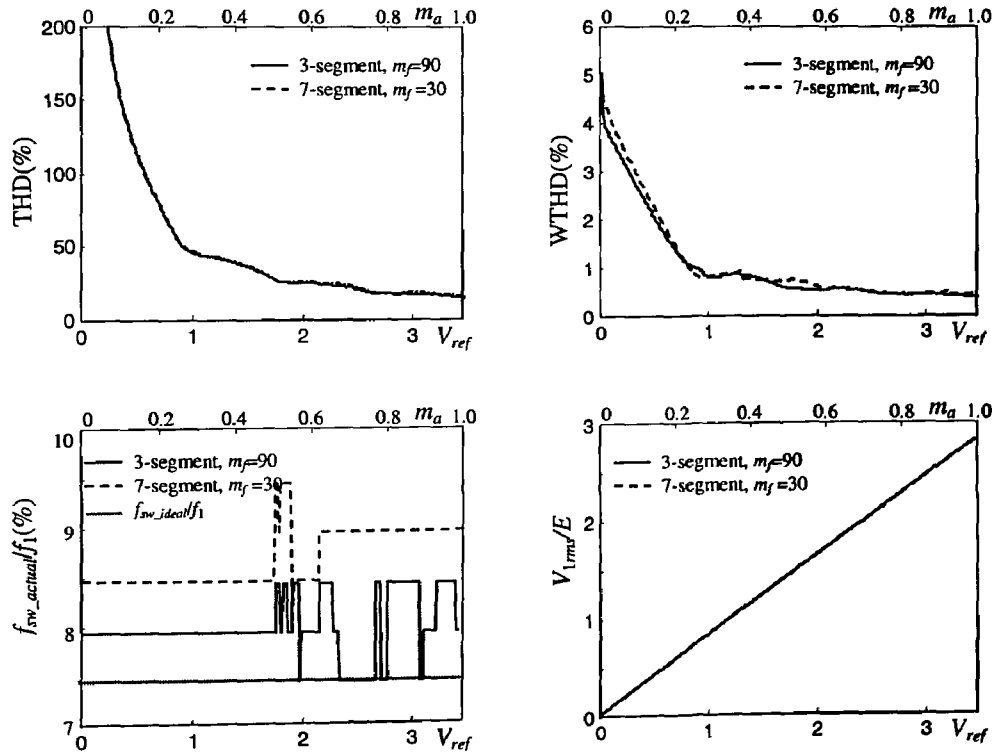
(2) $f_{sw_ideal}=270\text{Hz}$



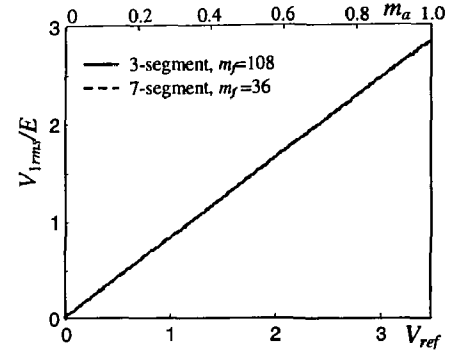
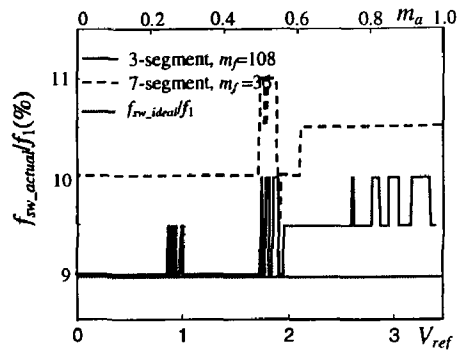
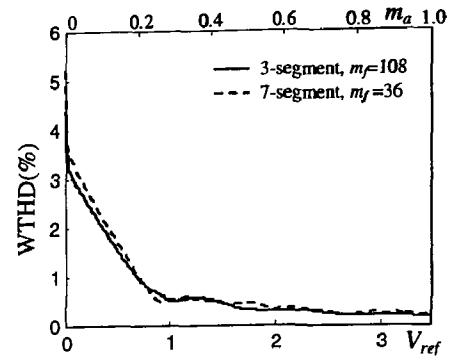
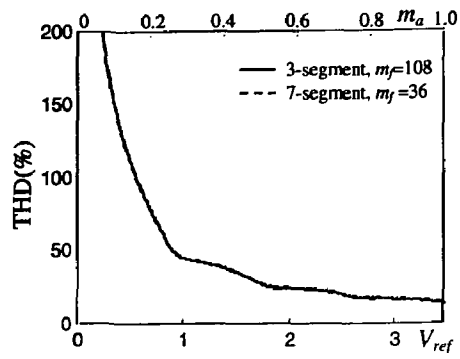
(3) $f_{sw_ideal}=360\text{Hz}$



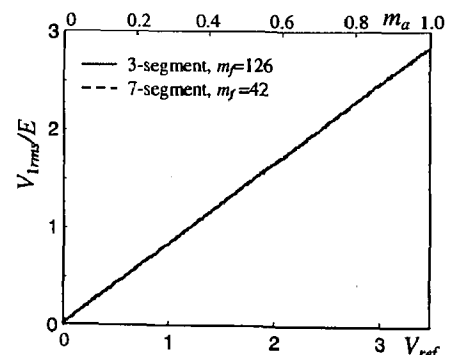
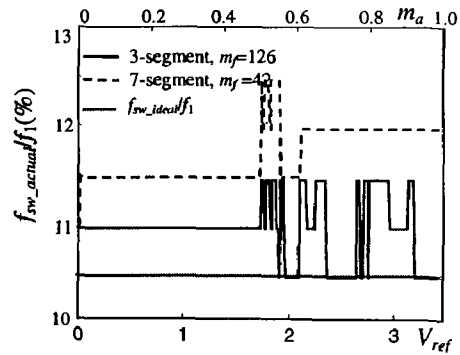
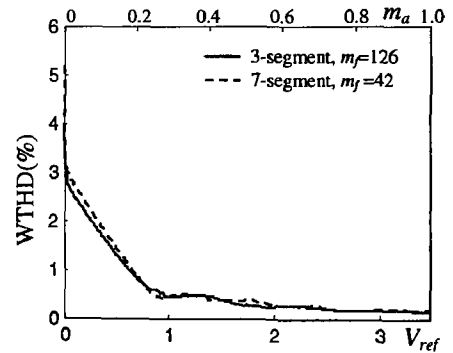
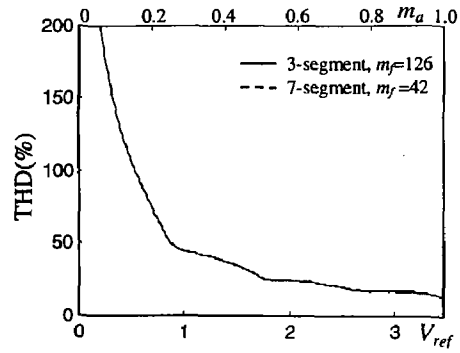
(4) $f_{sw_ideal}=450\text{Hz}$



(5) $f_{sw_ideal}=540\text{Hz}$



(6) $f_{sw_ideal}=630\text{Hz}$

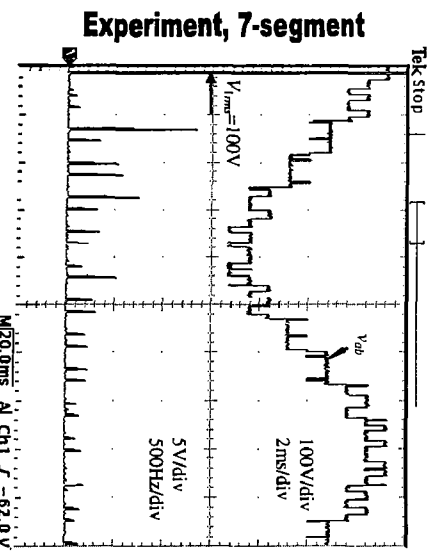
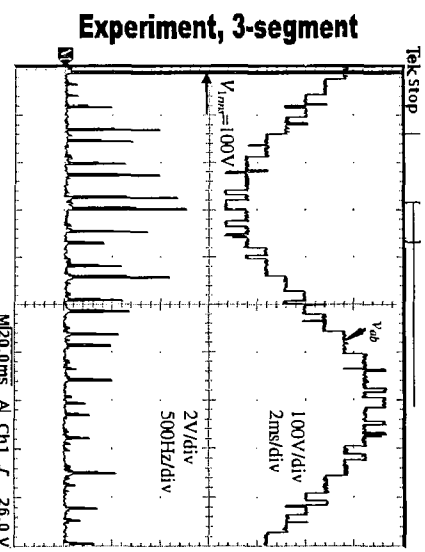
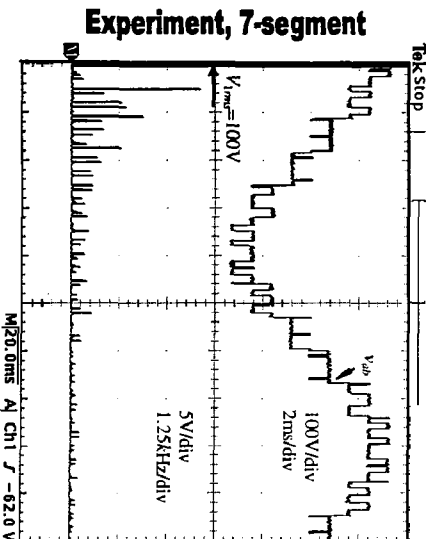
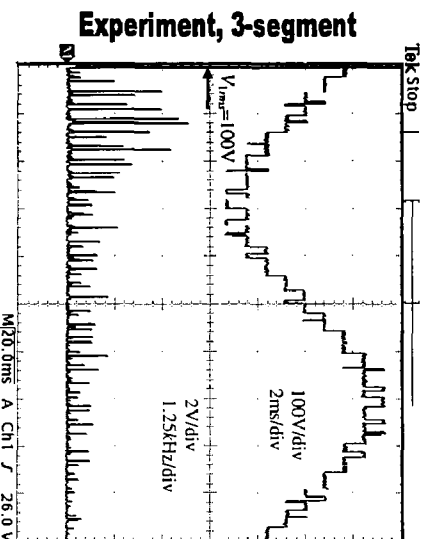
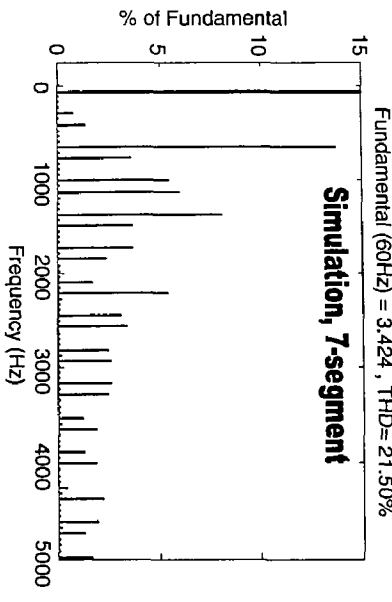
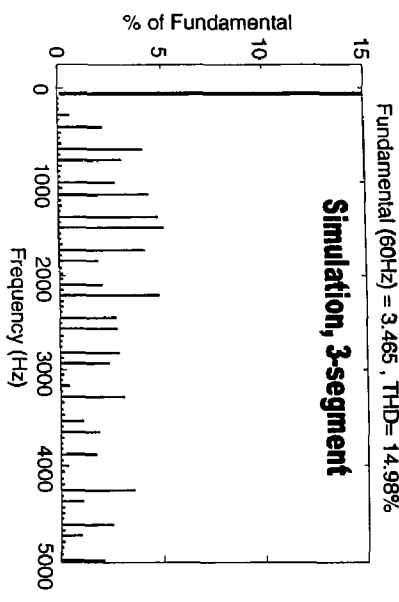
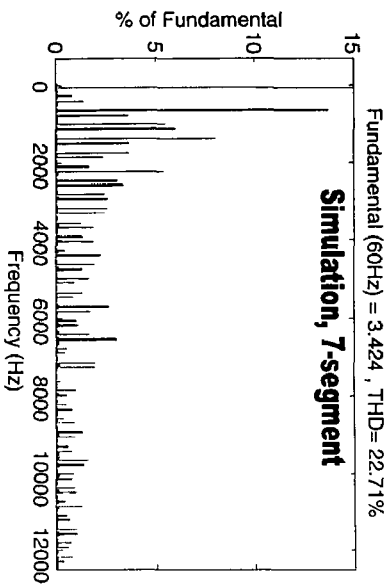
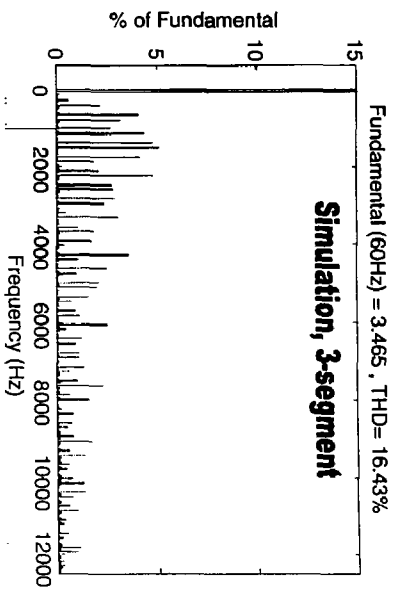


4. Spectra comparison

These waveforms appended here are to compare the spectra of the output line-to-line voltages of the two SVM algorithms. Both simulated and experimental waveforms are included comparatively. Comparisons are done for 11 different ideal average device switching frequencies: $f_{sw_ideal}=180\text{Hz}$, 270Hz , 360Hz , ..., 1080Hz . The modulation index is fixed at $m_a=0.867$ or $V_{ref}=3.0$ and the fundamental frequency $f_1=60\text{Hz}$. Eight spectra are included for each scenario and are arranged according to the following layout diagram:

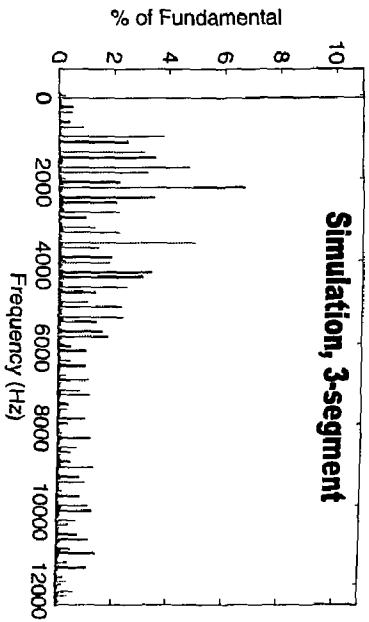
Simulated spectrum (0~12.5kHz) 3-segment SVM	Simulated and zoomed spectrum(0~5kHz) 3-segment SVM
Simulated spectrum(0~12.5kHz) 7-segment SVM	Simulated and zoomed spectrum(0~5kHz) 7-segment SVM
Experimental waveform and spectrum (0~12.5kHz) 3-segment SVM	Experimental waveform and zoomed spectrum (0~5kHz) 3-segment SVM
Experimental waveform and spectrum (0~12.5kHz) 7-segment SVM	Experimental waveform and zoomed spectrum(0~5kHz) 7-segment SVM

(1) $f_{sw_ideal} = 180\text{Hz}$

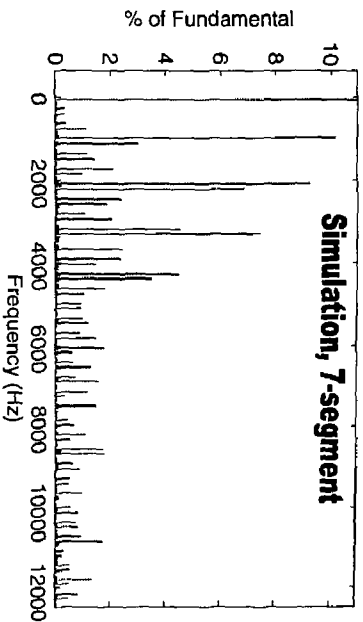


(2) $f_{sw_ideal} = 270\text{Hz}$

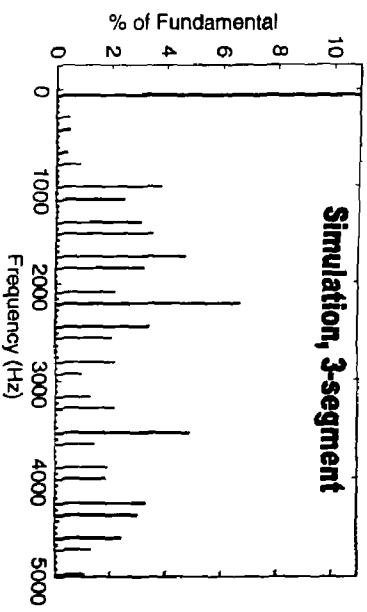
Fundamental (60Hz) = 3.467 , THD= 15.90%



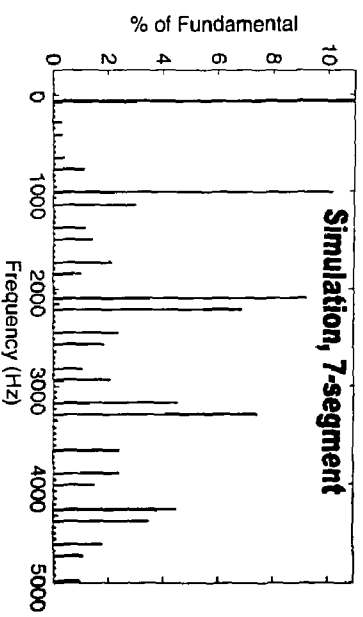
Fundamental (60Hz) = 3.445 , THD= 20.78%



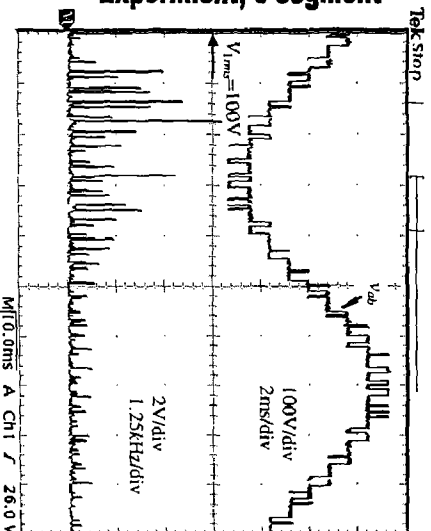
Fundamental (60Hz) = 3.467 , THD= 14.59%



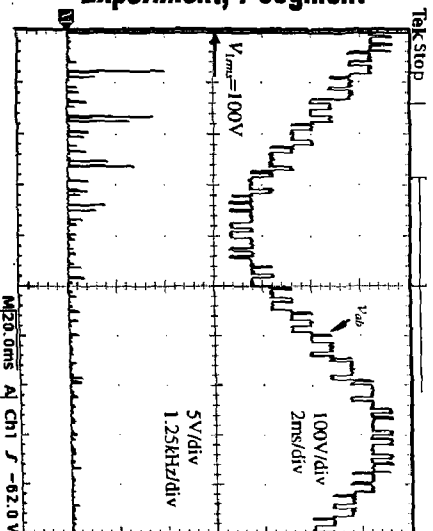
Fundamental (60Hz) = 3.445 , THD= 19.83%



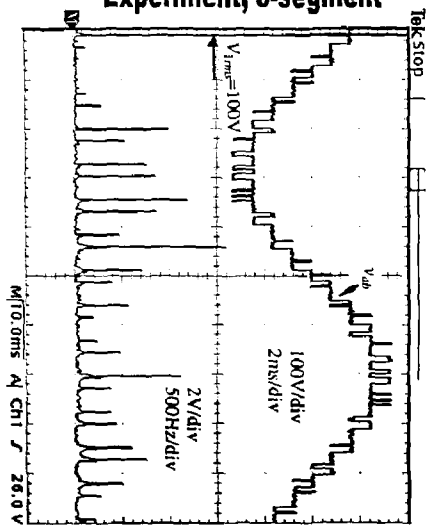
Experiment, 3-segment



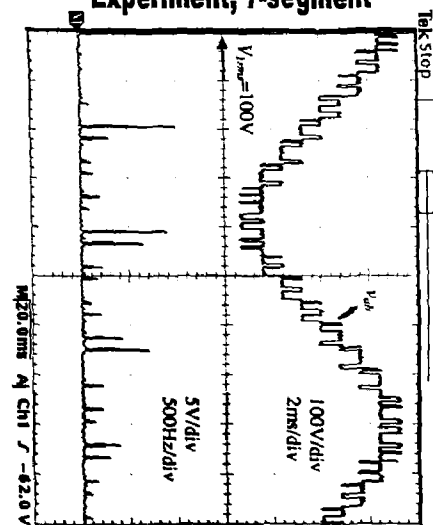
Experiment, 7-segment



Experiment, 3-segment

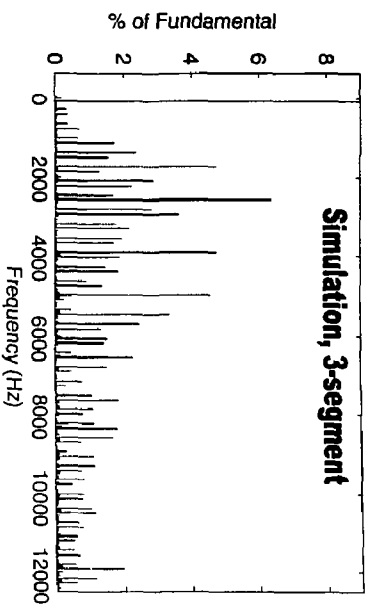


Experiment, 7-segment

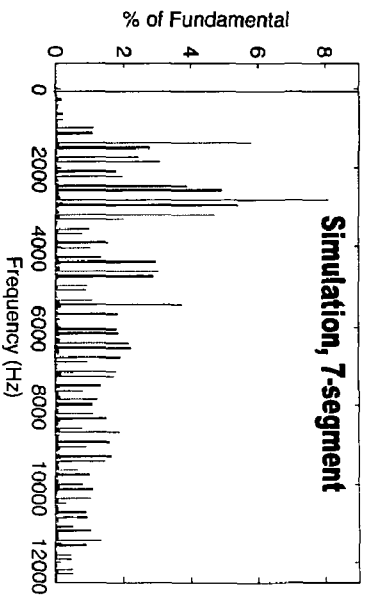


(3) $f_{sw_ideal} = 360\text{Hz}$

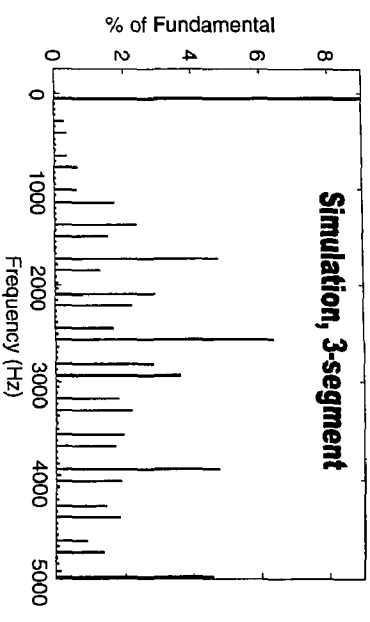
Fundamental (60Hz) = 3.464, THD= 15.63%



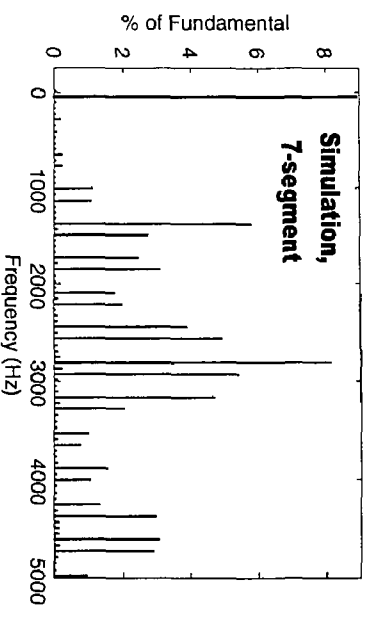
Fundamental (60Hz) = 3.464, THD= 18.36%



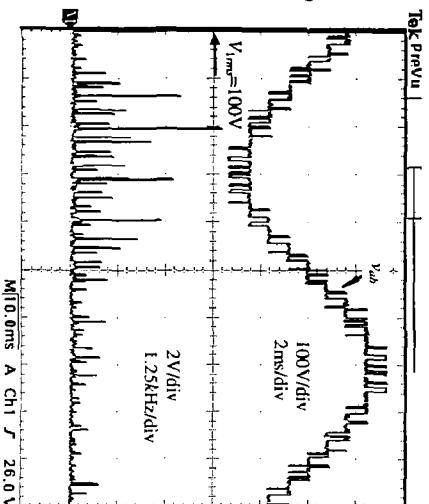
Fundamental (60Hz) = 3.464, THD= 13.53%



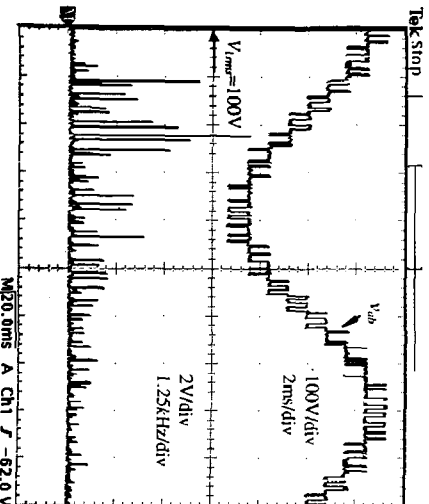
Fundamental (60Hz) = 3.464, THD= 16.11%



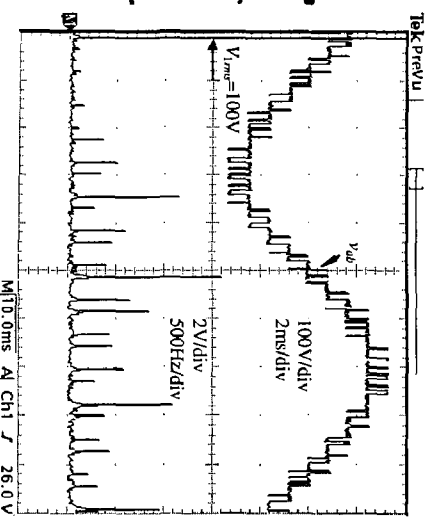
Experiment, 3-segment



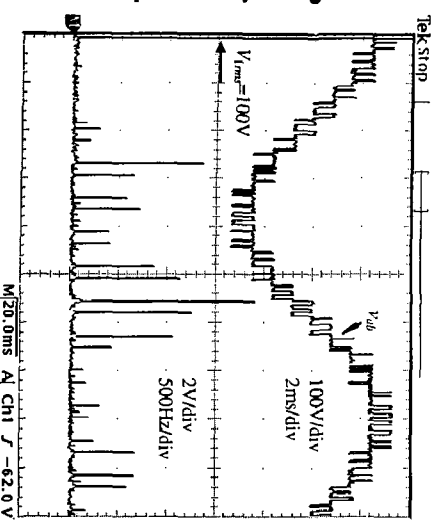
Experiment, 7-segment



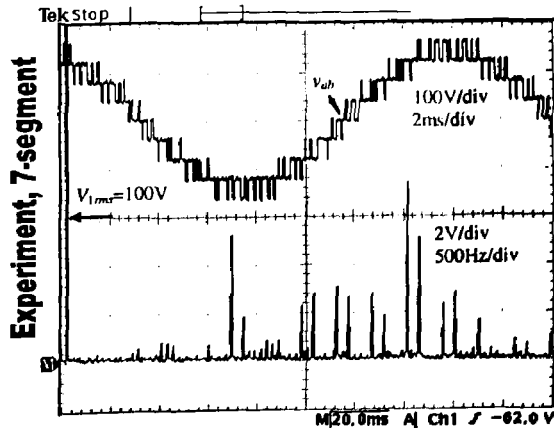
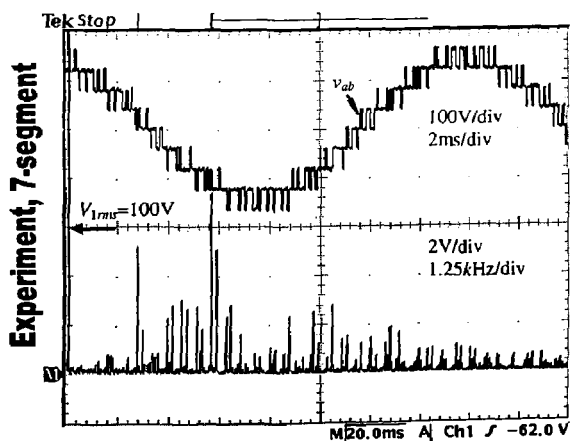
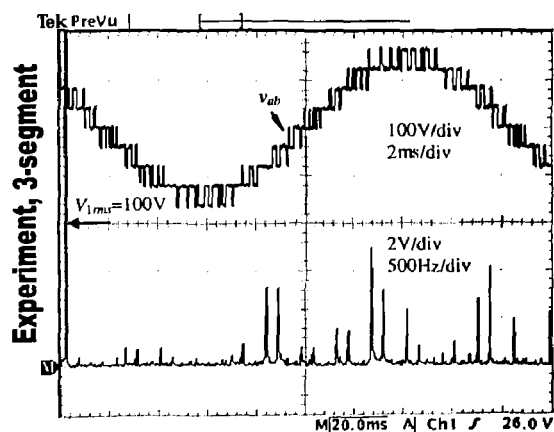
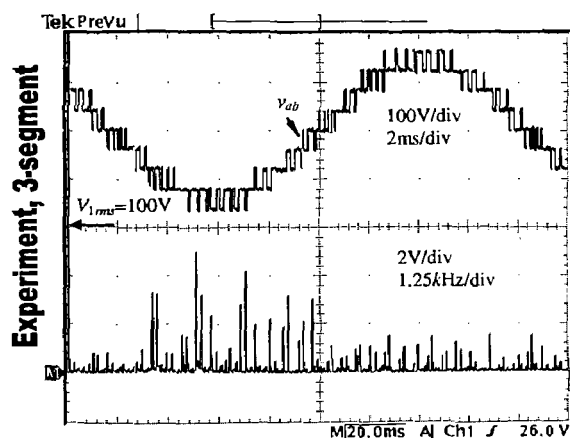
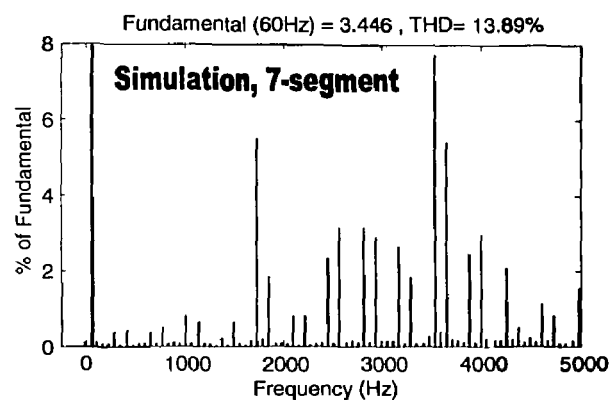
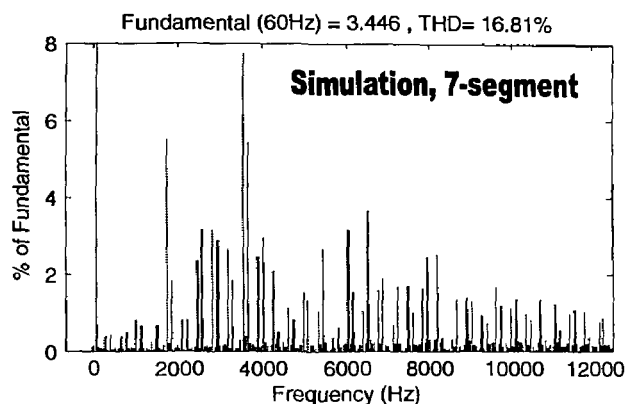
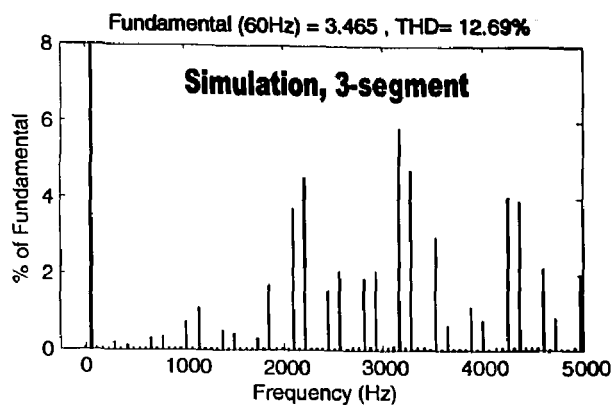
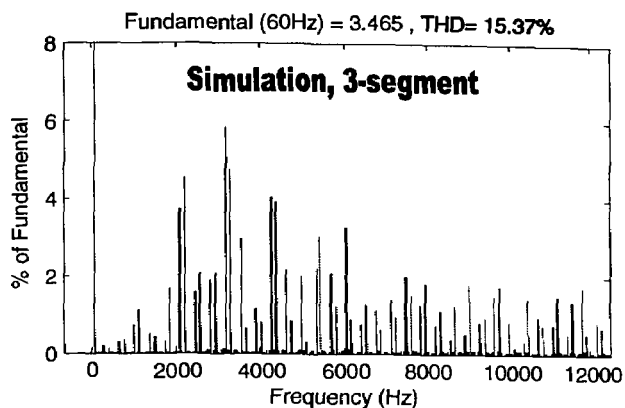
Experiment, 3-segment



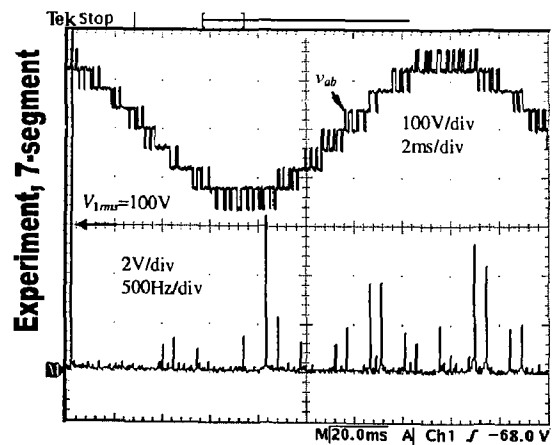
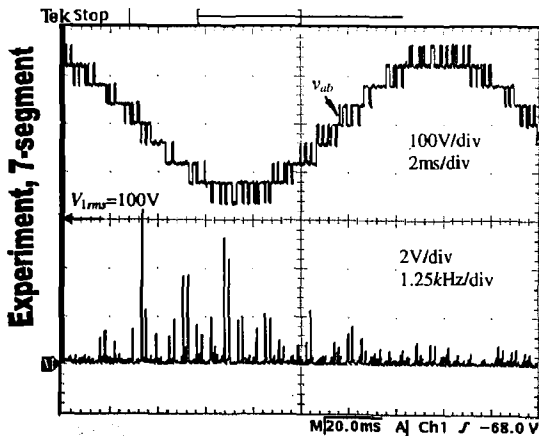
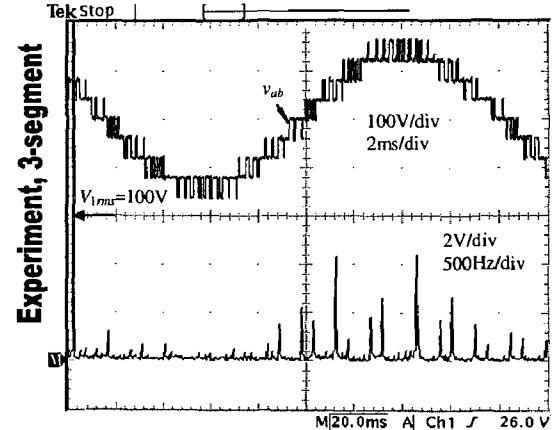
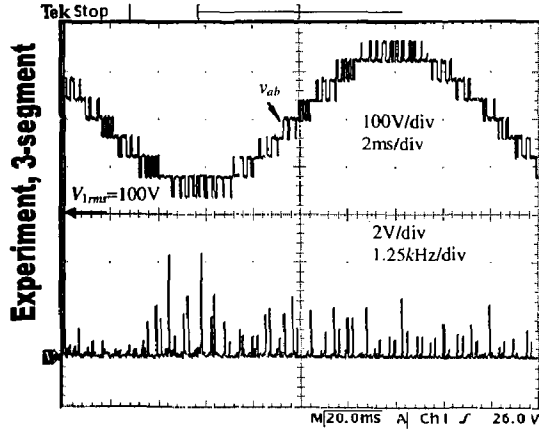
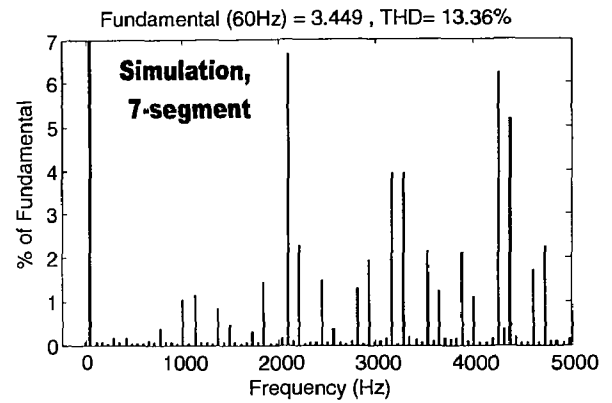
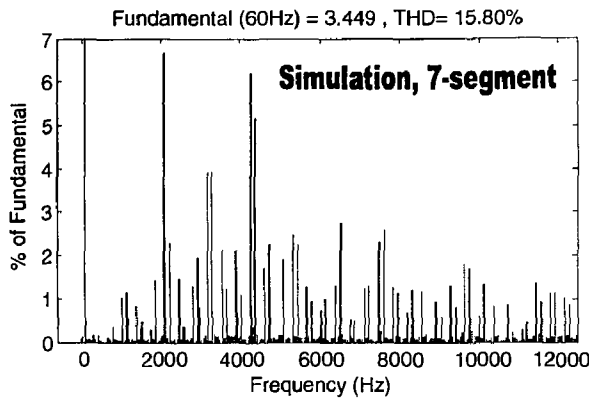
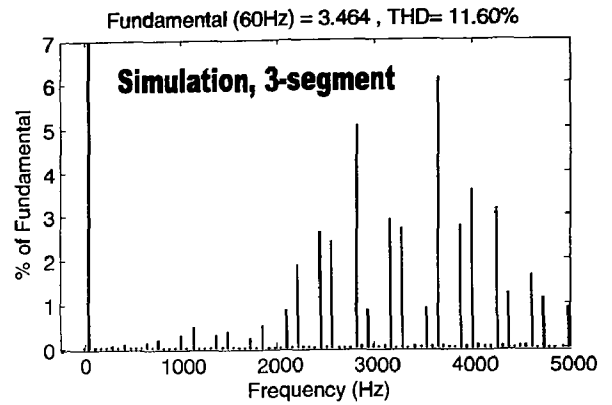
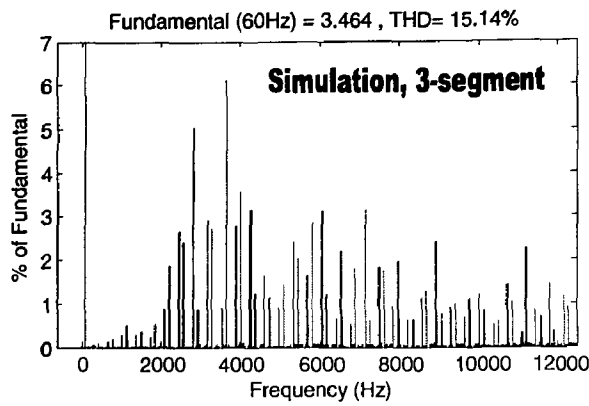
Experiment, 7-segment



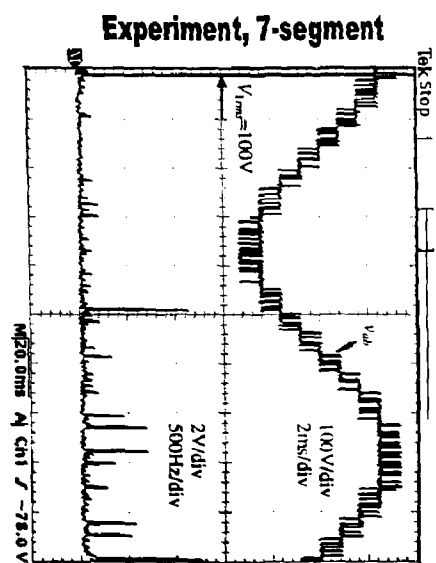
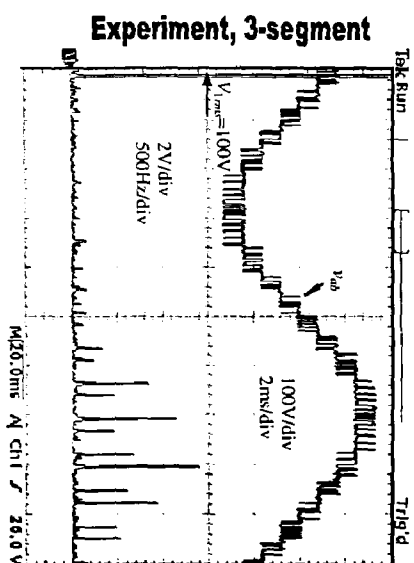
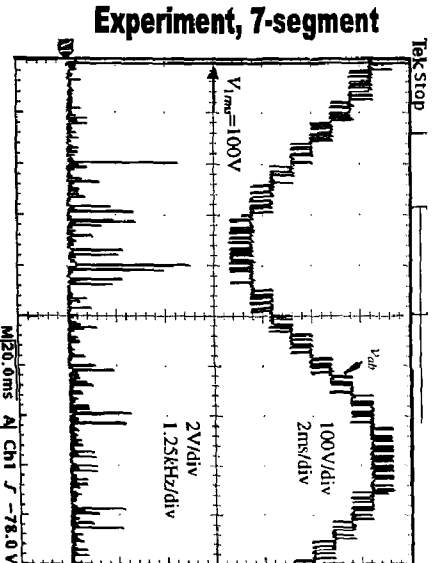
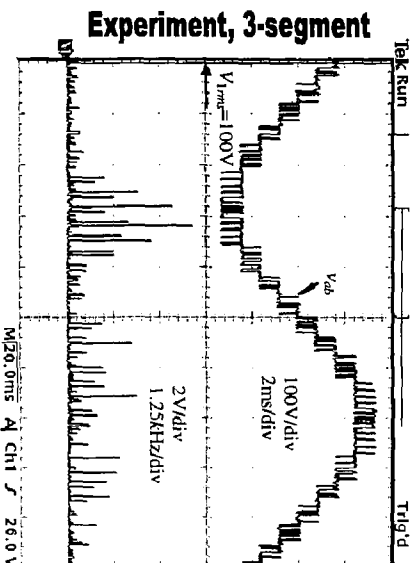
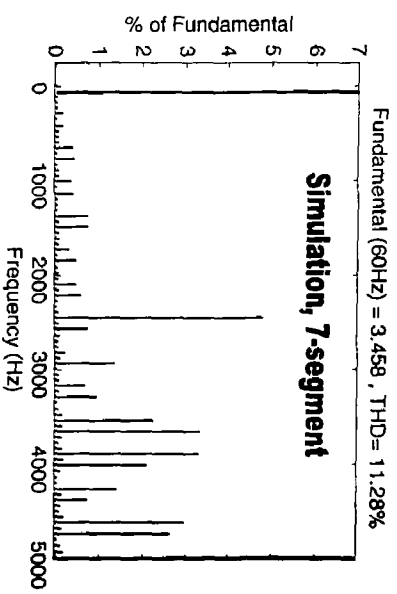
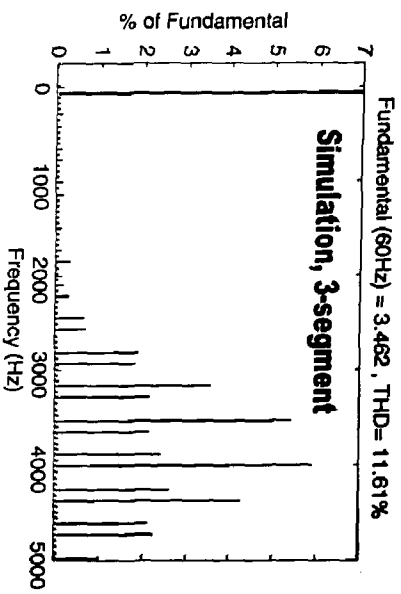
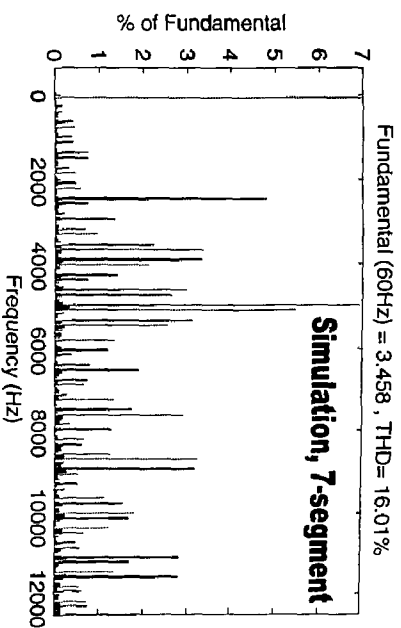
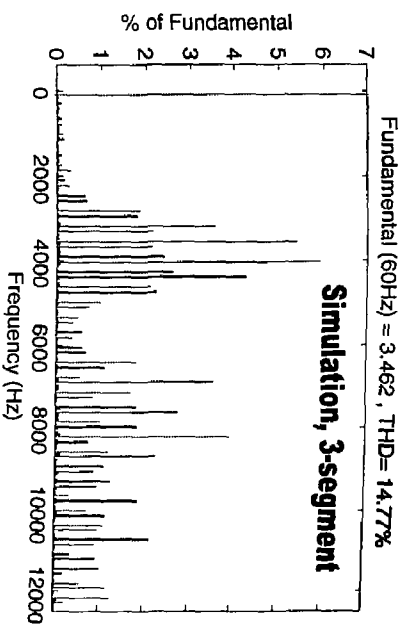
(4) $f_{sw_ideal}=450\text{Hz}$



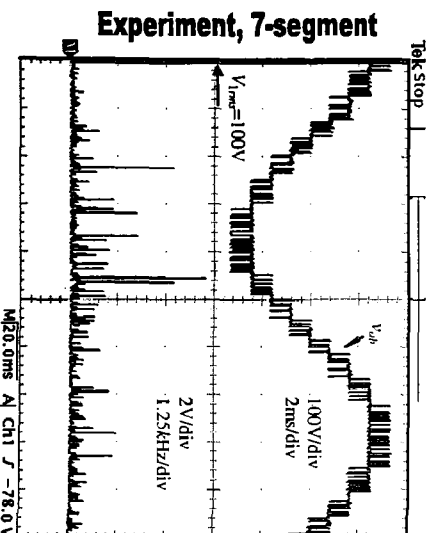
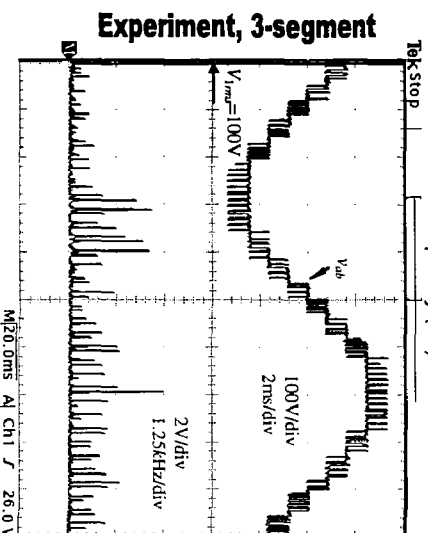
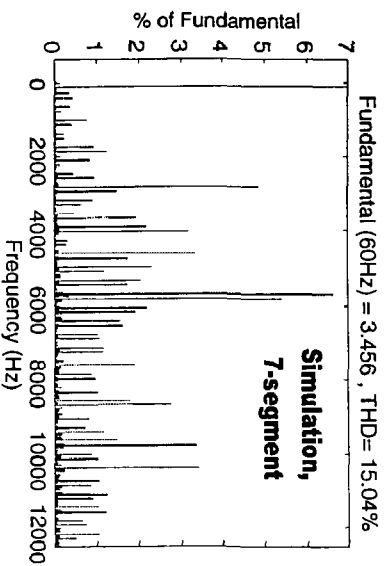
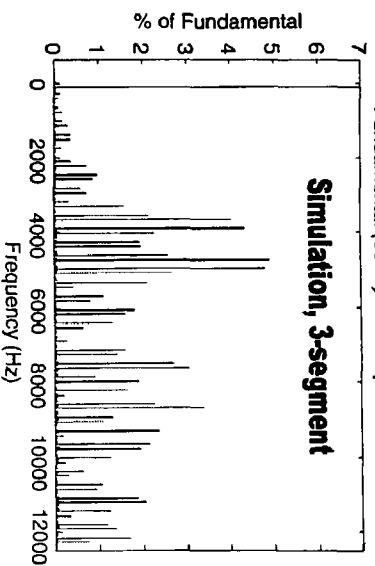
(5) $f_{sw_ideal}=540\text{Hz}$



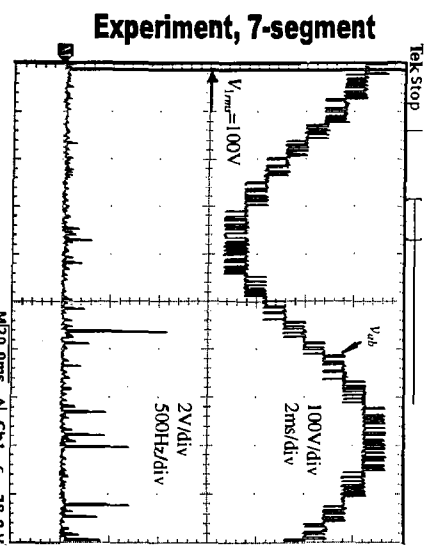
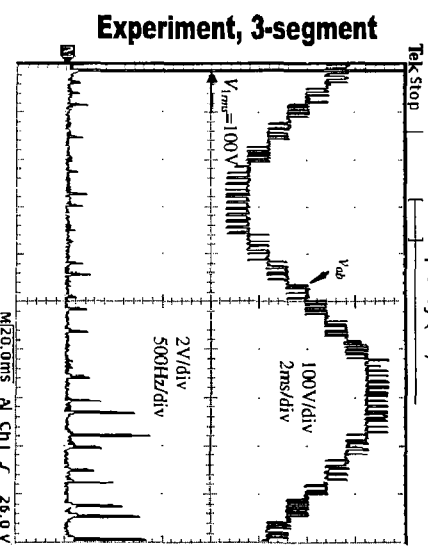
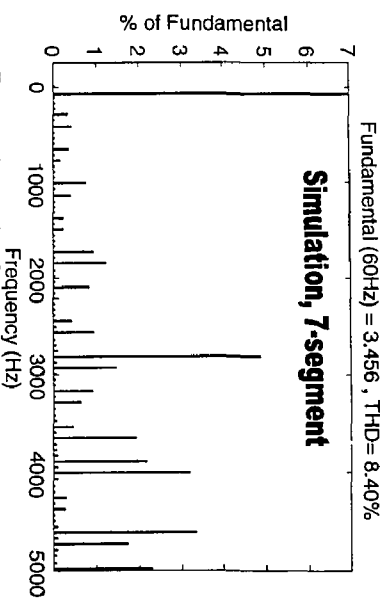
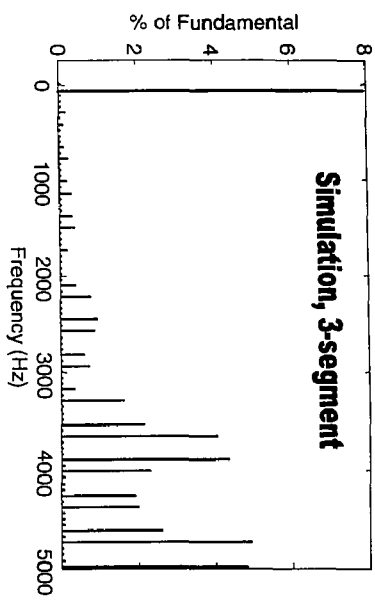
(6) $f_{sw_ideal}=630\text{Hz}$



(7) $f_{sw_ideal} = 720\text{Hz}$
 Fundamental (60Hz) = 3.464, THD = 14.64%

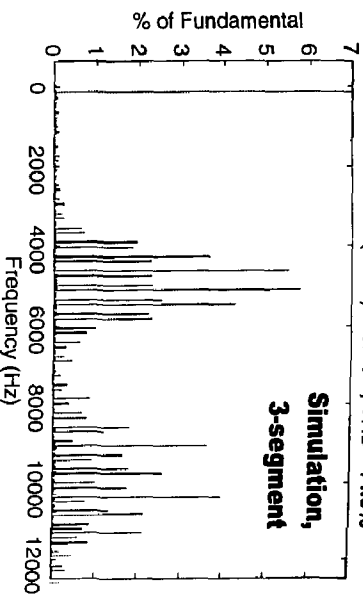


Fundamental (60Hz) = 3.464, THD = 10.58%

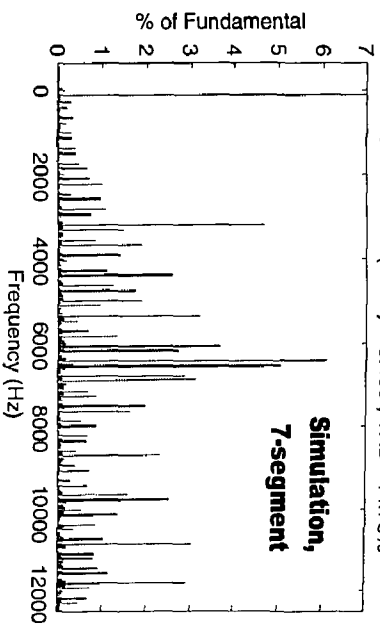


(8) $f_{sw_ideal} = 810\text{Hz}$

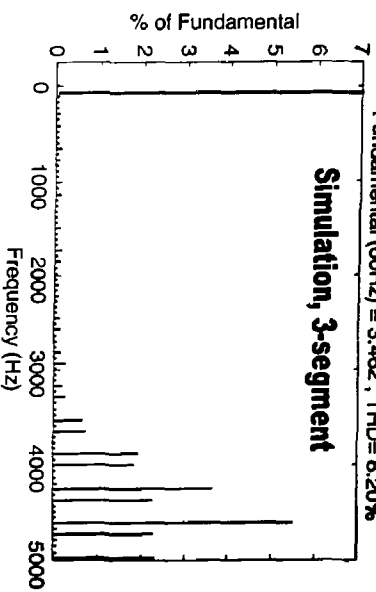
Fundamental (60Hz) = 3.462, THD= 14.3%



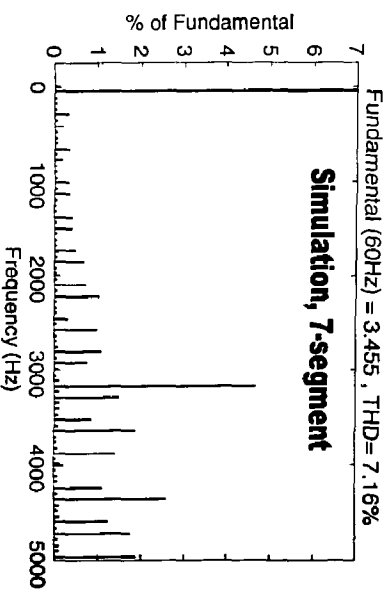
Fundamental (60Hz) = 3.455, THD= 14.76%



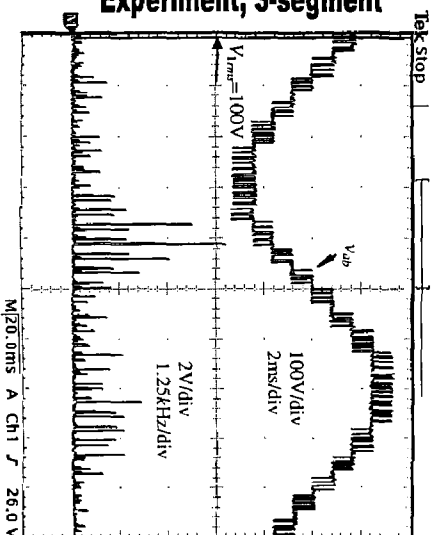
Fundamental (60Hz) = 3.462, THD= 8.20%



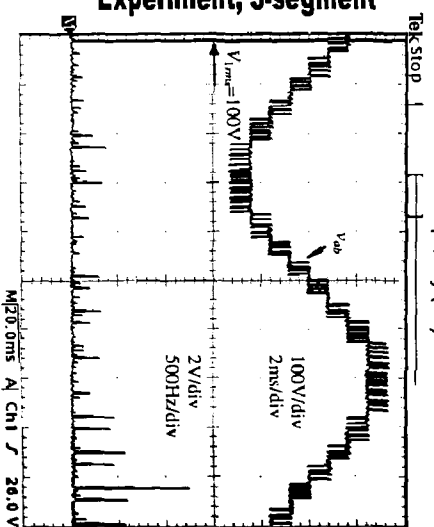
Fundamental (60Hz) = 3.455, THD= 7.16%



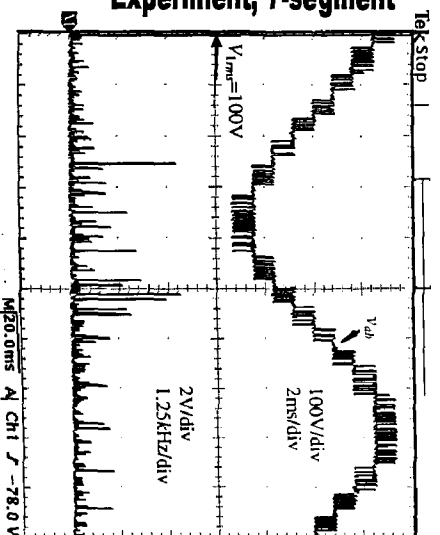
Experiment, 3-segment



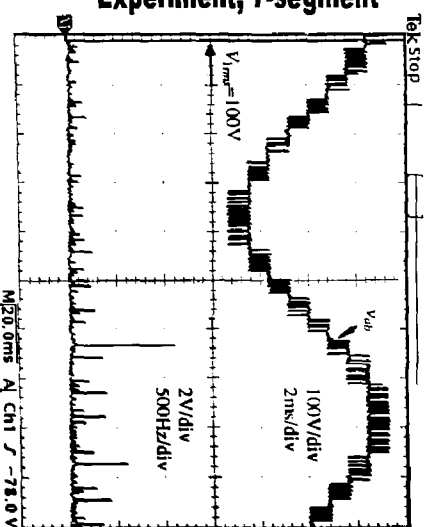
Experiment, 7-segment



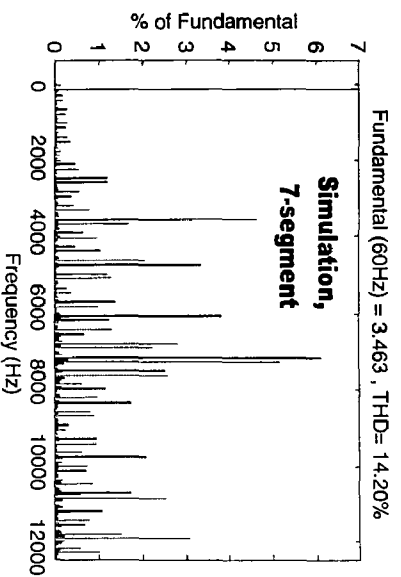
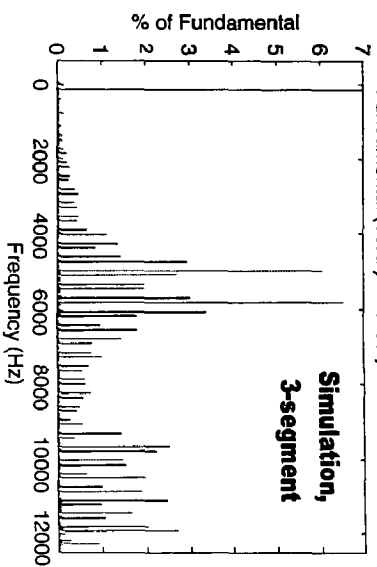
Experiment, 7-segment



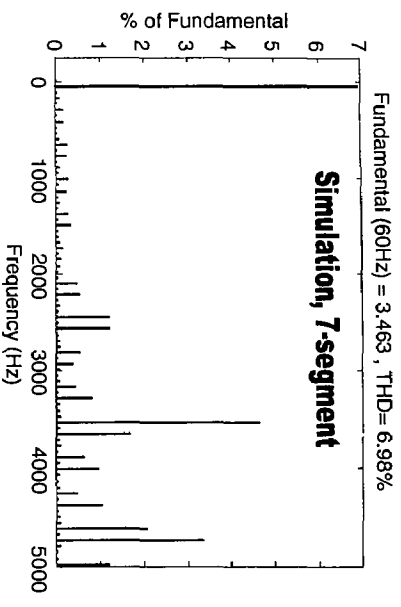
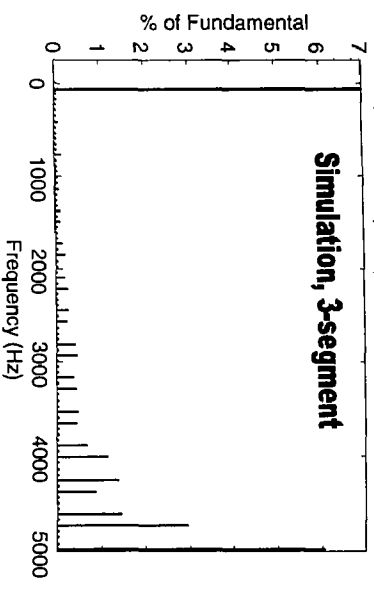
Experiment, 7-segment



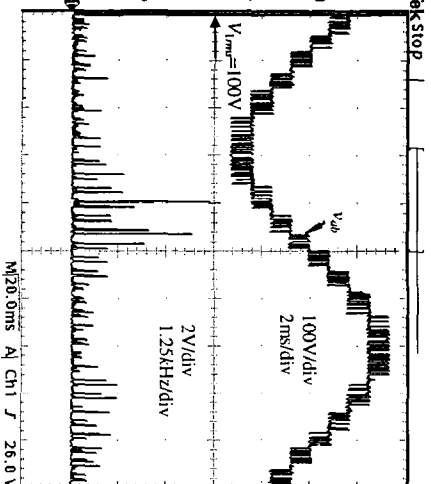
(9) $f_{sw_ideal} = 900\text{Hz}$
Fundamental (60Hz) = 3.465, THD = 14.01%



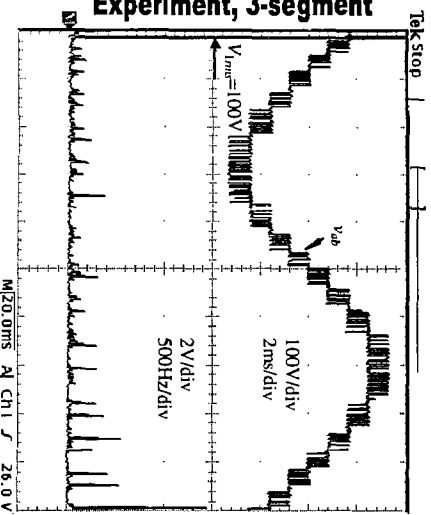
Fundamental (60Hz) = 3.465, THD = 7.27%



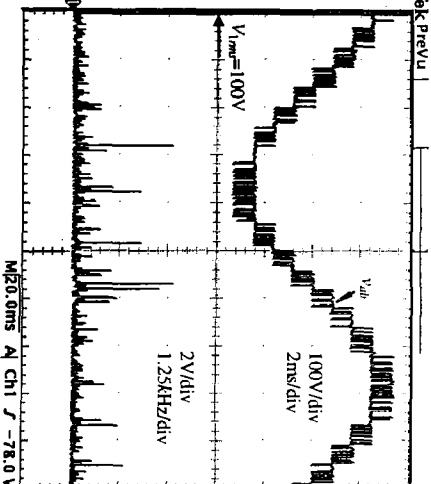
Experiment, 3-segment



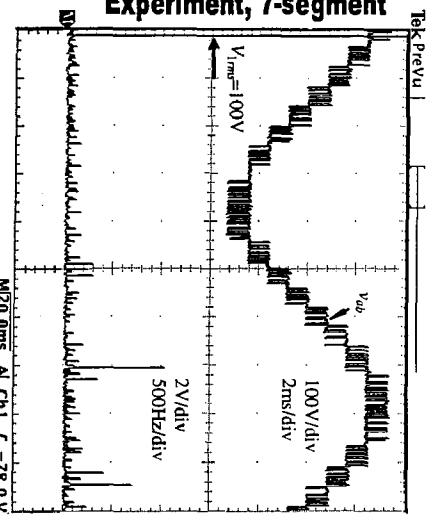
Experiment, 3-segment



Experiment, 7-segment

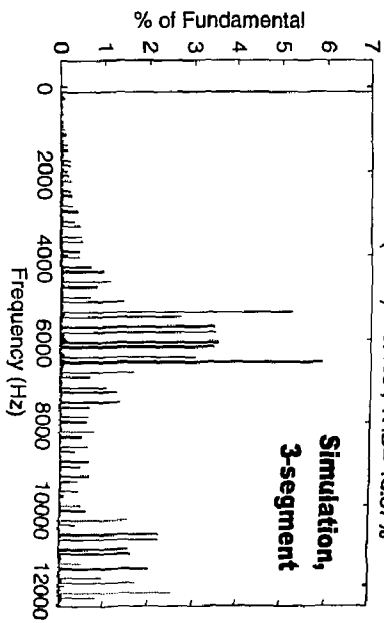


Experiment, 7-segment

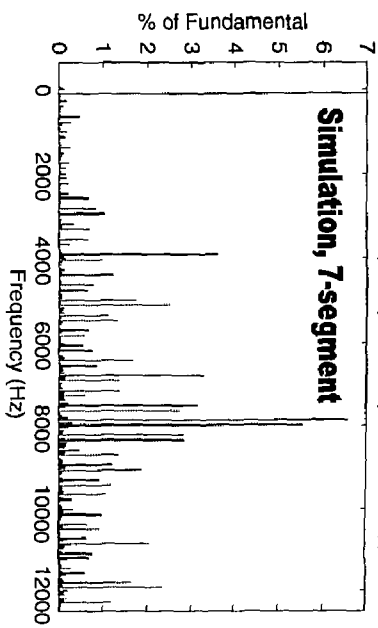


(10) $f_{sw_ideal} = 990\text{Hz}$

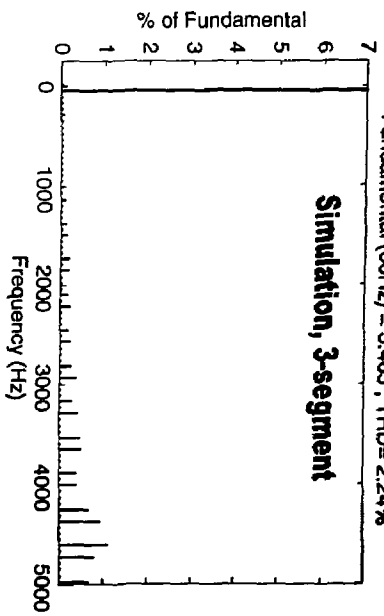
Fundamental (60Hz) = 3.465, THD = 13.37%



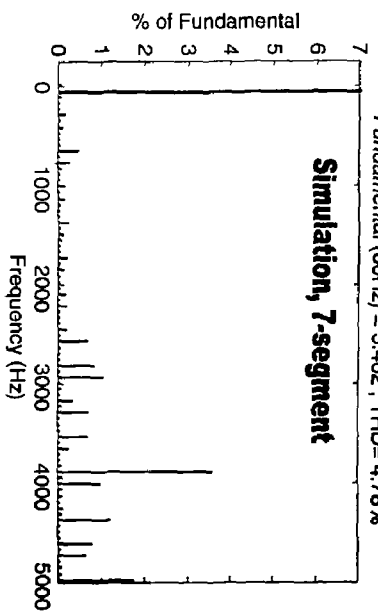
Fundamental (60Hz) = 3.462, THD = 13.71%



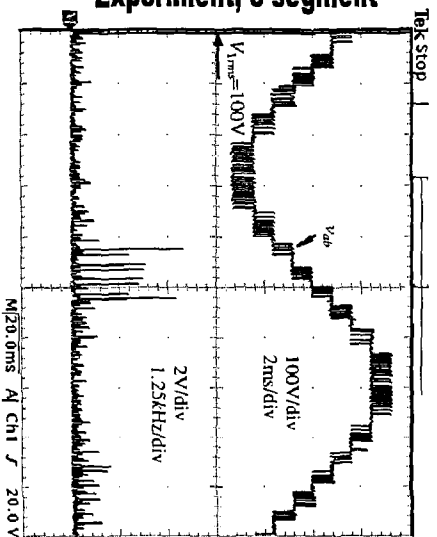
Fundamental (60Hz) = 3.465, THD = 2.24%



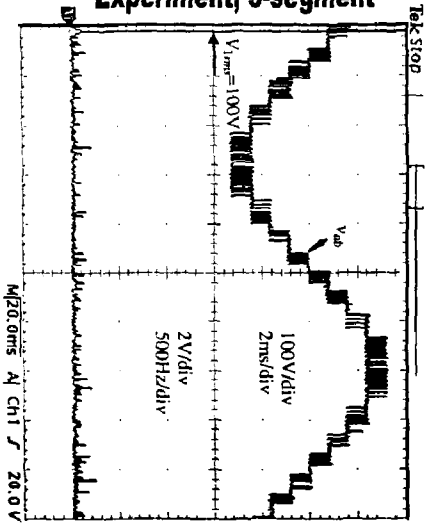
Fundamental (60Hz) = 3.462, THD = 4.78%



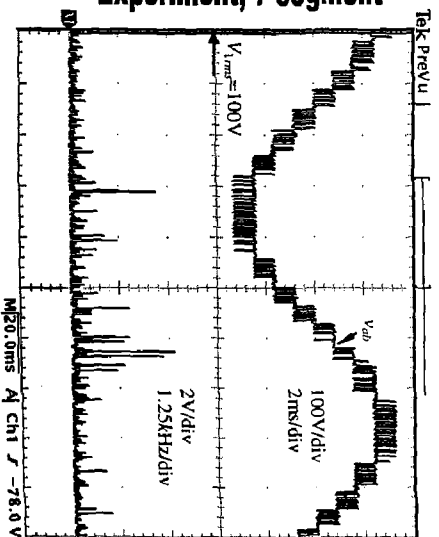
Experiment, 3-segment



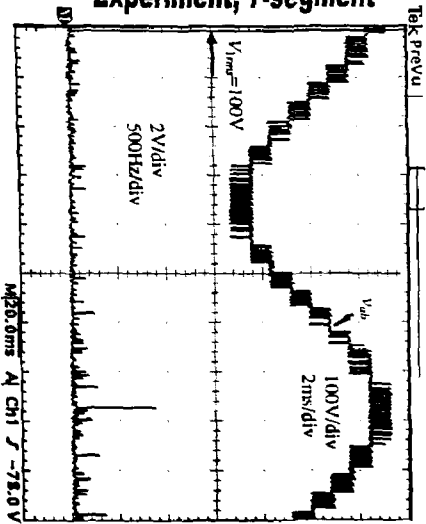
Experiment, 3-segment



Experiment, 7-segment

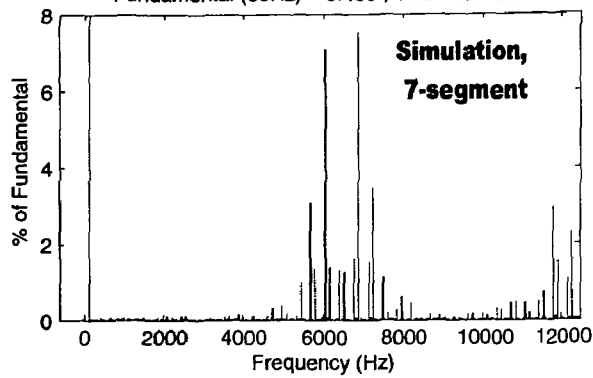


Experiment, 7-segment

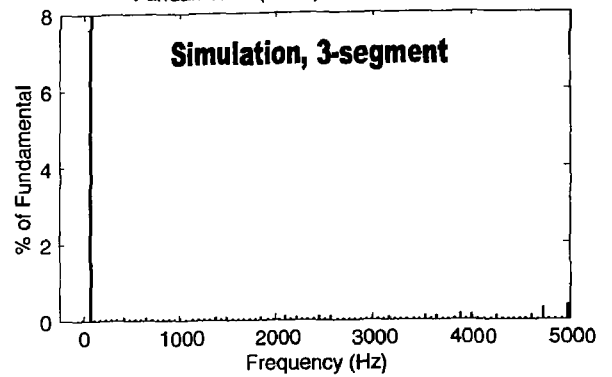


(11) $f_{sw_ideal}=1080\text{Hz}$

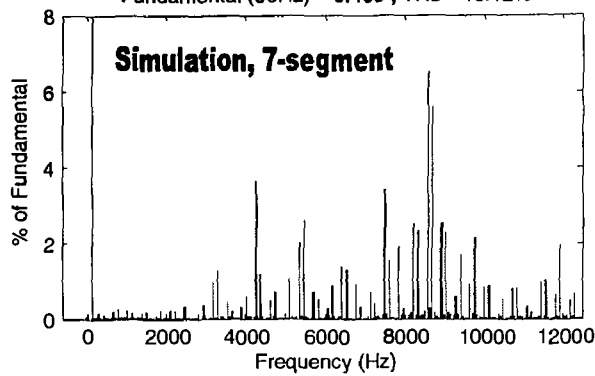
Fundamental (60Hz) = 3.465 , THD= 12.70%



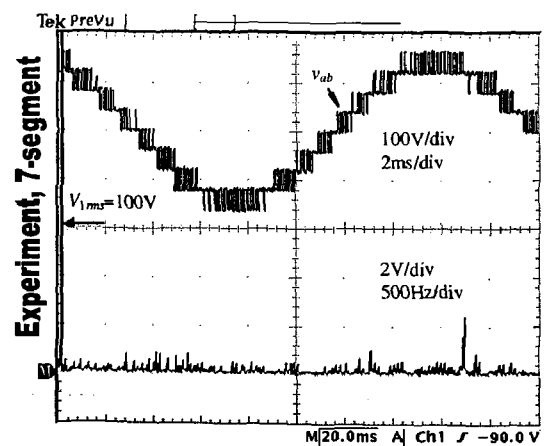
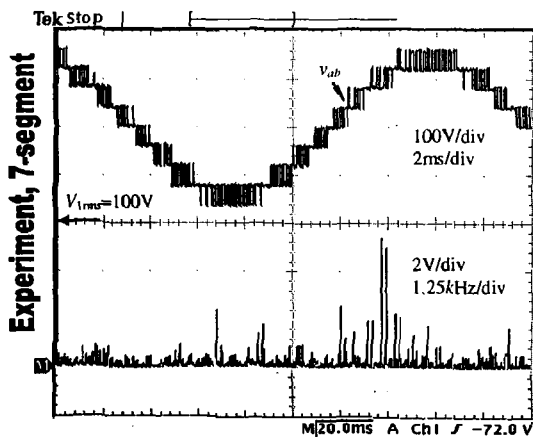
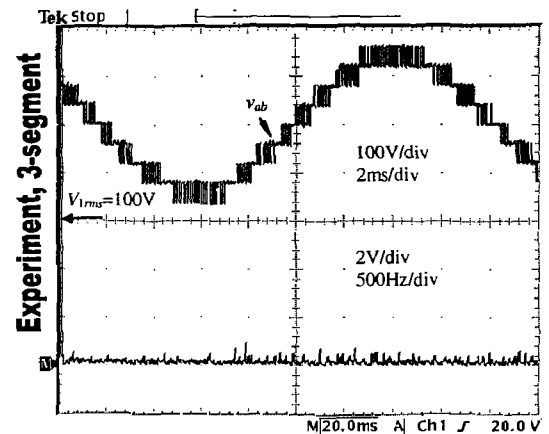
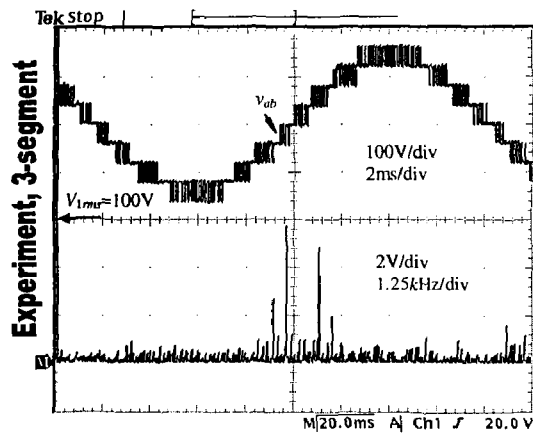
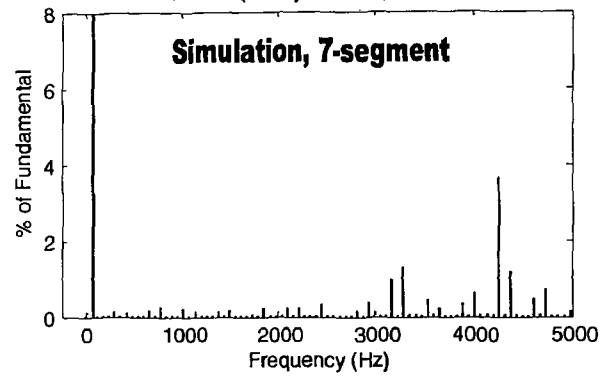
Fundamental (60Hz) = 3.465 , THD= 0.57%



Fundamental (60Hz) = 3.455 , THD= 13.12%



Fundamental (60Hz) = 3.455 , THD= 4.39%



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