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# CMOS Digital Pixel Sensors With In-Pixel Analog-To-Digital Conversion

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# CMOS DIGITAL PIXEL SENSORS WITH IN-PIXEL ANALOG-TO-DIGITAL CONVERSION

by

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A thesis
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**CMOS DIGITAL PIXEL SENSORS WITH IN-PIXEL ANALOG-TO-DIGITAL CONVERSION**, Master of Applied Science, 2008, Yong Chen, Electrical and Computer Engineering, Ryerson University.

# Abstract

This thesiss deals with the designing of CMOS image sensors with in-pixel analog-to-digital conversion. A 2-stage memory write scheme for Pulse-Width-Modulation digital pixel sensors is proposed. It utilizes the characteristics of Gray-code counters and partitions a single data write operation into two separated write operations such that the size of the in-pixel memory can be significantly reduced. A Pulse-Frequency-Modulation image sensor with in-pixel pre-amplification is also presented. By employing an amplifier before the comparator in the pixel, the proposed Pulse-Frequency-Modulation pixel significantly reduces the integration time without sacrificing the dynamic range. Finally, a Pulse-Frequency-Modulation Digital Pixel Sensor with an in-pixel variable reference voltage is proposed. As compared with conventional Pulse-Frequency-Modulation pixels, the proposed architecture improves the dynamic range by adaptively adjusting the reference voltage in the pixel. All proposed digital pixel sensors are designed in TSMC-0.18$\mu$m 6-Metal 1-Poly 1.8 V CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM3V3 device models. The effectiveness of the proposed digital pixel sensors is validated using simulation.

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# Abbreviations

ADC—Analog-to-Digital Conversion/Converters

AER—Address-Event Reorientation

APS—Active Pixel Sensors

BOM—Bill of Material

BSIM3V3—Berkeley Short-channel IGFET Model Version 3.3

CCD—Charge-Coupled Devices

CDS—Correlated Double Sampling

CMOS—Complementary Metal-Oxide Semiconductors

DAC—Digital-to-Analog Conversion/Converters

DNL—Differential Nonlinearity

DPS—Digital Pixel Sensors

DR—Dynamic Range

DRAM—Dynamic Random Access Memory

ENOB—Effective Number of Bits

FD—Floating Diffusion

FPN—Fixed-Pattern Noise

FSR—Full-scale range

HDTV—High-definition television

INL—Integral Nonlinearity

LFSR—Linear-Feedback-Shifting-Register

LSB—Least Significant Bit

MCBS—Multichannel Bit-Serial

MIM—Metal-Insulator-Metal

MSB—Most Significant Bit

MUX—Multiplexer

NUQ—Nonuniform time-domain Quantization

PFM—Pulse-Frequency-Modulation

PG—Photogates

PPD—Pinned Photodiodes

PPS—Passive Pixel Sensors

PWM—Pulse-Width-Modulation

QE—Quantum Efficiency

RAM—Random Access Memory

RMRE—Row Memory Read Enable

RRRE—Row Register Read Enable

SNR—Signal-to-Noise Ratio

SRAM—Static Random Access Memory

TG—Transmission Gates

TSMC—Taiwan Semiconductor Manufacturing Company

XNOR—Exclusive NOR gates

# Chapter 1

# Introduction

## 1.1 Background

Image sensors are devices that transform optical images to electric signals. Today image sensors can be found in various electronic products, such as mobile phones, digital still cameras, and camcorders. New application opportunities are also merged in automobile, security/surveillance, and medical systems.

There are two major categories of image sensors: Charge-coupled devices (CCDs) and CMOS image sensors. Both sensors utilize the same mechanism, called the photoelectric effect that transforms light into electric charge within a photodetector. A higher level of intensity of light implies a larger amount of charge generated in the device. The main difference between CCD and CMOS sensors is the way they process the generated charge.

CCD sensors work like analog shift registers that transport the charge through sequential CCD cells controlled by a clock signal, as shown in Fig.1.1. In the last stage, charge is converted to a voltage signal by a charge amplifier for further processing. Because of this charge transfer mechanism, CCDs do not introduce temporal noise or pixel to pixel variations due to device mismatches, known as fixed-pattern noise (FPN) [12]. Today CCD sensors are still widely used in systems that require high quality images, e.g. HDTV. However CCDs have several disadvantages:

(1) **Process incompatibility**: CCDs are fabricated in specialized technologies solely optimized for imaging and charge transfer, which means that all required control functions

have to be implemented into another chip such that the bill of material (BOM) cost of the systems is increased consequently.

(2) **Low speed**: Because of the serial charge readout, the speed of CCD sensors is low, which is unfavor for high-speed applications.

(3) **High power consumption**: CCDs requires high-speed, high-voltage clocks to improve the charge transfer efficiency, which increases power consumption.

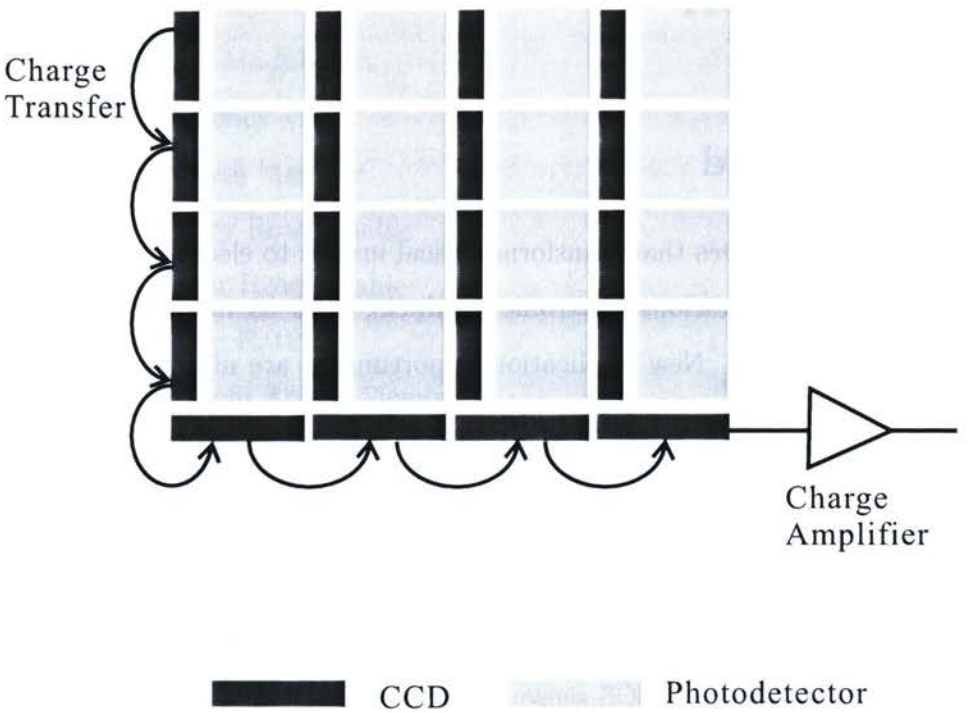



Figure 1.1: Architecture of interline transfer CCDs [12].

Modern CMOS image sensors were not popular until the mid 1980's when CMOS active pixel sensors (APSs) were introduced by VLSI Vision Ltd. and NASA's Jet Propulsion Laboratory [9]. Before the appearance of APSs, the firs generation of CMOS image sensors is passive pixel sensors (PPSs). However PPS devices have poor performance as compared with CCDs, which limited their applications. APSs overcome the shortcomings of PPSs by adding an amplification stage in every pixel, which significantly improves the signal-to-noise ratio (SNR). Meanwhile because APSs are built with CMOS technologies, most of control and

signal processing functions including analog-to-digital conversion (ADC) can be integrated into the same chip, resulting in a significant cost reduction. Fig.1.2 is the architecture of conventional CMOS image sensors with a global A/D converter.

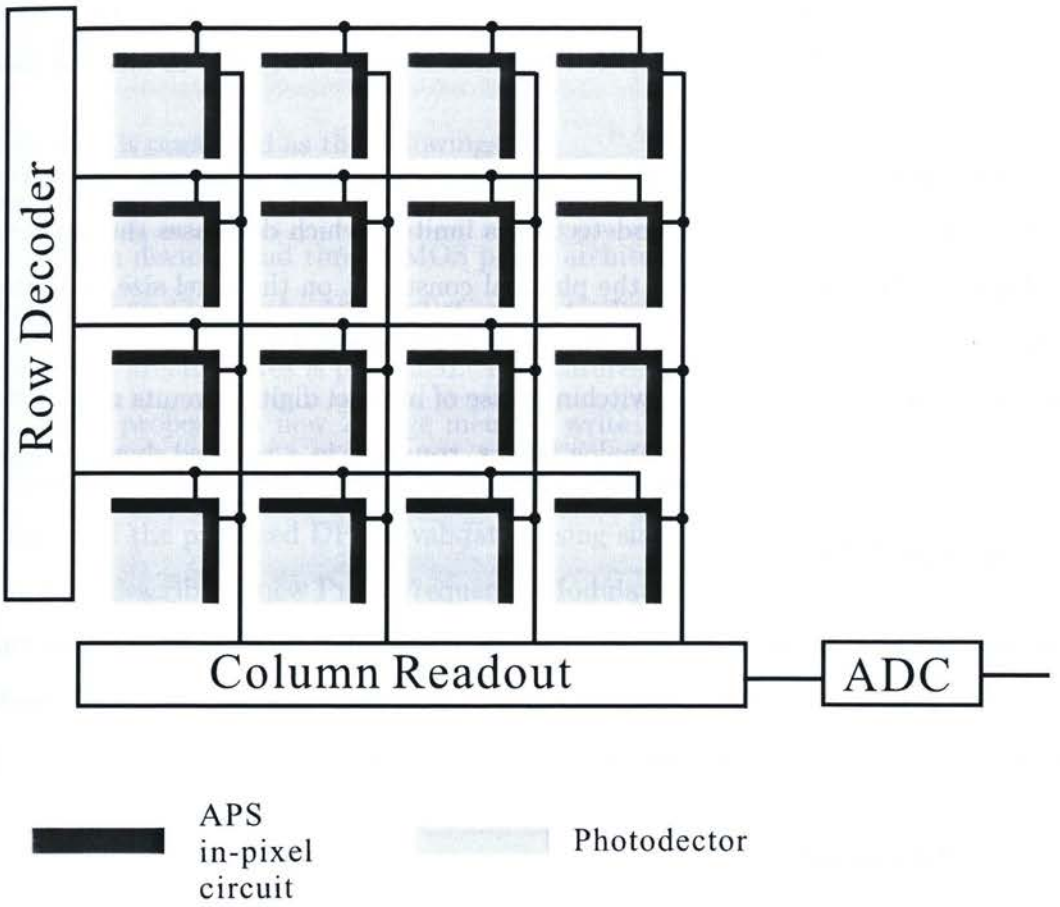



Figure 1.2: Architecture of CMOS APS sensors with a global ADC.

With the scale of CMOS image sensors increases, the conventional configuration of Fig.1.2 shows its limitations. First, the conversion speed of the ADC must be sufficiently high in order to meet timing requirements, which increases design challenges. Secondly, the analog output of the APS pixels is more vulnerable to noise and crosstalk, because heavy parasitics exist on the column lines [11]. In recent years, the idea of migrating A/D conversion into column level has become popular. In [29], a CMOS image sensor with 8.3 mega pixels was reported. In this design, the column-parallel gain amplifier and ADC are employed.

As CMOS technologies advance, the possibility of integrating an ADC into each pixel is becoming feasible. The first pixel with an in-pixel ADC, called digital pixel sensors (DPSs), was first reported in [10]. The massively parallel conversion provides the potential for high frame rate imaging applications, while digital data is read out in a manner similar to a random access memory (RAM) , which offers noise immunity. However DPSs face the following challenges:

(1) **Large pixel size/low fill-factor**: Since a large portion of the pixel is reserved for ADC and memory, the area for photodetectors is limited, which decreases the performance.

(2) **Low resolution**: Because of the physical constraint on the pixel size, a limited size of memory can be realized in the pixel, resulting in low resolution.

(3) **Low dynamic range**: The switching noise of in-pixel digital circuits may contribute significant noise to their vulnerable analog blocks, resulting in a reduced dynamic range.

## 1.2 Motivation

The proceeding discussion above leads to the motivation of this thesis: exploring the possibility to improve the performance of digital pixel sensors by increasing the fill-factor, enhancing the resolution, and improving the dynamic range.

## 1.3 Contributions

This thesis proposes three new CMOS image sensors with in-pixel analog-to-digital conversion:

(1) Pulse-Width-Modulation (PWM) digital pixel sensors with 2-stage memory write scheme. The DPS provides the highest resolution with the minimum pixel size.

(2) Pulse-Frequency-Modulation (PFM) digital pixel sensors with in-pixel amplification. The DPS improves the dynamic range by 20 dB as compared with other PFM pixels.

(3) PFM digital pixel sensors with in-pixel variable reference voltage. The DPS improves the dynamic range by 70 dB compared with conventional PFM pixels.

These DPSs have been implemented in TSMC-0.18$\mu$m 1.8 V CMOS technology and analyzed using Cadence Spectre with BSIM3v3 device models, and their performance has been validated using simulation.

## 1.4 Thesis Organization

The thesis is organized as the followings:

Chapter 2 reviews the background of CMOS image sensors including photoelectric effect, photodetection devices, and three CMOS pixels architectures.

Chapter 3 provides the background of analog-to-digital conversion. The literature review of digital pixel architectures is presented. The features of different DPSs are also discussed.

Chapter 4 proposes a new 2-stage memory write scheme for Pulse-Width-Modulation digital pixel sensors. The proposed scheme and implementation are presented in detail. The effectiveness of the proposed DPS is validated using simulation.

Chapter 5 describes a new Pulse-Frequency-Modulation (PFM) CMOS image sensor with in-pixel pre-amplification stage. The performance of the proposal PFM DPS is compared with that of the conventional PFM DPS.

Chapter 6 details new PFM DPS with an in-pixel variable reference voltage generator to increase the dynamic range of the pixel. The implementation and simulation results are demonstrated.

Chapter 7 concludes the thesis and provides the direction for future research.

# Chapter 2

# CMOS Pixel Sensors

The imaging quality of CMOS image sensors is largely dominated by the performance of photodetection devices. This chapter reviews the background of CMOS image sensors. Section 2.1 presents photoelectric effect in semiconductor. Section 2.2 discusses three popular photodetection devices including photodiodes, photogates and pinned photodiodes. The performance of these photodetectors are also investigated here. Section 2.3 describes three different generations of CMOS pixel architectures. In Section 2.4, the performance parameters of CMOS image senors are presented. The chapter is summarized in Section 2.5.

## 2.1 Fundamentals of Photoelectric Effect

*Photon absorption* is a fundamental process that is exploited to convert optical energy into electrical energy. Energy of a photon can be expressed as

$$E_{ph} = hc_0/\lambda_0, \tag{2.1}$$

where $h$ is Plank's constant, $c_0$ is the speed of light in vacuum, and $\lambda_0$ is the wavelength. When a photon with energy greater than the semiconductor band-gap ($E_g$) is incident on the semiconductor, an electron-hole (e-h) pair is generated by absorbing the photon energy and exciting the electron from valence band to conduction band as shown in Fig.2.1. The photon absorption is represented by the wavelength dependant absorption coefficient $\alpha(\lambda)$ [8].

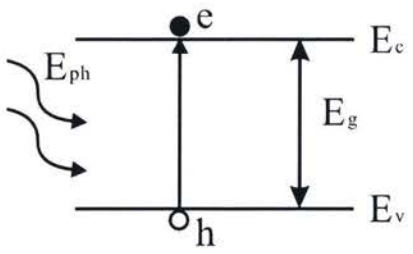



Figure 2.1: Photoelectric effect: an electron-hole generation by absorption a photon with energy $E_{ph} > E_g$.

For an indirect band-gap material, such as silicon, the minimum energy gap between the valence band and the conduction band exists at different crystal momentums. The electron-hole pairs are generated with the change in bands as well as the change in momentum.

There is another opposite mechanism called as *recombination*, which brings the semiconductor back to thermal equilibrium condition, by combining electrons and holes, and releasing energy [28]. In order to prevent the recombination when illumination, the generated e-h pairs must be separated and collected by some collection contacts.

For silicon, a reverse biased p/n junction diode is used for the e-h pairs generation and collection. With the built-in electrical field in the p/n junction, as shown in Fig.2.2, the e-h pairs are separated after generation, and collected by the cathode and the anode of the diode respectively. By increasing the reverse bias voltage, the depletion region of the p/n junction is increased, so is the electrical field, which makes the drifting of holes and electrons more easily. These currents are the drift component of the total photo current.

The e-h pairs generated in the diffusion regions ($L_n$, $L_p$) are diffusing to the depletion, which forms the diffusion current of the photo current. For e-h pairs generated outside these two regions, most of them will be recombined and do not contribute to the photo current.

Once the photo current is generated, there are two ways to measure the current. One is directly measuring the current, called as current-mode photodetectors. The other way is to integrate the current over a capacitor for a predetermined time period and read the changed potential after then. This type of image sensors is known as voltage-mode sensors.

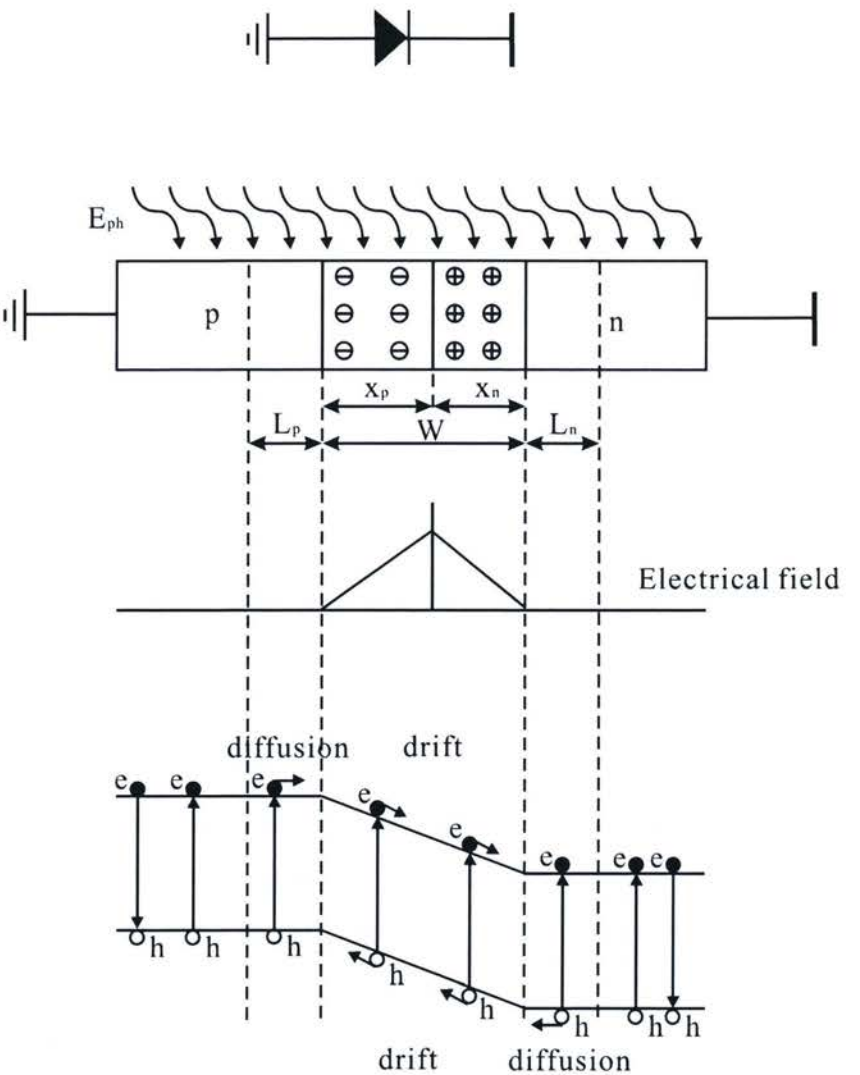
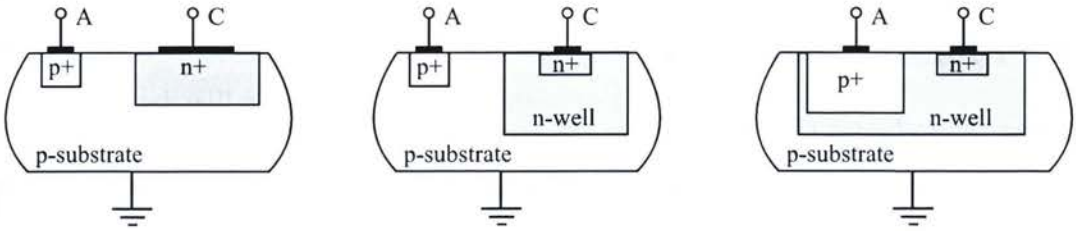



Figure 2.2: A reverse biased p/n junction diode under illumination.

## 2.2 Photodetectors

### 2.2.1 Photodiodes

Reverse biased p/n junction photodiodes are the most popular photodectors for CMOS image senors. Fig.2.3 shows three possible photodiode structures that can be implemented using p-substrate process: n+/p-substrate photodiode, n-well/p-substrate photodiode, and p+/n-well photodiode. Among them, the n+/p-substrate is widely used because of the outstanding spectral response and the simple layout. However this photodiode is vulnerable to crosstalk and noise due to the leak current through the substrate [4].




(a) n+/p-subtrate photodiode (b) n-well/p-subtrate photodiode (c) p+/n-well photodiode

Figure 2.3: Types of photodiodes.

### 2.2.2 Photogates

The structure of photogates is presented in Fig.2.4. Similar to CCDs, the photogate has four operation stages: reset, signal integration, signal charge transfer, and signal readout [21, 22].

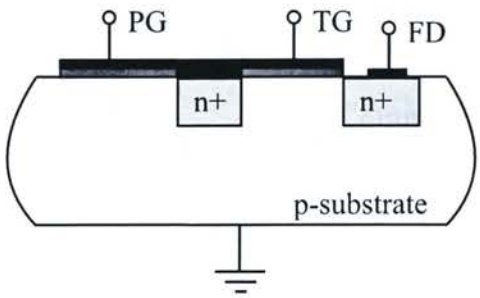



Figure 2.4: Structure of photogates.

Before integration, the photogate is reset by activating the transmission gate (TG). During integration, the generated charge is accumulated in the potential well under the photogate (PG). For readout, the floating diffusion (FD) is first reset and read out, then the charge is completely transferred via the TG to the FD. The difference of two voltages is proportional to the photon flux.

Because the sensing node and integration node are separated, the photogate enables true correlated double sampling (CDS), which can suppress $1/f$ noise and FPN. The dark current contributed by the surface defect is also reduced. The spectral response of the photogate is decreased due to the low transparency of the polysilicon gate.

### 2.2.3 Pinned Photodiodes

Pinned photodiodes (PPDs) improve the sensitivity and reduce the dark current by integrating p+/n/p-substrate diode instead. The architecture of pinned photodiodes is shown in Fig.2.5. As compared with photogates, the advantage of PPDs is the separation of the charge collection region away from the silicon surface into the bulk through the top p+ layer, resulting in a great reduction of dark current [19, 13]. Currently pinned photodiodes can be found in multi-megapixel image sensors [24].

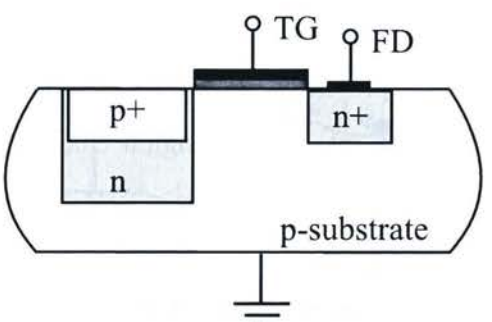



Figure 2.5: Architecture of pinned photodiodes.

### 2.2.4 Performance Parameters of Photodetectors

There are two important parameters to measure the performance of photodetectors.

**Quantum Efficiency (QE)**: QE defines the incident photon flux that contributes to the photo current in a photodetector with a specific wavelength. This parameter is strongly related to the photodetector layout geometry and manufacturing process such as doping concentrations.

**Dark Current**: Dark current is the current in the photodetector without any illumination. It affects the noise floor of pixels and determines image sensors performance under low illumination. The dark current depends on several factors: device temperature, number of silicon defects near the electric field, and electrical-field strength. The leakage current of CMOS transistors will also make a contribution to the dark current.

## 2.3 Architectures of CMOS Pixel Sensors

### 2.3.1 Passive Pixel Sensors (PPSs)

PPSs, shown in Fig.2.6, have only one transistor as a switch to transfer the charge to a column-based charge integration amplifier. PPSs can achieve a high fill factor, however, with high readout noise and a slow operation speed. This is because the large parasitic capacitance on the column line appears on the photodiode once the switch is on.

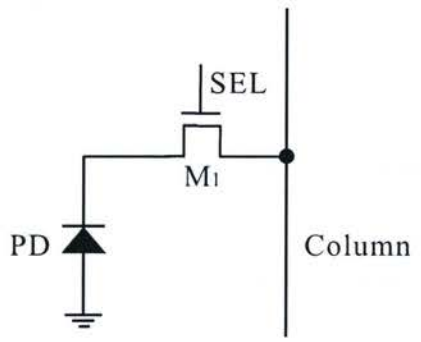



Figure 2.6: Schematic of passive pixel sensors.

### 2.3.2 Active Pixel Sensors (APSs)

APSs are the most popular pixel architectures for CMOS image sensors. Presented in Fig.2.7, APS pixels include a reset transistor ($M_1$), a source follower ($M_2$), and a row select transistor ($M_3$). The role of the source follower is to decouple the photodiode from all other pixels that are connected to the same column line.

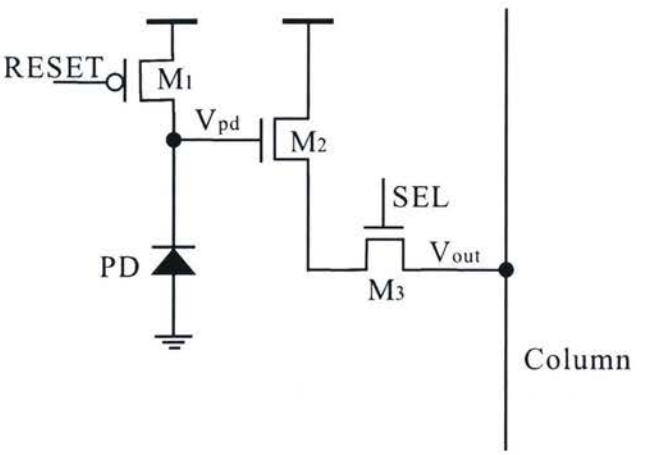



Figure 2.7: Schematic of active pixel sensors.

In Fig.2.8, the operation of the APSs is illustrated: Initially, the photodiode is charged to $V_{dd}$ by enabling the reset transistor $M_1$. This is called as the reset phase. By disabling $M_1$, the pixel enters the integration phase. The voltage at the cathode of the photodiode is dropping because of the illumination. After a predefined time period ($T_1$), the voltage is read out by enabling the transistor $M_3$ as the first value for CDS. At $T_2$, the reset transistor $M_1$ is switched on to recharge the photodiode again. The resetting voltage of the photodiode is also read out at $T_3$ as the second value for CDS. The pixel starts another integration by opening $M_3$ and $M_1$ respectively.

The level of the illumination is obtained by performing the CDS operation. CDS technique can eliminate the FPN noise of APSs. Compared with PPSs, the fill factor of APSs is lower. By sharing the readout circuit within the adjacent pixel cells, the fill factor can be improved. The most recent design is average 1.5 transistors per pixel, which is comparable to the fill factor of PPSs [15].

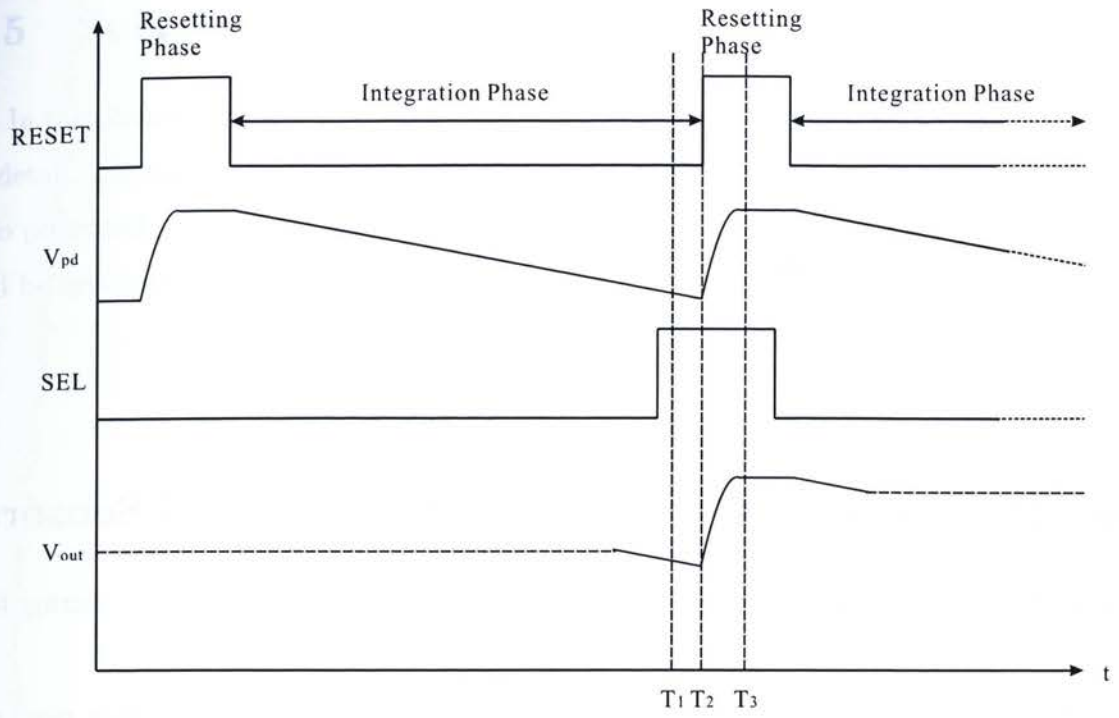



Figure 2.8: Operation of active pixel sensors.

Both PPSs and APSs have two disadvantages:

(1) The output signal from the pixel is in the analog domain.

(2) The pixel is accessed and processed through a row scan mode. With the increasing scale of the image sensors, this readout mode requires high-speed parallel readout circuits and analog-to-digital converters (ADCs) to meet the timing requirements.

### 2.3.3 Digital Pixel Sensors (DPSs)

DPSs resolve these two issues by implementing an ADC in every pixel, as shown in Fig.2.9. The ADC translates the light signal into a digital value at the immediate point of capture, thus minimizing signal degradation and cross-talk in the array and allowing for greater noise reduction methods [23].

Compared with PPSs and APSs, DPSs require more transistors integrated, lowering the fill factor and increasing the pixel size. Only simple ADC architectures can be implemented. The detailed of in-pixel ADC architectures will be discussed in Chapter 3.

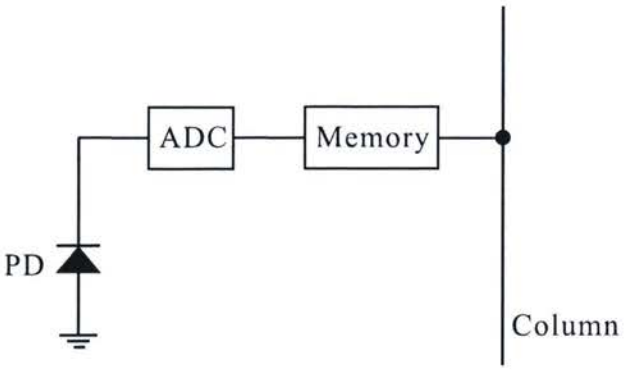



Figure 2.9: Schematic of digital pixel sensors.

## 2.4 Performance Parameters of CMOS Pixel Sensors

**Fixed Pattern Noise (FPN)**: FPN is caused by the transistors variations during fabrication. FPN can be eliminated by CDS as mentioned before.

**Fill Factor**: Fill factor is the ratio of the photo sensing area over the whole pixel cell area. Low fill factor will introduce distortion in the final image. For DPSs, high fill factor is a challenge, as more transistors are required for the in-pixel A/D conversion and digital memory.

**Dynamic Range**: Dynamic range of CMOS image sensors is defined as

$$DR = 20\log\left(\frac{I_{max}}{I_{min}}\right), \tag{2.2}$$

where $I_{max}$ is the maximum detectable photo current and $I_{min}$ is the minimum photo current. $I_{min}$ is mainly set by the dark current and other leakage currents.

**Resolution**: Resolution is the bit-width of ADC output. High resolution is strongly preferred for high-definition imaging applications. For CCD devices, there are already 14-bit ADCs available in market [2], while APSs can provide 10/12-bit resolution [26, 27].

**Frame Rate**: Frame rate is normally referred to how many pictures can be taken within one second. In some aerospace or military applications, a high-speed image sensor is required.

## 2.5 Summary

In this chapter, the photodetectors and CMOS pixel architectures have been investigated in detail. The performance parameters of photodetectors and CMOS pixel sensors have been also presented. In the next chapter, the detailed architectures of CMOS digital pixel sensors will be reviewed.

# Chapter 3

# CMOS Digital Pixel Sensors with In-pixel ADC

This chapter reviews the architectures of different digital pixel sensors reported in literature. The introduction of analog-to-digital converters is presented in Section 3.1. Section 3.2 intensively investigates the architectures of digital pixel sensors. The principles of Pulse-Width-Modulation and Pulse-Frequency-Modulation are also illustrated. Section 3.3 summaries the chapter.

## 3.1 Fundamentals of ADC

### 3.1.1 Performance Parameters of ADC

An ADC converts input analog signal ($V_{in}$) into digital signals ($D[N-1:0]$) by comparing it with a reference voltage $V_{ref}$. Normally the conversion is done with a sampling clock.

The smallest difference of $V_{in}$ that can be resolved by the ADC is called as Least Significant Bit (LSB) defined as [14]

$$LSB = \frac{V_{ref}}{2^N}, \tag{3.1}$$

where $N$ is the number of output digital bits. Full-scale range (FSR) refers to the maximum input amplitude that can be represented by the digital outputs. The relationship between the FSR and the LSB can be expressed as

$$FSR = 2^N LSB. \tag{3.2}$$

LSB and FSR only give information about the input signal range. There are a number of other parameters that quantity the performance of ADCs.

(1) **Resolution**: The resolution of an ADC is defined as the number of distinct analog levels corresponding to the different digital outputs. Usually the resolution is given in the number of output digital bits, $N$.

(2) **Quantization Noise**: Quantization noise is the inherent uncertainty in digitizing an analog value with a finite resolution A/D converter [1]. It is calculated as

$$Q_n = V_{in} - V_{dig}, \tag{3.3}$$

where $V_{dig}$=$D[N-1:0] \times LSB$=$\frac{D[N-1:0]}{2^N} \times V_{ref}$.

(3) **Offset Error and Gain Error**: Offset error and gain error are demonstrated in Fig.3.1. The slopes of an ideal ADC transfer characteristic and an actual ADC are presented in dot lines. The offset error (Fig.3.1(a)) is defined as the difference between the value of the first code transition of an actual ADC and the ideal value. The offset error is a constant value covering the whole conversion range. As shown in Fig.3.1(b), the gain error is represented as the difference between the slopes of the actual ADC and the ideal one.

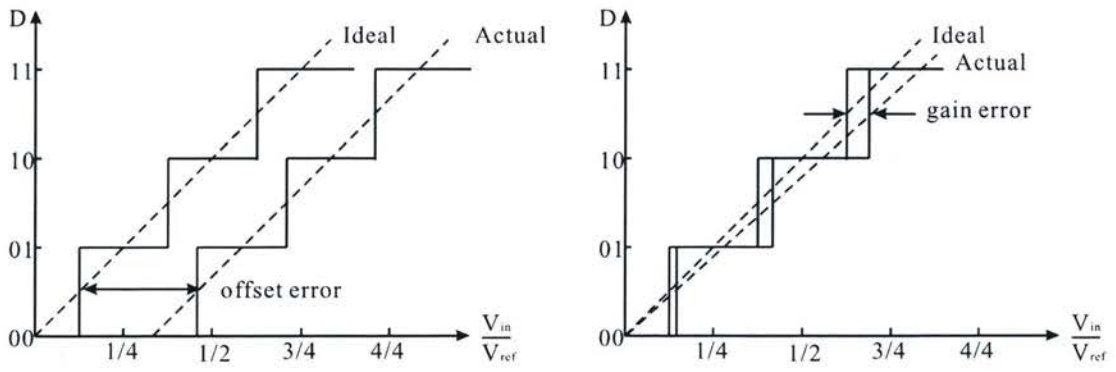



Figure 3.1: Offset error and gain error of 2-bit ADC.

(4) **Differential Nonlinearity (DNL) and Integral Nonlinearity (INL)**: DNL of an ADC is defined as

$$DNL = D_{code} - 1LSB, \tag{3.4}$$

where $D_{code}$ is the step width between two adjacent digital codes of the actual converter. The definition of INL is the maximum difference between the actual transfer characteristic and the ideal one.

(5) **Dynamic Range**: Dynamic range is specified as the ratio of the FSR over the LSB, and often represented in decibels

$$DR = 20log(\frac{FSR}{LSB}) = 20log(2^N) = 6.02N. \tag{3.5}$$

(6) **Signal-to-Noise Ratio (SNR) and Effective Number of Bits (ENOB)**: SNR is given as the ratio of the FSR over the rms value of the quantization noise. The rms value of the quantization noise can be obtained by taking the root mean square of the quantization noise [1]

$$rms = \frac{LSB}{\sqrt{12}} = \frac{FSR}{2^N\sqrt{12}}. \tag{3.6}$$

SNR can be expressed in decibels

$$SNR_{max} = 20log(\frac{FSR/(2\sqrt{2})}{FSR/(2^N\sqrt{12})}) = 6.02N + 1.76. \tag{3.7}$$

The ENOB of the ADC is derived from

$$ENOB = \frac{SNR_{real} - 1.76}{6.02}, \tag{3.8}$$

where $SNR_{real}$ is the SNR of the ADC.

### 3.1.2 Architectures of ADC

ADCs can be classified into two categories based on the sampling rate. The first category is called as Nyquist ADCs, as the input signal is sampled at the Nyquist rate, $f_r$=2$F$, where $F$ is the bandwidth of the signal and $f_r$ is the sampling rate. However in practice, the Nyquist converters operate at 1.5 to 10 times of Nyquist rate to reduce the difficulty in realizing anti-aliasing and reconstruction filters [14]. The main architectures of Nyquist ADC are:

(1) **Flash ADCs**: Flash ADCs have the highest speed among all types of ADCs, because the conversion is performed simultaneously with a group of comparators and resistors [5]. However the high area and power cost limit the application of Flash ADCs.

(2) **Pipelined ADCs**: Pipelined ADCs reduce the number of comparators by transforming the parallel conversion into a serial way. Similar to pipeline technology in digital signal processing, this type of ADC is suitable for high-speed applications. A special care must be taken when designing the first several stages, as the error of these stages will propagate through the converter and result in a large error at the end of conversion [14].

(3) **Successive Approximation ADCs**: Successive approximation ADCs perform the conversion as a binary search through all possible quantization levels, which are generated from a DAC (digital-to-analog converter). The simplicity of the architecture allows for high speed and high resolution applications with a low area cost. The accuracy mainly depends on the DAC.

(4) **Integrating ADCs**: Integrating ADCs convert the analog input into the digital domain by integrating the signal during a given time and correlating the time with a digital counter. One advantage of the architecture is the simple configuration of circuit. There are two types of integrating ADCs, single-slope architecture and double-slope architecture. The later improves the performance by integrating the signal twice in one conversion period such that noise will be cancelled out.

The other type of ADCs samples the signal at a rate much higher than the signal bandwidth. They are called as oversampling converters or $\Sigma$-$\Delta$ converters. Shown in Fig.3.2, a $\Sigma$-$\Delta$ converter consists of two major blcoks: a $\Sigma$-$\Delta$ modulator and a decimator. The mod-

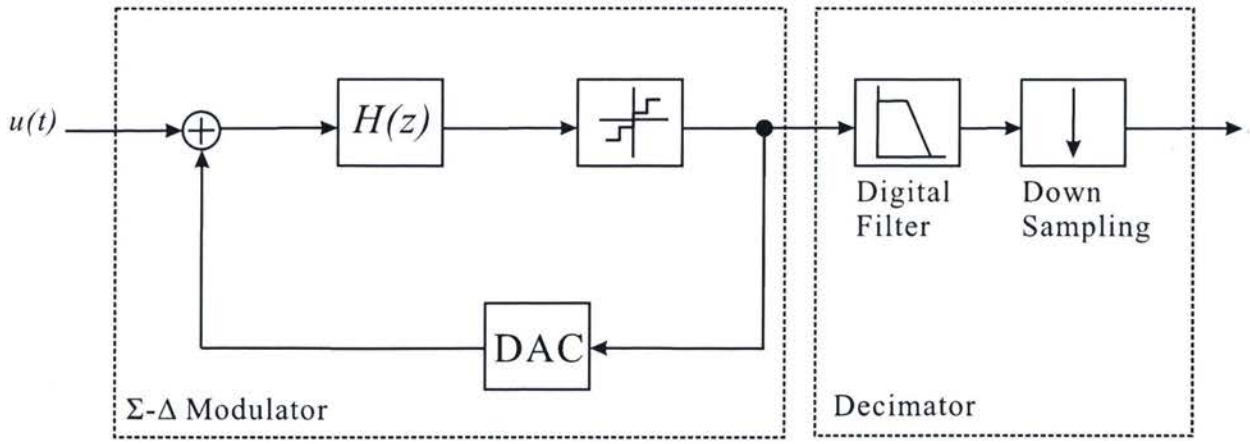



Figure 3.2: Block diagram of Σ-Δ converters.

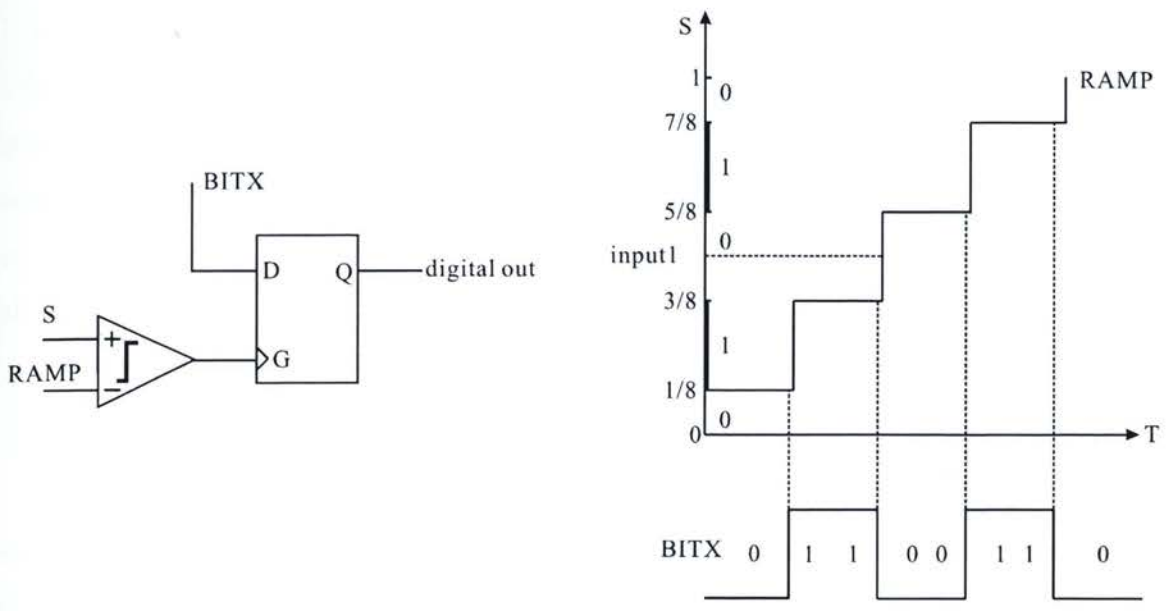
ulator performs A/D conversion by sampling and quantizing the band-limited signal as well as pushing the quantization error out of the band, while the decimator performs low-pass filtering and down-sampling in the digital domain. The low-pass filtering eliminates all the out-band noise whereas the latter reduces the output rate down to the Nyquist frequency with an output bit width, appropriate to the overall ADC resolution. The drawback of Σ-Δ converters is that the signal bandwidth is limited by the sampling rate.

## 3.2 Architectures of Digital Pixel Sensors with In-pixel ADC

As mentioned in the previous chapter, the fill factor constraint precludes the use of ADC architectures that can be realized in DPSs. The reported in-pixel architectures are reviewed in this section.

### 3.2.1 Digital Pixel Sensors with Successive Approximation ADC

The Nyquist-rate multichannel bit-serial (MCBS) proposed by Yang *et al.* [31] is an extension of successive approximation ADC. The block diagram is shown in Fig.3.3(a). The signal S is the output from a photodetection device, while the RAMP and BITX signals are generated by a global DAC and a digital control circuit, respectively.




(a) Comparator/latch pair

(b) RAMP and BITX generation for LSB

Figure 3.3: Diagram of Nyquist-rate multichannel bit-serial in-pixel ADC [31].

A 3-bit Gray code is presented in Table.3.1 for illustration. The Gray code is chosen to take the advantage of its low switching activity. In Fig.3.3(b), the waveforms of RAMP and BITX are presented for the LSB of the codeword. RAMP increases through the quantized values of the whole ADC input range, while the BITX signal indicates the code of that particular range. For instance, for input1 ranging between 3/8 and 5/8, the comparator flips when the RAMP signal is 5/8 at which BITX is logic 0. The latch will store the value of BITX and prevent further write-in. After RAMP completes the whole range, the value of the latch will be read out as the LSB value. Then RAMP and BITX are reset for the next bit comparison. In order to improve the fill factor, sharing the comparator and latch within adjacent pixels are applied [31, 32].

In general, for a $N$-bit of resolution, a total of $2^N - 1$ comparisons are needed for one pixel to generate the final digital output. This decreases the speed of image sensors.

Table 3.1: 3-bit quantization in Gray code.

| Analog Input Range (S) | Codeword |
|---|---|
| 0-1/8 | 000 |
| 1/8-1/4 | 001 |
| 1/4-3/8 | 011 |
| 3/8-1/2 | 010 |
| 1/2-5/8 | 110 |
| 5/8-3/4 | 111 |
| 3/4-7/8 | 101 |
| 7/8-1 | 100 |

### 3.2.2 Digital Pixel Sensors with Σ-Δ ADC

The in-pixel Σ-Δ ADCs proposed by Fowler *et al.* [10] and Yang *et al.* [33] are based on a synchronous first-order Σ-Δ modulator architecture. The schematic of the Sigma-Delta ADC in [33] is shown in Fig.3.4. The major components of the pixel include a clocked comparator and a 1-bit feedback DAC implemented as an analog shift register. By sharing the ADC with four photodetectors, the fill factor is improved by 30%. The dynamic range of the image sensor is 83 dB.

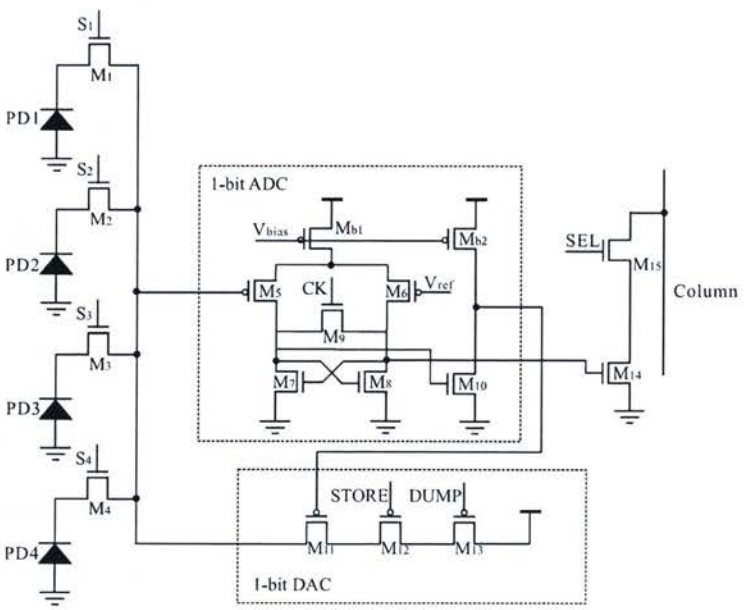



Figure 3.4: Pixel schematic of synchronous Σ-Δ in-pixel ADC [33].

In [20], McIlrath proposed another Σ-Δ in-pixel ADC architecture with an asynchronous self-reset oscillation approach, as shown in Fig.3.5. Compared with [10, 33], this design integrates a continuous differential comparator instead of the clocked one. Other major blocks of the pixel include a bistable half-latch to reset the photodiode and a regenerative circuit that disables the bistable latch and restarts the integration once the photodiode is fully charged. The dynamic range of this design is 104 dB.

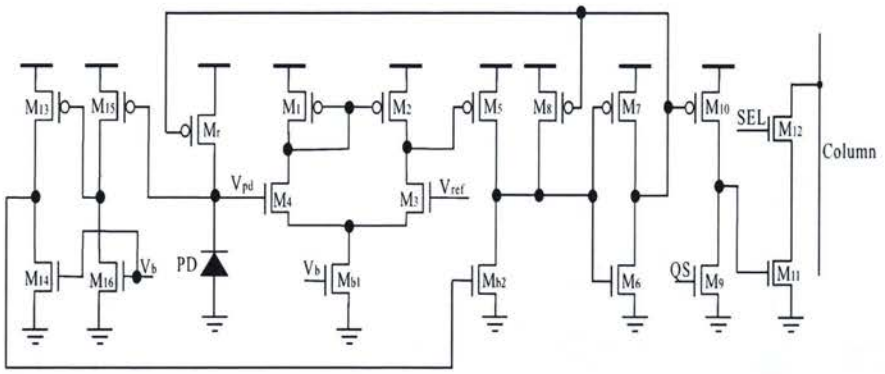



Figure 3.5: Schematic of DPS with an asynchronous Σ-Δ in-pixel ADC [20].

Unlike other in-pixel ADCs, the bit streams generated by Σ-Δ pixels must be decoded through a decimator outside the imager array to produce the final digital value. Due to the pixel size constraint, no design with high-order Σ-Δ modulator has been reported in literature.

### 3.2.3 Digital Pixel Sensors with Pulse-Width-Modulation ADC

The Single-slope integrating A/D conversion technique is also applied in in-pixel ADC designs. These DPSs are called Pulse-Width-Modulation (PWM) DPSs [17, 16].

The basic configuration of PWM pixels with a $N$-bit internal memory is shown in Fig.3.6. The operation of the PWM DPSs consists of two modes : *reset mode* and *sensing mode*. In the reset phase, the resent pMOS transistor is activated and the junction capacitor $C_{pd}$ of the photodiode PD is charged to $V_{DD}$ approximately. The comparator output $V_{comp}$ is set to logic 1. In the following sensing phase, the reset pMOS transistor is OFF and the voltage across

the photodiode $V_{pd}$ starts to drop due to the current of the photodiode. The photodiode current is set by the level of the illumination. In the mean time, a global counter outside the pixel is also activated. When $V_{pd}$ reaches the reference voltage $V_{ref}$ set by users, the output of the comparator $V_{comp}$ changes to logic 0 and the content of the global counter outside the pixel is written into the in-pixel memory. The intensity of the illumination is represented by the content of the in-pixel memory, as shown graphically in Fig.3.7. At here, the in-pixel memory can be implemented as SRAM, DRAM or registers, depending on the applications requirement.

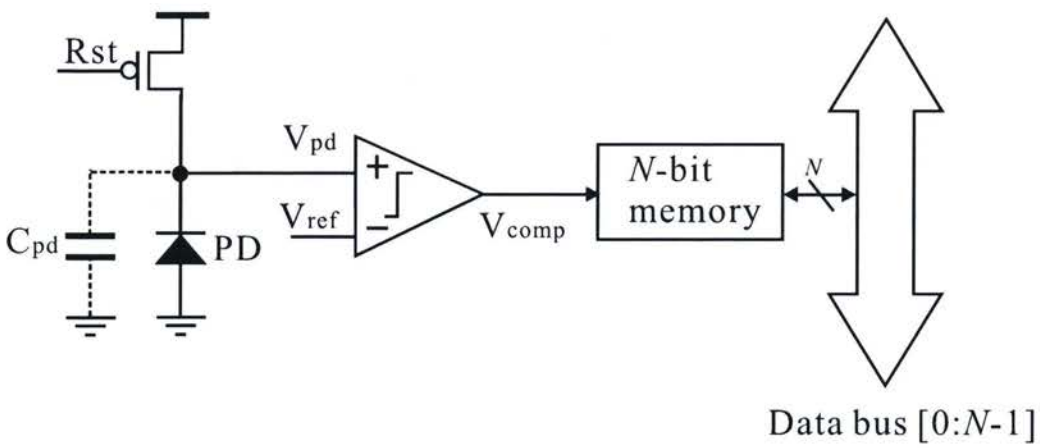



Figure 3.6: PWM digital pixel sensor with a $N$-bit internal memory.

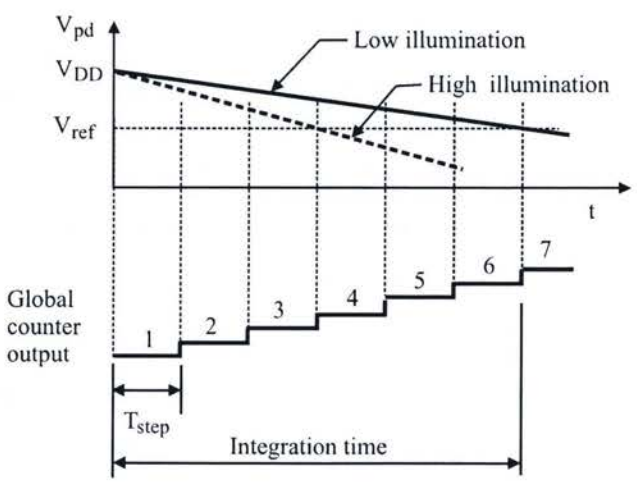



Figure 3.7: Voltage waveform of PWM DPSs.

The integration time, denoted by $T_{pd}$, can be obtained from

$$T_{pd} = \frac{(V_{DD} - V_{ref})C_{pd}}{I_{pd} + I_d}, \tag{3.9}$$

where $I_{pd}$ is the average discharge current of the photodiode, $I_d$ is the dark current and other leakage currents in the pixel, and $C_{pd}$ is the total capacitance at the cathode of the photodiode. If we assume that the time step of the counter is $T_{step}$, the value stored in the internal memory of the pixel at $t = T_{pd}$, denoted by $N_{pixel}$, is obtained from

$$N_{pixel} = \frac{T_{pd}}{T_{step}} = \frac{(V_{DD} - V_{ref})C_{pd}}{(I_{pd} + I_d)T_{step}}. \tag{3.10}$$

The average photo current $I_{pd}$, which represents the level of illumination, can therefore be obtained from (3.10).

The sensor of [17] integrates a 8-bit dynamic memory cell in every pixel, resulting in 9.4$\mu$m $\times$ 9.4$\mu$m pixel size with a 15% fill factor. With 352 $\times$ 288 array size, it can operate at 10,000 frames/second.

It is shown in (3.9) that the relationship between the photo current and the integration time is nonlinear. In order to compensate for the nonlinear effect, [16] proposed a nonuniform time-domain quantization (NUQ) scheme to automatically adjust the time step of the counter, $T_{step}$. The results demonstrated that the image sensor could achieve over 100 dB with a 8-bit in-pixel memory.

### 3.2.4 Digital Pixel Sensors with Pulse-Frequency-Modulation (PFM) ADC

PFM is also a time domain encoding scheme, similar as PWM. It has been widely used in [34, 3, 7, 30].

The configuration of conventional PFM DPSs with a $N$-bit in-pixel counter is shown in Fig.3.8. In the reset phase, the voltage across the photodiode PD, denoted by $V_{pd}$, is charged to $V_{dd}$ approximately when the reset pMOS transistor is ON. The output of the comparator is set to Logic-1. The reset pMOS transistor is then switched off and marking the on-set of the sensing phase. $V_{pd}$ starts to drop due to the conduction of the photodiode. The photodiode

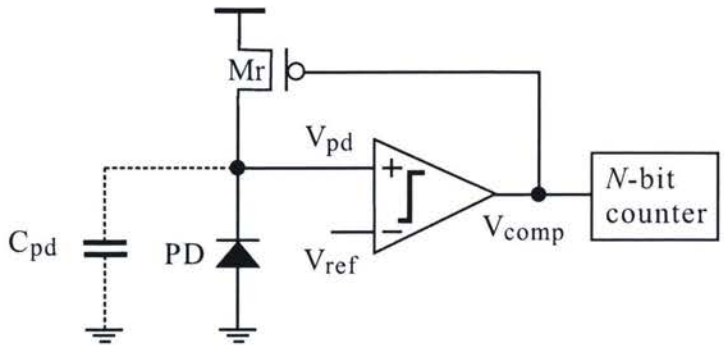
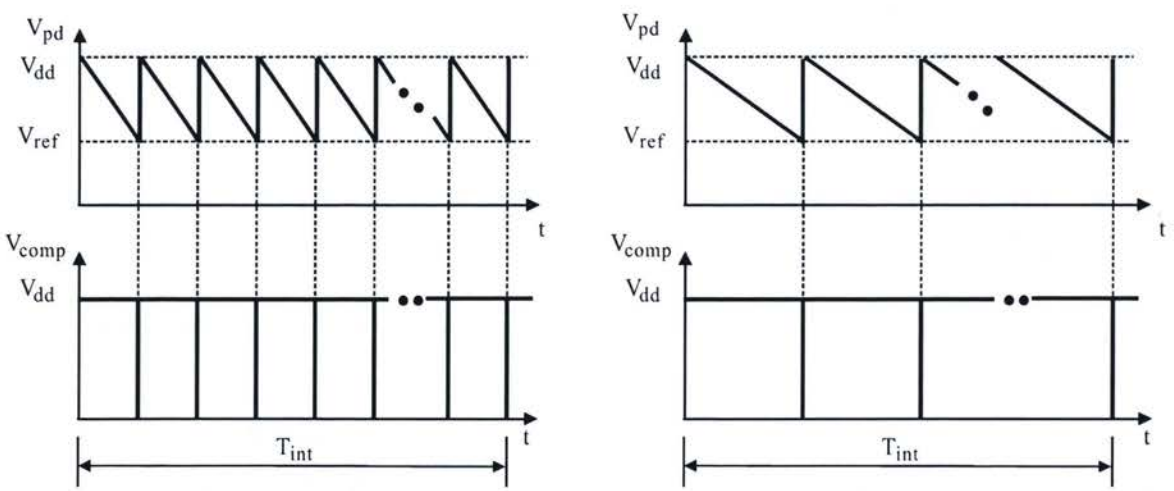



Figure 3.8: Configuration of PFM DPSs with a constant reference voltage.

current $I_{pd}$ is set by the level of illumination. When $V_{pd}$ reaches the reference voltage $V_{ref}$, the output of the comparator $V_{comp}$ will switch from Logic-1 to Logic-0, forcing the in-pixel counter to increment. It also will turn on the reset pMOS transistor and recharge the photodiode to $V_{dd}$. Because $V_{pd} > V_{ref}$, the comparator output is set to Logic 1, switching off the pMOS transistor. The sensing process repeats. The level of illumination is represented by the the content of the in-pixel counter, i.e. the number of times that the output of the comparator flips (frequency modulation) for a given integration time $T_{int}$. Fig.3.9 shows the timing diagram of the PFM DPSs with a constant reference voltage.




(a) High level of illumination

(b) Low level of illumination

Figure 3.9: Timing diagram of PFM DPSs with a constant reference voltage.

The pulse width at the comparator output of the PFM DPSs can be obtained from

$$T_{pd} = \frac{(V_{dd} - V_{ref})C_{pd}}{I_{pd} + I_d}, \tag{3.11}$$

where $C_{pd}$ is the total capacitance at the cathode of the photodiode, $I_{pd}$ and $I_d$ are the current of the photo diode and the dark current of the photodiode, and $T_{pd}$ is the discharge time, i.e. the time duration from the start of the discharge to the time instant at which $V_{pd} = V_{ref}$. In one integration time $T_{int}$, the number of the pulses at the output of the comparator is contained from

$$N_{pixel} = \frac{T_{int}}{T_{pd}} = \frac{(I_{pd} + I_d)T_{int}}{(V_{dd} - V_{ref})C_{pd}}. \tag{3.12}$$

The average current of the photodiode, denoted by $I_{pd}$, can therefore be obtained from (3.12).

$$I_{pd} = (V_{dd} - V_{ref})\frac{C_{pd}}{T_{int}}N_{pixel} - I_d. \tag{3.13}$$

It is seen from (3.13) that the average photo current of the photodiode is directly proportional to the number of the pulses at the output of the comparator (frequency modulation). The higher the reference voltage, the lower the average photo current. Also, the longer the integration time, the lower the average photo current of the photodiode.

The first in-pixel PFM image sensor was proposed by Yang in 1994 [34], and illustrated in Fig.3.10. The pixel structure is very simple, with a photodiode, a reset nMOS, and a four-stage inverter chain as a comparator to provide enough delay for resetting the photodiode. Initially, the photodiode is reset to ground. Incident light generates a photo current and causes the voltage at the photodiode node to increase. When the voltage reaches the threshold of the first inverter, the output of the inverter chain flips after certain delay and the photodiode is reset. The pulses are counted by an off-chip counter. The measured pulse frequency ranges from 1 Hz with no light to 1 MHz under high illumination, and thus around 120 dB dynamic range was achieved.

Fig.3.11 shows the DPS proposed in [3]. The ADC is also a chain of inverters. The photodiode resetting mechanism is different from [34], as the reset current is adjustable with

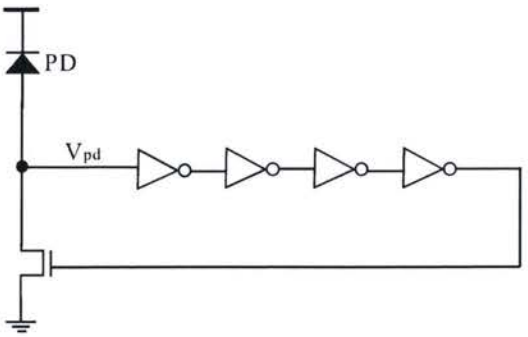



Figure 3.10: Schematic of DPS proposed in [34].

the value of the eighth bit of the counter.

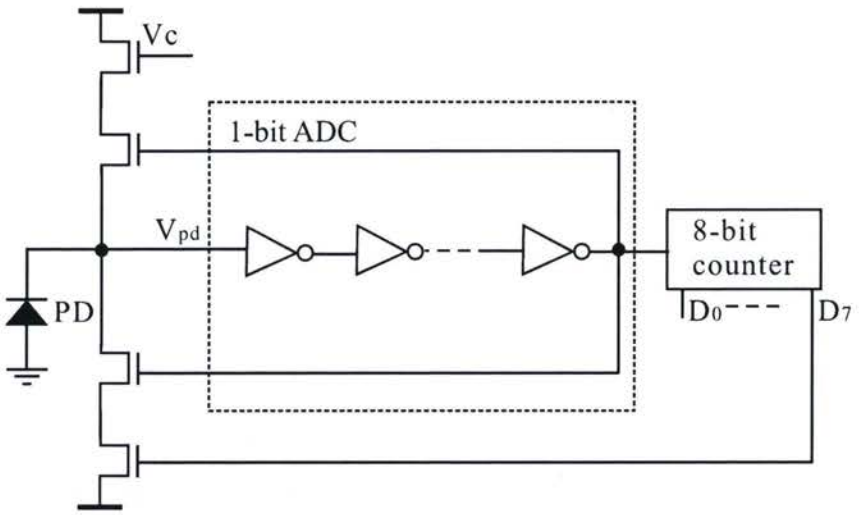



Figure 3.11: Schematic of DPS proposed in [3].

The authors of [7] designed an address-event reorientation (AER) digital pixel sensor, which mimics the processes of biological vision. In each pixel, a spike generator circuit is implemented instead of the comparator and in-pixel memory of the PFM architecture. The pixel outputs a spike to arbitration circuit once the photodiode voltage reaches the threshold voltage, after then the arbitrator sends the address information out of the pixel array. However one issue encountered in the AER-based imagers is the temporal jitter due to event collision, which decreases the SNR.

## 3.3 Summary

This chapter has reviewed the main ADC architectures first. The in-pixel ADC architectures of CMOS digital pixel sensors have been discussed, particularly the PWM and PFM ADCs. In the following three chapters, three improved Pulse-Width-Modulation and Pulse-Frequency-Modulation DPSs will be presented in detail.

# Chapter 4

# 2-Stage Memory Write Scheme for Pulse-Width-Modulation Digital Pixel Sensors

The principle of Pulse-Width-Modulation has been discussed in the last chapter. This chapter presents an improved PWM architecture with high resolution. Section 4.1 discusses the relationship between dynamic range and resolution. Section 4.2 presents the proposed 2-stage memory write scheme for PWM DPSs. In Section 6.2, the implementation is detailed. The Sections 4.4 presents the simulation results for the new architecture. Section 4.5 concludes this chapter.

## 4.1 Resolution of Pulse-Width-Modulation Digital Pixel Sensors

In Chapter 3, the mechanism of PWM was discussed. The relationship between the resolution and the in-pixel memory size will be investigated at here. The dynamic range of PWM ADC is defined as [16]

$$DR = 20\log\left(\frac{T_{max}}{T_{min}}\right), \tag{4.1}$$

where $T_{max}$ is the maximum integration time and $T_{min}$ is the minimum integration time. The $T_{step}$ of the counter is determined from

$$T_{step} = \frac{T_{max} - T_{min}}{2^N}, \tag{4.2}$$

where $N$ is the number of the bits of the in-pixel memory. Eqs.(4.1) and (4.2) show that for a given dynamic range, the larger the number of bits of the in-pixel memory, the smaller step $T_{step}$ and the higher the resolution of the pixel.

Conventional PWM digital pixels suffer from the drawback of a low resolution. This is because the constraint of fill factor sets the limitation. To increase the resolution of the pixel, the number of data bits of the in-pixel must be increased. This will increase the pixel size or equivalently lower the fill factor if the pixel size is fixed. Secondly, because the number of the data bits of the in-pixel memory is the same as that of the global counter, the silicon area for routing the interconnects for these data bits is large. The data communication between the pixel and the global counter is also high. Due to these two constraints, most reported PWM digital pixels use only a 8-bit in-pixel memory [17, 16].

## 4.2 Pulse-Width-Modulation Digitial Pixel Sensors with 2-stage Memory Write Scheme

In this section, a novel 2-stage memory write scheme is proposed to lower the number of the bits of the in-pixel memory and reduce the silicon area needed for routing data lines from the global counter to pixels without sacrificing the resolution of the pixel. To evaluate the efficiency of the proposed scheme, a 64 $\times$ 64 prototype image sensor with a 12-bit resolution is implemented.

We first introduce the concept of *Cycle*. A cycle composes of sixteen continuous states in Gray codes to take the advantage of their low switching activities. Fig.4.1 tabulates the first 64 states of a 12-bit Gray code counter. These states are grouped in 4 cycles. If we neglect the lower four bits of each state, the difference among these four cycles only exists in the upper eight bits. It switches only once every 16 states at the end of each cycle. This observation indicates that a write operation from the global counter to the in-pixel memory can be split into two separate write operations : one to write the lower 4 bits and the other

to write the upper 8 bits.

As an example, consider two pixels denoted by PD1 and PD2. The value of the pixels PD1 and PD2 are 11111100_0000 and 11111100_0100, respectively. Both of them belong to Cycle 2. When the content of the global counter reaches 11111100_0000, PD1 stores the lower 4 bits 0000 of the counter. The counter continues to count while the upper 8 bits of the counter remain unchanged. When the counter reaches 11111100_0100, the voltage of the pixel PD2 drops below its reference voltage. The output of its comparator activates the in-pixel memory and stores its lower four bits of the current content of the counter 0100. Both pixels do not have to record the upper eight bits until the end of Cycle 2 at which the upper eight bits of the counter become 11111100.

| Cycle 0 | Cycle 1 | Cycle 2 | Cycle 3 |
|---|---|---|---|
| 111111111111 | 111111100111 | 111111001111 | 111111010111 |
| 111111111110 | 111111100110 | 111111001110 | 111111010110 |
| 111111111100 | 111111100100 | 111111001100 | 111111010100 |
| 111111111101 | 111111100101 | 111111001101 | 111111010101 |
| 111111111001 | 111111100001 | 111111001001 | 111111010001 |
| 111111111000 | 111111100000 | 111111001000 | 111111010000 |
| 111111111010 | 111111100010 | 111111001010 | 111111010010 |
| 111111111011 | 111111100011 | 111111001011 | 111111010011 |
| 111111110011 | 111111101011 | 111111000011 | 111111011011 |
| 111111110010 | 111111101010 | 111111000010 | 111111011010 |
| 111111110000 | 111111101000 | 111111000000 | 111111011000 |
| 111111110001 | 111111101001 | 111111000001 | 111111011001 |
| 111111110101 | 111111101101 | 111111000101 | 111111011101 |
| 111111110100 | 111111101100 | 111111000100 | 111111011100 |
| 111111110110 | 111111101110 | 111111000110 | 111111011110 |
| 111111110111 | 111111101111 | 111111000111 | 111111011111 |

Figure 4.1: First 4 cycles of 12-bit Gray-coded counter.

The proceeding analysis demonstrates the data write operation of individual pixel can be performed in two separate steps:

- Once the comparator flips, the lower 4 bits of the global counter are written into the 4-bit in-pixel memory immediately.

- The upper 8 bits of each pixel can be moved out of the pixel array and updated at the end of the cycle.

In order to record the cycle number, we introduce one more memory cell called *cycle register* in each pixel, which samples the comparator output ($V_{comp}$) at the end of each cycle. If its value is set to logic 1 for the first time, the cycle number will be written into the corresponding out-pixel memory, and the main controller will forbid further writing access before the current frame is finished. As a result, only a 5-bit memory is required to be integrated in the pixel for a 12-bit resolution, resulting in a large reduction in the pixel size and a significant improvement in the fill factor. Because the value of the cycle register is updated once every cycle, it must be scanned out before the new cycle number is generated. The timing requirement for scanning the cycle register out of the pixel array sets the design timing constraint. For a $W \times H$ pixel array with a $N$-bit resolution, if we integrate $i$-bit in-pixel memory, one cycle period can be obtained from

$$T_{cycle} = T_{step} \times 2^i. \tag{4.3}$$

The average scan out time for the cycle register is derived

$$T_{scan} = \frac{T_{cycle}}{min(W, H)} = \frac{T_{step} \times 2^i}{min(W, H)}. \tag{4.4}$$

The use of $min(W, H)$ indicates that the scan-out chain can be implemented in either column level or row level based on which one has the minimum number of cells. The 2-Stage memory write scheme must find a balance between the number of the bits of the in-pixel memory and the average scan time such that the speed for scanning the cycle register is not too high.

## 4.3 Implementation

The proposed PWM image sensor was designed in TSMC-0.18$\mu$m 1.8V CMOS technology. The pixel array was designed at the transistor level while the control logic including the global counter was designed in Verilog from Cadence Design Systems.

The configuration of the PWM DPS with the proposed 2-stage memory write scheme is shown in Fig.4.2. In Fig.4.2, the *cycle register* R0 is connected to a column-based *Pixel Ready* signal. R0 is implemented as a high-level sensitive latch to minimize the number of transistors inside the pixel. The 4-bit in-pixel memory is responsible for storing the lower four bits of the global counter *Data Bus*[0:3].

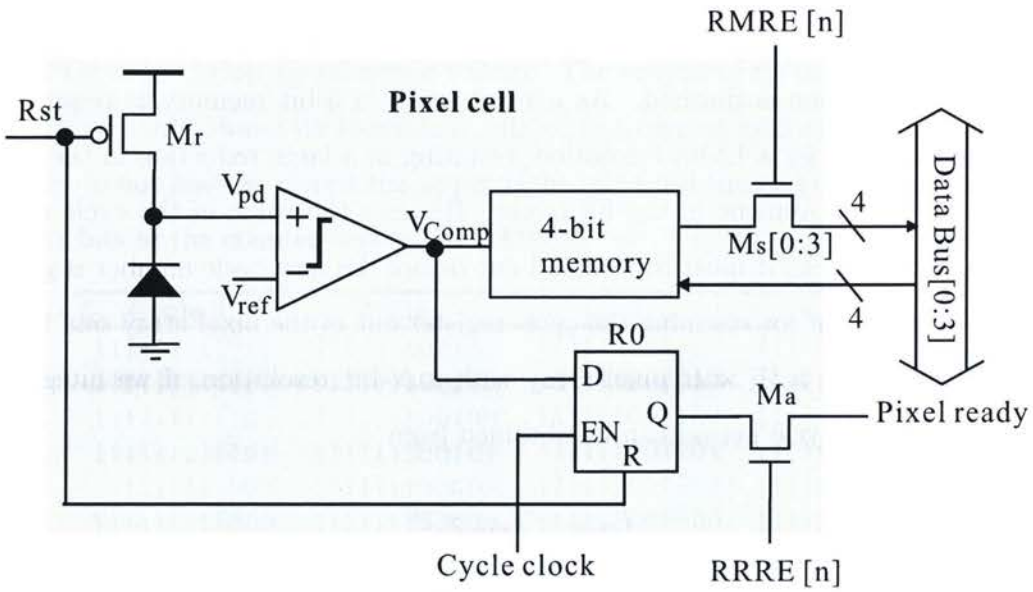



Figure 4.2: Configuration of PWM digital pixel with a 2-stage memory write scheme.

Its timing diagram given in Fig.4.3. In Fig.4.3, we assume that the pixel reaches its reference voltage at time instant $T_{pd}$ at which $V_{comp}$ switches from LOW to HIGH. In the mean time, the memory MEM[0:3] stores *Data Bus*[0:3]. The content of R0 will not be latched until the time instant $T_{cycle}$ at which *Cycle Clock* is at its falling edge, while the cycle number also changes. The global signal *Cycle Clock* is at the end of each cycle so that the latch R0 will sample $V_{comp}$ once every cycle. Eq.(4.4) can be modified to

$$T_{scan} = \frac{T_{step} \times 2^i - T_{cclk}}{H}, \tag{4.5}$$

where $T_{cclk}$ is the pulse width of *Cycle Clock* and we assume that $H \leq W$. After *Cycle Clock* is LOW, a column-level signal *Row Register Read Enable (RRRE)* enables the readout of R0

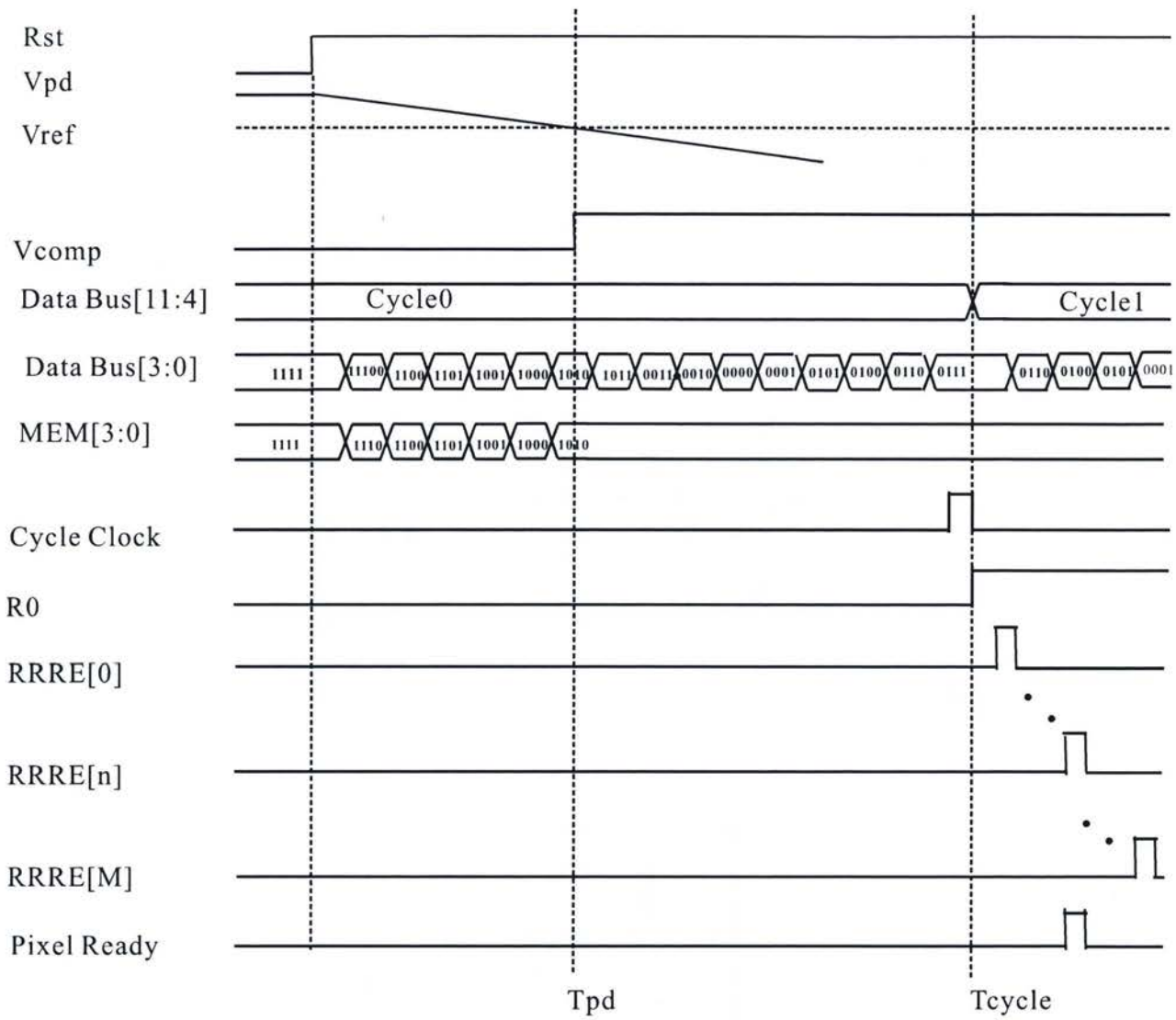



Figure 4.3: Timing diagram of the proposed 12-bit PWM DPS array with a 2-stage memory write scheme. $n$ is the number of columns of the array.

that asserts *Pixel Ready* during every cycle. Once the main controller detects *Pixel Ready*, the control logic will write the cycle number into the out-pixel memory and forbid further writing access. The $W$ columns of *RRRE* should not be overlapped so that bus hazards on *Pixel Ready* can be eliminated. After the sensing mode is finished, the lower 4-bit memory of each pixel will be scanned out with *Row Memory Read Enable signal (RMRE)* and combined with the cycle number in the out-pixel memory to yields $T_{pd}$.

The schematic of the reset transistor and the comparator is shown in Fig.4.4, while the width of the transistors is tabulated in Table.4.1. The channel length of all transistors length was 0.18$\mu$m except that of the reset transistor $M_r$, which was 0.5$\mu$m. The reference voltage, $V_{ref}$ is set to 1.5V, while $V_{bias1}$ is set to 0.4V such that transistors $M_{b1}$ and $M_{b2}$ are biased in the sub-threshold region to reduce the power consumption of the pixel.

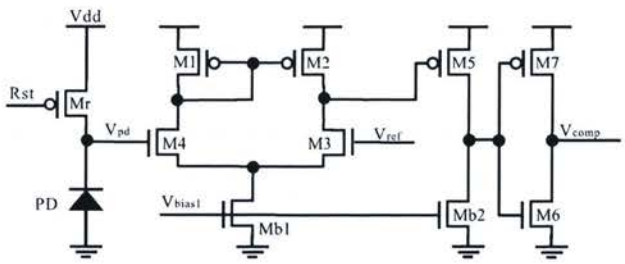



Figure 4.4: Schematic of PWM digital pixel sensors (memory is not shown).

Table 4.1: Transistor width of PWM digital pixel sensors (memory is not listed).

| Transistor | Width ($\mu$m) |
|---|---|
| $M_r$ | 0.5 |
| $M_1$ | 0.5 |
| $M_2$ | 0.5 |
| $M_3$ | 0.5 |
| $M_4$ | 0.5 |
| $M_5$ | 1.5 |
| $M_6$ | 0.5 |
| $M_7$ | 0.5 |
| $M_{b1}$ | 1.5 |
| $M_{b2}$ | 0.5 |

The 4-bit in-pixel memory and cycle register R0 are implemented using the 3T dynamic memory cells proposed in [17] to increase the fill factor, as shown in Fig.4.5. The transistors size is shown in Table.4.2. The size of $M_2$ is chosen such that no refresh mechanism needed during operation.

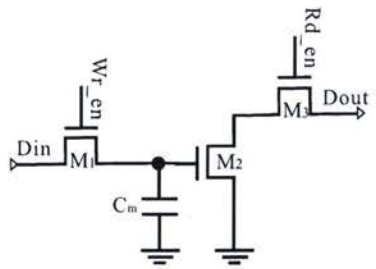



Figure 4.5: Schematic of dynamic memory.

Table 4.2: Transistor size of dynamic memory.

| Transistor | Width ($\mu$m) | Length ($\mu$m) |
|---|---|---|
| $M_1$ | 0.25 | 0.18 |
| $M_2$ | 1 | 1 |
| $M_3$ | 0.25 | 0.18 |

To assess the performance of the proposed 2-stage write scheme, an ideal current source is used to model the photo current of the pixel. The target dynamic range is from 100 nA to 1 pA, corresponding to 100 ns to 1 ms of the integration time. The time step $T_{step}$ of the counter is obtained using (4.2) and is set to 1 $\mu$s. To simplify the design, the pulse width of the cycle clock $T_{cclk}$ is set to $T_{step}$. The cycle time $T_{cycle}$ and the average scan out time $T_{scan}$ are obtained from (4.3) and (4.5). The pulse width of $RRRE$ is set to 200 ns.

## 4.4 Simulation Results

An ideal current source of 300 pA is used to model the photo current of the pixel. The design is analyzed using Spectre with BSIM3V3 device models and Verilog-XL co-simulation from Cadence Design Systems. Fig.4.6 plots the waveform of the critical nodes of the pixel.

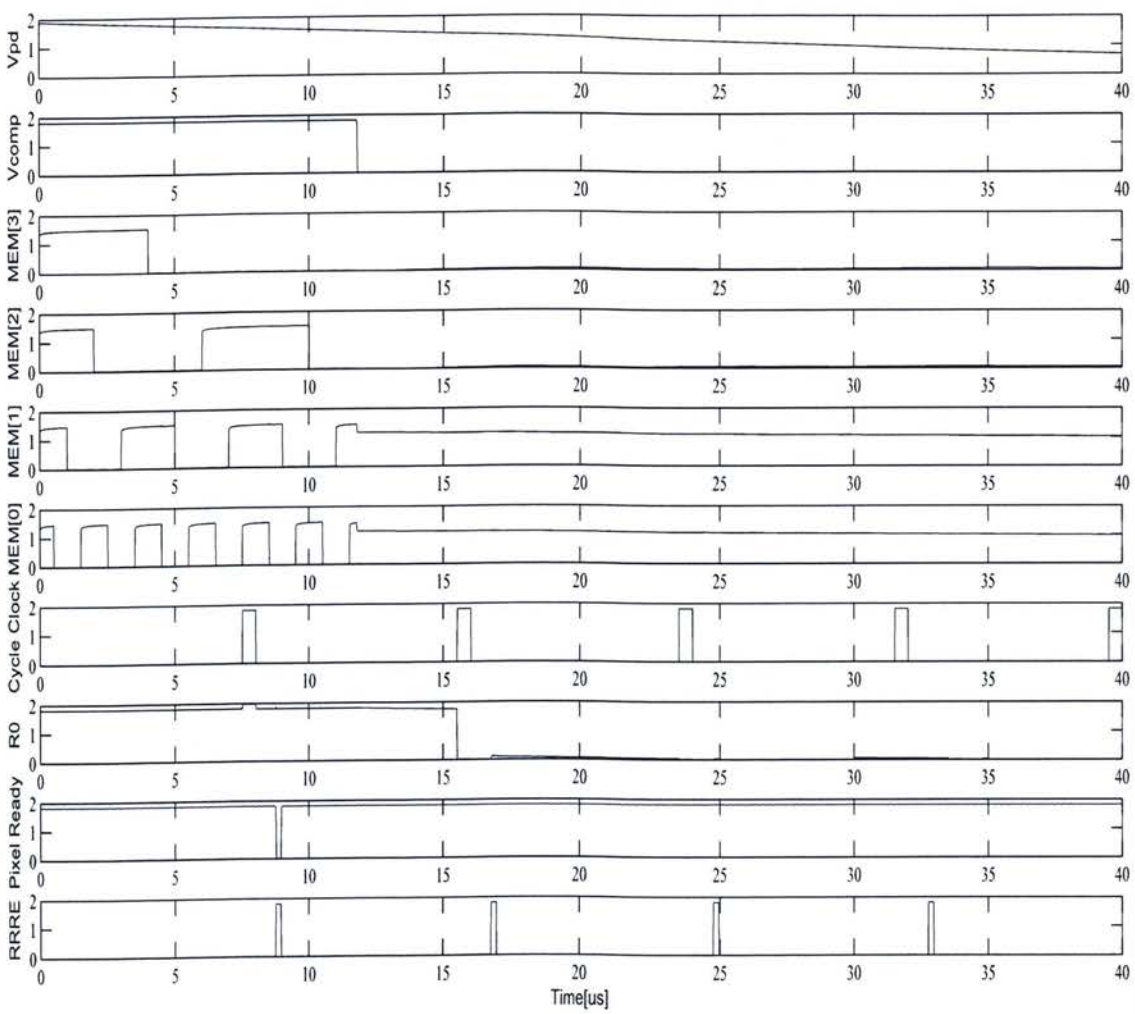



Figure 4.6: Simulation results.

The comparator flips at 11.79 $\mu$s and the internal memory stores the low 4 bits 0011 from the counter. R0 switches at Cycle 1 (15.5$\mu$s) representing the upper 8-bit 11111110. The combination of the cycle number and the internal memory yields the final result 111111100011.

The layout of the proposed pixel is shown in Fig.4.7. The fill factor is 20%. Table.4.3 compares the resolution, fill factor, and size of the proposed pixel and those of cited work.

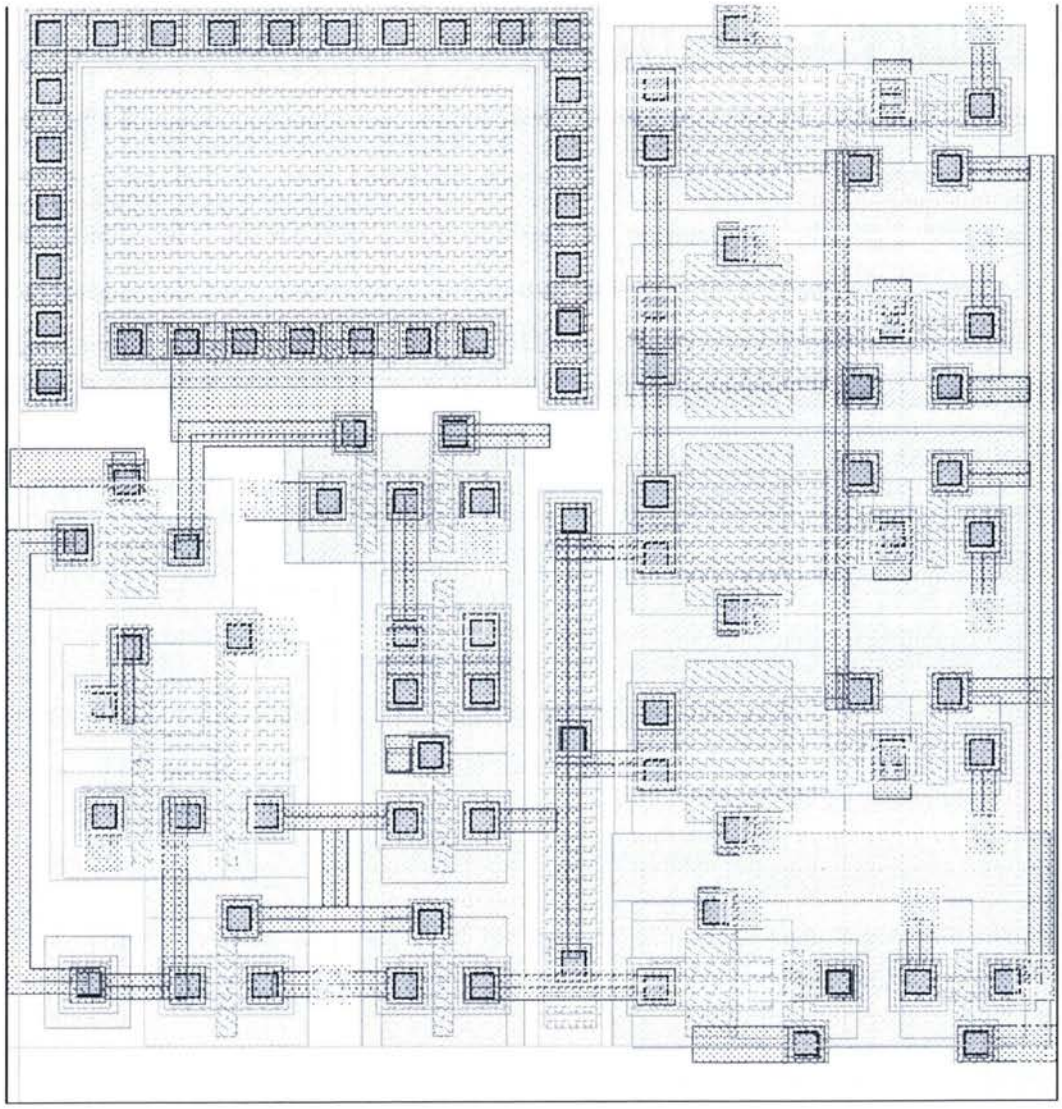


Figure 4.7: Layout of the proposed PWM digital pixel sensors (Pixel size : 9$\mu$m $\times$ 9$\mu$m).

Table 4.3: Performance comparison.

| Design | Resolution | Technology | Pixel Size | Fill-factor |
|---|---|---|---|---|
| This work | 12-bit | 0.18$\mu$m | 9$\mu$m $\times$ 9$\mu$m | 20% |
| [17] | 8-bit | 0.18$\mu$m | 9.4$\mu$m $\times$ 9.4$\mu$m | 15% |
| [16] | 8-bit | 0.35$\mu$m | 45$\mu$m $\times$ 45$\mu$m | 25% |
| [30] | 10-bit | 0.18$\mu$m | 23$\mu$m $\times$ 23$\mu$m | 25% |

## 4.5 Summary

In this chapter, the relationship between resolution and dynamic range of CMOS Pulse-Width-Modulation digital pixel sensors has been discussed first. A 2-stage memory write scheme has been presented to improve the resolution of PWM DPSs. The architecture and design of a new 12-bit Pulse-Width-Modulation digital pixel sensor with the proposed 2-stage memory write scheme have been presented. The proposed DPS offer an improved fill factor to 20% by only integrating 5-bit memory totally in the pixel to achieve 12-bit resolution. The removal of a large portion of the memory significantly reduces the silicon area of the pixel and data traffic between the pixel and the global counter. Implemented in TSMC-0.18$\mu$m 1.8 V CMOS technology, the effectiveness of the proposed DPS is validated by simulation.

# Chapter 5

# Pulse-Frequency-Modulation Digital Pixel Sensors with In-pixel Amplification

From the circuit perspective, Pulse-Width-Modulation and Pulse-Frequency-Modulation share some commons. Both architectures require an in-pixel comparator to determine the time instance at which the voltage across the photodiode drops below a user-defined reference voltage. A number of memorable cells are integrated in both types of pixels.

However differences still exist. PWM DPSs use the output of the in-pixel comparator as a *write enable signal* to write the value of a global counter located outside the pixel array into in-pixel internal memories. The content of the in-pixel memories is then read in the read phase. The performance of PWM DPSs is affected by the following factors :

- A high speed clock is needed to drive the global counter.
- The time delay from the output of the global counter to each pixel will introduce an error on the final value of the in-pixel memories.
- The number of the bits of the global counter. When a large number of bits are used, the silicon area for routing these data lines from the global counter to each pixel will be costly.
- The load of the global counter is large as its output will be written into all in-pixel

memories.

PFM DPSs avoid these difficulties by replacing the global counter of PWM DPSs with in-pixel counters that are controlled by the output of the in-pixel comparators. The in-pixel counter of each DPSs pixel increases its value each time the voltage of respective the photodiode drops below the reference voltage [30]. The level of illumination is represented by the number of times the output of the comparator flips for a given integration time. A main drawback of PFM DPSs is that when illumination is low, the integration time has to be set long enough in order to have a good resolution. In [26], an adaptive high-gain column-level amplifier is employed to amplify the low signal before analog-to-digital conversion. This approach, however, does not have in-pixel ADC. This chapter proposes new PFM DPSs with in-pixel amplification to improve the resolution of PFM DPSs in the low illumination condition without an over-long integration time. Section 5.1 describes the proposed PFM scheme with in-pixel amplification. Section 5.2 details the circuit implementation. Simulation results of PFM DPS with in-pixel amplification is presented in Section 5.3. The chapter is concluded in Section 5.4.

## 5.1 Pulse-Frequency-Modulation Digital Pixel Sensors with In-pixel Amplification

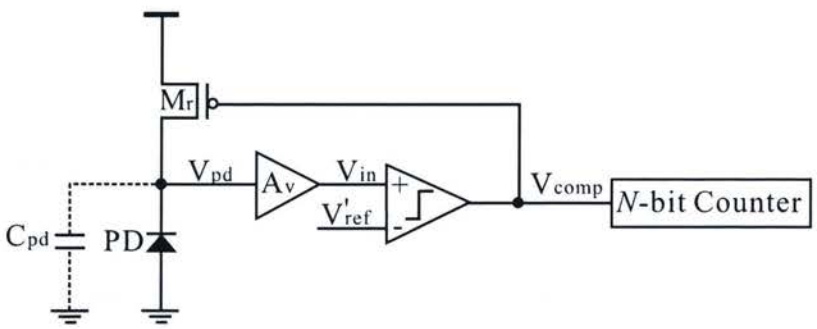



Figure 5.1: PFM digital pixel sensors with in-pixel amplification and a $N$-bit counter.

The configuration of the proposed PFM digital pixel sensor with in-pixel amplification

is shown in Fig.5.1. Assume that the junction capacitor of the photodiode is charged to $V_{dd}$ and the output of the amplifier $V_{in}$ is set to $V_a$ initially. During the sensing phase,

$$V_{in}(t) = V_a - A_v V_{pd}(t) = V_a - A_v \frac{(I_{pd} + I_d)t}{C_{pd}}, \tag{5.1}$$

where $A_v$ is the voltage gain of the amplifier. The pulse width at the comparator output is obtained from

$$T'_{pd} = \frac{(V_a - V'_{ref})C_{pd}}{(I_{pd} + I_d)A_v}, \tag{5.2}$$

where $V'_{ref}$ is the reference voltage. If we set

$$V_a - V'_{ref} = V_{dd} - V_{ref} = \Delta V, \tag{5.3}$$

$T'_{pd}$ can be expressed as

$$T'_{pd} = \frac{\Delta V C_{pd}}{(I_{pd} + I_d)A_v} = \frac{T_{pd}}{A_v}. \tag{5.4}$$

It can be seen from (5.4) that the pulse width of the PFM DPSs with in-pixel amplification is $\frac{1}{A_v}$ that of the corresponding PFM DPS without in-pixel amplification. If the two PFM digital pixel sensors have the same number of pulses at the output of the comparator, i.e.

$$N'_{pixel} = N_{pixel} = \frac{T_{int}}{T_{pd}} = \frac{T'_{int}}{T'_{pd}}, \tag{5.5}$$

then the new integration time $T'_{int}$ of the DPS with in-pixel amplification is obtained from

$$T'_{int} = \frac{T_{int} T'_{pd}}{T_{pd}} = \frac{T_{int}}{A_v}. \tag{5.6}$$

The integration time of the DPS with in-pixel amplification pixel is only $\frac{1}{A_v}$ that of the corresponding DPS without in-pixel amplification. Therefore the dynamic range is improved.

## 5.2 Implementation

### 5.2.1 Amplifier and Comparator

The schematic of the proposed PFM DPS with in-pixel amplification is shown in Fig.5.2. In Table.5.1, the transistors width is presented. The lengths of transistors are set to $0.18\mu m$, except $L_r = 0.8\mu m$. The photodiode is a n+/p-substrate diode with dimensions 13 $\mu$m $\times$ 11 $\mu$m. The amplification stage consists of $M_a$, $M_b$, and $M_c$. $M_a$ is a source follower to shift the voltage of the photodiode $V_{pd}$ down by one threshold voltage approximately. $M_b$ is a common-gate amplifier with $M_c$ the current source load and voltage gain

$$A_v \approx g_{m,b}(r_{o,b} || r_{o,c}), \tag{5.7}$$

where $g_{m,b}$ is the transconductance of $M_b$, $r_{o,b}$ and $r_{o,c}$ are the output impedance of $M_b$ and $M_c$, respectively. In our design, the gain of the amplification stage is set to 20 dB approximately. For the same $\Delta V$, the pulse width of the output of the comparator of the DPS with in-pixel amplification is $\frac{1}{10}$ times of that without in-pixel amplification. Following the amplifier is a conventional PMOS two-stage comparator. The inverter drives the in-pixel counter and the reset transistor $M_r$.

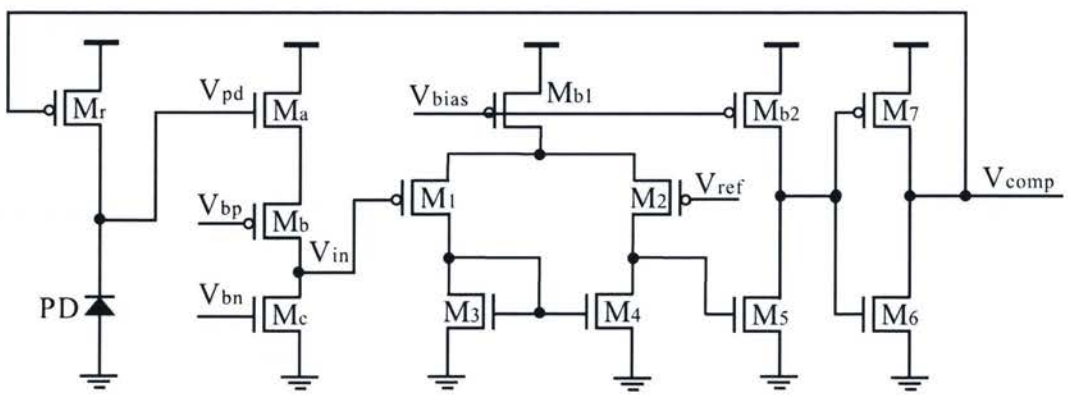



Figure 5.2: Simplified schematic of digital pixel sensors with in-pixel amplification (counter is not shown).

Table 5.1: Transistor width of PFM digital pixel with in-pixel amplification (counter is not listed).

| Transistor | Width ($\mu$m) |
|---|---|
| $M_r$ | 0.5 |
| $M_a$ | 2 |
| $M_b$ | 4 |
| $M_c$ | 0.8 |
| $M_1$ | 2 |
| $M_2$ | 2 |
| $M_3$ | 1 |
| $M_4$ | 1 |
| $M_5$ | 2 |
| $M_6$ | 1 |
| $M_7$ | 2 |
| $M_{b1}$ | 2 |
| $M_{b2}$ | 4 |

### 5.2.2 Counter

An area-efficient counter is strongly desired because it has a direct impact on the fill factor and pixel size. Illustrated in Fig.5.3, the Linear-Feedback-Shifting-Register (LFSR) can be used as a counter, which only requires 10 registers and a two inputs exclusive NOR (XNOR) gate. The simple connections in Fig.5.3 also indicate that the layout can be very compact. The other benefit of adopting LFSR as a counter is that the content of the registers can be read out by shifting them to the highest register ($Q_9$), therefore additional readout circuit is not required. The main drawback of LFSR is that it does not increase its value in a binary sequence or Gray code, therefore a digital decoder is required off the pixel array.

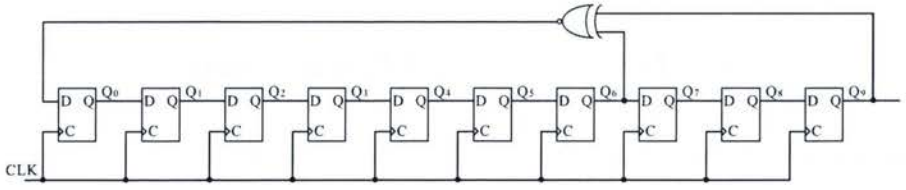



Figure 5.3: Schematic of 10-bit LFSR.

In Fig.5.4, two more MUXs are inserted for modes switching. The input signal SEL is

the mode switching signal. If SEL is high, the counter is in the counting mode. If SEL is low, the vaule of LFSR is read out. EXTCLK is the clock signal in the data readout mode, and SERIALIN is the data input port to reset the counter during the readout phase.

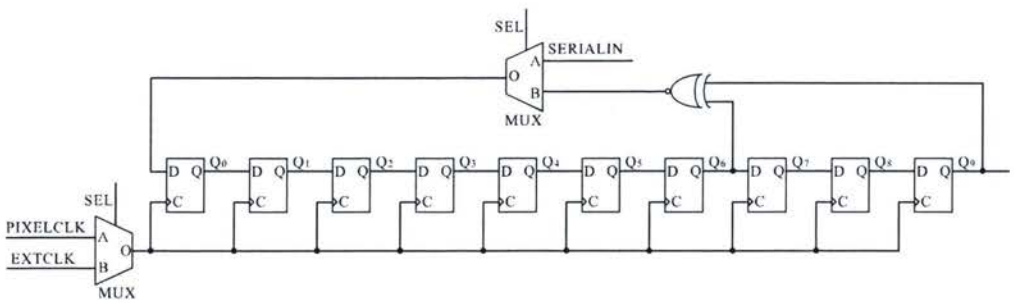



Figure 5.4: Schematic of modified 10-bit LFSR as a counter for PWM pixel.

### 5.2.3 Register

Compared with other D flip-flops architectures, a single-clock 6 transistors dynamic D flip-flop requires the minimum number of transistors. A drawback of the dynamic D flip-flop is its need for a refresh mechanism to prevent data loss when the illumination is low and there is no clock activities for a long time. In [30], the authors added a refresh circuit to prevent the counters from losing their bit values. However in that design, the counter will increase with every refresh pulse, which decreases the dynamic range. A modified dynamic D flip-flop shown in Fig.5.5 is used in this design. With a weak transistor $M_7$ (small channel width), the charge loss of the second latch is reduced. The transistors width is tabulated in Table.5.2.

## 5.3 Simulation Results and Discussion

For the purpose of comparison, the PFM DPS proposed in [30] is also implemented with a two-stage nMOS comparator. The dimension of the photodiode and reset transistor are set to be the same in order to have a fair comparison. Both DPSs are implemented in TSMC-0.18$\mu$m 1.8 V CMOS technology and analyzed using Spectre from Cadence Design Systems

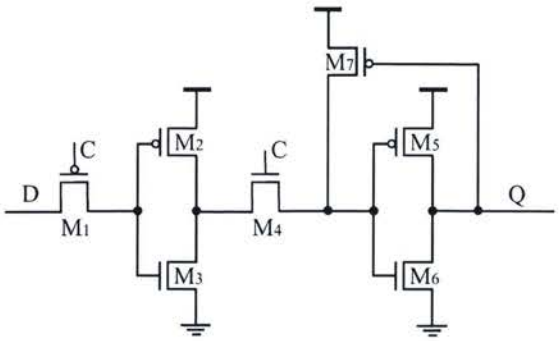



Figure 5.5: Schematic of D flip-flop.

Table 5.2: Transistor width of D flip-flop.

| Transistor | Width ($\mu$m) |
|---|---|
| $M_1$ | 1 |
| $M_2$ | 1 |
| $M_3$ | 0.5 |
| $M_4$ | 0.5 |
| $M_5$ | 1 |
| $M_6$ | 0.5 |
| $M_7$ | 0.25 |

with BSIM3V3 device models. Ideal current sources are used to model the current of the photodiodes.

Fig.5.6 plots that the voltages of two PFM pixels with a 10 $p$A photo current and 700 $\mu$s integration time. The bias voltages are $V_{bias}$=1.3 V, $V_{bp}$=0.34 V, and $V_{bn}$=0.55 V. The reference voltage of the pixel sensor without in-pixel amplification is set to 1.6 V. $V_{ref}$ of the pixel with in-pixel amplification is 0.2 V and $V_a$ is 1.0 V.

As can be seen from the figure that the output voltage of the comparator $V_{comp}$ of the pixel with in-pixel amplification has 10 pulses with pulse width 69.5 $\mu$s. The pixel without in-pixel amplification has only 3 pulses with pulse width 222.5 $\mu$s. The integration time of the pixel with in-pixel amplification is 3.2 times shorter. The voltage gain of the amplification stage is 22 dB approximately.

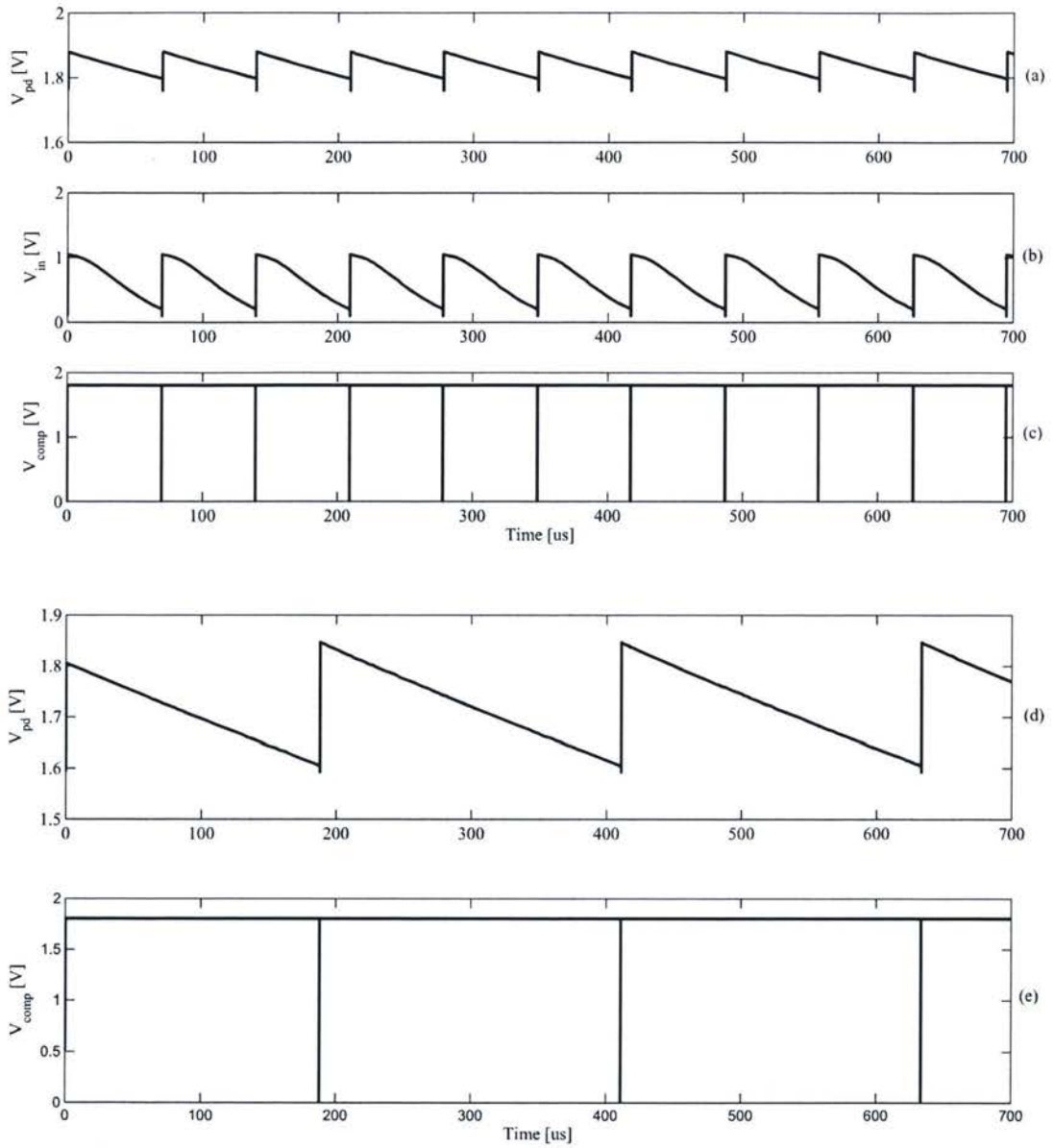



Figure 5.6: Simulated waveform of voltages of DPSs with and without in-pixel amplification. Figures (a), (b) and (c) show the signal of PFM with in-pixel amplification. Figures (d) and (e) show the signals of PFM without in-pixel amplification.

The whole pixel with 10-bit LFSR is also verified through simulation. Fig.5.7 is a part of simulation results with 10 nA photo current.

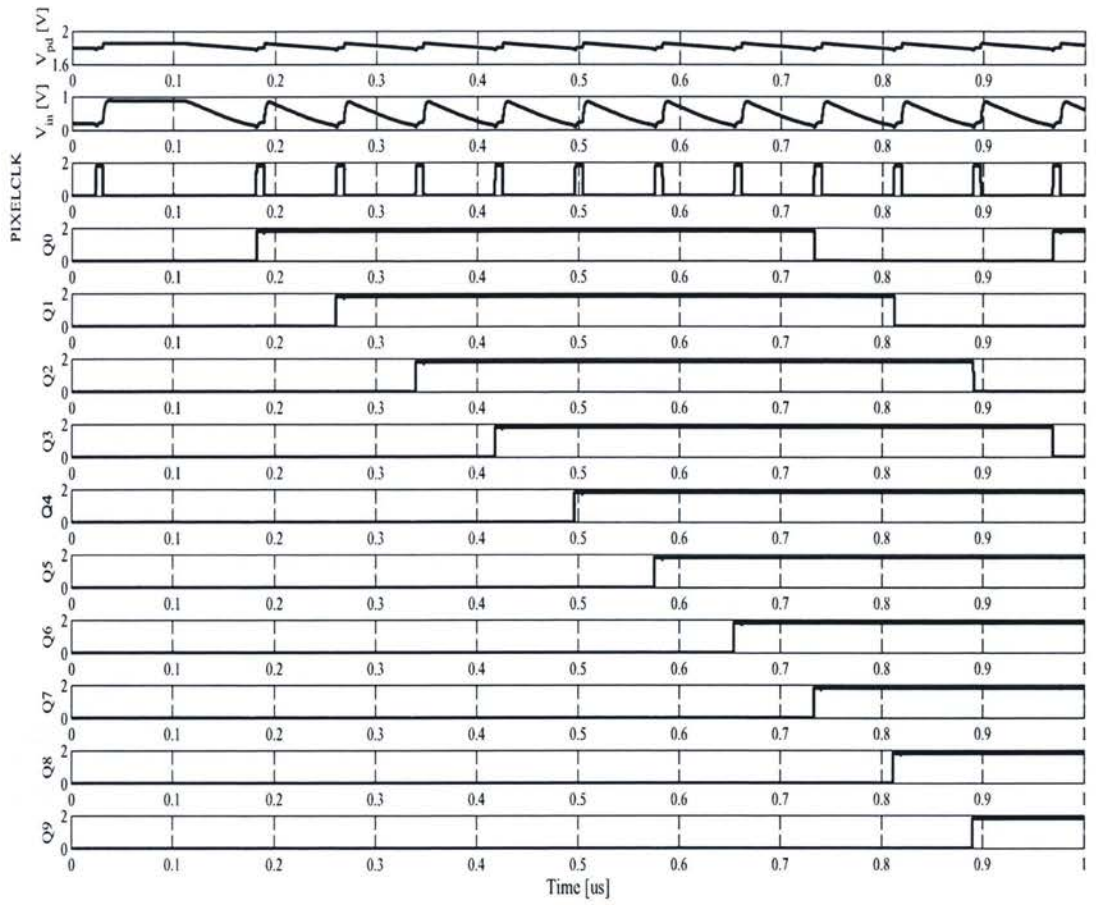



Figure 5.7: Waveform of proposed DPS with 10 nA photo current.

The dynamic range of two PFM DPSs are compared in Fig.6.9 with the integration time set to 250 $\mu$s. The dynamic range of the proposed PFM DPS is approximately 100 dB whereas that of the conventional PFM DPS is only 80 dB. The upper bound of the dynamic range of the two DPSs is approximately the same. This is because at high illumination, the voltage gain of the amplification gain decreases.

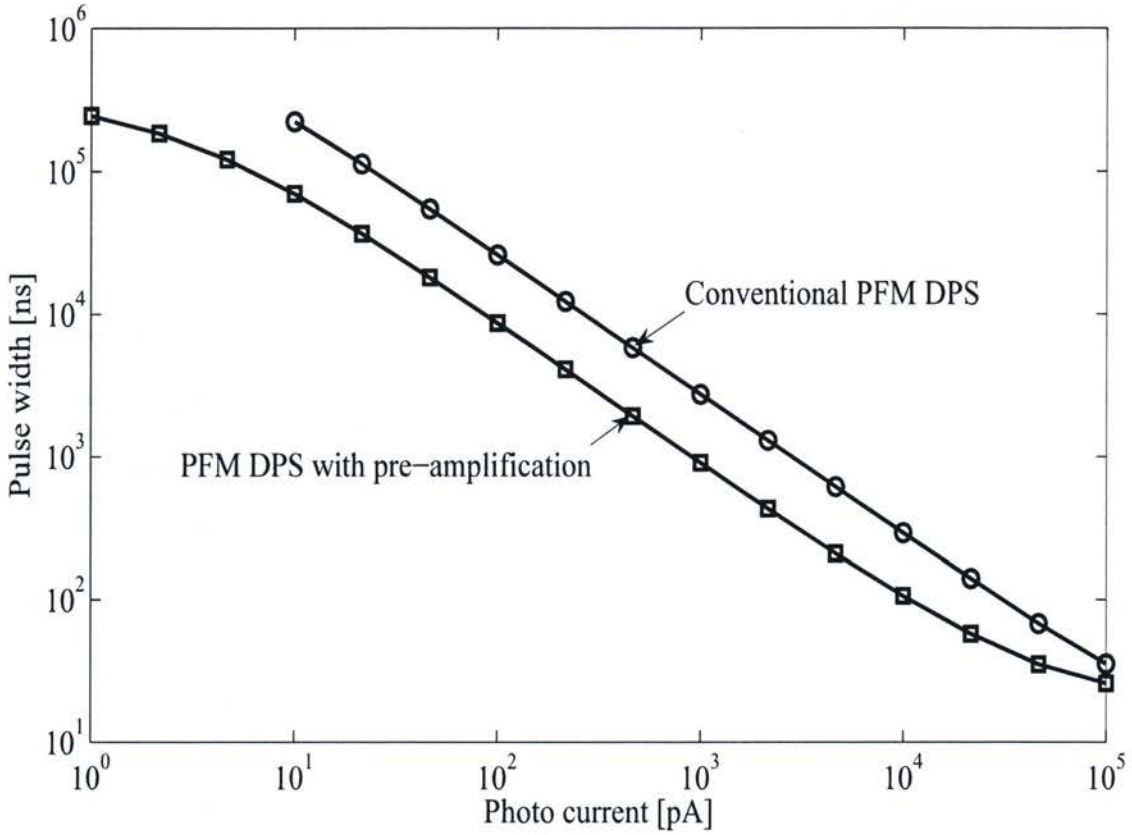



Figure 5.8: Dynamic ranges of proposed PFM DPS and that of conventional PFM DPS for 250 $\mu$s integration time.

Corner analysis is also performed to evaluate the performance of the proposed PFM DPS. Fig.5.9 shows the dynamic range of the proposed DPS at process corners. The bias voltages $V_{bn}$ and $V_{bp}$ are adjusted to ensure that the dynamic range remains nearly unchanged. The bias conditions are presented in Table.5.3. This observation reveals that by a proper change of the biasing conditions, the effect of process variation can be minimized.

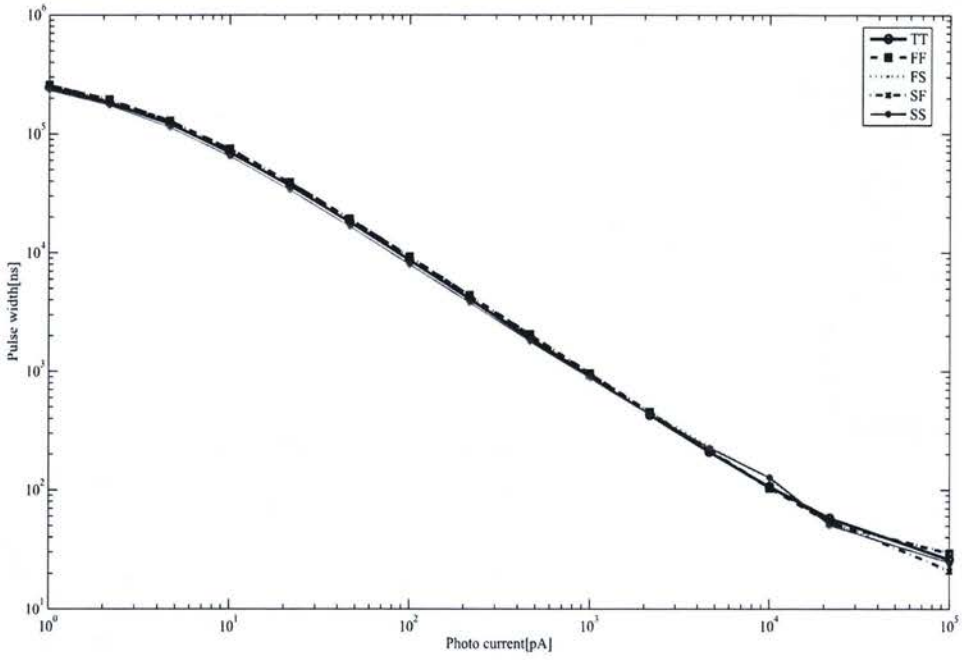



Figure 5.9: Dynamic range of proposed PFM DPS for 250 $\mu$s integration time at process corners.

Table 5.3: Bias conditions at process corners.

| Codition | $V_{bp}$(V) | $V_{bn}$ $(V)$ |
|---|---|---|
| $TT$ | 0.34 | 0.55 |
| $FF$ | 0.52 | 0.45 |
| $FS$ | 0.37 | 0.45 |
| $SF$ | 0.32 | 0.64 |
| $SS$ | 0.23 | 0.55 |

The layout of the PFM digital pixel sensor with in-pixel amplification is shown in Fig.6.12. The size of the pixel is 25 $\mu$m $\times$ 23 $\mu$m with the fill factor of 25%, which is comparable to the pixel reported in [30].

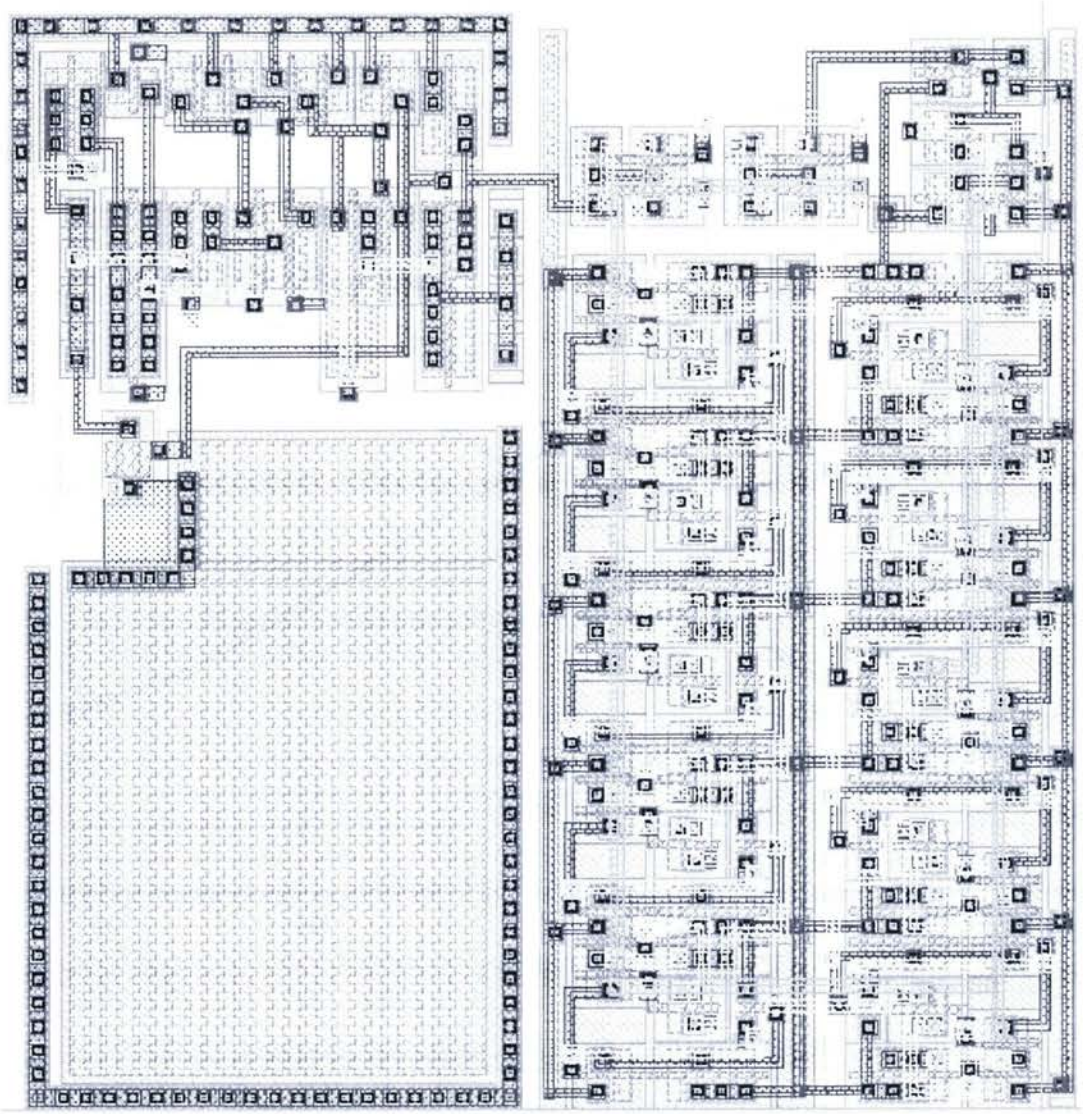


Figure 5.10: Layout of PFM pixel with in-pixel amplification.

## 5.4 Summary

The characteristics of Pulse-Width-Modulation and Pulse-Frequency-Modulation have been discussed first. New pulse-frequency-modulation (PFM) digital pixel sensors (DPSs) with in-pixel amplification has been proposed to expand the dynamic range of the sensor at the low illumination. It has been shown that the proposed PFM DPS offer the attractive characteristics of a reduced integration time when the level of illumination is low with the fill factor comparable to that of PFM DPS without in-pixel amplification. Simulation results of PFM DPS implemented in TSMC-0.18$\mu$m 1.8 V CMOS technology have shown that the dynamic range of the DPS with in-pixel amplification is 20 dB larger than that without in-pixel amplification.

# Chapter 6

# Wide Dynamic Range Pulse-Frequency-Modulation Digital Image Sensors with In-pixel Variable Reference Voltage

A main drawback of timing domain encoding pixels such as PFM and PWM, is that the integration time has to be set long enough so that the counter can capture low-illumination. Techniques to improve the conversion speed is emerged in recent years. For image sensors with column-level A/D converters, global ramp-up reference voltage generators were applied [25, 27]. The block diagram of multiple-ramp single-slope (MRSS) ADC architecture in [27] is presented in Fig.6.1. The A/D conversion is performed by means of a number of comparisons between a dynamic reference signal and the analog input voltage. Measurements demonstrated that the conversion speed of an MRSS ADC is 3.3 times that of a single-slope ADC [27].

In [18], Law *et al.* introduced a global ramp-up reference voltage generator for PWM pixels. By integrating a 4-level reference voltage scheme, the integration time is reduced by 70%. Directly applying this approach to PFM pixels, however, requires the distribution of this global ramp-up reference voltage to all pixel cells, increasing silicon cost and the complexity of routing.

This chapter presents new PFM DPSs with an in-pixel variable reference voltage gener-

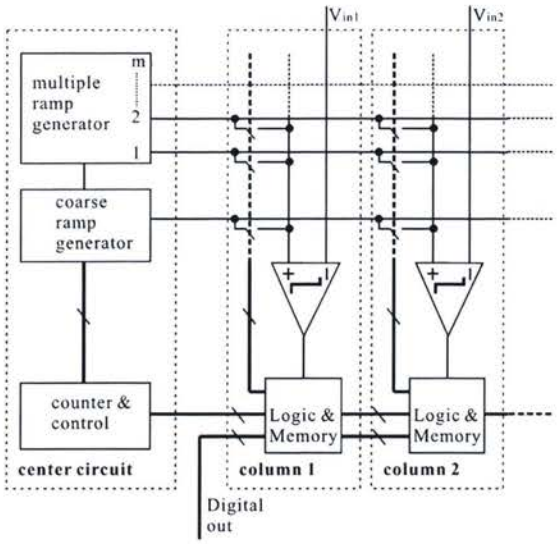



Figure 6.1: Diagram of MRSS ADC architecture [27].

ator to increase the resolution of the pixel, especially when the level of illumination is low. As compared with the PFM DPS proposed in [30] and PWM DPS with global variable references proposed in [18], the proposed PFM DPS offer the following attractive characteristics :

- The integration time can be significantly reduced by ramping up the reference voltage when the level of illumination is low.
- No global ramp-up reference voltage generator is needed. The complexity of routing and silicon consumption are greatly reduced.
- The additional hardware cost of implementing the proposed PFM DPS is only a capacitor and two static inverters.

The fill factor of the proposed PFM DPS is thus comparable to that of the PFM DPS proposed in [30], however, with a significantly improved dynamic range.

The chapter is organized as follows : Section 6.1 describes the proposed PFM DPS. Section 6.2 details the pixel-level implementation. The performance of the proposed PFM pixel is compared with that of the conventional PFM pixel. The dynamic range and integration

time of the proposed PFM DPS and those of conventional PFM DPS are also compared in the section. Section 6.4 concludes the chapter.

## 6.1 Pulse-Frequency-Modulation Digital Pixel Sensors with In-pixel Variable Reference Voltage

For PFM DPS with a constant reference voltage, the relationship between the average photo current of the photodiode, and the number of the pulses at the output of the comparator is presented in (3.10) as

$$N_{pixel} = \frac{T_{int}}{T_{pd}} = \frac{(I_{pd} + I_d)T_{int}}{(V_{dd} - V_{ref})C_{pd}}. \tag{6.1}$$

It is seen from (3.9) and (6.1) that the larger the reference voltage $V_{ref}$, the smaller the pulse width $T_{pd}$, the higher the number of the pulses $N_{pixel}$. Note that the reference voltage must be set to a value lower than the supply voltage. The reference voltage can not be set too high. This is because in high illumination conditions, a high reference voltage will result in reset pulse width that is comparable to the photodiode discharging time, introducing a nonlinear effect [30]. Also, in low illumination conditions, a low reference voltage will result in an over-long discharge time of the photodiode, reducing the dynamic range of the DPS. It becomes evident that a variable reference is desirable as it offers the advantages of a small discharge time in low illumination conditions and reduced nonlinear effect in high illumination conditions.

The configuration of the proposed PFM DPS with in-pixel variable reference generator is shown in Fig.6.2. As compared with the conventional PFM DPS shown in Fig.3.8, the proposed PFM DPS employ a reference capacitor $C_{ref}$ to generate a ramping reference voltage. To see how this image sensor works, assume that the output of the comparator is Logic-0. The reset pMOS transistor is ON and the junction capacitor of the photodiode is charged to $V_{dd}$. The inverter in the reference voltage path forces $M_b$ to turn on to reset $C_{ref}$. The output of the comparator switches to Logic-1 and the reset pMOS transistor switches off. $V_{pd}$ starts to drop due to illumination. The reference capacitor $C_{ref}$ is charged due to

the turn-on of $M_a$. As a result, $V_{ref}$ arises. When $V_{pd} = V_{ref}$, the output of the comparator switches to Logic-0. This process repeats. The timing diagram of this process is shown graphically in Fig.6.3.

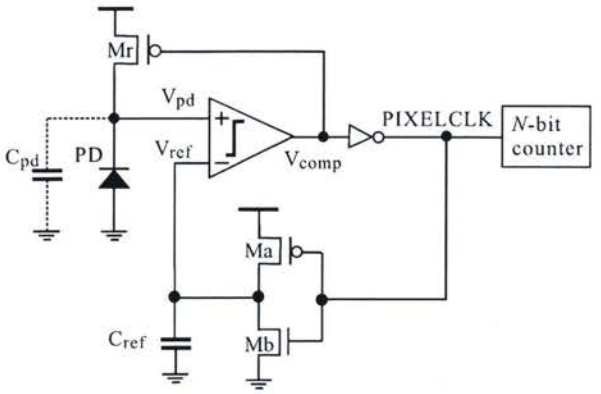
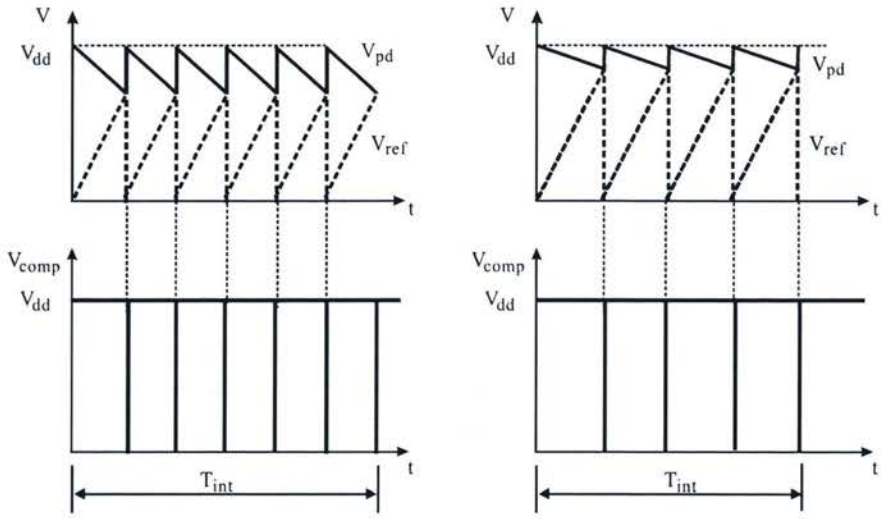



Figure 6.2: PFM digital pixel with in-pixel variable reference voltage.




(a) High level of illumination

(b) Low level of illumination

Figure 6.3: Timing diagram of the proposed PFM DPS with in-pixel variable reference voltage.

It becomes evident that the in-pixel ramping reference voltage will increase the number of pulses at the output of the comparator for a given integration time, specially at low illumination. This increases the dynamic range of the pixel cell. Also note that by varying the value of the reference capacitance $C_{ref}$, the dynamic range of the pixel cell can be changed. This offers the programmability of the dynamic range of the proposed DPS.

## 6.2 Implementation

The schematic of the proposed PFM DPS is shown in Fig.6.4 where the in-pixel counter is omitted for clarity. The transistors width is presented in Table.6.1. The length of transistors is set to $0.18\mu m$, except $L_r = 0.8\mu m$.

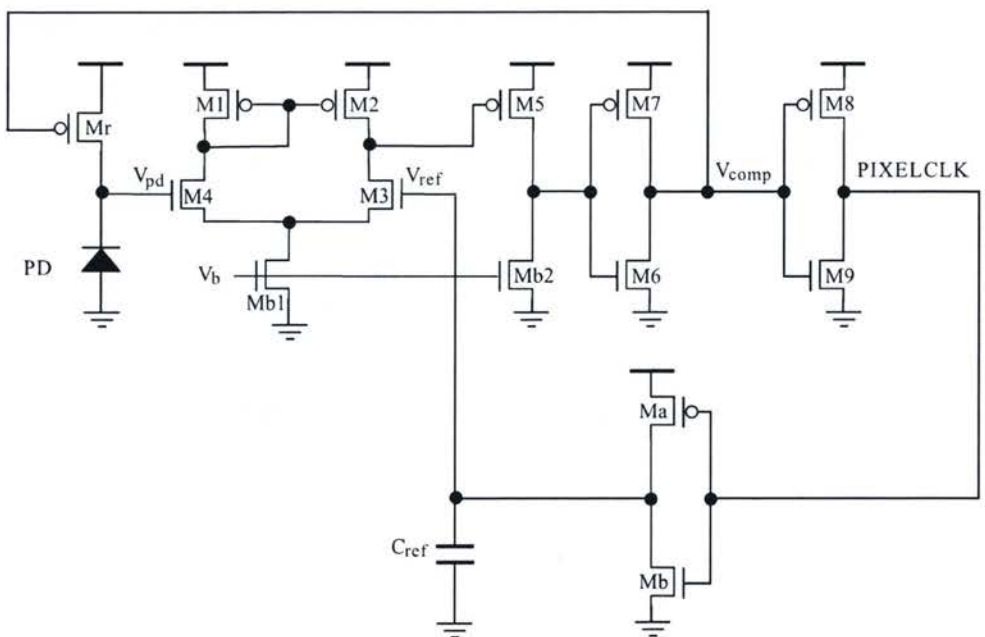



Figure 6.4: Simplified schematic of proposed PFM DPS.

The photodiode is implemented using n+/p-substrate with its dimension $10\mu$m $\times$ $10\mu$m. For the purpose of comparison, the PFM DPS proposed in [30] is also implemented with the same transistor/diode dimensions. Both DPSs are implemented in TSMC-$0.18\mu$m 1.8V CMOS technology and analyzed using Spectre simulator from Cadence Design Systems with

Table 6.1: Transistor width of PFM digital pixel sensors with a variable voltage reference.

| Transistor | Width ($\mu$m) |
|---|---|
| $M_r$ | 0.5 |
| $M_1$ | 2.5 |
| $M_2$ | 2.5 |
| $M_3$ | 1.25 |
| $M_4$ | 1.25 |
| $M_5$ | 5 |
| $M_6$ | 1 |
| $M_7$ | 2 |
| $M_{b1}$ | 2.5 |
| $M_{b2}$ | 2.5 |
| $M_a$ | 0.5 |
| $M_b$ | 0.5 |

BSIM3V3 device models.

The supply voltage is set to 1.2 V, while the reference voltage of the conventional PFM DPS is set to 1.18 V. The bias voltage $V_b$ is set to 0.4 V such that transistors $M_{b1}$ and $M_{b2}$ are biased in the subthreshold region to save the power. The capacitor is selected as 50 fF, considering the pixel size constraint. The photo currents are modeled as an ideal current source. The 10-bit LFSR in Chapter 5 is used here as the counter and the transistors dimensions are not modified.

## 6.3 Simulation Results

Fig.6.5 shows the simulation results of the two PFM DPSs with a low photo current, 1 pA. Because the capacitor $C_{ref}$ is charged to $V_{dd}$, 1.2 V. The comparator of the PFM DPS with a variable reference voltage outputs 4 pulses while the PFM DPS with $V_{ref} = 1.18$V only generates 1 pulse in the given time period of 200 $\mu$s. The pulse width of the proposed PFM DPS is 50.57 $\mu$s whereas that of the PFM DPS with $V_{ref} = 1.18$ V is 159.2 $\mu$s.

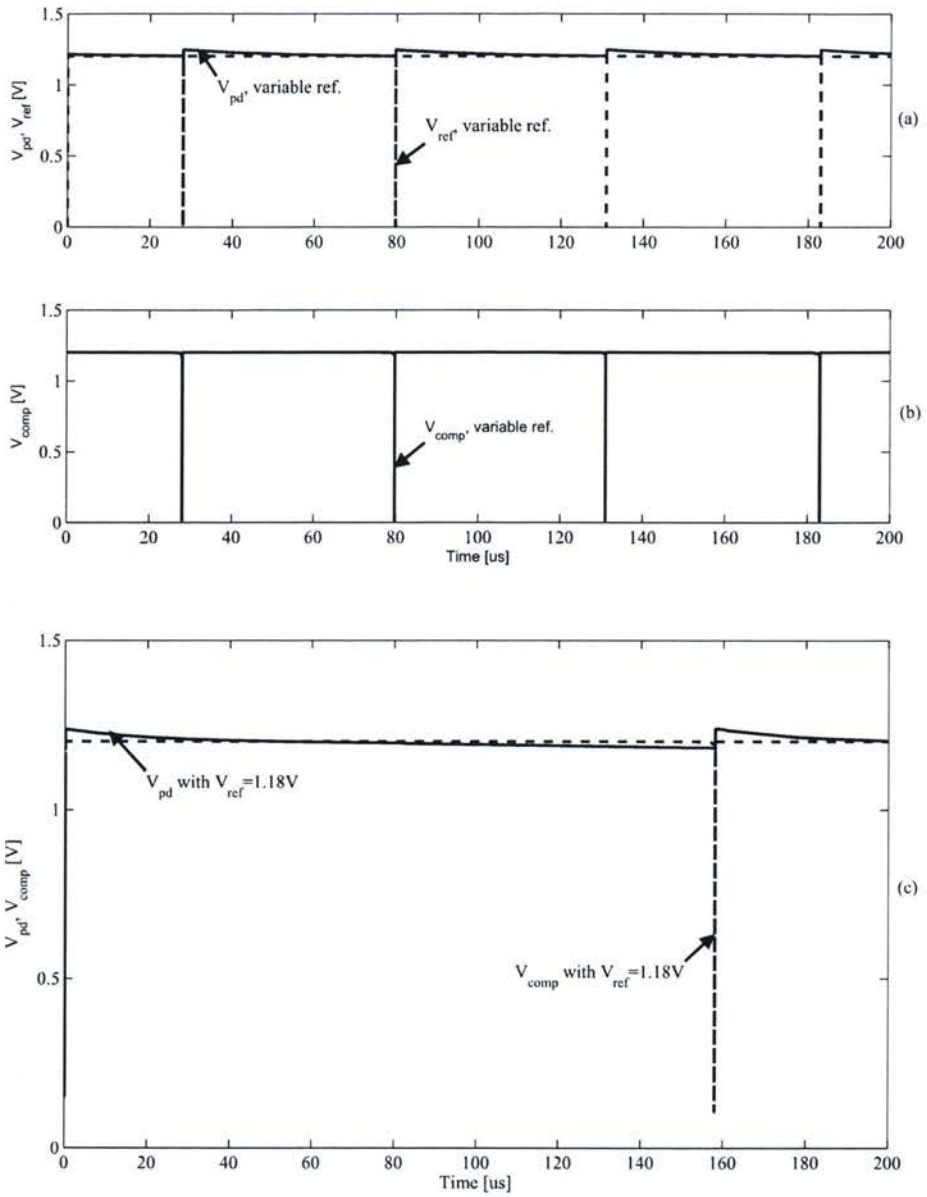



Figure 6.5: Simulation results with 1 pA photodiode current. Figures (a) and (b) show the signals of PFM with a variable reference voltage. Figure (c) shows the signals of PFM with a constant reference voltage.

Fig.6.6 plots the voltages of two PFM DPSs when the diode photo current is 2 $\mu$A. As can be seen that the output of the comparator $V_{comp}$ of the proposed PFM DPS toggles when $V_{ref} = V_{pd}$ whereas that of the PFM DPS with the 1.18 V reference voltage is locked at Logic-0 after the first switch.

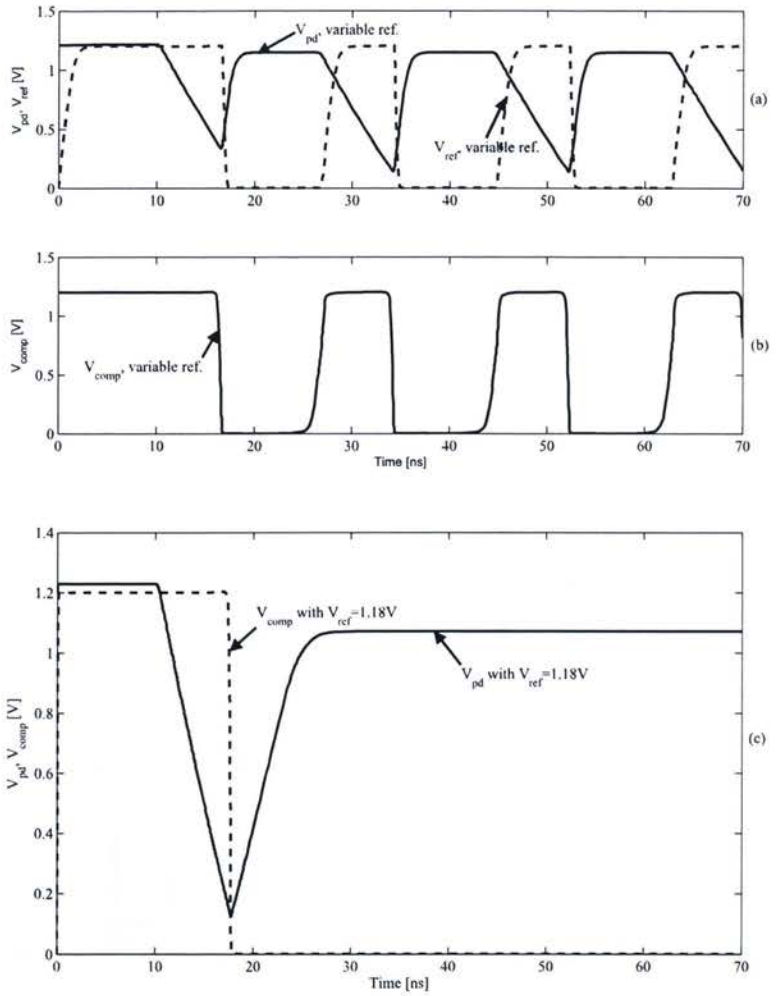



Figure 6.6: Simulation results with a 2$\mu$A photodiode current. Figures (a) and (b) show the signals of PFM with variable reference voltage; Figure (c) shows the signals of PFM with constant reference voltage.

The charging current or reset current of the two PFM DPSs are compared in Figs.6.7 and 6.8.

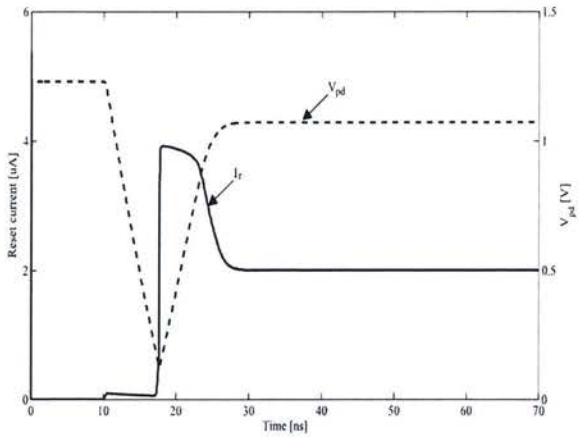



Figure 6.7: Photodiode charging current and $V_{pd}$ of PFM DPS with constant reference voltage.

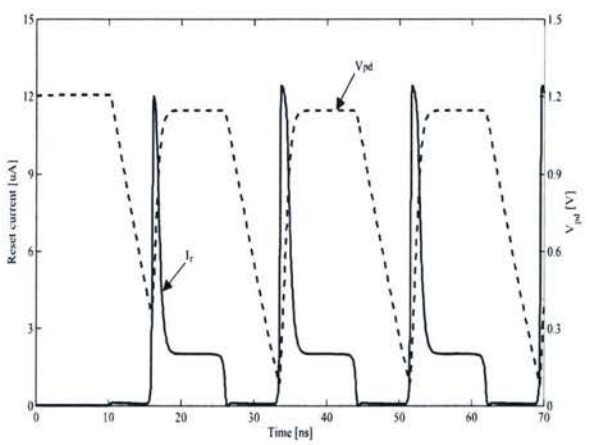



Figure 6.8: Photodiode charging current and $V_{pd}$ of PFM DPS with variable reference voltage.

For the PFM DPS with 1.18V reference voltage, when $V_{pd}$ is charged to 1.15 V, the photo current becomes comparable to the charging current, preventing $V_{pd}$ to rise further. $V_{pd}$, however, is still lower than the reference voltage 1.18 V. As a result, the DPS can not respond to the change of illumination. For the PFM DPS with a variable reference voltage,

$V_{pd}$ will drop to 0.1 V, given the delay time to switch the transistor $M_r$ on and charge the photodiode. As a result, the initial charging current of the photodiode will be larger as compared with that of the PFM DPS with 1.18 V reference voltage. The comparator can switch to Logic-1 when $V_{pd} > V_{ref}$, and the pixel enters the sensing phase again.

The dynamic ranges of two PFM DPSs are compared in Fig.6.9 where the integration time is set to 60 $\mu$s.

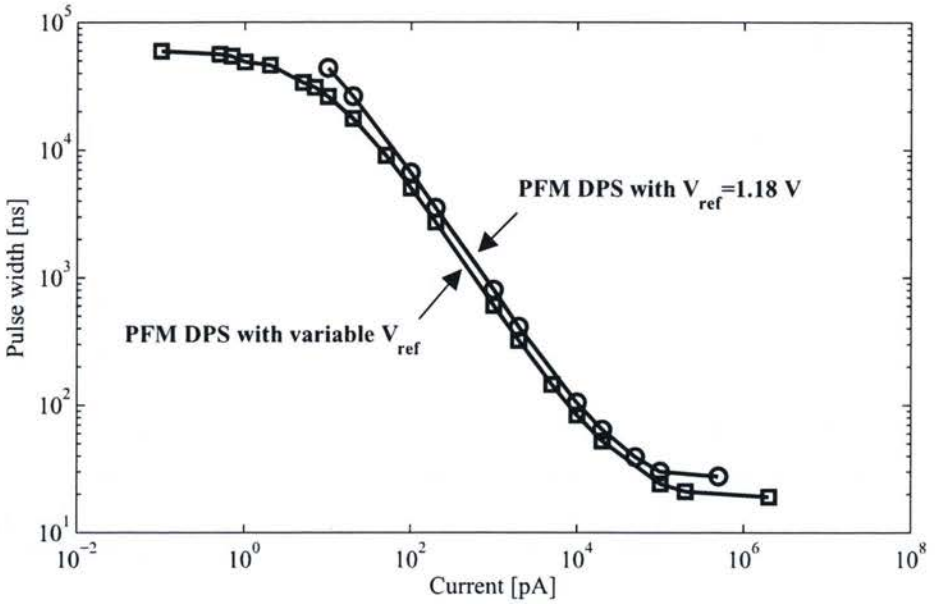



Figure 6.9: Dynamic ranges of proposed PFM DPS and conventional PFM DPS with 60 $\mu$s integration time.

The dynamic range of the proposed PFM DPS is approximately 150 dB whereas that of the conventional PFM DPS is only 77 dB. The maximum detectable photo current of the proposed PFM DPS is 2 $\mu$A whereas that of the conventional PFM DPS is only 700 nA. These results are obtained with the minimum photo current of both DPSs set to 100 fA. It is observed that the conventional PFM DPS fails to produce output pulses when the photo current is less than 10 pA. The proposed PFM DPS, however, continues to produce output pulses when the photo current reaches 100 fA. The response of the proposed DPS becomes flat at both high and low levels of illumination. The former is due to the small photo current

whereas the latter due to the reset delay.

Fig.6.10 presents the comparator output $V_{comp}$ of the PFM DPS with a 10 nA photo current at process corners. The bias voltage $V_b$ is adjusted to ensure that the pulse width remains nearly same. The bias conditions are presented in Table.6.2. The reset phase of FS mode is longer than other conditions, because of the weaker reset pMOS $M_r$.

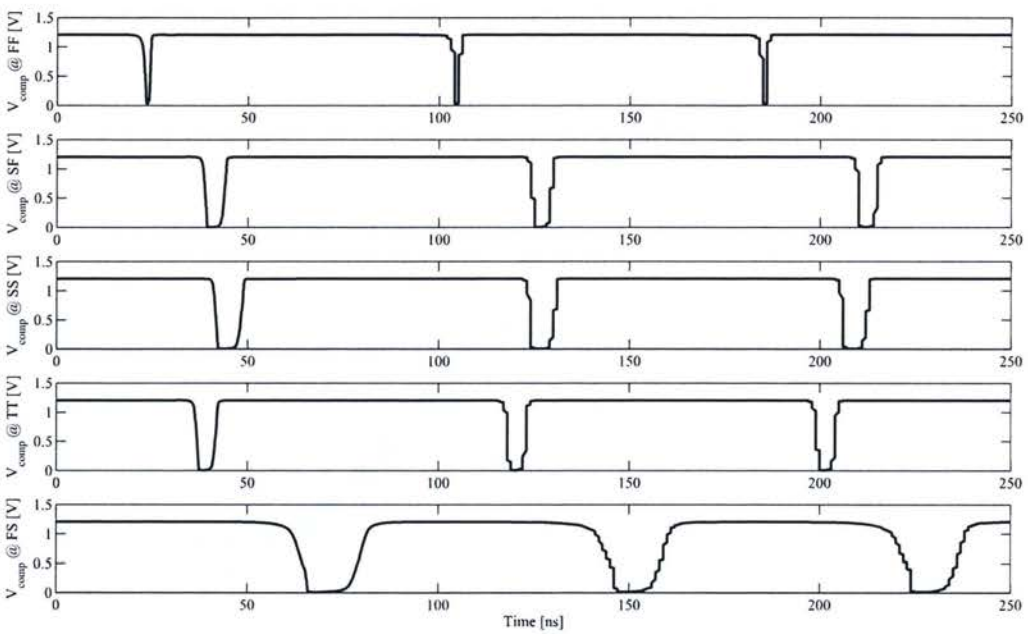



Figure 6.10: PFM DPS with a 10 nA photo current at process corners.

Table 6.2: Bias conditions at process corners..

| Condition | $V_b$ $(V)$ |
|---|---|
| $TT$ | 0.4 |
| $FF$ | 0.35 |
| $SF$ | 0.5 |
| $SS$ | 0.5 |
| $FS$ | 0.24 |

Fig.6.11 is the reference voltage generator with an ideal charging enable signal at process corners. The maximum timing difference is below 0.85 ns, which is acceptable.

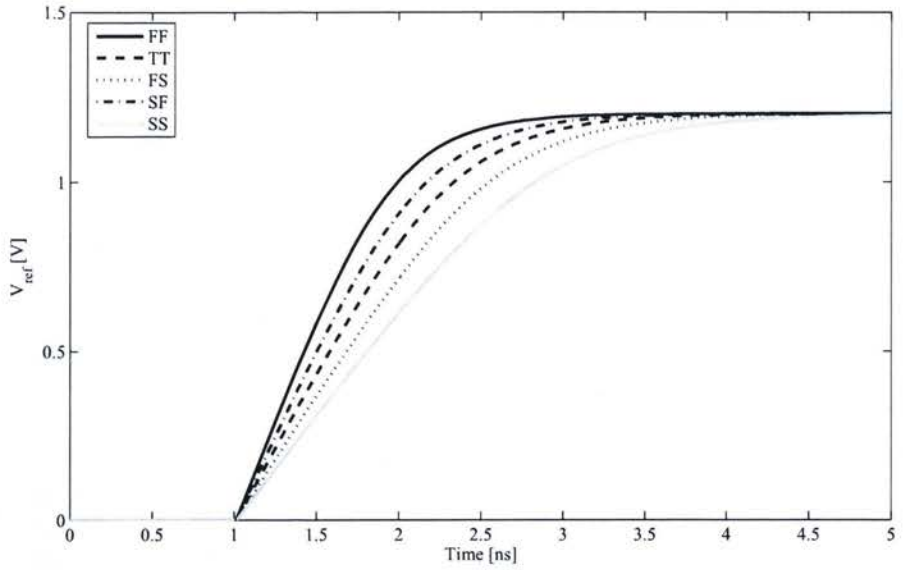



Figure 6.11: In-pixel reference voltage generator at process corners.

The complete layout of the proposed PFM pixel is shown in Fig.6.12. The pixel size as 25 $\mu$m $\times$ 23 $\mu$m, with a fill factor of 20%, which is comparable to the pixel reported in [30]. The capacitor is realized using a MIM capacitor. Various layout techniques are used to reduce digital-analog coupling and crosstalk.

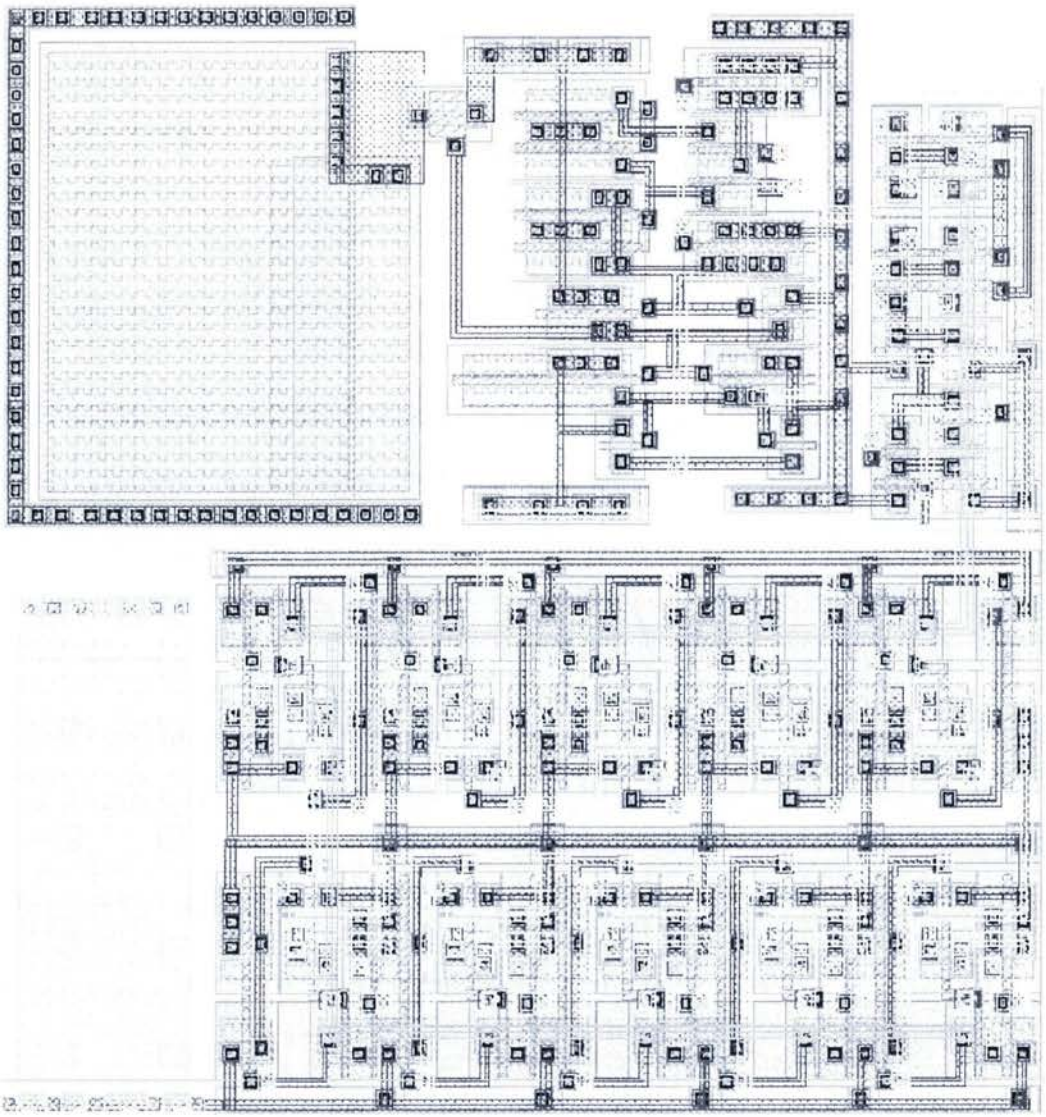


Figure 6.12: Layout of the PFM pixel with a variable reference generator.

Fig.6.13 is the post-layout simulation results with a $2\mu$A photo diode current. The pulse width difference between the schematic simulation (Fig.6.6) and the post-layout simulation is $1ns$, demonstrating the layout is working properly.

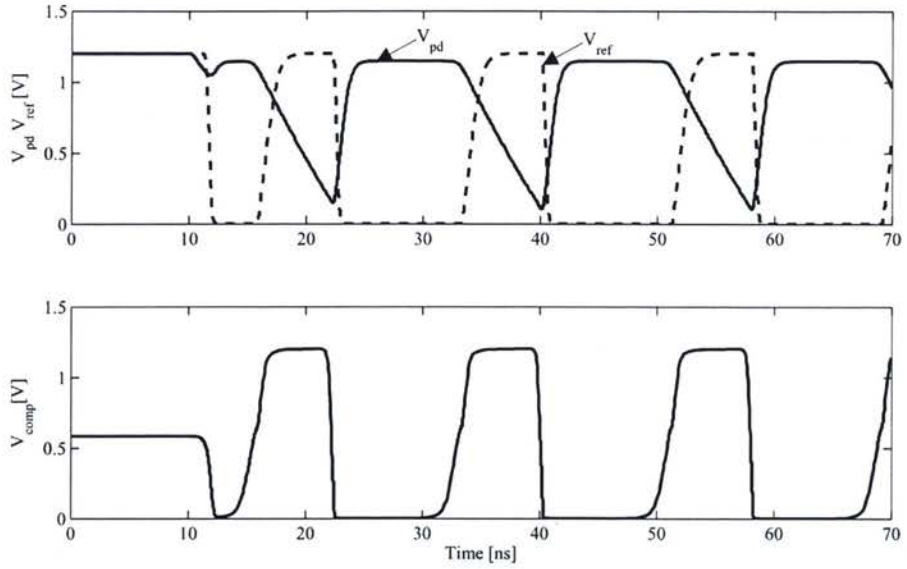



Figure 6.13: Post-Layout Simulation results with a $2\mu$A photo diode current.

## 6.4 Summary

PFM DPSs with an in-pixel variable reference voltage generator have been proposed to increase the resolution of the pixel, especially when the level of illumination is low. It has been shown that the proposed PFM DPSs offer the attractive characteristics of a reduced integration time when the level of illumination is low, reduced complexity of routing and silicon cost, and fill factor comparable to that of conventional PFM DPSs, however, with a significantly improved dynamic range. The proposed digital image sensor has been implemented in TSMC-0.18$\mu$m 1.8V CMOS technology and validated using Spectre with BSIM3V3 device models. Simulation results have demonstrated that the PFM digital pixel has a dynamic range of 150 dB when integration time is set to $60\mu$s, approximately 70 dB more than the conventional PFM digital pixel sensors.

# Chapter 7

# Conclusions and Future Work

## 7.1 Conclusions

Since the inception, CMOS image sensors have won the domain positions in low-end consumer optical products and are challenging CCDs in high resolution markets including digital still cameras and medical imaging applications. With the development of CMOS technologies, the architectures of CMOS image sensors are also evolved from analog passive pixels to pixels with in-pixel A/D conversion. DPSs have several deficiencies, such as a low fill factor/large pixel size, a finite resolution, and a low dynamic range.

In this thesis, CMOS image sensors with in-pixel A/D conversion have been reviewed. PWM and PFM schemes have been analyzed in detailed. One new PWM scheme and two improved PFM architectures have been presented.

2-Stage Memory Write Scheme for PWM Digital Pixel Sensors has been proposed to improve the resolution and the fill factor. The scheme utilizes the characteristics of Gray code counter and partitions a single data write operation into two separated operations such that a portion of pixel embedded memory can be moved out of the pixel to increase the fill factor and reduce the silicon area of the pixel. A prototype with the scheme achieves 12-bit resolution with an improved fill factor. The effectiveness of the proposed DPS is validated with simulation.

New PFM CMOS image sensors with in-pixel amplification have been also proposed. By inserting an amplifier before the comparator, the PFM DPSs reduce the integration time

while improving the dynamic range. Simulation results have demonstrated that the dynamic range of the proposed PFM digital pixel is 20 dB larger than that of corresponding PFM DPS without in-pixel amplification.

Finally PFM DPSs with an in-pixel variable reference voltage generator have been presented. This architecture increases the resolution of the pixel, especially when the level of illumination is low. The proposed PFM DPSs offer the attractive characteristics of a reduced integration time when the level of illumination is low, the reduced complexity of routing and silicon cost, and a fill factor compared to that of conventional PFM DPS, however, with a significantly improved dynamic range. Simulation results demonstrate that the PFM digital pixel has a dynamic range of 150 dB when integration time is set to 60 $\mu$s, approximately 70 dB more than that of the conventional PFM digital pixel sensors.

## 7.2 Future Work

Although these three new proposals improve the DPSs performance from different perspectives, there are still some works to do in future.

- Fabricating these designs are strong desired. In this thesis, the photodetection devices are simulated with the diodes models provided by TSMC, which are not specified for CMOS image sensors designs. Accurate devices models and fabrication will evaluate the design more throughout.

- FPN reduction is critical for CMOS DPSs. Compared with conventional CMOS image sensors, DPSs suffer larger FPN due to the variation of the in-pixel comparators. New architectures should be proposed to reduce this noise into an acceptable level.

# Appendix A

# List of Publications

- Y. Chen, F. Yuan and G. Khan, "A 2-Stage Memory Write Scheme for CMOS Pulse-Width-Modulation Digital Pixel Sensors," *Proc. of IEEE Mid-West Symp. Circuits and Systems*, pp. 125-128, Knoxville, TN, Aug. 2008.

- Y. Chen, F. Yuan and G. Khan, "A New Wide Dynamic Range CMOS Pulse-Frequency-Modulation Digital Image Sensor with In-pixel Variable Reference Voltage," *Proc. of IEEE Mid-West Symp. Circuits and Systems*, pp. 129-132, Knoxville, TN, Aug. 2008.

- Y. Chen, F. Yuan and G. Khan, "A Wide Dynamic Range CMOS Image Sensor with Pulse-Frequency-Modulation and In-pixel Amplification," *Microelectronic Journal.* Submitted in June 2008.

- Y. Chen, F. Yuan and G. Khan, "A Wide Dynamic Range CMOS Digital Image Sensor with Pulse-Frequency-Modulation and in-Pixel Variable Reference Voltage," *Analog Integrated Circuits and Signal Processing.* Submitted in August 2008.

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