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AN INTEGER-N FREQUENCY SYNTHESIZER FOR MEDICAL IMPLANTABLE DEVICES

by

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An Integer-N Frequency Synthesizer for
Medical Implantable Devices

Master of Applied Science, 2009

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Abstract

This thesis proposes an Integer-N frequency synthesizer in TSMC 0.18 μm technology. The design is aimed for MICS(Medical Implantable Communication Services)devices operating at 402-406 MHz. A low phase noise, wide frequency range Quadrature Voltage Controlled Oscillator (QVCO)has been designed and simulated. The simulated phase noise @ 160 KHz offset is -100.3 dBc/Hz with the power consumption of 0.9 mW. This design addresses the small size, low phase noise and low power requirements for the Implantable devices. A wide frequency range Source Coupled Logic (SCL)32/33 prescaler divider has been designed. The Program counter and Swallow counter have been implemented in Verilog-A which allow a division ratio of 2690 from the output of the QVCO. A phase frequency detector based on a modified TSPC D-Flip Flop is designed, which leads to a faster response time. The phase frequency detector, the charge pump, and the loop filter would consume 0.5 mW power. The total power consumption of the synthesizer is at 4.6 mW with 2% steady state settlement time of 160 μs.

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I dedicate this thesis to all who went through several difficult and challenging steps in their lives, but never quit. They are the achievers.

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List of Abbreviations

CP	Charge Pump
DAS	Direct Analog Synthesizer
DDS	Direct Digital Synthesizer
DLL-FS	Delay Locked Loop Frequency Synthesizer
IPG	Implantable Pulse Generator
K_{VCO}	Voltage Controlled Constant
LF	Loop Filter
MICS	Medical Implantable Communication Services
PFD	Phase Frequency Detector
PLL-FS	Phase Locked Loop Frequency Synthesizer
QVCO	Quadrature Voltage Controlled Oscillator
SAW	Surface Acoustic Wave
SCL	Source Coupled Logic
TSPC	True Single Phase Clock
TSMC	Taiwan Semiconductor Manufacturing Company

Chapter 1
Introduction

1.1 Motivation

Since the initial development of implantable cardiac pace makers over thirty years ago, the field of Biomedical Engineering has developed different implantable devices [1]. One of the recent applications of implantable neurostimulation involves the treatment of epilepsy [1]. Intelligent implantable epilepsy devices will likely process multiple channels of data and they may need to transmit these data. These devices not only detect but also predict the seizures [2]. The Vagal Nerve Stimulators (VNS)are the first implantable medical device approved by the FDA for the treatment of epilepsy [2]. These devices decrease the frequency of seizures by an average of 20-30% and with an approximately 10% chance of making the patients seizure free [2]. Figure 1.1 depicts the picture of an Implantable Pulse Generator (IPG).

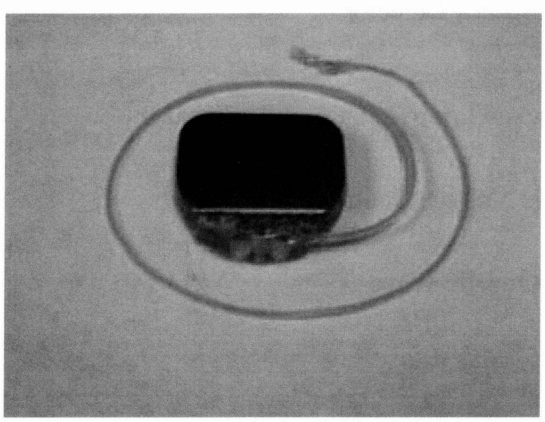


Figure 1.1: Picture of an Implantable Pulse Generator (IPG), lead and electrodes for nerve stimulation [3].

Beside the transceiver and the power source, there are other interfaces such as media access controller for controlling the signals and measurements from the sensors are also operational within the implantable devices.

The application of implantable devices can be extended to the cardiac pacemakers, and implantable defibrillators (ICDs) too. By integrating a small low power transmitter into a pacemaker, larger data records could be downloaded about a patient's heart performance [4].

It is estimated that two-third of the overall mortality form Coronary artery disease comes from sudden cardiac death due to malignant ventricular arrhythmias [1]. Ventricular fibrillation results when the heart rate becomes so fast that the heart simply stops pumping or pumps uncontrollably. It is long been known that a sever electrical shock can stop the fibrillation and allow the heart to resume a normal operation [1].

The implication of tiny, stand alone sensor / transceivers for patient care vary from the profound to the merely convenient [4]. The implanted sensors allow the medical professionals to obtain data from inside a patient's body without having to deal with wires or tubes which penetrate under the skin. This in turn reduces the possibility of infection [4].

Some of the implantable devices work based on inductive coupled link topology. However these systems are rugged and the short range of the magnetic coupling action, combined with the limited data rates and relatively large size of the coils have prompted a wider range of research [5].

These recent devices work at higher frequencies such as MICS 402-405 MHz by utilizing small battery cells. The size, power consumption, and quality of the produced signals have special importance in the implantable ICs. The improvement of frequency synthesizers for wireless MICS applications is a crucial area of research which has come to focus only in recent years. A frequency synthesizer is one of the most critical building blocks in any integrated wireless transceiver system

[6]. Decreasing the size of the synthesizer would be achieved by differential ring oscillators rather than spiral inductors. However obtaining a lower phase noise, lower reference frequency, lower power consumption, and lower price would be the challenges that are being addressed in this thesis.

1.2 Objective

One of the objectives of this thesis is to address the issue of achieving a low phase noise for the QVCO by means of ring oscillators. Ring oscillators would be a good design alternative Since the LC tanks are not going to be used in this topology due to their larger chip area. However the phase noise of the ring oscillator has to be brought down to the acceptable level for the MICS purposes. Having not utilized the LC tanks the size of the designed Integer-N PLL synthesizer decreases dramatically. The biasing of the QVCO should not rely on external circuitry except the feedback control voltage. This constraint is being considered due to the maximum optimization effort in obtaining a smaller size ring oscillator. Also from the power point of view the design should address a low power consumption for the implantable device for the sake of longevity of the implanted battery's life cycle. These objectives can be achieved at the QVCO level by using the current reuse topology offered in this thesis. One of the other objectives of this thesis is providing a larger tuning range for the QVCO and other components of the design which allows them to be suitable for different medical implantable devices. This capability would allow the inter-modularity of the components of the Integer-N synthesizer, such as Prescaler divider, Charge Pump, and Phase Frequency Detector.

1.3 Contributions

The work on this thesis has made the following contributions:

- A small size, low phase noise, and wide frequency range quadrature VCO topology for Medical Implantable Devices(MICS)by utilization of the current reuse technique has been introduced. The smaller size of QVCO also decreases the dimensions of the implantable devices.

- The proposed QVCO has been implemented in an Integer-N frequency synthesizer, which has a small size, low power consumption, and also offers inter-modularity for other Biomedical applications.

- A prescaler divider 32/33 is simulated which is capable of dividing at wider frequency range (from 200 - 827 MHz) that also provides the alternative of utilization for other implantable devices at different frequencies.

A modified design of a True Single Phase Clock (TSPC)D-Flip Flop with a reset signal has been offered in this thesis. This design provides a quick response time, due to not having any feedback circuits, and also benefiting from a low level of power consumption. A modified circuit design of a charge pump (CP) is also introduced which has an impact on decreasing the amount of power consumption of the whole synthesizer. The Proposed Integer-N synthesizer's simulation is offering promising results for industrial implementation. The design has been compared to Zarlink Corporations' Medical Implantable RF transceiver (ZL70101)aspects. The power consumption of the Integer-N synthesizer, inter-modularity of the design, and the small size (by comparing to LC spirals) are some of the advantages of this design. Having a smaller reference frequency also injects a lower level of noise into the synthesizer overall performance. A lower reference crystal oscillator is also inexpensive than the high frequency crystals, and that in turn causes the decrease in the price of the final product.

1.4 Organization

In Chapter 2 review of different synthesizer's architectures are introduced. Direct Analog Synthesizer (DAS), Direct Digital Synthesizer (DDS), Phase-Locked loop Frequency Synthesizer (PLL-FS), Delay –Locked Loop Frequency Synthesizer (DLL-FS), and Multiple Loop PLL Frequency Synthesizer are briefly explained. Also different approaches for creating MICS signals either in the form of direct modulation or synthesizer design are reviewed and compared with the proposed topology of this thesis. Pseudo open loop modulation design, and Surface Acoustic Wave (SAW) resonator synthesizer are also investigated. A topology of an Integer-N synthesizer which is designed to be used for MICS devices has been introduced in this Chapter. In Chapter 3 a new wide range, low phase noise, and low power quadrature Voltage Controlled Oscillator (QVCO)has been proposed. In Chapter 4 the design of a wide range SCL based 32/33 prescaler divider is presented. Chapter 5 consists of three components (a Phase Frequency Detector, a Charge Pump, and a Loop filter). Due to the close operational relations between all of the components (PFD, CP, LF) they all have been presented in one Chapter. A modification of a True Single Phase Clock (TSPC) D-Flip Flop with a reset signal has been introduced in this Chapter along with a slight modification of a charge pump circuit. Close loop and open loop behavior of the full Integer-N synthesizer have been calculated. The thesis is concluded and the future work is addressed in Chapter 6.

Chapter 2
Literature Review

2.1 A Brief over look of Different synthesizers

A frequency synthesizer generates one or many frequencies from one or a few frequency sources [7]. In order to generate a high frequency and stable clock signal, frequency synthesis is necessary [8]. Among many choices, frequency synthesizers using a Phase Locked Loop (PLL)are the most popular in particular for high frequency and low power signal generation [8]. Basically a PLL based synthesizer is a feedback system used to generate a stable clock signal based on a reference frequency [8]. Ideally synthesizer's output is a pure sinusoidal waveforms [7]. Synthesizers can be grouped into five classes:

Direct Analog Synthesizer (DAS)
Direct Digital Synthesizer (DDS)
Phase-Locked loop Frequency Synthesizer (PLL-FS)
Delay –Locked Loop Frequency Synthesizer (DLL-FS)
Multiple Loop PLL Frequency Synthesizer

2.1.1 Direct Analog Synthesizer (DAS)

Direct Analog Synthesizer is designed by cascading stages of different components such as multipliers, dividers, mixers and band-pass filters. Variety of frequencies can be generated from a single reference. Figure 2.1 represents a DAS. In this example the output frequency can be measured as following:

$$F_{out} = F_1 + 0.1F_2 + 0.01F_3 \qquad (2.1.1)$$

Based on the above formula it can be concluded that the F_{out} can be varied with the accuracy of $0.01F_{in}$. This type of synthesizer has higher power consumption [7].

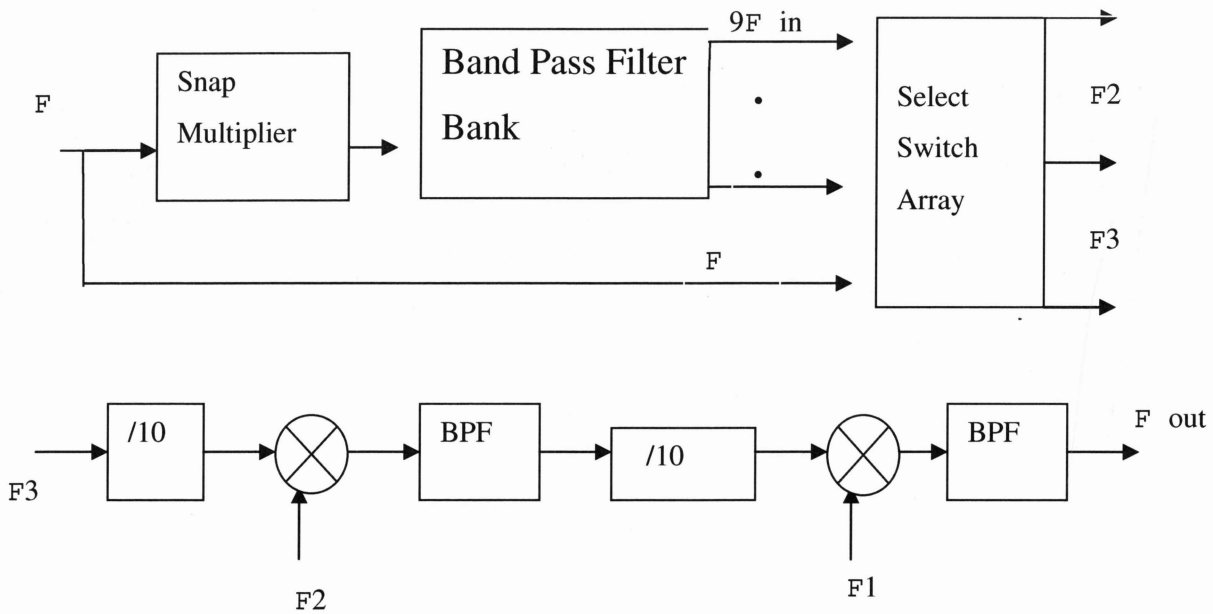


Figure 2.1: Example of a Direct Analog Synthesizer (DAS) [7].

2.1.2 Direct Digital Frequency Synthesizer

This frequency synthesizer is made of two major components, a Numerically Controlled Oscillator and a Digital to Analog Converter. Figure 2.2 depicts this topology. The Numerically Controlled Oscillator consists of an adder register pair (Phase Accumulator)and a ramp to sine wave look up ROM. The output frequency of the DDS is related to the phase accumulator input with the following equation [7],[9]:

$$f_{out} = \frac{K}{2^N} f_{Clock} \qquad (2.1.2)$$

N: Bit length of the accumulator

K: Accumulator's input

The frequency switching speed is faster in this type synthesizer.

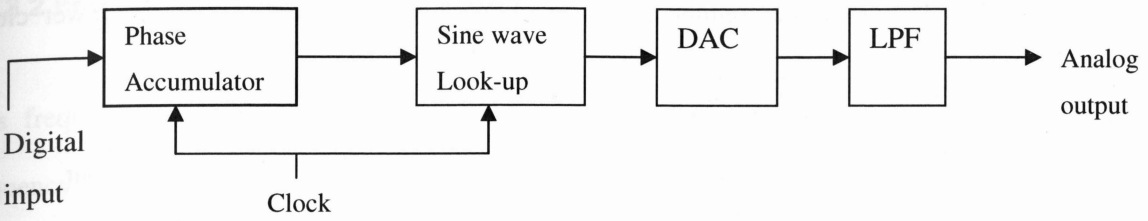


Figure 2.2 : Block diagram of DDS [7].

DDS can only generate frequencies up to half of the clock rate of the digital circuitry [7]. The disadvantage of the Direct Digital Synthesizers is the high spurious content caused by quantization and linearity limitation of the DAC [7],[9].

2.1.3 Phase Locked Loop Frequency Synthesizers

2.1.3.1 Integer - N Frequency Synthesizer

This is the most common type of frequency synthesizer. A PLL is a negative feedback system [7],[9]. It consists of a Voltage Control Oscillator (VCO), a Phase and Frequency Detector (PFD), a Charge Pump (CP), and a loop filter (LF). In fact a PLL will lock both the phase and frequency of the oscillator. Figure 2.3 depicts the PLL's block diagram.

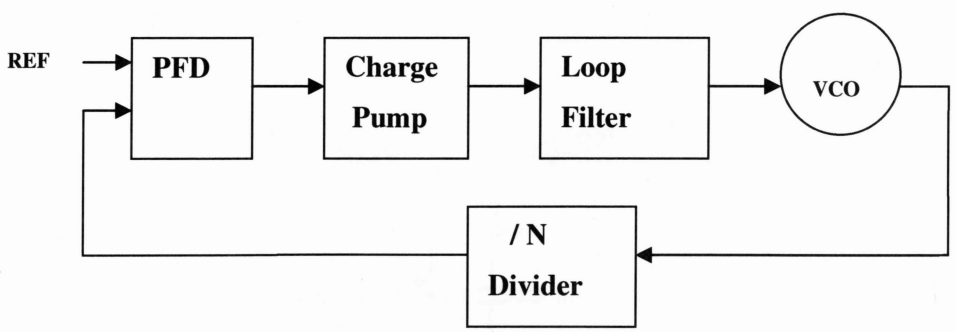


Figure 2.3 : The block diagram of Integer-N PLL synthesizer [7].

In some cases the reference frequency can be divided by a certain factor to a lower clock frequency. Figure 2.4 shows the dividing ratio of Crystal Reference Frequency.

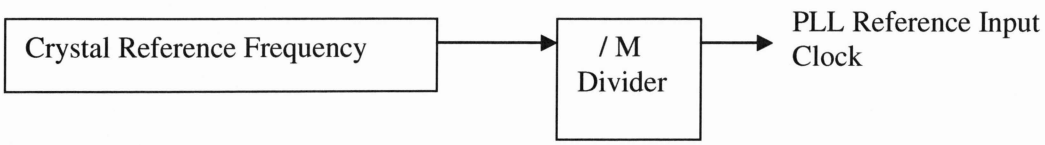


Figure 2.4 : Crystal Reference Frequency divider.

Divider M which is mentioned above is optional. If both dividers N and M are being used the following formula would provide the basic concept for the output frequency [7].

$$F_{VCO} = F_{REF} \frac{N}{M} \tag{2.1.3}$$

The phase frequency detector compares the divided output frequency of the VCO by the reference input Clock frequency and also tries to adjust the phases of the two signals by implementing the difference into the charge pump. The charge pump will deliver a current (I_{cp}) to the loop filter. The output of the loop filter would be the control voltage. In fact the PFD produces up and down signals to drive the charge pump to drive up or drive down the loop filter. These two signals are generated by the phase and frequency error of the PFD inputs. Figure 2.5 depicts the second order loop filter.

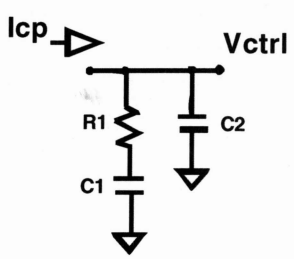


Figure 2.5 : Second order loop filter.

2.1.3.2 Fractional-N Frequency Synthesizer

This frequency synthesizer would allow fractional division ratios and therefore the reference frequency can be much larger than the frequency steps of the channel spacing. The output frequency can be represented as following [7]:

$$F_{output} = NF \times (N+1)F \tag{2.1.4}$$

N, N+1 : Integer division ratios

F: A fraction number between 0 and 1

Figure 2.6 depicts the block diagram of the Fractional-N frequency synthesizer.

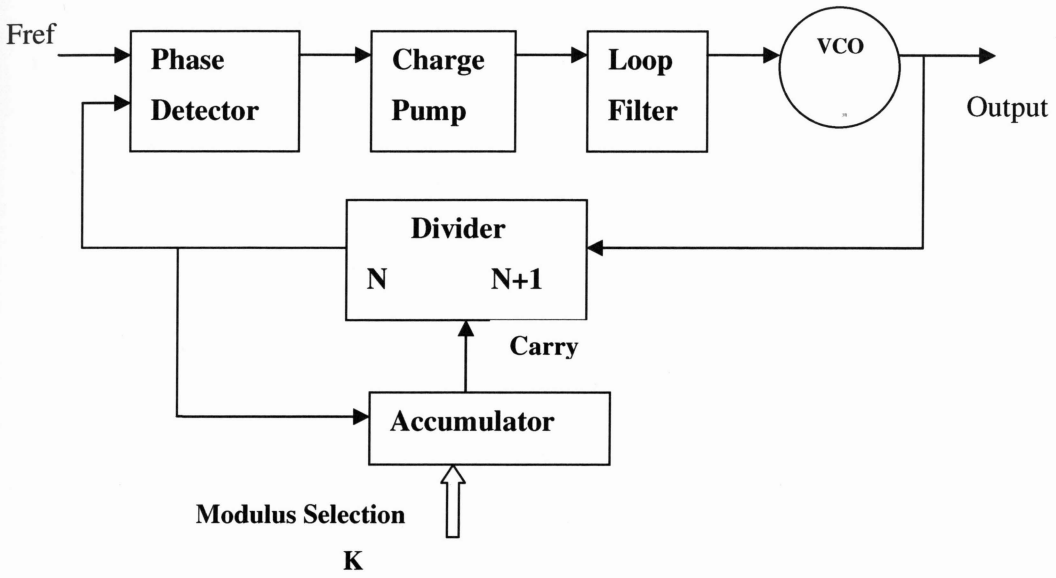


Figure 2.6: Fractional-N frequency synthesizer [7].

The two division ratios (N, N+1)would be altered from one to another to create a decimal average ratio. This phenomena helps to lower the division ratio and results in an increase in the reference frequency. In return the PLL loop bandwidth also increases. The implication of this method generates a faster response time and also an improvement on the PLL phase noise since the total division ratio decreases. However the main disadvantage of fractional-N synthesizer is the

introduction of the spurs [7]. The spurs are generated due to instantaneous switching of the feed back division ratios. Another disadvantage of the Fractional-N synthesizers is that since the reference frequency is larger therefore the complexity and the power consumption of the accumulator will increase [7].

2.1.3.3 Sigma – Delta Fractional - N Synthesizer

As it has been indicated in the above section the issue of spurs can be resolved by using Σ- Δ modulator. The modulator generates a binary stream representing a defined average value [10]. Figure 2.7 depicts the Σ-Δ modulator.

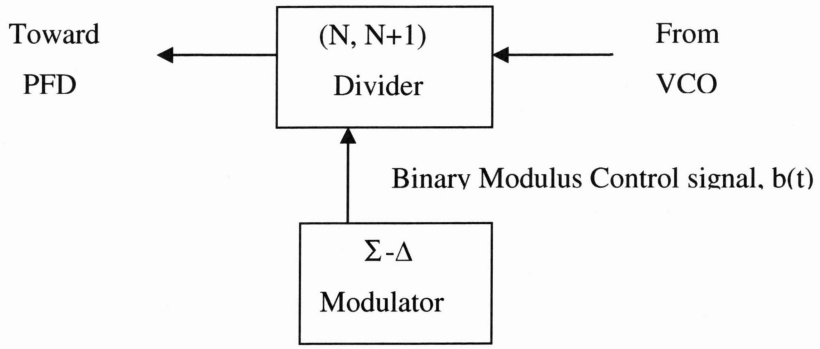


Figure 2.7 : Noise shaping with Σ-Δ modulator [10].

The Binary Modulus Control Signal (BMCS)is also indicated as b(t). Therefore the instantaneous division ratio would be indicated as N + b(t). Where b(t) is a value between 0 or 1.

2.1.4 DLL- based Frequency Synthesizer

Figure 2.8 represents the Block diagram of DLL-FS. However DLL-FS isn't programmable and also suffers from high power consumption [7]. Other problems such as limited multiplication factor also

limit the applications of DLL-FS. In Figure 2.8 the Voltage Controlled Delay Line is made up of cascade of identical gain stages with variable delays. This design utilizes multiple input frequencies which is performed by an edge combiner. The reference signal determines the next transition point signal. These types of systems have a superior jitter performance [11].

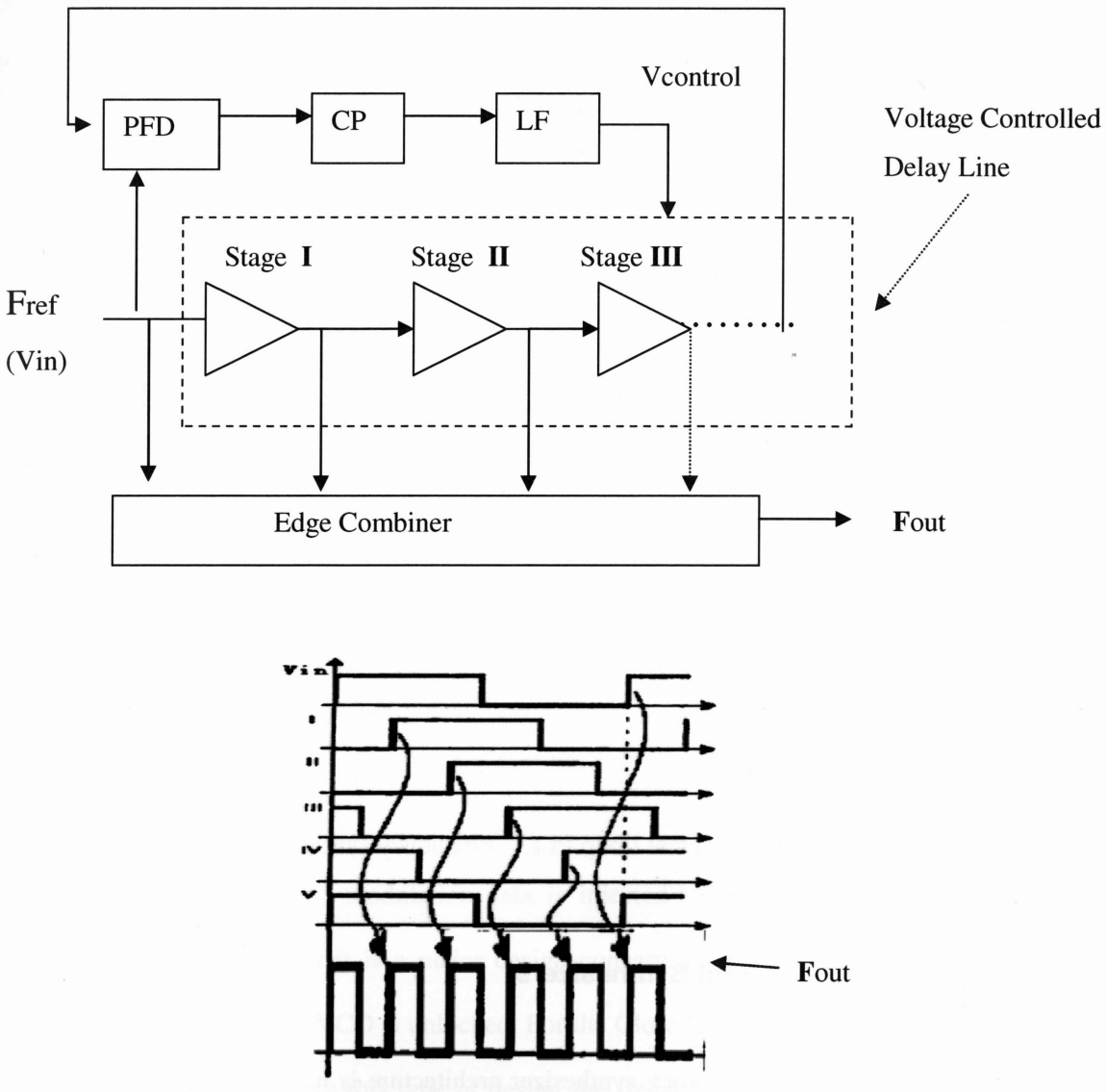


Figure 2.8 : Block Diagram of DLL-FS.

2.1.5 Multi Loop PLL Frequency Synthesizer

In an Integer-N PLL synthesizer to reduce the division ratio utilization of multiple loops would be an improvement to the design. There are different types of Multi loop PLL frequency synthesizers. Figure 2.9 represents two different types of Dual loop synthesizers. In Figure 2.9(a)output of PLL1 is being used as input to a mixer that up converts the PLL2 and PLL1's signals. PLL 1 generates tunable IF frequencies while PLL2 generates a fixed RF frequency. In Figure 2.8(b)the output of PLL1 is considered the reference frequency for PLL2.

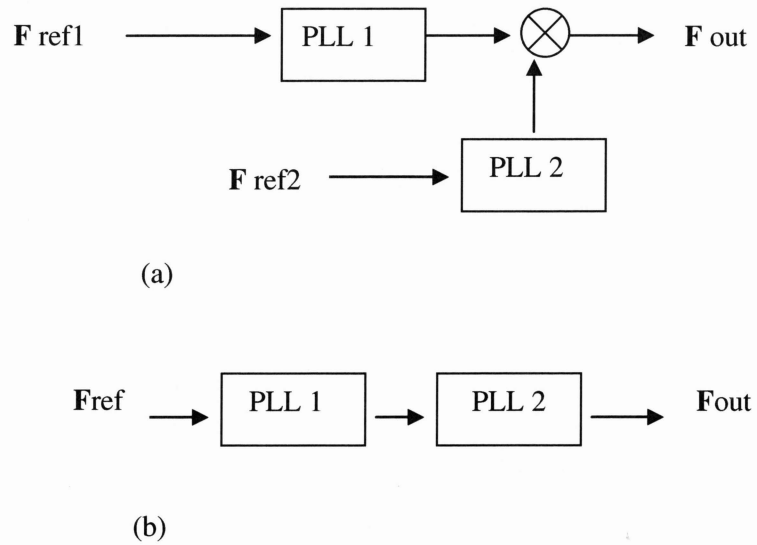


Figure 2.9 : Dual Loop PLL – Frequency synthesizers[7].

2.1.6 Comparison of different Synthesizers

In industry the widely used frequency synthesizer architecture is based on PLL design. Since PLL design can be integrated easily and it consumes a reasonable lower power consumption [7]. Direct Analog Synthesizers may find some applications at microwave frequencies, where very high

frequencies needed to be generated. Direct Digital synthesis is used where frequency switching time is very short; such as frequency Hopping Spread Spectrum systems [7]. Table 2.1 shows a comparison amongst the frequency synthesizer architectures.

Table 2.1 : Comparison of frequency synthesizers [7].

Architecture	Pros	Cons
Direct Analog Synthesizer	Fast Switching, low noise spurs	Huge size and Power consumption
Direct Digital Synthesizer	Fast switching, fine resolution	Huge size and Power consumption
Integer-N Synthesizer	Low power, low noise	Slow switching
Fractional-N Synthesizer	Relatively faster Switching	Huge fractional spurs
Delay Locked Loop	Very low phase noise	Non-programmable , huge power consumption

2.2 Different modulation and synthesizer schemes for MICS devices

2.2.1 Pseudo-open loop direct modulation

There are two major types of direct modulation transmitters.

1) Open loop topology

2) Closed loop topology

In the open loop topology the modulation data is injected to control the VCO directly [12]. However, the VCO frequency drift is a major design concern since the modulation is performed while the PLL is opened and the VCO is unlocked. For the Closed loop topology modulation is done while the PLL's loop is closed. In this type of design the frequency drift is avoided but the signal bandwidth is constrained by the PLL bandwidth [12].

In [13] a new open-loop direct modulation transmitter has been proposed for Medical implantable devices. Figure 2.10 depicts the block diagram of a Pseudo-open loop architecture.

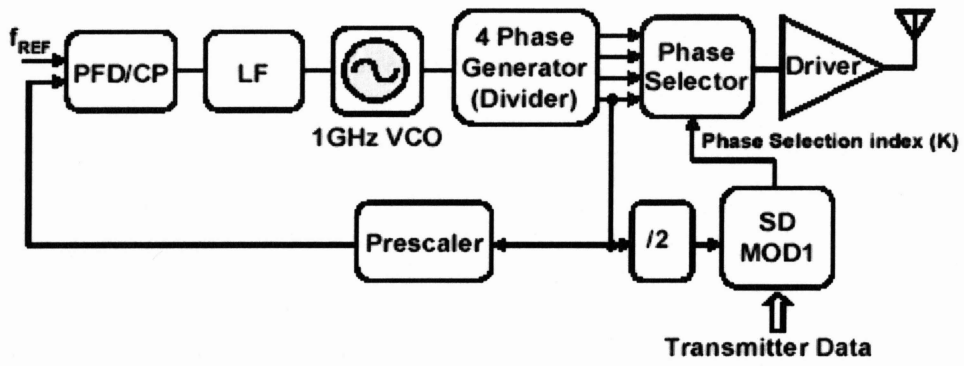


Figure 2.10 : Pseudo-open loop direct modulation transmitter[13].

The PLL remains locked to produce stable four phase signals. These multi-phase signals are utilized to generate modulated output through edge combining operation. The edge combining is performed through a proposed phase selector circuit, which is essentially a fractional divider with the divide ratio of 1+K/4 and K = 0 or 1. As the transmission data is applied to the Sigma-Delta modulator (SD-MOD1) a randomized bit stream is generated to dither the phase selector [13]. If the selection index K is 1 the phase selector selects the 4 phases sequentially to the output and equivalently divides the input frequency by 1.25. For K = 0 the selected phase is fixed and the output and input frequencies are the same. The Clock for the SD-MOD1 is being produced by dividing one of the four phase signals by 2. Total implantable transceiver runs on 12.75 mW power consumption [13]. However as it was indicated earlier due to presence of SD-MOD 1 the noise spurs contribute to a lower phase noise in this design. The LC spiral 1GHz VCO takes a larger space than ring oscillators. The complexity of the design is also another issue that should be addressed.

The proposed design in this thesis would address the phase noise problem of the entire PLL Integer-N on bases of producing low phase noise and having a lower reference frequency. By

utilizing a ring oscillator also the size of the total design would decrease dramatically. The complexity of the design will also decrease as the Integer-N PLL has less complex circuitry.

2.2.2 Surface Acoustic Wave Synthesizer

The design of a Surface Acoustic Wave (SAW) synthesizer is depicted in conjunction with the Medical implantable transmitter in Figure 2.11. This approach has been proposed in [14].

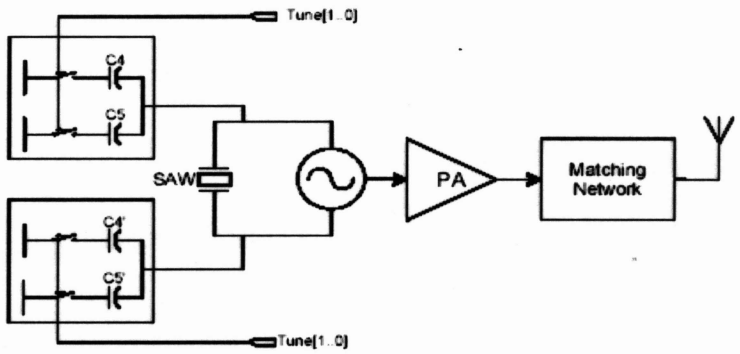


Figure 2.11 : Block diagram of the transmitter[14].

The advantage of using a resonator (SAW Resonator) is to avoid frequency division, thus reducing the power consumption. SAW ceramic resonators allow for frequency divisions of tens of kilo Hertz [14]. As shown in Figure 2.12 the frequency modulation is performed with the tune signal that switches the capacitances (C4,C5) and (C4',C5')of the SAW resonator that are added in parallel to C1 and C2 (depicted in Figure 2.11) by shifting the reactance of the loop and thus causing the resonance frequency to change.

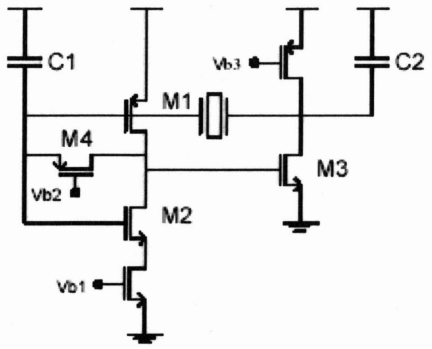


Figure 2.12 : Proposed oscillators for SAW synthesizer[14].

The phase noise of oscillator is very low due to high signal swings which avoid loading the resonator. However this design is tunable from 403.15MHz to 403.494 MHz. The power consumption of this design has been low while it only produces a differential signal rather than quadrature signals.

The proposed topology of this thesis QVCO allows a wider frequency range with a reasonable power consumption while trying to keep the phase noise at a low level.

2.2.3 Four Stage differential ring QVCO

As an alternative to the LC spiral, a ring oscillator topology is being offered in [15] which produces quadrature signals. Figure 2.13 shows the topology for MICS application. Since the phase noise of the MICS devices is relatively relaxed therefore a ring oscillator would be a good choice to be used in this devices. There are no extra steps required to generate quadrature outputs by this method.

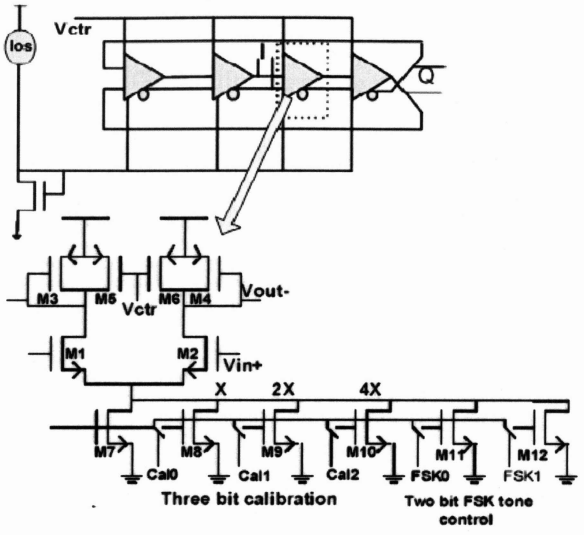


Figure 2.13 : Design of a QVCO for MICS [15].

In this design a four stage differential VCO was optimized to obtain a low phase noise quadrature signal [15]. Every delay cell has a three bit calibration control and a two bit FSK control signals. These two bit FSK data turn long channel devices M11 and M12 on and off [15]. This causes a slight amount of change in the sink current. To compensate this change the calibration control bits are introduced to keep the current at a constant level.

This topology produces the MICS frequency range signal with the measured phase noise of -82 dBc/Hz @160 KHz offset and the power consumption of 1 mW.

The proposed topology of the QVCO in this thesis meets the challenges of the power consumption, size and phase noise requirements which have been addressed by the design in [15]. The QVCO in this thesis produces a lower phase noise and slightly lower power consumption.

2.3 The proposed design of Integer-N Synthesizer

The design of the proposed Integer-N frequency synthesizer has been depicted in Figure 2.14.

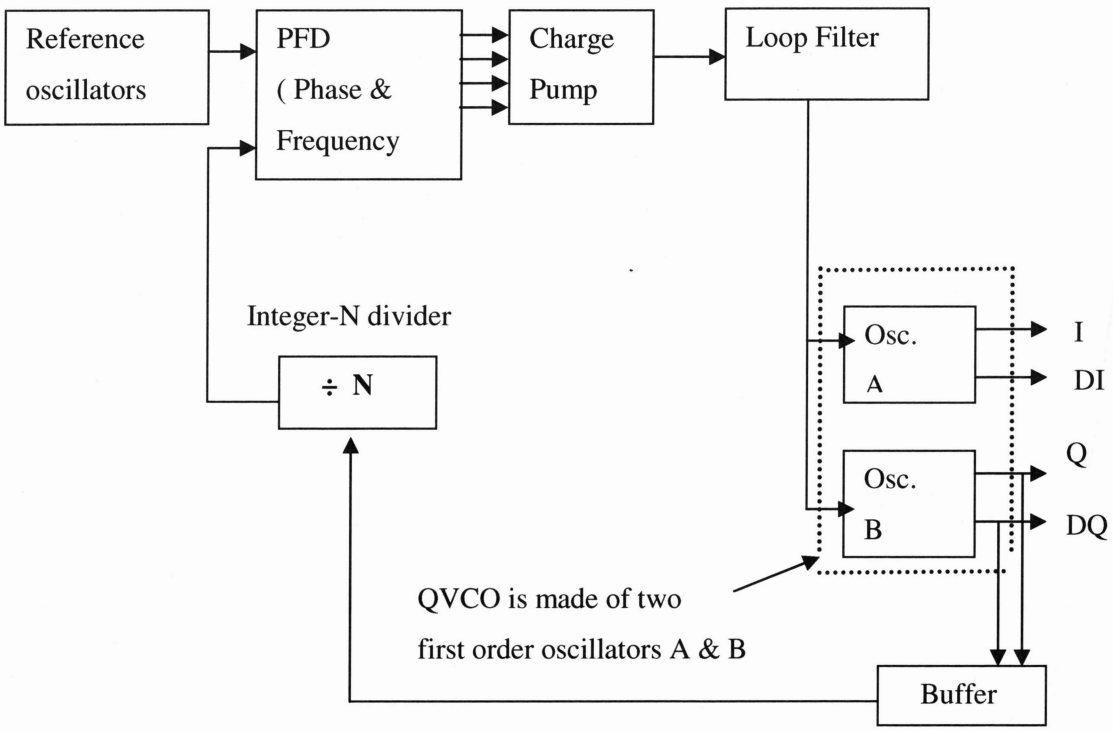


Figure 2.14 : Block diagram of an Integer-N , Phase Locked Loop synthesizer.

In this topology the QVCO is made of two first order oscillators(A & B). Two of the outputs (D , DQ)are going to be buffered and converted to the clock signals which will be fed to the Integer-N divider. This topology has a lower complexity, smaller size, wide tuning range, and the offered QVCO's phase noise is at a low level which is far beyond the MICS acceptable standard. Phase Frequency Detector compares the result of the divider circuit with a reference clock. The phase and frequency difference will be converted to pulse width and it gets converted to current by the Charge Pump. The loop filter produces control voltage from the charge pump current and tunes the QVCO's output frequency. In this topology since the QVCO is based on ring oscillator therefore there should

be a special consideration regarding lowering the phase noise of the QVCO. The divider is the Mixed-mode part of the topology. Generally speaking the divider is programmable for integer division ratios. The output signal from the divider is operating at a lower frequency and it will be compared to a reference(Crystal oscillator) of 150 KHz. The Phase Frequency Detector behaves as an error detector to sense the phase and frequency error between the reference clock signal and the divider output signal. Four output signals are being generated from the PFD and they can be the controlling signals in determining whether the current from the charge pump is being on or off at the time of operation. The control voltage of the QVCO is dynamically adjusted by the charge pump and the loop filter until the system is locked. The loop filter is also acting as a low pass filter in converting the output current of the charge pump to the control voltage of the QVCO. The loop filter is also a contributing factor in taking some of the noise from the control voltage in generating a more accurate signal. The output signal can be varied by Integer-N divider. As it has been shown in the previous sections different architectures can fulfill different requirements and thus can be more suitable for different applications. However in this case since the chip area, power consumption, and operational range have been some of the design constraints therefore Integer-N topology can be more suitable to meet the desired constraints. This topology also offers a less complexity and therefore a better power consumption.

Chapter 3

Design of a QVCO for the Integer – N, PLL Synthesizer

3.1 Analysis of the proposed QVCO

This design is based on In-phase coupling method for quadrature signal generation. In-Phase coupling design has been proposed by [16]. In fact the proposed topology is made of two first order oscillators. The mutual coupling mechanism has been used when the desired specifications can only be reached by a good cooperation between the two timing references. In this approach a coupled system of two equal oscillators yields a better noise performance than each of the two free-running oscillators individually [16]. Figure 3.1 depicts the design of the QVCO.

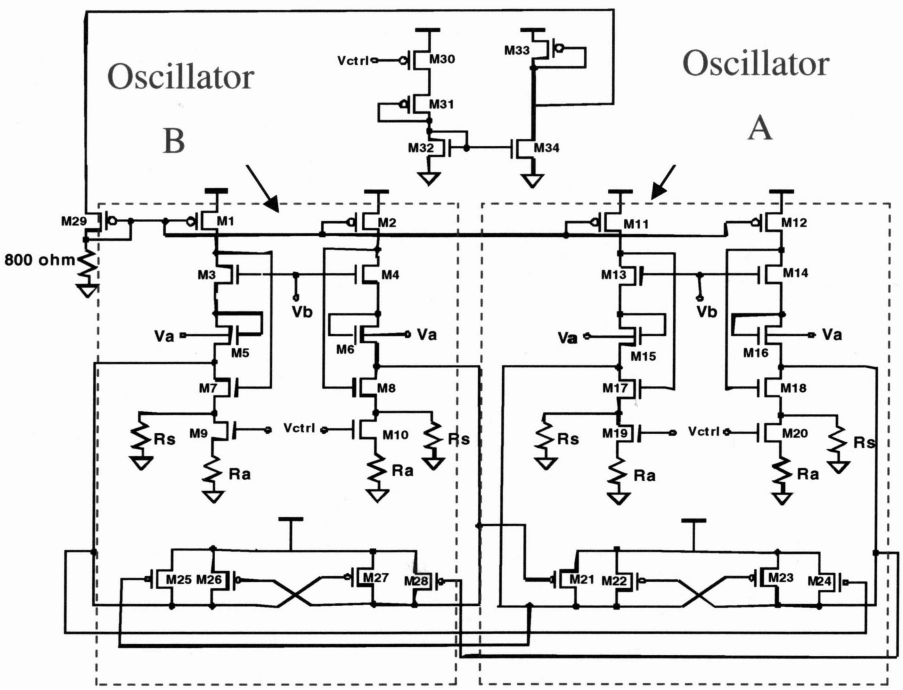


Figure 3.1 : Proposed QVCO.

A first order oscillator can be used to create large tuning range. In Figure 3.1 the output of the oscillator is fed to a frequency divider which in turn divides the output frequency. This signal is then

being passed into the Phase Frequency Detector(PFD)where the phase and frequency is being compared to a reference signal. The output of PFD is led to the tuning input of the oscillator via a charge pump and a low pass loop filter.

The QVCO's coupled system consists of two oscillators A and B running at the same frequency. In Figure 3.1 transistors M25 and M28 are the coupling transistors in parallel to the switching transistors M26 and M27. On the second oscillator transistors M21 and M24 are the coupling transistors while transistors M22 and M23 are the switching transistors. In this setting when one of the oscillators crosses a predefined reference level its output voltage initiates a transition in the other oscillator. Figure 3.2 depicts the different parts of the QVCO.

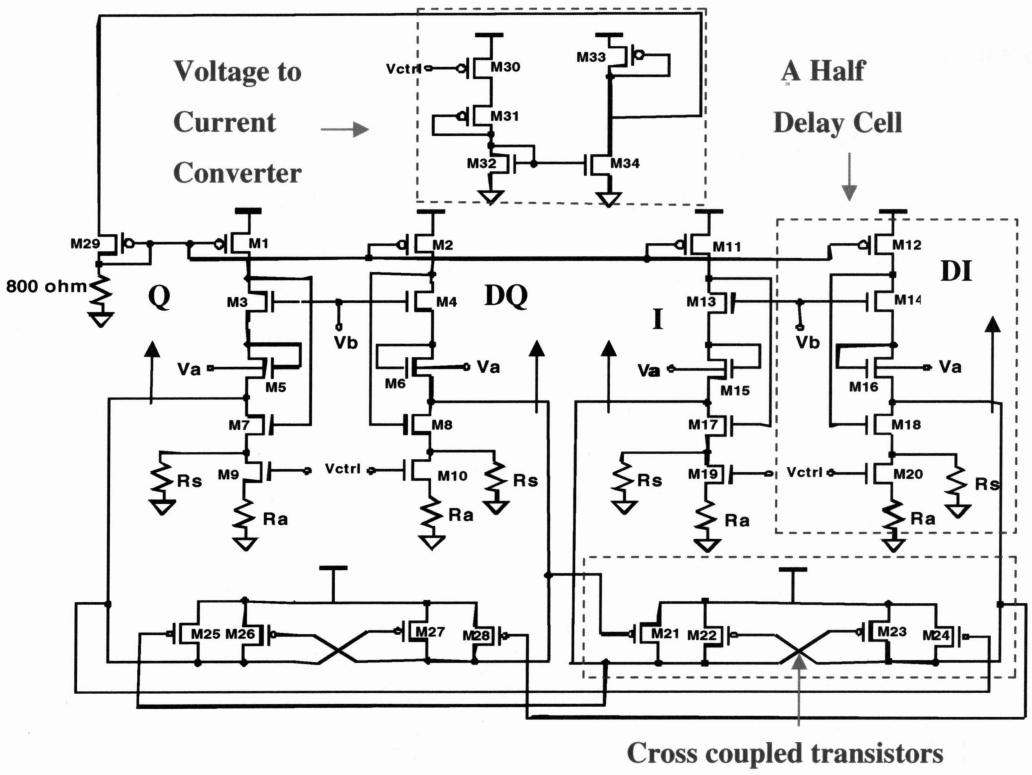


Figure 3.2 : The block representation of the components of the QVCO.

A technique that can be used to improve the phase noise behavior of first order oscillators is called In-Phase Coupling [16]. The coupling transistors contribute to the quadrature phase operations of the

oscillator. The operation of QVCO is divided into four phases in one oscillation period. In phase 1 transistors M22, and M24 are on. In phase 2 transistors M23, and M24 are operational. In phase three and four transistor sets of M21, M23 and transistors M21,M22 are operational, respectively.

In Figure 3.2 the voltage to current converter provides a slightly adjustable current for each delay cells. The converter utilizes the current mirror transistors M32, and M34 to generate the output current from transistor M30 and the diode connected transistor M31.

At the top of each delay cells the presence of the second current mirrors (transistors M29 - M1 , transistors M29-M2, transistor M29-M11, transistors M29-M12)contribute to creation of the driving currents of each delay cell. This design gives the advantage of having slight control over the changes of the reference current of each delay cell at low and high frequencies. In this approach due to the current mirrors the circuit would be less susceptible to noise.

The basic component of each half delay cell has been made of a Common Gate (CG) stage on top of a Common Source Degenerated (CSD). Figures 3.3 depict these ideas.

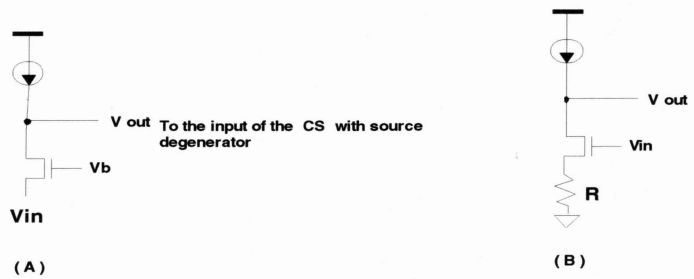


Figure 3.3 : (A) A Common Gate(CG)stage,
(B) A Common Source Degenerated(CSD)stage.

Figure 3.4 represents how the Common Gate(CG)current is being reused by the Common Source Degenerated(CSD)circuits. Utilization of the current reuse topology also contributes to a lower phase noise for the QVCO. Figure 3.5 represents the schematics of a half delay cell. In fact the

output of the CG circuit would be the input to the CSD circuits. By "Stacking" the two types of circuits (CG on top of CSDs circuits) the current would be shared amongst the two components of CG and CSDs. Figure 3.6 (A) & (B)also shows the intrinsic capacitances of each components of a delay cell. The Common Gate transistor (M1)is acting like resistive load and indicated as RD. The symmetry of the oscillation outputs of each half circuit which are achieved by linear resistive loads also contribute to a lower phase noise [16]. Transistor M5 acts as a diode connection to provide a constant current (indicated by "b" in Figure 3.6 (B)). The introduction of the bias voltage of "Va" that is equal to -1.8V to the bulk of the transistor M5 would create the "body effect" which causes the increase in the channel length modulation. This voltage is also optional in the design which can otherwise be grounded. This phenomenon provides a slight improvement in the phase noise of the QVCO. The bias voltage of "Vb" has been set to be at the constant voltage of 1.8 Volts. In fact in this design by feeding the output voltage of the CG to the input of the CSD1 the need for another bias voltage has been diminished.

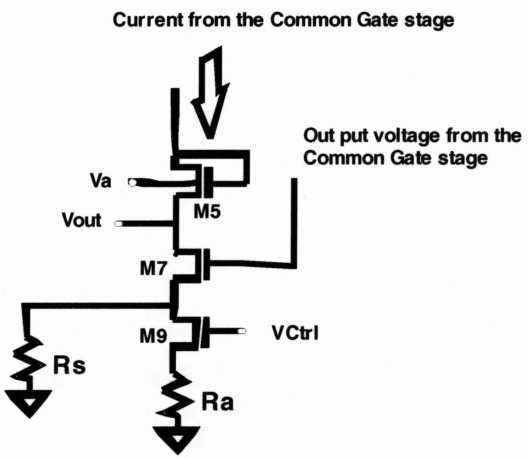


Figure 3.4: Representation of the current stacking.

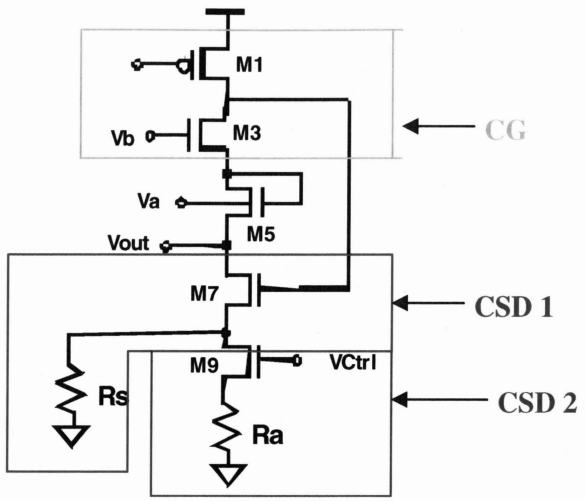


Figure 3.5 : The schematic dissection of a half-delay cell.

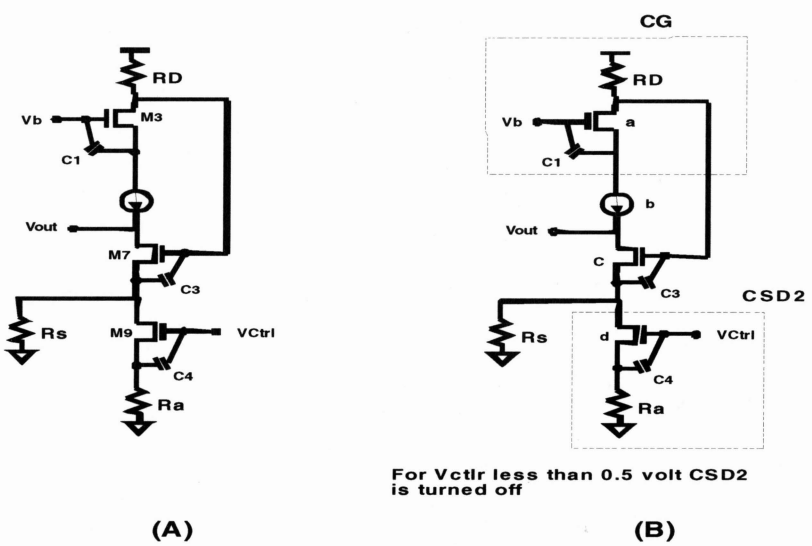


Figure 3.6 : (A) The schematics depiction of the Capacitors.
(B) The Block diagram of the delay components.

For Vctrl of less than 0.5 Volt the CSD2 is turned off and only CSD1 is operational. The conception of such a circuit is shown in Figure 3.7. In Figure 3.6(B)For ease of mathematical expressions; transistors M3, M5, M7, and M9 are named as transistors "a", "b", "c", and "d" respectively.

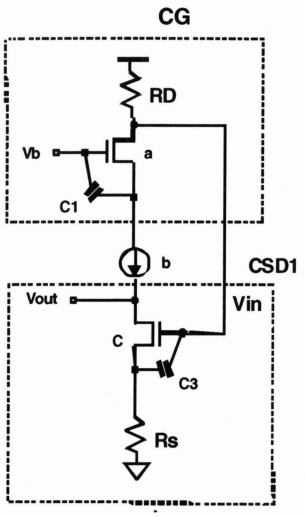


Figure 3.7 : The operation of the delay cell for Vctrl under 0.5 volt.

In Figure 3.8 the delay cell is being represented while the Vctrl is above 0.5 volt. In this case transistor "d" is being turned on and the topology of the circuit changes and CSD2 becomes operational. However since the value of the Rs is extremely huge most of the current would pass through transistor "c" and it will go to the ground via transistor "d" and the resistor "Ra". Resistor "Ra" is relatively small.

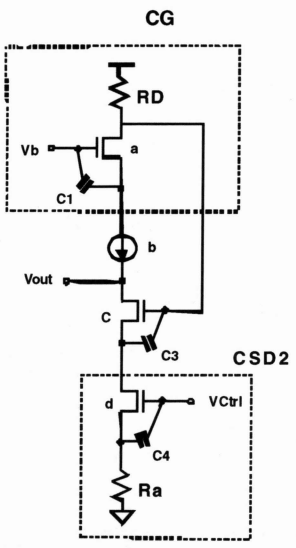


Figure 3.8 : CSD1 and CSD2 are shown in fully operational mode.

3.2 The small signal analysis of the QVCO

The impedance looking at the Common Gate from transistor "b" is being measured in Figure 3.9.

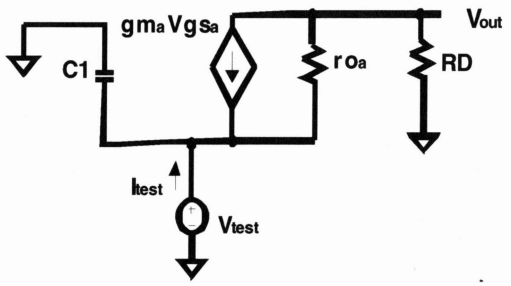


Figure 3.9: Impedance of the Common Gate stage.(by applying a Vtest)

Based on the current signal analysis the impedance would be calculated as following:

$$I_{test} = gm_a Vgs_a + \frac{(V_{out} - V_{test})}{ro_a} + \frac{-V_{test}}{(\frac{1}{C_1 S})} \tag{3.2.1}$$

$$I_{test} = -gm_a V_{test} + \frac{(I_{test}.RD - V_{test})}{ro_a} - V_{test}.C_1 S \tag{3.2.2}$$

$$I_{test} - \frac{I_{test}.RD}{ro_a} = (-gm_a - \frac{1}{ro_a} - C_1 S)V_{test} \tag{3.2.3}$$

$$\frac{V_{test}}{I_{test}} = \frac{(1 - \frac{RD}{ro_a})}{(-gm_a - \frac{1}{ro_a} - C_1 S)} \tag{3.2.4}$$

Since: $1 - \frac{RD}{ro_a}$ is approximately equal to $-\frac{RD}{ro_a}$

$$Z_{C.G} = \frac{V_{test}}{I_{test}} = \frac{(\frac{RD}{ro_a})}{(gm_a + \frac{1}{ro_a} + C_1 S)} \tag{3.2.5}$$

The small signal analysis of the CSD1 is depicted in the Figure 3.10.

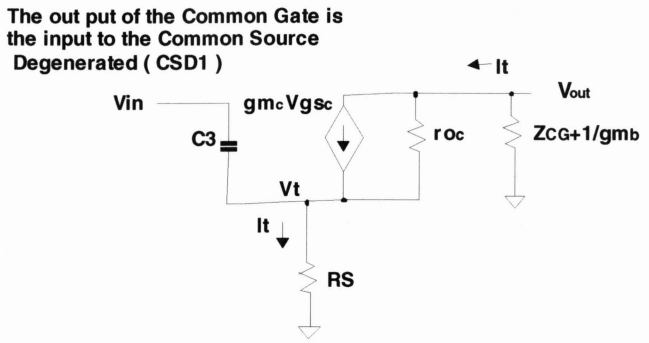


Figure 3.10 : The small signal of CSD1 with considering the resistances.

Considering Figure 3.10 the open loop transfer function can be calculated as following:

Assuming $\gamma = Z_{CS} + \frac{1}{g_m}$

$$(V_{in} - V_t)C_3S + gm_c Vgs_c + \frac{V_{out} - V_t}{r_{oc}} \approx I \tag{3.2.6}$$

$$(V_{in} - R_s(-\frac{V_{out}}{\gamma})C_3S + gm_c(V_{in} - V_t) + \frac{V_{out} + R_s\frac{V_{out}}{\gamma}}{ro_c} = \frac{V_{out}}{\gamma} \tag{3.2.7}$$

$$(V_{in} + R_s\frac{V_{out}}{\gamma})C_3S + gm_c(V_{in} + R_S\frac{V_{out}}{\gamma}) + \frac{V_{out} + R_S\frac{V_{out}}{\gamma}}{ro_c} = \frac{V_{out}}{\gamma} \tag{3.2.8}$$

$$V_{in}(C_3S + gm_c) = V_{out}[-R_S C_3\frac{1}{\gamma} - gm_c R_S\frac{1}{\gamma} - (\frac{1+\frac{R_S}{\gamma}}{ro_c}) + \frac{1}{\gamma}] \tag{3.2.9}$$

Since R_S = 52 KΩ it can be considered : $\gamma << R_S$

$$\frac{V_{out}}{V_{in}} = \frac{C_3 S + gm_c}{-\frac{R_S C_3 S}{\gamma} - \frac{gm_c R_S}{\gamma} - \frac{\gamma + R_S}{ro_c \gamma} + \frac{1}{\gamma}} \tag{3.2.10}$$

Since $\gamma << R_S$ therefore $\gamma - R_S \approx -R_S$

$$\frac{V_{out}}{V_{in}} = \frac{C_3 S + gm_c}{\frac{1}{\gamma}[(-R_S C_3 S) - gm_c R_S + \frac{R_S}{ro_c} + 1]} \tag{3.2.11}$$

By considering: $\delta = -gm_c R_S + \frac{R_S}{ro_c} + 1$

Since $\frac{1}{gm_b}$ is smaller than $\frac{-\frac{R_D}{ro_a}}{-gm_a - \frac{1}{ro_a} - C_1 S}$ therefore γ can be indicated as following:

$$\gamma \approx \frac{-\frac{R_D}{ro_a}}{-gm_a - \frac{1}{ro_a} - C_1 S} \tag{3.212}$$

$$\frac{V_{out}}{V_{in}} = \left(\frac{\frac{-R_D}{ro_a}}{-gm_a - \frac{1}{ro_a} - C_1 S}\right)\left(\frac{\frac{1}{\delta}\left(\frac{C_3}{gm_c} S + 1\right)}{\frac{1}{gm_c}\left(\frac{-R_S C_3 S}{\delta} + 1\right)}\right) \tag{3.2.13}$$

Substituting δ into Equation 3.2.13 :

$$\frac{V_{out}}{V_{in}} = \frac{\frac{-R_D}{ro_a}\frac{1}{\delta}\left(\frac{C_3}{gm_c} S + 1\right)}{\frac{1}{gm_c}\left(-gm_a - \frac{1}{ro_a} - C_1 S\right)\left(\frac{-R_S C_3}{\delta} S + 1\right)} \tag{3.2.14}$$

By considering: : $\beta = gm_a + \frac{1}{ro_a}$

$$\frac{V_{out}}{V_{in}} = \frac{gm_c \frac{1}{\beta}\frac{1}{\delta}(\frac{C_3}{gm_c}S+1)}{(1+\frac{C_1}{\beta}S)(-\frac{R_S C_3}{\delta}S+1)} \qquad (3.2.15)$$

The obtained poles and zeros from equation 15 are for the case when the "Vctrl" is less than 0.5 Volt. At this condition the CSD2 is turned off . A half delay cell is depicted in Figure3.7.

$$\text{Pole 1: } \frac{gm_a + \frac{1}{ro_a}}{C_1}$$

$$\text{Pole 2: } \frac{gm_c R_S + 1 + \frac{R_S}{ro_c}}{R_S C_3}$$

$$\text{Zero 1: } \frac{gm_c}{C_3}$$

Pole1 and Zero1 are located at the left hand side of the S-Plane. Pole2 is at the right hand side of the S-Plane and it can be ignored. Since "gm_c" is larger than "gm_a" therefore zero1 is far away from the origin and it can also be ignored.

However at the time that "Vctrl" passes the Threshold voltage of 0.5 volt the small signal analysis schematics of the circuit for Figure 3.8 is being depicted in Figure 3.11.

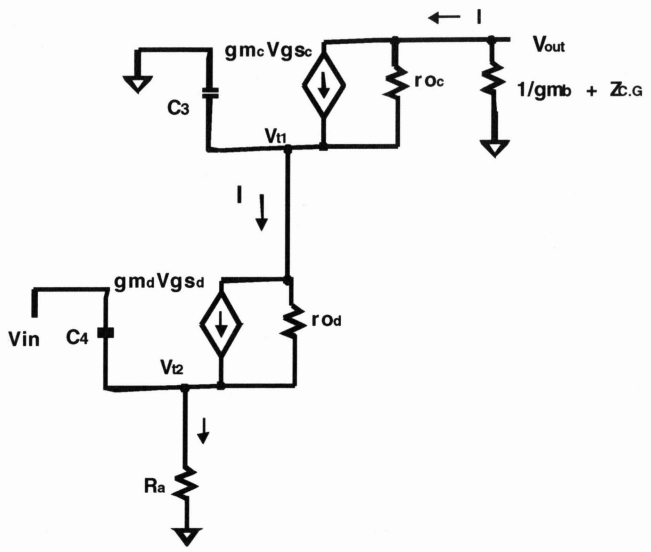


Figure 3.11: Small signal analysis of Figure 3.8. (CSD1 & CSD2 are operational)

$$(V_{in} - V_{t2})C_4 S + gm_d(V_{in} - V_{t2}) + (\frac{V_{t1} - V_{t2}}{ro_d}) \approx I \tag{3.2.16}$$

By considering $V_{t2} = I \times R_a = \frac{V_{out}}{\gamma} R_a$

$$(0 - V_{t1})C_3 S + gm_c(0 - V_{t1}) + (\frac{V_{out} - V_{t1}}{ro_c}) \approx I \approx \frac{V_{out}}{\gamma} \tag{3.2.17}$$

$$-V_{t1}(C_3 S + gm_c + \frac{1}{ro_c}) = V_{out}(\frac{1}{\gamma} - \frac{1}{roc}) \tag{3.2.18}$$

$\frac{1}{ro_c}$ is negligible and can be ignored in Equation 3.2.18.

Also from Equation 3.2.12 and considering $\beta = gm_a + \frac{1}{ro_a}$ the following results would be obtained:

$$\gamma = \frac{R_D}{ro_a(\beta + C_1 S)} \tag{3.2.19}$$

$$-V_{t1}(C_3 S + gm_c) = V_{out}\frac{ro_a(\beta + C_1 S)}{R_D} \tag{3.2.20}$$

$$V_{t1} = -\frac{ro_a(\beta + C_1 S)}{R_D(C_3 S + gm_c)}V_{out} \tag{3.2.21}$$

From Equation 3.2.16 the following can be resulted :

$$V_{in}(C_4 S + gm_d) - V_{t2}(C_4 S + gm_d + \frac{1}{ro_d}) + V_{t1}\frac{1}{ro_d} = V_{out}\frac{ro_a(\beta + C_1 S)}{R_D} \tag{3.2.22}$$

In Equation 3.2.22 the amount of $\frac{1}{ro_d}$ is negligible since ro_d is comparable to ro_a the result of $V_{t1}\frac{1}{ro_d}$, considering 3.2.21, becomes $-\frac{(\beta + C_1 S)}{R_D(C_3 S + gm_c)}V_{out}$ therefore:

$$V_{in}(C_4 S + gm_d) - V_{t2}(C_4 S + gm_d) - \frac{(\beta + C_1 S)}{R_D(C_3 S + gm_c)}V_{out} = V_{out}\frac{ro_a(\beta + C_1 S)}{R_D} \tag{3.2.23}$$

$$(C_4 S + gm_d)(V_{in} - \frac{V_{out}}{\gamma}R_a) - \frac{(\beta + C_1 S)}{R_D(C_3 S + gm_c)}V_{out} = V_{out}\frac{ro_a(\beta + C_1 S)}{R_D} \tag{3.2.24}$$

From Equations 3.2.24 and 3.2.12 it can be concluded:

$$(C_4 S + gm_d)V_{in} - V_{out}\frac{1}{\gamma}R_a(C_4 S + gm_d) - \frac{(\beta + C_1 S)}{R_D(C_3 S + gm_c)}V_{out} = V_{out}\frac{ro_a(\beta + C_1 S)}{R_D} \tag{3.2.25}$$

$$(C_4 S + gm_d)V_{in} = V_{out}\{\frac{1}{\gamma}R_a(C_4 S + gm_d) + \frac{(\beta + C_1 S)}{R_D(C_3 S + gm_c)} + \frac{ro_a(\beta + C_1 S)}{R_D}\} \tag{3.2.26}$$

$$(C_4S + gm_d)V_{in} = V_{out}\frac{ro_a(\beta + C_1S)}{R_D}\{R_a(C_4S + gm_d) + \frac{1}{(C_3S + gm_c)ro_a} + 1\} \quad (3.2.27)$$

By looking at Equation 3.2.27 it can be deduced that $R_a gm_d$ might be ignored due to the small value of gm_d. Also $R_a C_4 S$ might be neglected without any effect on the total result.

Value of $\beta = gm_a + \frac{1}{ro_a}$.

$$\frac{V_{out}}{V_{in}} = \frac{R_D(C_4S + gm_d)}{ro_a(\beta + C_1S)\{\frac{1}{(C_3S + gm_c)ro_a}\}} \quad (3.2.28)$$

From Equation 3.2.28 the Transfer Function would be obtained as following:

$$\frac{V_{out}}{V_{in}} = R_D\frac{(gm_a + \frac{1}{ro_a})}{(gm_c gm_d)}\frac{(\frac{C_4}{gm_d}S + 1)(\frac{C_3}{gm_c}S + 1)}{(\frac{C_1}{(gm_a + \frac{1}{ro_a})}S + 1)} \quad (3.2.29)$$

The above Transfer Function results in two left hand zeros and a left hand pole.

$$\text{Left hand zero 1} : \frac{-gm_d}{C_4}$$

$$\text{Left hand zero 2} : \frac{-gm_c}{C_3}$$

$$\text{Left hand pole 1} : -\frac{gm_a + \frac{1}{ro_a}}{C_1}$$

For the Left hand zero 2 since $gm_c >> gm_a$ therefore it is apparent that the zero which is pushed further away on the S-plane can be discarded. For the left hand Zero 1 since gm_d is larger than gm_a

this zero is located also further away than gm_a on the S-plane and it can be ignored. As the result only left hand Pole 1, can be the main contributor to the first order quadrature coupled oscillator.

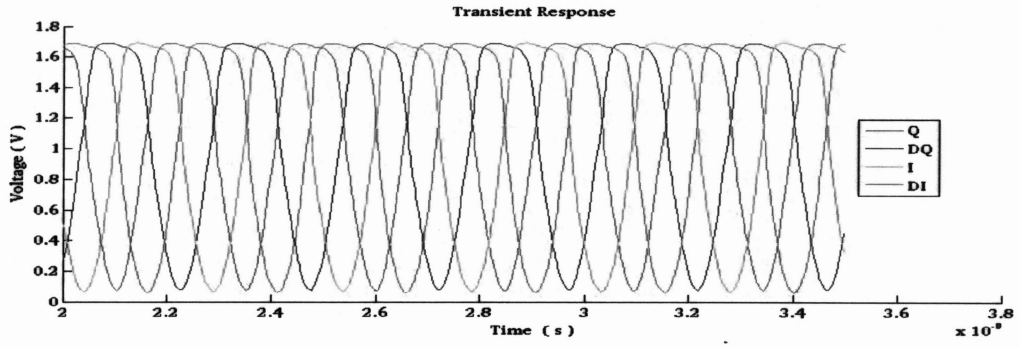


Figure 3.12: Transient response of the quadrature VCO at 404.7 MHz.

The phase noise obtained for the quadrature oscillator for 404.7 MHz oscillation @160KHz offset is -100.3 dBc/Hz.

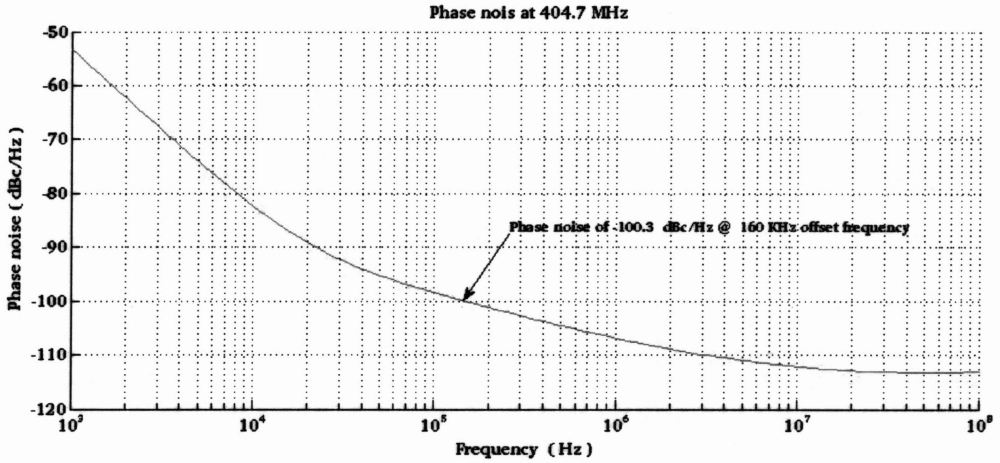


Figure 3.13 : Phase noise of -100.3 dBc/Hz @160KHz for oscillation frequency of 404.7MHz

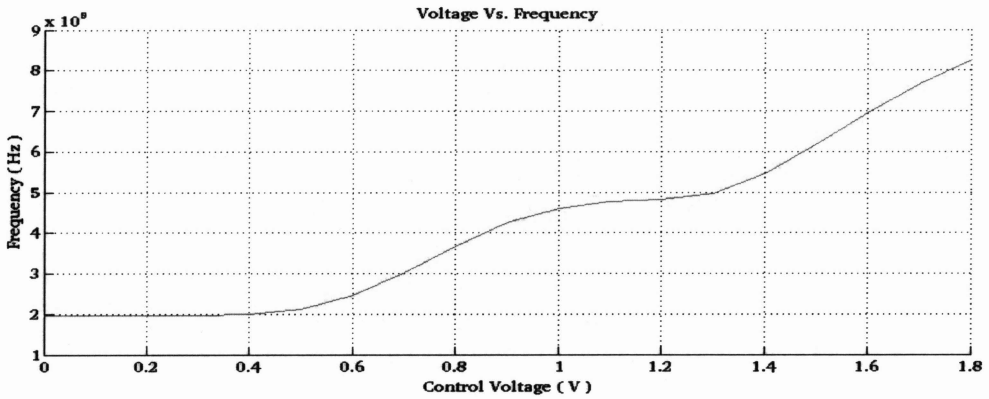


Figure 3.14 : The tuning characteristics of the QVCO

The QVCOs gain is also referred to as K_{VCO} [Hz/V]. By looking at the Figure 3.14 it can be deduced that the slope of the linear line parallel to the Voltage Vs. Tuning Frequency curve would be approximately calculated as $K_{VCO} = \frac{(827MHz - 200MHz)}{(1.8V - 0.5V)} = 482 \ MHz/V$

When the oscillator's Control Voltage is at zero volt the output frequency is at 200MHz. This frequency is called the Center Frequency (F_{center}). The frequency of the QVCO is dependent on the voltage at its tuning input which is called (V_{tune}). The relationship between the output frequency F_{OUT}, the Control Voltage (V_{ctrl}), and the tuning voltage (V_{tune})can be approximately written as $F_{OUT} \approx F_{center} + KVCO\ (V_{tune})$ [9].

The eye diagram of the output signal that is depicted in Figure 3.15 is an indicator measurement of the timing accuracy of the output signal. Phase noise is another measure of variations in signal timing, but the results are displayed in the frequency domain [17]. In fact jitter and phase noise characterize the same phenomenon [17] This Figure is also an indicator of the total amount of timing noise in the frequency range of interest.

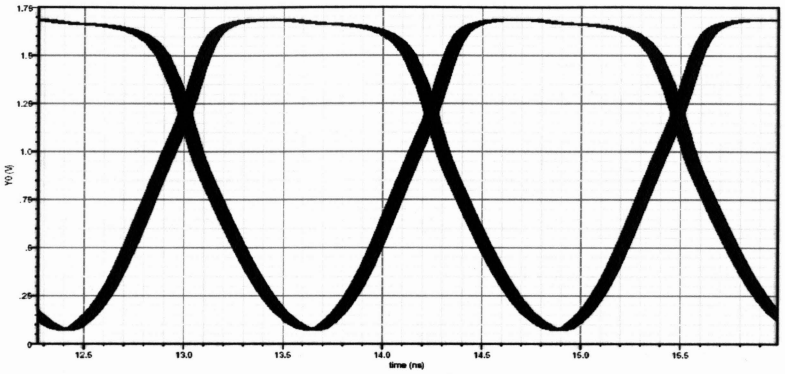
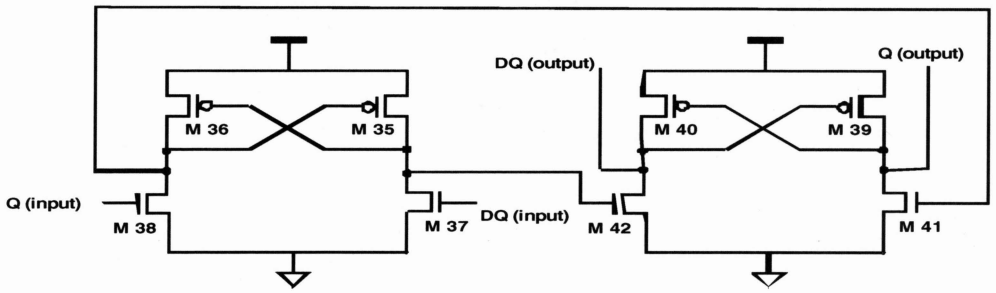


Figure 3.15: The eye diagram of the output signal.

Figure 3.16 depicts the schematics of the differential buffers for the output stage of the QVCO. The design of the output buffer should be in a fashion that it can generate the proper output signal at frequencies from 200 MHz to 827 MHz while providing the proper duty cycle. For this reason the power consumption of this module has been slightly higher to make this part reliable at both high and low frequencies.



3.16 : The schematics of the QVCO synthesizer output differential buffer

Figures 3.17 and 3.18 represent the output signals of the QVCO buffer. These signals will be used as the clock inputs (CLK+, CLK-) for the next stage. These signals converted by the Buffers to the clock signals to provide a better performance for the divider circuit.

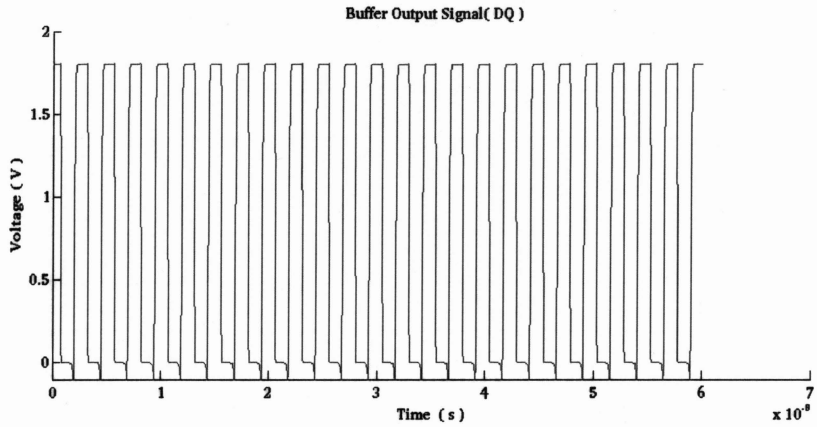


Figure 3.17: Buffer output signal (DQ) at 403.5 MHz

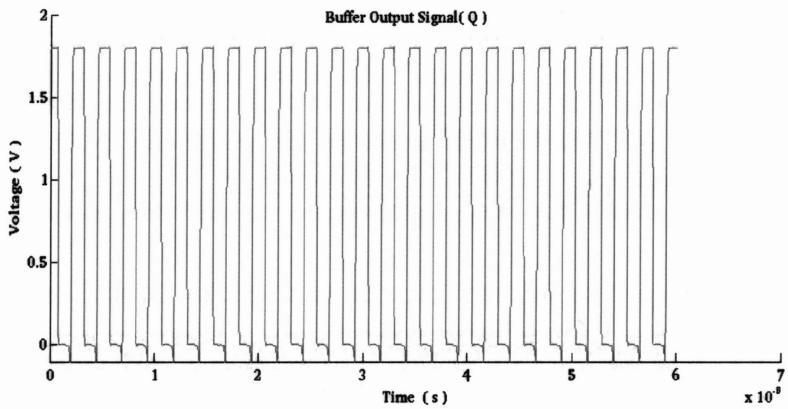


Figure 3.18: Buffer output signal (Q) at 403.5 MHz.

Due to the gate source capacitances of transistor pairs of M41, M42 and M38, M37 at the output of the buffers, a slight amount of current drop at zero voltage level occurs. This issue can be eliminated in the next stage (the Divider clock input) by a slight increase in the length of the clock transistors.

3.3 Summary

We have proposed a QVCO in this chapter based on current reuse technique. Ring oscillators occupy a smaller chip area than the LC tanks and by bringing down the phase noise level of the

QVCO to -100 dBc/Hz both the phase noise and the size constraints of the design have been addressed. The entire QVCO is not dependent on any other external circuitry for biasing and it also contributes to a small size for the QVCO. Switching and coupling transistors are also causing the generated signal to be more of the symmetrical shape therefore helping to bring down the phase noise of the overall design. A wide frequency range operation (from 200-827 MHz)would allow the design to be more inter-modular for other Biomedical applications. The proposed QVCO also utilizes the notion of adjusting the current at each half delay cell to have a better control over the current consumption of the whole entire quadrature oscillator. This process is done by voltage to current converter. The QVCO power consumption is at 0.9 mW.

Chapter 4
Frequency Divider for the Synthesizer

4.1 Prescaler and the Positive Edge Counters

The output of the previous section (buffer output signals DQ and Q) would be used as the input clocks (CLK + , CLK -) to the first stage of the 32 / 33 divider prescaler. In this topology the first stage is referred to as synchronous counter, divider 4/5. The second module of the divider can also be called the asynchronous part as they have been depicted in Figure 4.2. Since the input to the second stage has been at least divided by 4 the rest of the divisions shall be done at lower frequencies. The first two stages are also called Prescaler(32/33). As depicted in Figure 4.1 the third stage consists of a "Program Counter" and a " Swallow Counter" in turn each of which would count the number of the positive edges of the divided signals and generate the signal which would be matched to the reference frequency. The frequency divider can easily be the most power hungry digital circuit in the radio portion of the receiver [18].

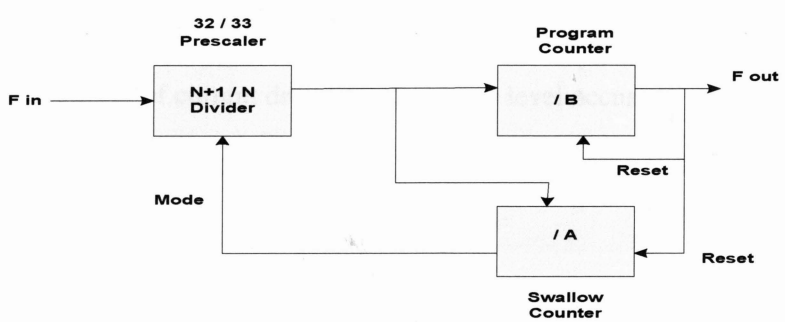


Figure 4.1 : The general overview of the dual modulus presecaler(32/ 33), swallow and program Counter in the frequency synthesizer [19].

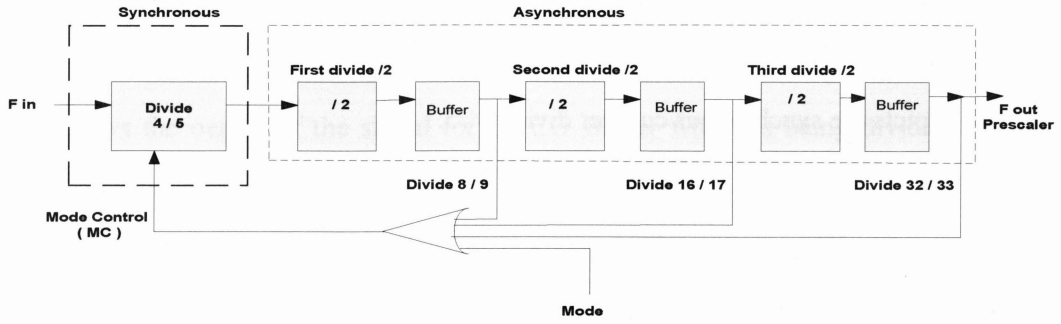


Figure 4.2 : Divide by 32 /33 dual modulus prescaler.

In Figure 4.3 the schematics of the SCL D- Flip Flop has been shown. Since this part of the design works at higher frequency therefore it has been decided to be operational at synchronous level (due to presence of the clock signal from the QVCO buffers). SCL circuits also exhibit improved noise performance due to their differential nature as compared to single ended circuits [20]. SCL D-Flip Flops can be used at high speed digital circuits. These Flip Flops are non-saturation, constant current, reduced swing logic devices which can perform at high frequency with relatively lower power consumption [20]. Due to the reduced swing output signal of SCL D-Flip Flop a differential buffer is being placed after two consecutive D-Flip Flops.

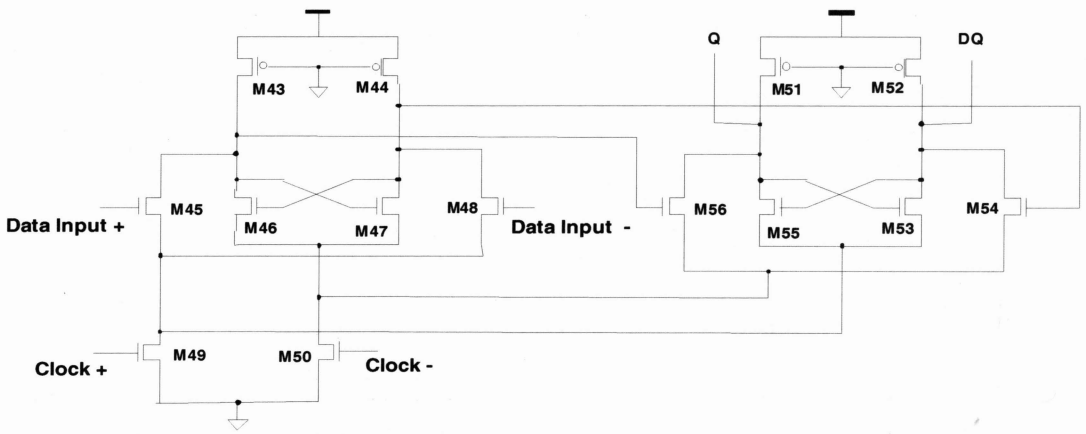


Figure 4.3: Schematics of the SCL D-Flip Flop.

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4.2 Synchronous Counter divide by 4/5

Figure 4.4 depicts the synchronous counter divider 4/5.

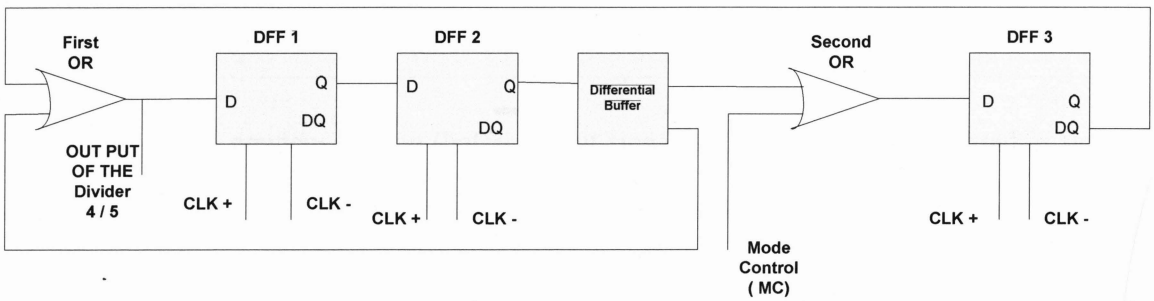

Figure 4.4: The Synchronous counter divider circuit, divider by 4/5.

The fist stage of the Divider circuit sets the division ratio of 4 or 5. If the Control signal "Mode Control"(MC) has been assigned the value of "1"then the divider input frequency(at the output of the fist "OR") would be divided by 4. The comparison has been depicted in Figure 4.5.

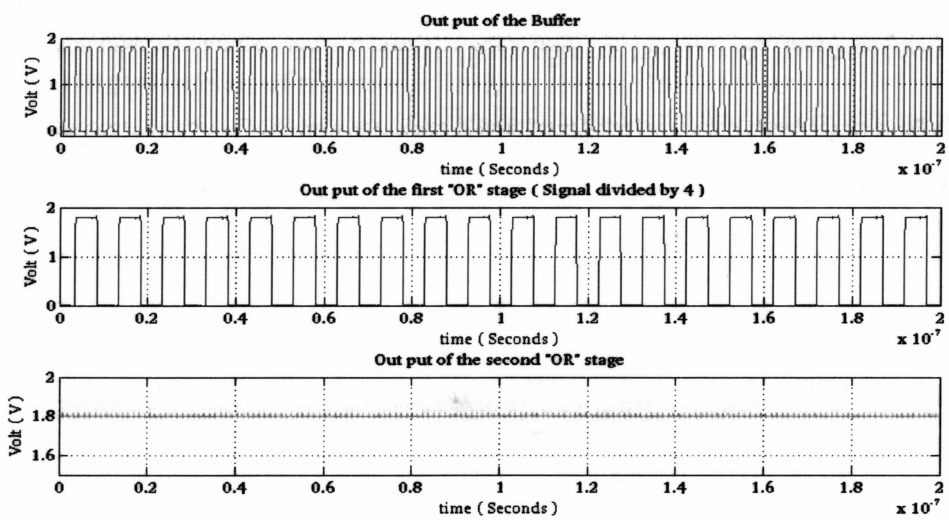

Figure 4.5 : Comparison of the outputs of the QVCO Buffer (403.5MHz), Divided by 4 at the output of the first "OR" stage.

In Figure 4.5 the output of the first "OR" is 100.8MHz. Since the MC(Mode Control)signal is set to be at 1(as depicted in the third graph of Figure 4.5)the output of the second "OR" stage is at 1.8 V. Figure 4.6 shows the output of the signal for QVCO Buffer which is being divided by 5 at 80.7 MHz.

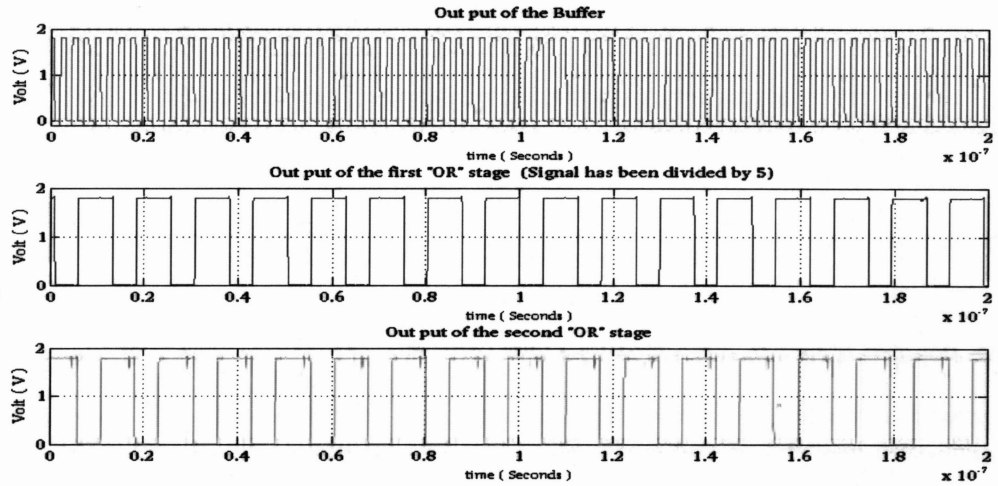

Figure 4.6 : Comparison of the outputs of the QVCO Buffer (403.5MHz), Divided by 5 at output of the first "OR" stage.

The output of the second "OR" stage would change due to the fact that one of the second "OR" inputs is set to be "zero." Therefore the output values of the second "OR" also vary as it is depicted in Figure 4.6.

Figure 4.7 depicts the schematics of divide by 2 circuit. The loading transistors of M92, M93, M98, and M99 are operating in the linear region. This would cause a lower RC constants associated with the output nodes of the D-Flip Flops [21]. The full voltage swing of the output signal, generates the turn on and turn off voltages for the next divide by 2 stage. In design of each transistor the width and length are considered in a fashion to reduce the capacitance of internal and external nodes. This in turn would lead to propagation delay and the desired output signal.

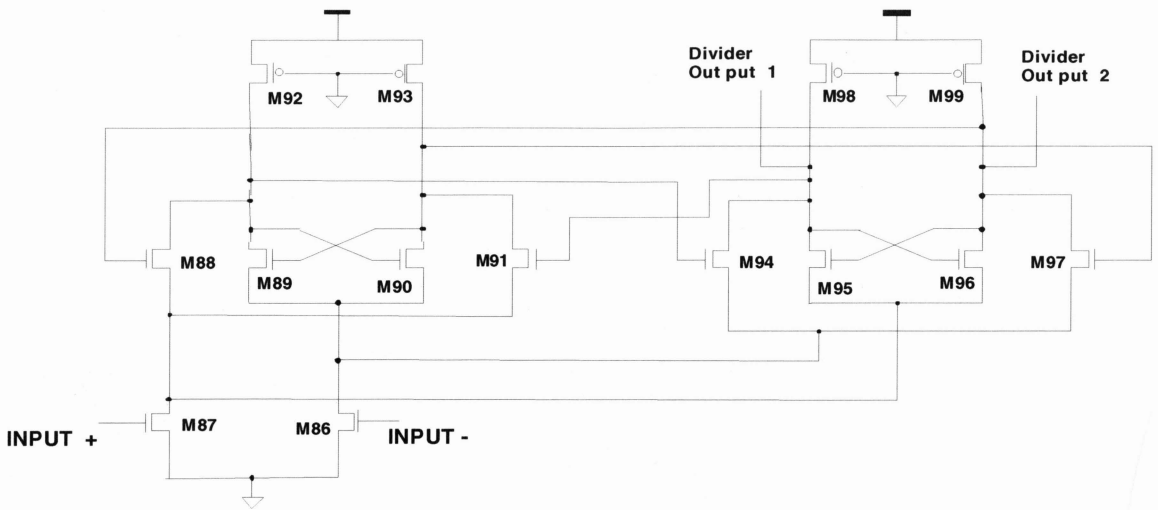

Figure 4.7 : Schematics of the Divide by 2 circuit.

A cross coupled transistor pair exhibit a negative resistance of $\frac{-2}{g_m}$ and this value of resistance can be controlled by the bias current. In fact a negative resistance can be placed in parallel to a positive resistance. In reality the SCL design is a Differential stage with variable negative resistance load. Figure 4.8 represents the idea of the negative resistance in the SCL circuit. Figure 4.9 also depicts the half circuit for the SCL D-Flip Flop.

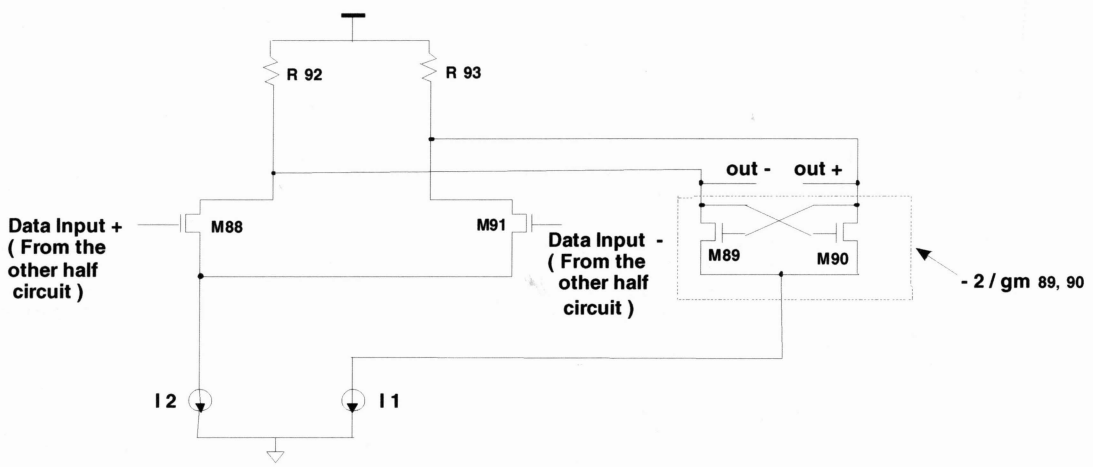

Figure 4.8 : The schematic diagram of the divide by 2 half cell circuit.

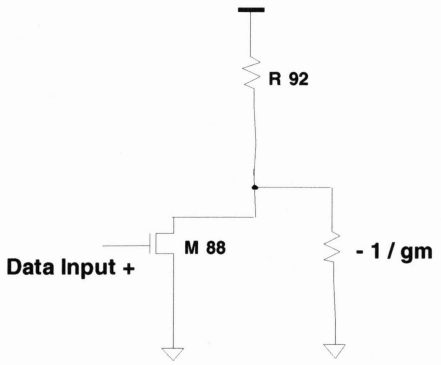

Figure 4.9: The schematic of a half circuit of Figure 4.8.

The load of the differential pair in Figure 4.8 consists of resistors R92, R93 and the cross coupled transistors M89 and M90. With an increase in current I1 the amount of negative resistance

$(\frac{-2}{g_{m89,90}})$decreases [22]. By considering the circuit at Figure 4.9 the equivalent resistance can be shown as following :

$$R_{92} \parallel (\frac{-1}{g_m}) = \frac{R_{92}}{1 - R_{92} g_m}$$

In this case by a decrease in the amount of g_m the equivalent resistance increases and therefore lowering the frequency of oscillation. By considering the right transistor sizes the output signal would be divided by two.

By looking at Figure 4.2 the selection of the division ratio(32 /33)is performed by "Mode" signal. When "Mode" signal is equal to 1 the prescaler is dividing the input frequency by 32 and when the"Mode"signal is at 0 the division ratio is being set to 33. These changes have been depicted at Figure 4.11 and Figure 4.15. In Figure 4.2 after each divide by 2 section an inverter buffer is placed to provide the driving capability of the next divider.

4.3 Synchronous and Asynchronous Counter divide by 32/33

By considering Figures 4.10 and Figure 4.11 the signals of the 403.5 MHz input to the prescaler is being divided by 32 and 33 respectively.

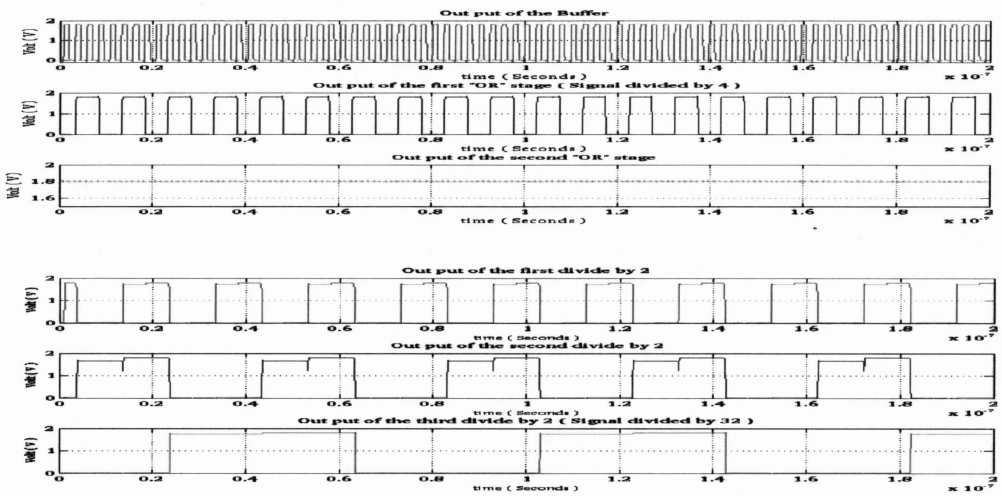

Figure 4.10: The QVCO output signal (403.5 MHz) divided by 32 (12.61 MHz).

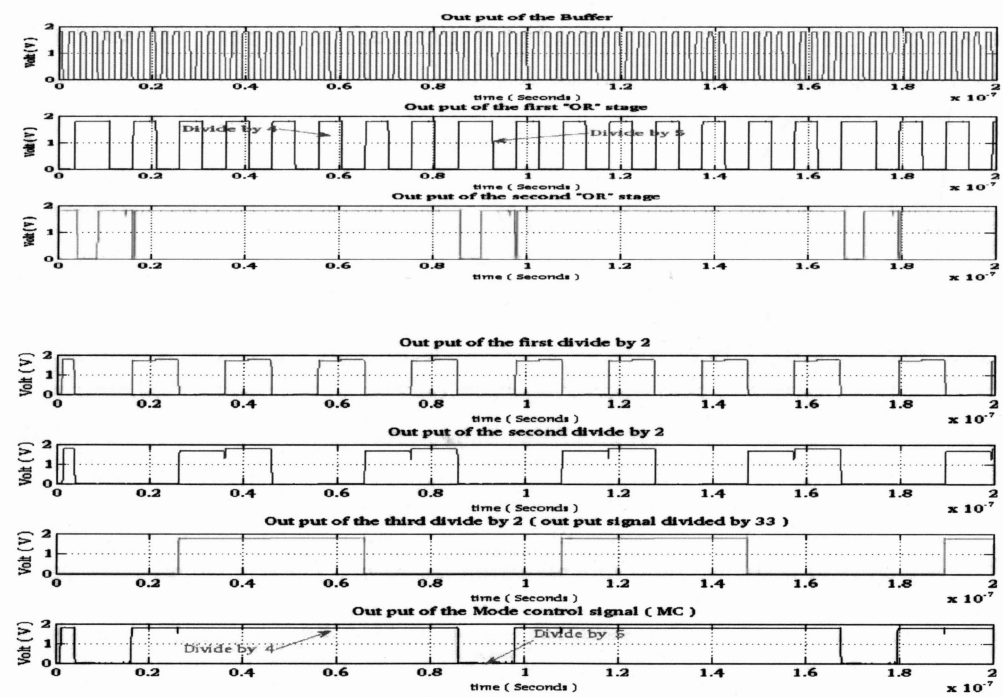

Figure 4.11: The QVCO output signal (403.5 MHz) divided by 33 (12.22 MHz).

One of the considerations of the divider circuit is the inter-modularity of the design. The circuit would perform from 200MHz range till 827 MHz oscillation frequency.

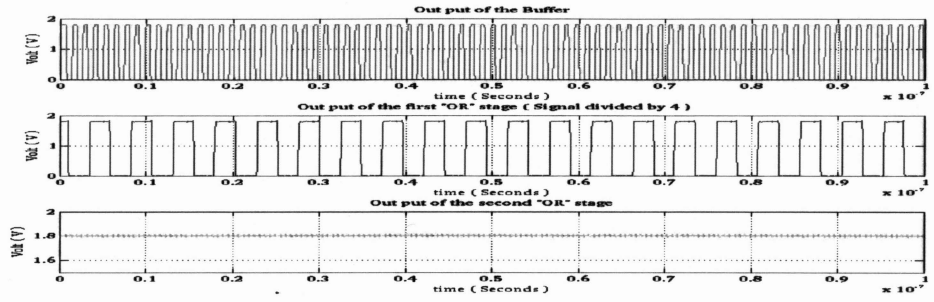

Figure 4.12 : The output signal of QVCO (827 MHz) divided by 4.

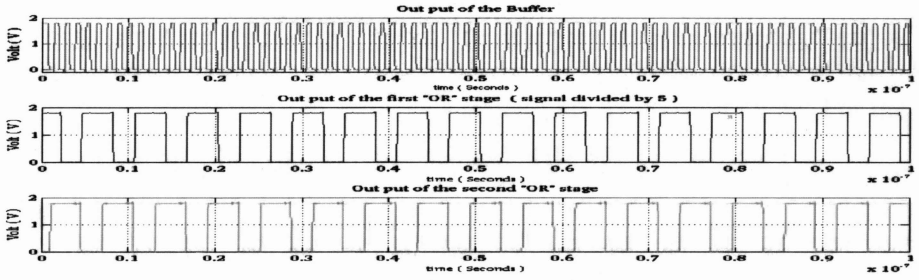

Figure 4.13: The output signal of QVCO (827 MHz) divided by 5.

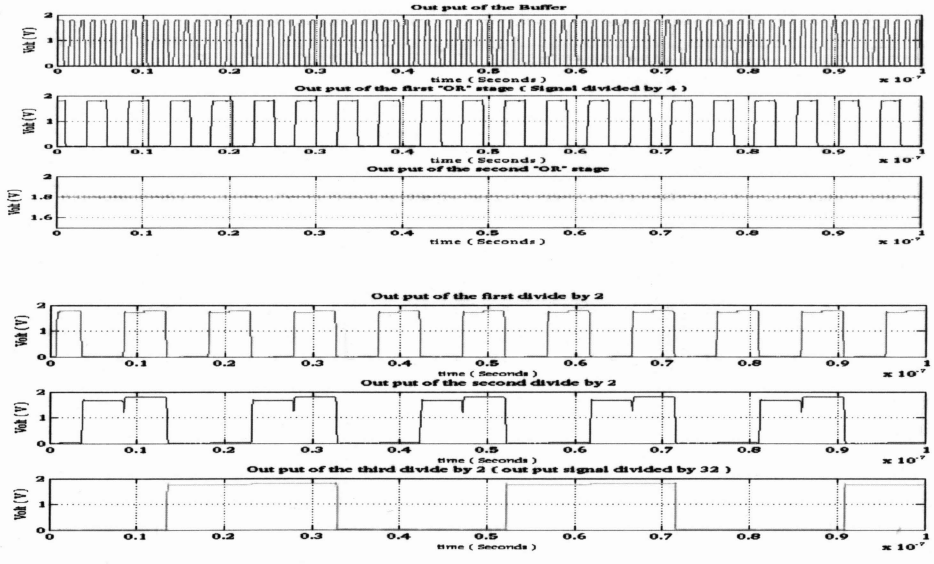

Figure 4.14 : 827 MHz frequency divided by 32(25.84 MHz)

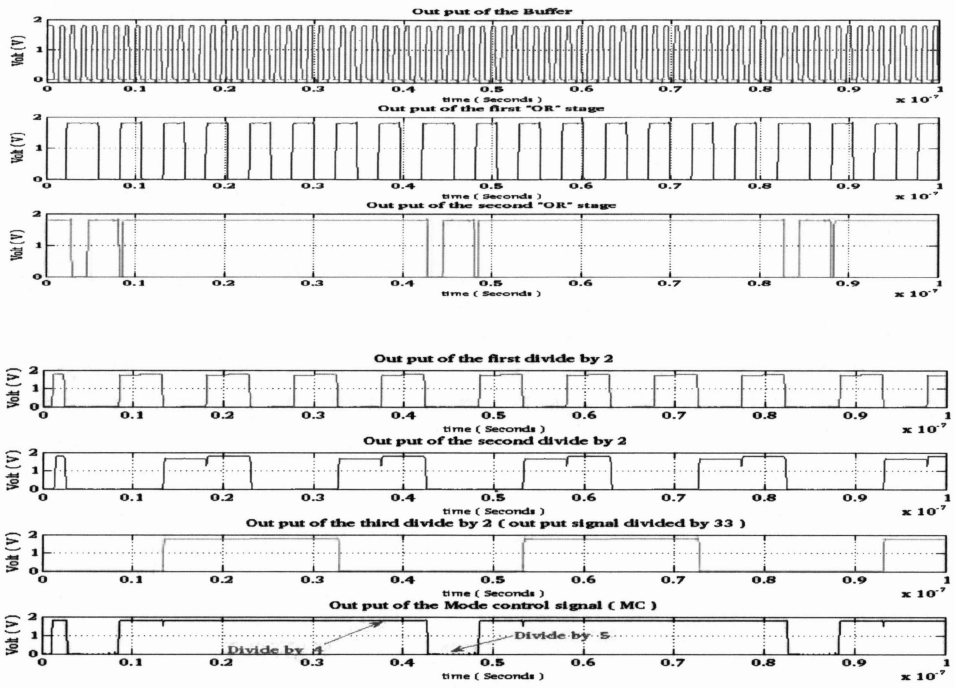

Figure 4.15 : 827 MHz frequency divided by33(25.06 MHz)

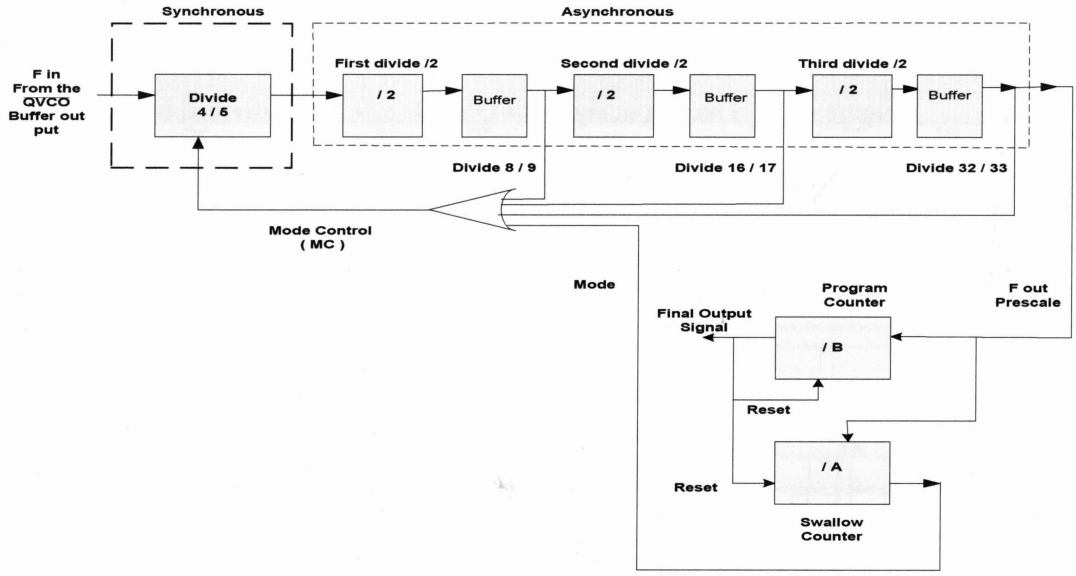

Figure 4.16 : The complete system level blocks of the synthesizer divider.

In Figure 4.16 the output of the 32 /33 divider is fed to the program counter and the swallow counter. First the prescaler begins the operation by dividing N+1(/33) until the swallow counter "A"

is full. The prescaler is then set to divide by N(/32)through issuing the "Mode = 1"signal and counter "A" is disabled. The division continues until the programmable counter B is also full and it triggers the "Reset" signal which in turn resets both counters "A" and "B." The following formula represents the above procedure.

(B-A)N+A(N+1) = NB+A

A= 2, B = 84

(84-2) (32) + 2 (33) = 2690 (number of total division ratio)

403.5 MHz ÷ 2690 = 150 KHz

As it has been depicted in Figure 4.17 "Final_Output_Signal"of the divider is 150 KHz. The "Mode"signal is being changed twice to zero. This signal implies division by 33. For the rest of the period the "Mode" signal is equal to"1"(divide by 32). In Figure 4.18 a segment of the "Mode" signal is equal to zero (divide by 33) has been enlarged. The code for the Digital component

(Swallow Counter and the Program Counter) has been written in Verilog-A.

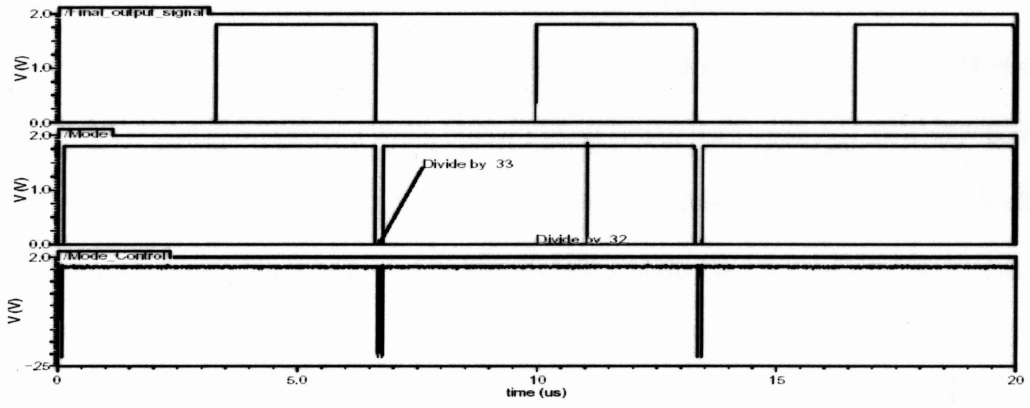

Figure 4.17 : The output of the frequency divider, "Final_output_signal" at 150.0 KHz.

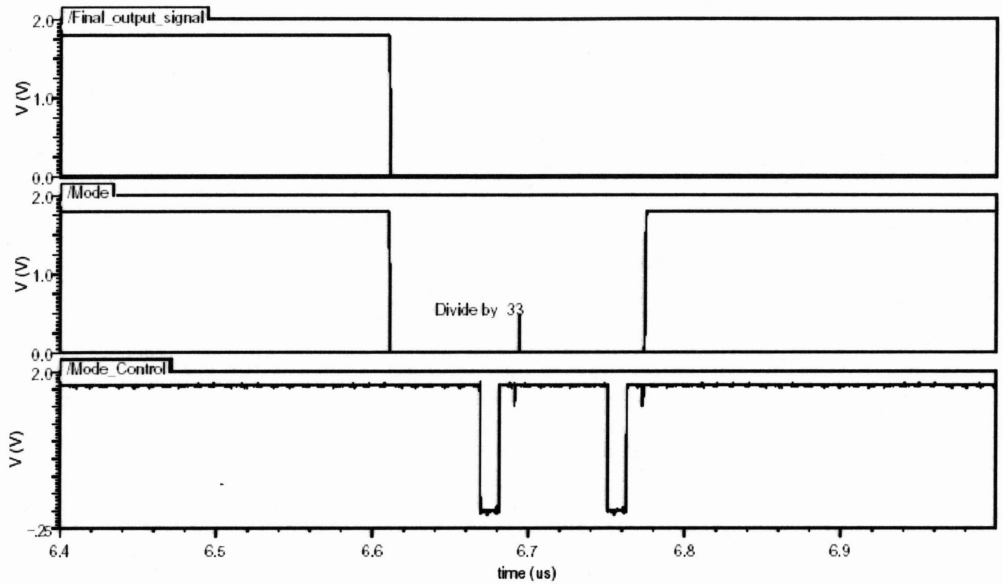

Figure 4.18 : Enlarged section for the "Divide by 33"section . Two continues divide by 5 are being used at the Mode_Control Section to obtain the divide by 33.

4.4 Summary

In this chapter an integer divider(divide by 2690)has been simulated. This divider has been implemented in Mixed-mode design. It consists of a 32/33 divider, a swallow counter, and a program counter. By the proper combinations of the 32/33 divisions the desired Integer-N division can be obtained. The SCL topology used in this design would allow a wider frequency range(200-827MHz) for the divider. That in turn would allow the inter-modularity of the design. The dual modulus prescaler 32/33 is made of a 4/5 divider and three divide by two components. Slight modifications have been done to the SCL D-Flip Flops and SCL divide by 2 schematics by removing the bias transistors at the bottom of the differential pairs. This in turn would also help in decreasing the topology's dependence on external bias sources. The divider consumes approximately 2.3 mW of power.

Chapter 5
Phase and Frequency Detector (PFD), Charge Pump(CP), and Loop Filter(LF)

Since the Phase Frequency Detector (PFD), Charge Pump, and Loop Filter operate in a close interconnected manner all three components should be investigated together at the system and schematics level. The PFD relates the phase and the frequency differences between the reference frequency (150 KHz) and the output signal of the divider. These signals are being converted to 2 output signals "Down Positive," and "UP Negative" which in turn would be converted to current by the Charge Pump. This current can be turned into a voltage by means of the Loop Filter(Low Pass Filter). The interrelations of these components have been shown in Figure 5.3.

5.1 Phase Frequency Detector (PFD)

The basic Phase Frequency Detector(PFD)has been depicted in Figure 5.1. This topology consists of two D-Flip Flops and an AND gate. However in this design due to the fact that the Crystal Oscillator's output signal is sinusoidal; the inverter buffer converts this signal to a rectangular wave form which makes the PFD more accurate. The buffer also provides the Crystal Oscillator the driving capabilities for the next D-Flip Flop stage. Figure 5.2 represents the True Single Phase Clocking (TSPC) circuit for low frequency operations. This type of circuit has been chosen for their superior power savings and their speed at the desired frequency range [23]. The Data input of each D-Flip Flops has been set to high (VDD). Therefore using a low power design circuit for the D-Flip Flop would be crucial. A clock transition of the right polarity turns on the associated D-Flip Flop. If "Input A" is high then signal "A" would go to high and if "Input B" is high consequently signal "B" would go to high. Signal "A" and signal "B" are considered as "Down Positive" and "UP Positive"

signals, respectively. However if either "A" or "B" are high simultaneously as detected by the AND gate, the feedback topology resets both D-Flip Flops. The wave forms of the Figures 5.5 - 5.8 indicate such a transition for the Reset signal as a spike. An active "B" signal tells the synthesizer to raise the frequency of the QVCO since the QVCO is lagging behind the input signal. An Active "A" signal provides the opposite behavior [24]. Therefore "Up Positive" and "Down Positive" outputs provide directions of phase and frequency error.

In fact the magnitude of the phase error is indicated in the width of the "A"or "B" pulse signals. This notion has been shown (in red)in Figures 5.6 , 5.8 at Signal " B". The pulse widths are at 90 degrees and 270 degrees respectively. The change in the frequency has been shown in Figure 5.9 at signal "B" for the time that frequency has to increase and in Figure 5.10 at signal "A" as to reverse should be implemented by the synthesizer due to an increase in the output frequency of the QVCO. From operational point of view signal "A"(DownPostive)in this Figure is issuing the order to decrease the frequency of the QVCO in the synthesizer.

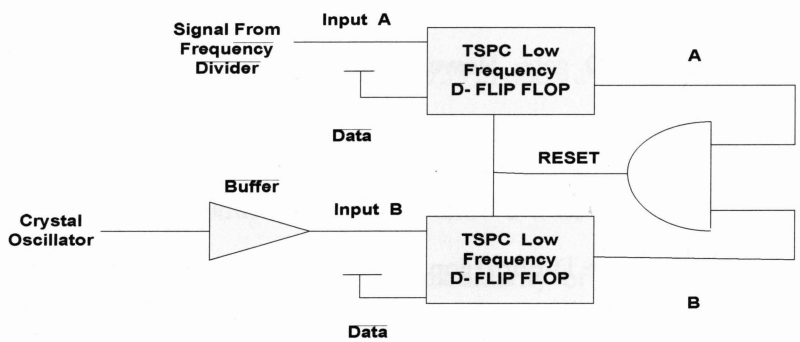

Figure 5.1: System level design of the Phase and Frequency Detector (PFD)

Each D Flip Flop has been designed by utilizing TSPC low frequency circuit. Due to the nature of TSPC circuit since there is no feedback in the D-Flip Flop the speed of these circuits can go up to a few GHz. However this design has been modified from [24] by introducing a "Reset"signal and a

NMOS transistor (M66). Considering the "Reset" signal is equal to 1, the behavior of the TSPC D-Flip Flop is as following:

This design works based on the Gate Source (GS), Gate Drain (GD), and Drain Source (DS) capacitances of the transistors. When Clock is high as the result transistors M58, M63 are OFF and transistors M59, M65, M70 are turned on. As Data signal goes high (VDD) it causes transistor M59 to be turned on and transistors M57 to be turned off. Therefore it forces the input to the inverter which is made of M60 and M61 to go to zero and the output of the inverter becomes high. This phenomena turns transistor M62 to ON position. At this time transistor M64 is turned off. Since M63 is off and the "Reset" signal is high therefore M66 is operational and the input to the transistors M67 and M68 (another inverter circuit)would be set to zero. Transistor M69 is ON due to the facts that the output of the first inverter circuit (M60, M61)is high. As it was stated before transistor M70 is also turned ON .Therefore the input to the third inverter circuit (M72 and M73) is high and the output of the third inverter is low. To accelerate this transfer a feedback transistor M71 is being used as pull up transistor. The introduction of the transistor M66 as the reset transistor causes the output to go to zero rapidly.

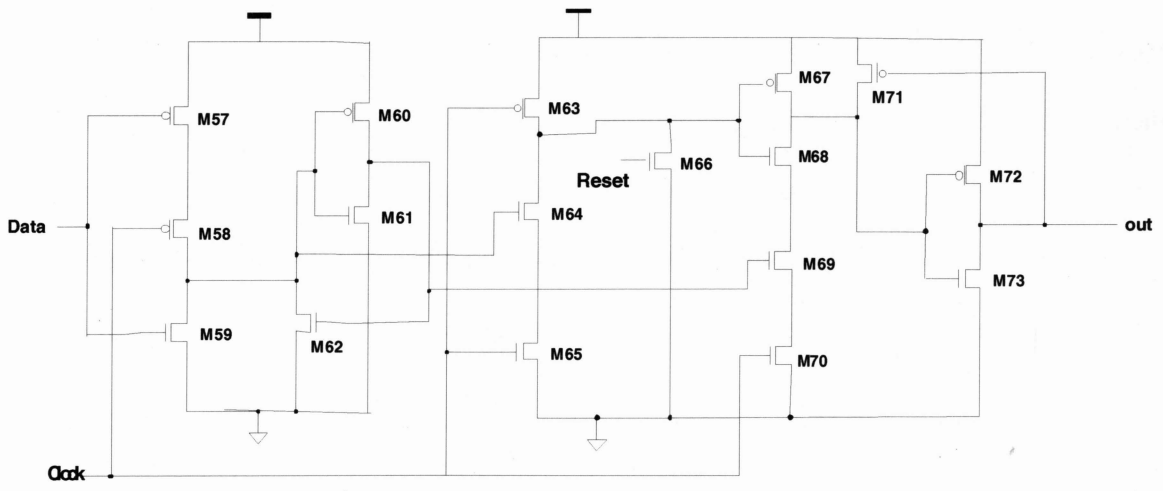

Figure 5.2 : The Schematic design of the D-Flip Flop (TSPC low Frequency)

If the positive edges of the "Input A" and "Input B" are exactly aligned then the two D- Flip Flops, turn on together, very quickly (signals "A" and "B" in Figure 5.5). The net output of this condition creates glitches resulting from imbalances between "A" and "B"signals. These glitches constitute the phase detector ripple waveform when the synthesizer is in equilibrium [25]. The ripple energy is very small and its spectral content is widely spread [25]. It is also important to design a D-Flip Flop and AND gate that is quick to response to the changes of the outputs of the D-Flip Flops.

5.2 Charge Pump and Loop Filter (LF)

5.2.1 Charge Pump

Design of the charge pump has been depicted in Figure 5.4. The implemented circuit has been modified from [5]. This topology is also called differential charge pump single ended output. Transistors M 74, M 76 and M 84, M 85 are used to switch the current in the differential pattern. There are three sets of current mirrors used in this design. Pair of M75, M 78 , the pair transistors of M79, M 80, and the pair transistors of M81, M 83. Additional transistors M77 and M82 would improve the transient performances of the charge pump by bringing M78 and M81 gate voltages back to VDD when "UpPositive" and "DownPositive" signals are disabled [24]. In Figure 5.5 when there is no difference between the phases of the "Input A "and "Input B" signals, therefore signals "A" and "B" don't show any phase differences. As the result output voltage of the loop filter doesn't make any changes. The Charge Pump thus remains idle and capacitor C2 sustains a constant voltage.

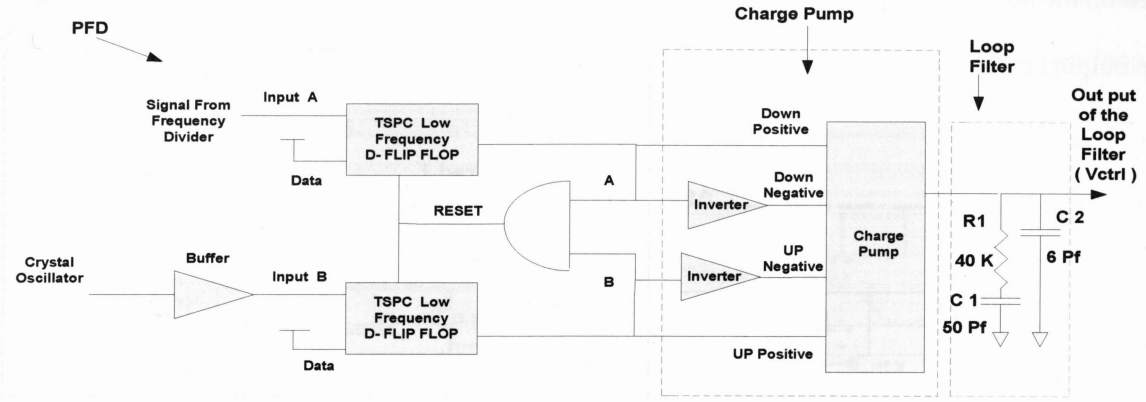

Figure 5.3 : The Open Loop system level design of the PFD + Charge Pump (C.P) + Loop Filter (Low Pass Filter)

In fact a charge pump converts the widths modulated output signals of the PFD (which consists of "UpPositive," "UpNegative," "DownPositive," "DownNegative") into a current whose amplitude is constant and its direction is controlled mainly by the "UpPositive" (signal B), or "DownPositive" (signal A). A charge pump can be considered as digital to analog converter. The higher the output amount of the charge pump current the higher the amount of the contributed noise to the PLL synthesizer. Therefore in the design of the charge pump special care should be given to the amount of the current which is being used by this device. One of the design constrains would be the fact that the higher charge pump current the higher the overall power consumption of the synthesizer.

By looking at Figure 5.9 the height of the charge pump current can be considered as I_{CP}. As it has been depicted from Figures 5.5 to 5.8 when the phase of the input signal (to the PFD) changes with respect to the reference signal, the duty cycle of the output signal of the PFD grows linearly with change of phase ($\Delta\Theta$). Therefore the average current of the charge pump is: $I_{out} = I_{cp} \frac{\Delta\Theta}{2\Pi}$.

Based on the above assumption a constant for the PFD/CP can be defined (as the average charge pump output current) for phase differences.

$$K_{PDF} = \frac{I_{out}}{\Delta\Theta} = \frac{I_{CP}}{2\Pi} \qquad [\text{A / rad}] \tag{5.2.1}$$

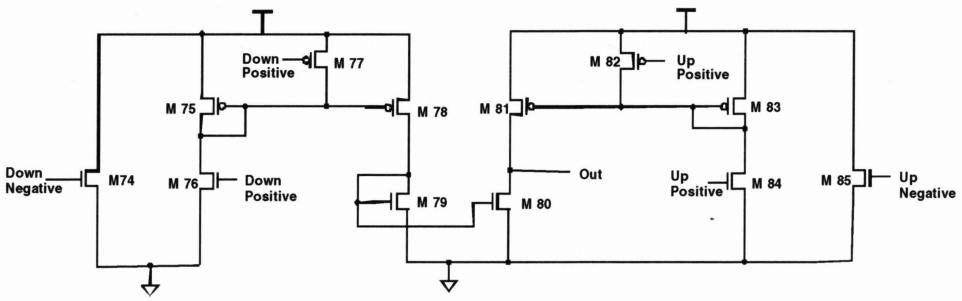

Figure 5.4 : The schematics of the Charge pump (CP).

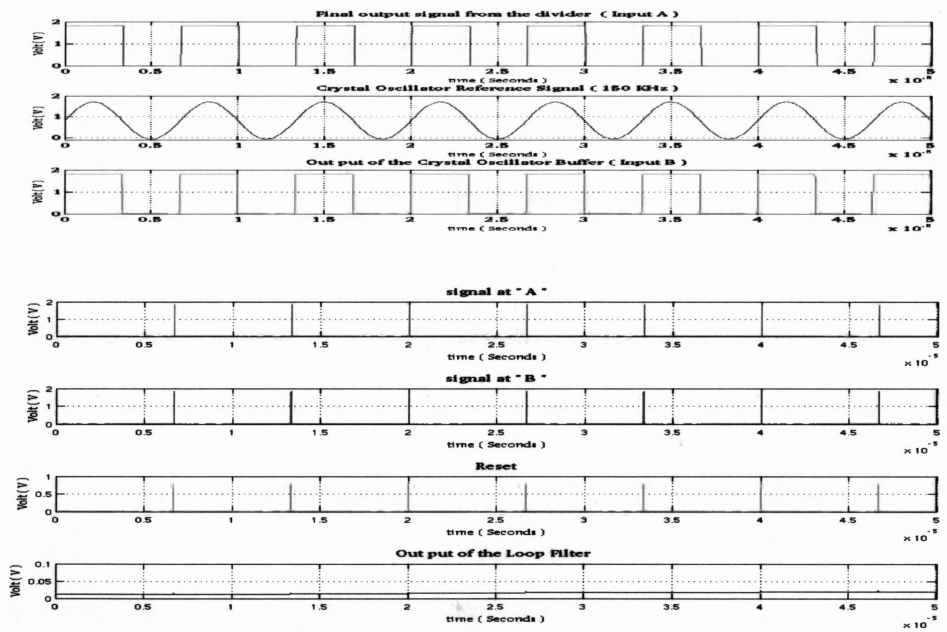

Figure 5.5 : Zero Phase difference between the Reference frequency and the divider output frequency. (open loop signal for the PFD, CP, and LF)

In Figures 5.6, 5.7, and 5.8 the phase difference of 90, 180, and 270 degrees have been introduced to the PFD, CP, and the Loop Filter. Each phase difference has been detected at the open loop test and translated as pulse widths.

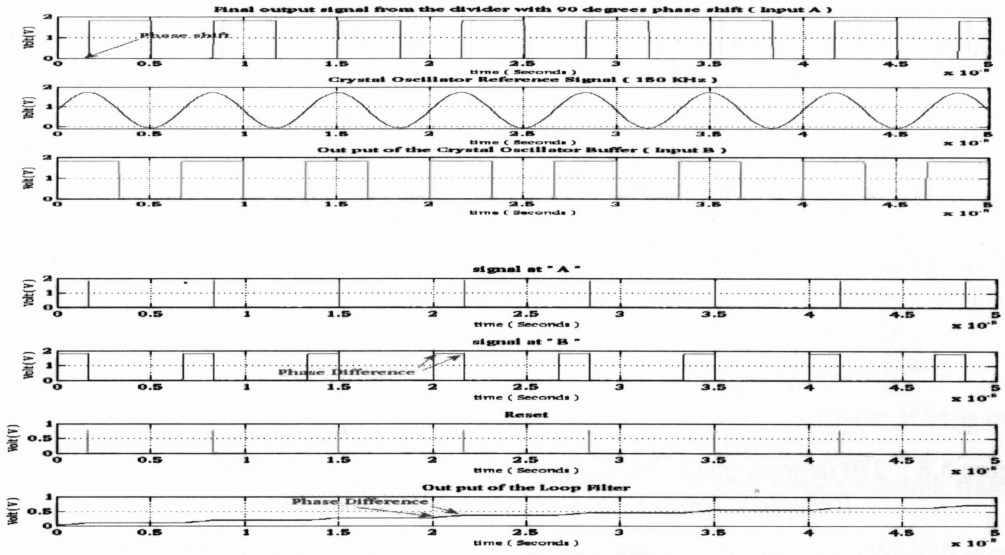

Figure 5.6 : 90 degrees phase difference between the Reference frequency and the divider output frequency. (open loop signal for the PFD, C P, and LF)

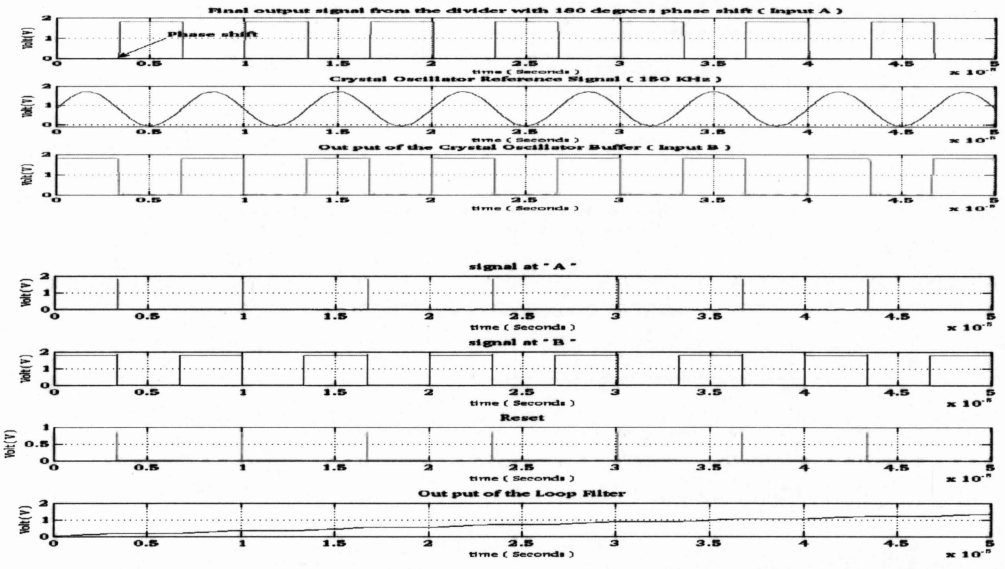

Figure 5.7 : 180 degrees phase difference between the Reference frequency and the divider output frequency. (open loop signal for the PFD, CP, and LF)

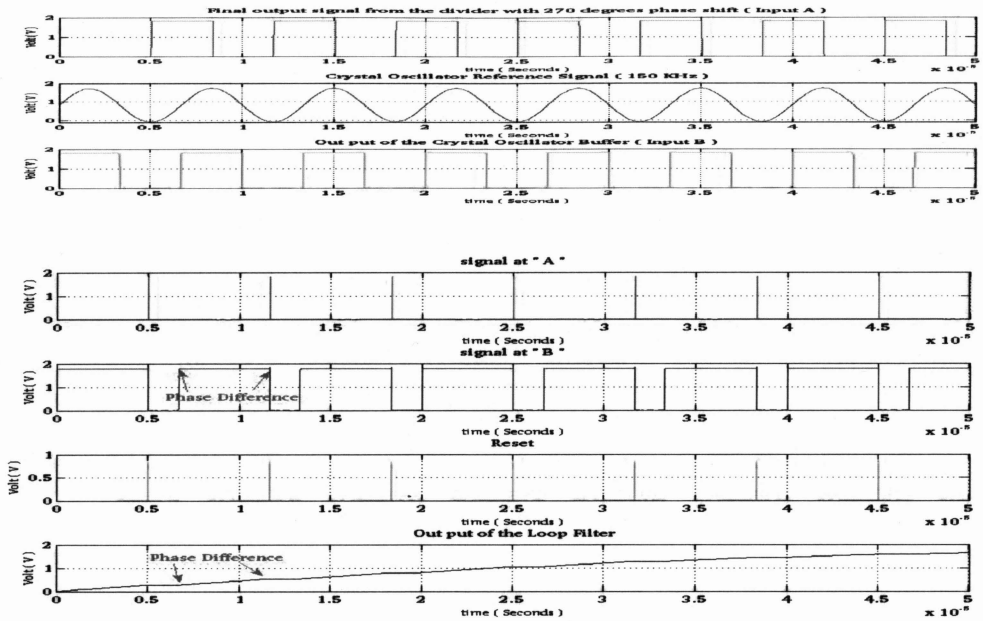

Figure 5.8 : 270 degrees phase difference between the Reference frequency and the divider output frequency. (open loop response signal for the PFD, CP, and LF)

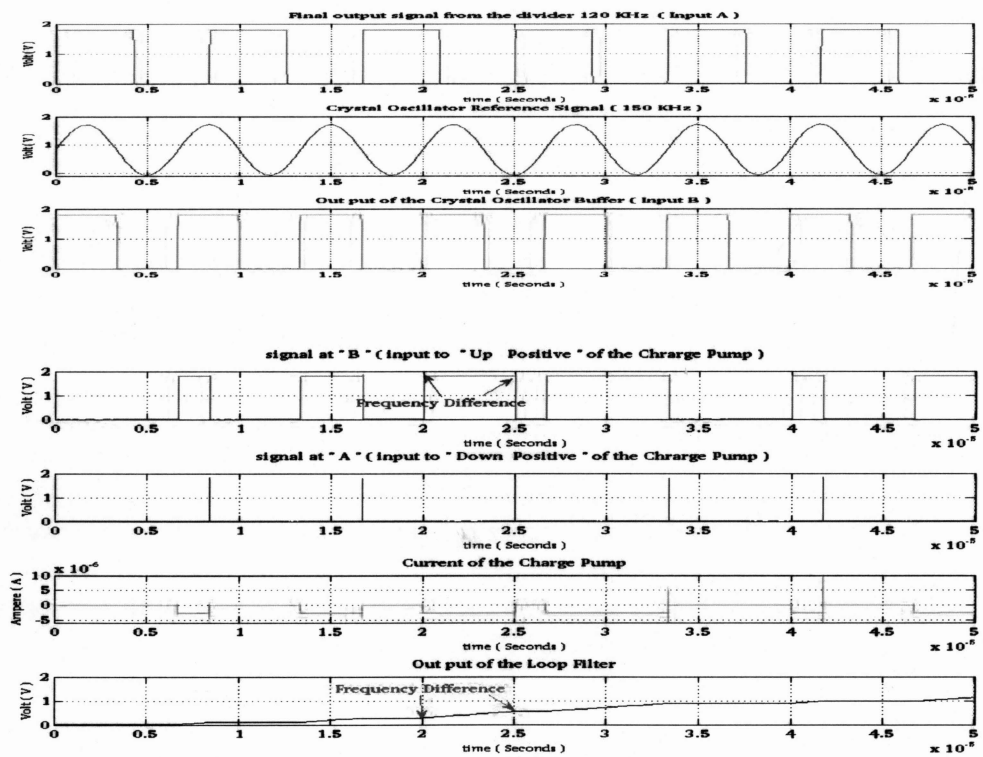

Figure 5.9 : The frequency difference of 120 KHz from the divider output and the 150KHz reference frequency.

Figure 5.9 represents the condition when the input frequency of the PFD is lower than the reference frequency. At this stage the PFD after detecting the frequency difference(shown at signal "B")increases the "UpPositiove" input to the charge pump which in turn increases the output voltage of the loop filter(Vctrl). That is why this signal is called the "UpPositive" signal. The current of the charge pump has been shown in Figure 5.9.

In Figure 5.10 by an increase in the input frequency to 160 KHz, the PFD detects the frequency difference and signal "A"("DownPositive") causes the change in output current of the charge pump which in turn it decreases the output voltage of the loop filter (Vctrl).

In Figure 5.4 when the "UpPositive"(signal "B") pulse width is high, the transistor M84 is on and the current mirror transistors M83 and M81 are also on. The current that passes through transistor M81 will be conducted to the output of the charge pump. The dimension ratio(Width/Length)of transistors M83 and M81 would be kept as unity. Since one of the main objectives of the design is a decrease in the power consumption the length of the transistors M85 and M84 has been increased by 17 times the minimum length. When the "DownPosivite"(Signal "A") is high, transistor M76 is operational and the current mirror transistor M75 and M78 are also in use. The ratio of the transistor lengths of M79 is 1.5 times more than the transistor M80. This design precaution has been implemented merely due to the fact that when the QVCO's control voltage has reached its peak voltage(maximum control voltage percent overshoot). The synthesizer circuit would have a faster decrease in voltage, to allow the closed loop response to reach to the steady state voltage level.

The dead zone phenomenon happens when there is no output from the charge pump in response to the phase error at the input of the PFD [26]. The usual cause of the dead zone is the sluggish response of the charge pump current switches reaction to the "UpPositve"(signal B)and

"DownPositive"(Signal A) coming from the PFD. Therefore great caution must be given in the design of the charge pump to make PFD/CP combination robust.

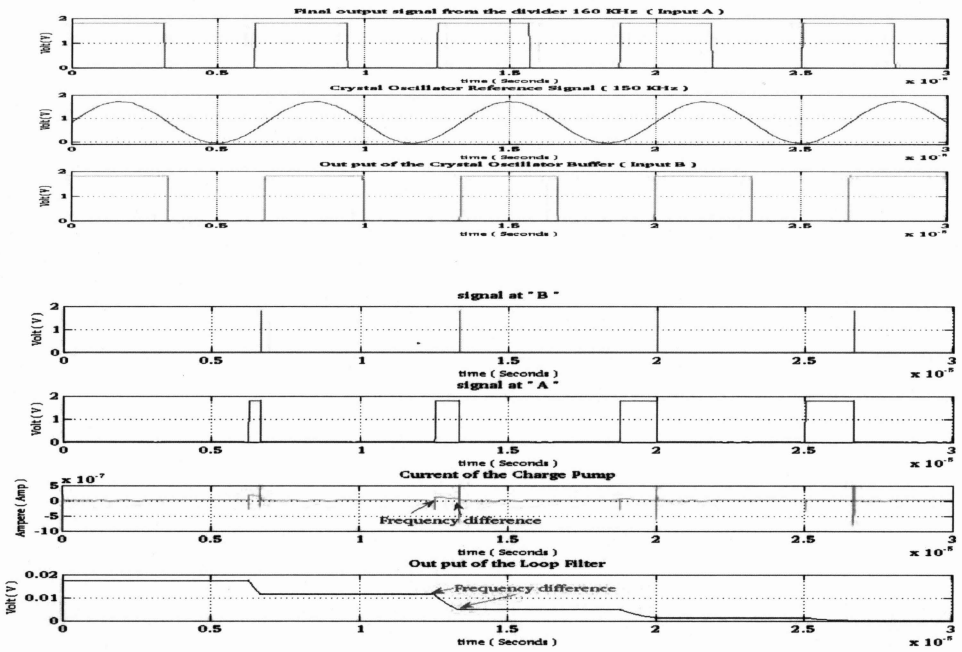

Figure 5.10 : The frequency difference of 160 KHz from the divider output and the 150KHz reference frequency

5.2.2 Loop Filter (Low Pass Filter)

The loop Filter (Low Pass Filter) which has been used in this design is shown in Figure 5.3. The disadvantage of using an active loop filter in the proposed synthesizer would be the increase in the complexity of the circuit, increase in the power consumption, and creation of more noise sources . This loop filter introduces a Pole and a zero to the overall design of the Synthesizer. Previously in Chapter 3 it was indicated that the QVCO also contributes a pole to the overall design of the circuit. Therefore the synthesizer order is of 3rd order, type II PLL.

The pole in the loop filter is created by capacitor "C1"(if considered by itself). It should be noted that introduction of another perfect integrator in the PLL loop leads to instability. To remedy this

scenario often a resistor is placed in series with the integrator capacitor (C1). This adds a zero to the trans-impedance of the loop filer. The "RC" combination causes a phase advance in the PLL open loop transfer response therefore solving the stability problem [9]. This synthesizer is considered type II due to the presence of the two perfect integrators in the topology. At the time that the charge pump is operational, the charge pump drives the series combination of R1 and C1. At each time that the current is being injected into the loop filter, the control voltage (Vctrl) experiences a large jump [22]. The resulting ripple severely disturbs the QVCO and corrupting the output phase [22]. That is why capacitor C2 has been introduced in parallel to R1, and C1. Capacitor C2 takes the ripple noise off the Vctrl signal. It should be considered that the value of the C1 > C2. Capacitor C1 should be one tenth to one fifth of the Capacitor C2 [22].

The overall role of the loop filter in the synthesizer is to convert the current pulses generated by the charge pump (as depicted in Figure 5.12) to a filtered voltage. This filtered voltage would control the QVCO output frequency. The loop filter frequency response has huge impact on the dynamic behavior of the Integer-N synthesizer. Figure 5.11 represents the Closed loop Control Voltage (Vctrl) at the output of the loop filter. Very often the PLL has to cope with DC leakage currents in the tuning line of the QVCO. The loop reacts to the leakage current by increasing the duty cycle of the charge pump output signal [9]. The amplitude of the spectral components of the charge pump current grows in direct proportion to the duty cycle [9]. Therefore some of the undesired signal components of the output current which are represented in Figure 5.12 as spikes in current are also converted to the voltage by the loop filter. The Voltage ripples that are created on the QVCO's Control Voltage would have the contribution to the output signal of the oscillator. Due to the high accuracy of the Figures 5.11 & 5.12 the 2% settling time can be found to be at 160μs and the charge pump current for 100 μs is also shown.

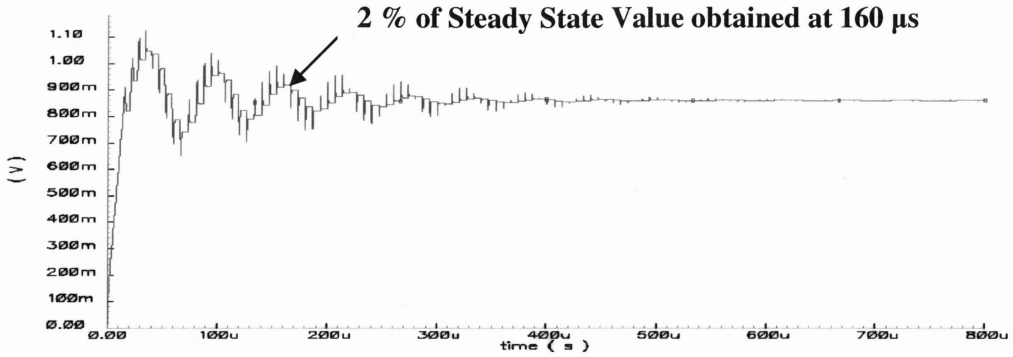

Figure 5.11 : The Closed loop Control Voltage transient response. (Vctrl)

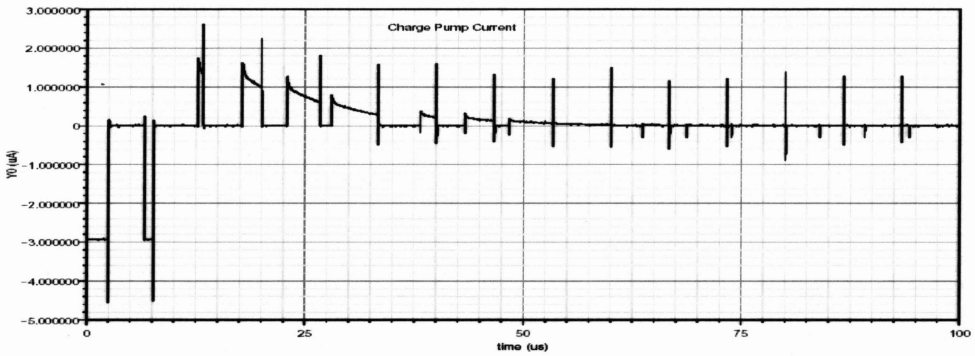

Figure 5.12 : The charge pump current

5.3 Open Loop and Closed Loop transfer functions

The loop considered in this design consists of a QVCO of gain K_{VCO} [Hz/V], a programmable divider of the ratio of N, a Phase Frequency Detector and a Charge Pump (PFD/CP), with the gain of $K_{PFD/CP} = I_{CP}/2\Pi$. (I_{CP} is the nominal charge pump current). Since there is a zero located at the loop filter therefore this zero can be expressed as $S_z = \frac{-1}{R_1 C_1}$. For simplicity the LF transfer function can also be shown as $Z_f(S)$ at Laplace domain [9]. However with the help of the similar analogy for the QVCO's Laplace domain (as the QVCO acts as an integrator in the PLL synthesizer Loop) the transfer function could be obtained as $2\Pi\frac{Kvco}{S}$. At the time when the loop is locked

the phase of the divided output signal accurately tracks the phase of the reference signal (Crystal Oscillator). The open loop transfer function of the design can be shown at Equation 5.2.2.

$$G(S) = K_{PDF/CP} Z_f(S) \frac{2\Pi K_{VCO}}{S} \frac{1}{N} \tag{5.2.2}$$

$$G(S) = \frac{I_{CP}}{2\Pi} Z_f(S) \frac{2\Pi K_{VCO}}{S} \frac{1}{N} \tag{5.2.3}$$

The Close Loop transfer function shall be obtained as Equation 5.2.5.

$$H(S) = \frac{G(S)}{1+G(S)} \tag{5.2.4}$$

$$H(S) = \frac{2\Pi K_{PDF/CP} Z_f(S)(K_{VCO}/N)}{S + 2\Pi K_{PDF/CP} Z_f(S)(K_{VCO}/N)} \tag{5.2.5}$$

The above closed loop transfer function H(S) shows that PLL synthesizer has a low pass transfer characteristic [9].

By looking at the loop filter, two time constants can be obtained as $\tau 1 = R_1 C_1$, and

$\tau 2 = R_1 \frac{C_1 C_2}{C_1 + C_2}$. The first time constant $\tau 1$ is also called "time constant of stabilizing Zero" and the second time constant $\tau 2$ is called the "time constant of the pole" which is used to attenuate the reference frequency and its harmonics [25]. The ratio of C_1/C_2 is called "b". Therefore in the Figure 5.3 the Loop Filters $\tau 1 = R_1 C_1 = (40K\Omega)(50\,pF) = 2\ \mu s$.

and $\tau 2 = R_1 \frac{C_1 C_2}{C_1 + C_2} = (40K\Omega)\frac{(50pF)(6pF)}{50pF + 6pF} = 0.214\ \mu s$.

The obtained value for "b" is equal to 8.33. For the purpose of the fast settling time, the close loop natural frequency ω_r of the synthesizer should be maximized but it can be close to about 1/10th of the reference frequency for the stability reasons [24]. Therefore $Z_f(S)$ can be expressed as:

$$Z_f(S) = \frac{1 + S(R_1 C_1)}{S(C_1 + C_2)(1 + SR_1 \frac{C_1 C_2}{C_1 + C_2})} \tag{5.2.6}$$

The Phase Margin Φ_m of the synthesizer can be calculated as indicated in [9] :

$$\Phi_m = \arctan(\frac{b-1}{2\sqrt{b}}) = \arctan(\frac{7.33}{2\sqrt{8.33)}}) = 52° \tag{5.2.7}$$

Since $\Phi_m = Cos^{-1}\xi$, (ξ the damping ratio)[27]. Therefore the obtained ξ = 0.6. From the Control Voltage (Vctrl) of the synthesizer (Figure 5.11) the 2% settling time is observed to be at 160 μs. The settling time is defined as the time the PLL takes to settle with in the lock range and is primarily dependent on ξ [28]. Substituting this data in Equation 5.2.8 would result in the approximate value of ω_n (the open loop band width frequency).

$$T_{settlement2\%} \cong \frac{4}{\xi\omega_n} \tag{5.2.8}$$

$$\omega_n \cong 41.6 \text{ KHz}$$

The Close loop resonant frequency (ω_r) of the PLL synthesizer can be approximated obtained by Equation 5.2.9 to be equal to 21 KHz. [29].

$$\omega_r = \omega_n \sqrt{1 - 2\xi^2} \tag{5.2.9}$$

$$\omega_r \cong (41.6K)\sqrt{1 - 2(0.6)^2} \tag{5.2.10}$$

$$\omega_r \cong 21 \text{ KHz}$$

The approximate value for ω_r is close to one tenth of the reference frequency. The overall current usage of the Analog components of the Integer-N PLL synthesizer is at 2.6mA. This in turn would result in 4.68 mW power consumption.

5.4 Summary

The Phase Frequency Detector (PFD) has been designed based on TSPC low frequency topology. In this design a reset transistor has been introduced to the TSPC circuit and this topology is capable of producing a faster response time. The output of the PFD is the representation of the phase and frequency error between the divided signal and the reference clock signal. The charge pump converts the pulse width generated by the PFD to current. The charge pump designed has been a simplified to decrease the power consumption mean while maintaining a faster response time. The loop filter also introduces a zero and a pole to the overall circuit topology. The loop filter also takes away the noise ripple of the control voltage. The total power consumption of the PFD, CP, and LF is about 500 μW.

Chapter 6
Comparison and Conclusion

6.1 Comparison

This thesis presents a low phase noise, wide frequency range, QVCO topology with current reuse technique. Also slight modifications of TSPC D-Flip Flop and a differential charge pump are proposed. The power consumption of the different modules of the Integer –N PLL synthesizer has been indicated in Table 6.1.

Table 6.1 : The power consumption for each component.

Module	Power consumption
QVCO (without Buffer)	0.9 mW
QVCO (with Buffer)	1.8 mW
Prescaler 32/33 (divider)	2.3 mW
PFD+CP+LF	0.5 mW

The total power consumption of the synthesizer is approximately at 4.6 mW by considering the leakage currents and total power consumption of all components. The comparison of the measured values of QVCO results from the authors at [15] and the simulated results of this thesis have been depicted in Table 6.2. The authors at [15] have produced two different types of QVCOs. One by utilizing LC tanks (spirals) and another one with the use of ring oscillators.

This thesis proposed design is capable of producing frequencies from 200MHz to 827 MHz. However the proposed design has been targeted mainly for the MICS(Medical Implantable Communication Services) at frequencies 402-406 MHz. As indicated in [15] the acceptable phase noise level for the MICS band devices is at -83 dBc/Hz. One of the improvements that has been

observed in this thesis is achieving a low level of phase noise without utilizing any spiral (LC tank). The amount of power dissipation of the QVCO has been kept at a reasonable level with respect to the total power consumption of the Integer-N synthesizer.

Table 6.2: Comparison of QVCOs

	Proposed Method	A. Tekin, 2006 First method [15]	A. Tekin, 2006 Second method [15]
Output type	QVCO	QVCO	QVCO
Type of oscillator	Ring oscillator	Ring oscillator	LC tank (Spiral)
Technology	TSMC 0.18 μm	TSMC 0.18 μm	TSMC 0.18 μm
Frequency Range	402-406 MHz (200 – 827 MHz)	402-406 MHz (370 – 440 MHz)	402-406 MHz (350 – 460 MHz)
Power supply	1.8V	1.5 V	1.5 V
Power consumption	0.9 mW	1 mW	1.2 mW
Phase noise for 400 MHz oscillation @160 KHz offset	-100.3 dBc/Hz	-83 dBc/Hz	-98 dBc/Hz
# of stages	2	4	_____
Temperature	37° C	_____	_____

Table 6.3 indicates the comparison between the design of the proposed QVCO and a VCO by authors at [30]. The obtained results would indicate that this thesis QVCO's power consumption is almost comparable to the power consumption of VCO circuit at higher technology level which makes this design more desirable for low power devices. This phenomena is achieved without relative loss of phase noise.

Table 6.3 : Comparison of the proposed QVCO with another VCO

	Proposed Method	A. Ayed, 2007 [30]
Technology	TSMC 0.18 μm	CMOS AMS 0.35 μm
Oscillator type	Ring oscillator	Ring oscillator
Output type	QVCO	VCO
Frequency Range	433 MHz	433 MHz
Voltage swing	1.6 V	0.3 V
Power supply	1.8 V	1.5 V
Power consumption	0.9 mW	0.8 mW
Phase noise for 433 MHz	@ 160 KHz offset -99.5 dBc/Hz	@ 500 KHz offset -100 dBc / Hz

The Integer-N PLL synthesizer that is offered by the author shall also find some practical usage in industry. At the time of writing this thesis there are products available in the industry by Zarlink Semiconductor for Implantable devices at MICS and 2 channels (433-434 MHz).This transceiver is also designed in 0.18 μm technology. Based on the Medical Implantable RF Transceiver (ZL70101) data sheet the power supply on this device runs at 2.1V - 3.5 V. The total chip has the power consumption of (@ 5mA current) 10.5 mW-17.5 mW [31]. With respect to the total amount of the power which is being dissipated by the entire transceiver the amount of the power usage of the Integer-N synthesizer offered by this thesis is at a reasonable level. There are also other aspects such as usage of a lower reference frequency (Crystals)of 150KHz, which would lead to a lower price for the final product. However one of the trade offs such a consideration would be a slightly bigger size for crystal oscillator. At this time (based on Digikey Corporation's catalog) a 24 MHz crystal oscillator's (ABM10 Series 2.5-2.0 SMD) size is 2mm× 2.5mm× 0.55mm and a 150 KHz crystal oscillator's size (ECS-31-Series) after modification approximately is 6.2mm ×2.1mm× 1mm.

As it is shown above the size of the external components of the device might increase slightly however it should be considered that the proposed Integer-N synthesizer has the power supply of 1.8 V which in turn utilizes a smaller size battery. A 150 KHz crystal oscillator also has a lower price and a lower phase noise by comparison to a 24 MHz crystal oscillator. This in turn contributes to the lower overall phase noise of the PLL synthesizer. ZL70101 uses LC spirals for the oscillators combined with divide by 4 circuits which make the implantable device larger [32]. However since the required phase noise of the MICS devices are at -83 dBc/Hz therefore the presence of the large spirals could be replaced by a ring oscillator [15].

6.2 Conclusion

The proposed Mixed-mode Integer-N PLL based synthesizer has been simulated in TSMC 0.18 μm technology with 1.8V power supply. A QVCO with a wide operational range, low power dissipation, and a low phase noise based on current reuse method has been designed. With respect to the spiral inductors this design also has a smaller size. A 32/33 prescaler with frequency operation of up to 827 MHz was designed. This inter-modularity of the prescaler makes the schematics also more promising for other industrial applications. The phase frequency detector of the synthesizer was created by introducing a reset signal to a TSPC D-flip flop which makes the design faster. The overall result of the simulation achieved the expected 2% steady stage settling time for the closed loop control voltage at around 160 μs with a reasonable power consumption of 4.6 mW with respect to the overall power dissipation of the total transceiver chip (10.5mW-17.5mW).

6.3 Future Work

The chip can be fabricated in TSMC 0.18 μm technology. Due to the limitations of the software at Ryerson university programming of the Digital part of the counters could be done in a fashion that the user can adjust the frequency channels. There is also the issue of bringing the power consumption of the divider component to a lower level. In fact decreasing the power dissipation in the prescaler has the highest priority in the overall improvement of the design. This can be done by sacrificing the inter-modularity of the design and providing a divider which only operates at 200MHz – 540MHz. Also performing the phase noise analysis of the whole entire synthesizer based on specifications of each module can be addressed in the future.

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