SUBTHRESHOLD FREQUENCY SYNTHESIS FOR IMPLANTABLE MEDICAL DEVICES

by

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Subthreshold Frequency Synthesis for Implantable Medical Devices

Master of Applied Science 2010

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Electrical and Computer Engineering

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In this thesis, several novel circuits for use in an ultra-low power integer-n frequency synthesizer operating in the 402 MHz to 405 MHz Medical Implant Communication Service spectrum have been proposed. The proposed designs include a current-reuse quadrature voltage-controlled oscillator, a novel subthreshold source-coupled logic D-latch with clear and preset functionality, a programmable frequency divider and phase/frequency detector based on the aforementioned D-latch, and a modified current-steering charge pump. A design methodology for low-power CMOS oscillators was proposed based on the MOS EKV model and g_m/i_d design methodology. The proposed designs were implemented using IBM CMRF8SF 130 nm CMOS technology and simulated using Cadence Spectre. Simulation results for the proposed current-reuse quadrature voltage-controlled oscillator and programmable frequency divider consume 420 μW and 200 μW respectively from a 0.7 V supply, a significant improvement compared to existing designs. The simulated phase noise of the proposed oscillator is -127.2 dBc/Hz at a 1 MHz offset. Measurement results from a fabricated prototype of the current-reuse quadrature verify the simulation results and serve as a proof-of-concept for the proposed design. The proposed designs were used to implement an integer-n frequency synthesizer and were submitted for fabrication. Simulation results show that the synthesizer consumes 635 μW from a 0.7 V supply and has a locking time of 250 μs.

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Although the research performed in this thesis was an individual effort on my part, there were many people who contributed in different ways to its completion.

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Finally the committee members for my thesis defence, Dr. James Smith, Dr. Vadim Geurkov and Dr. Farah Mohammadi for taking the time to read my thesis and provide comments from their unique perspectives.

Dedication

To my late grandmother, Qamar Jabbar, who passed away in March 2010.

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Chapter 1

Introduction

1.1 Motivation

Over the last decade in Canada, the medical devices industry has received a significant amount of attention. The Auditor General's 2004 Report to Parliament noted that "medical devices play an important role in all stages of delivery of health care [1]," and the National Research Council has "identified Canadas medical devices industry as one of the key sectors in which its expertise, multi-disciplinary competencies and infrastructure can make significant scientific and technological contributions to help industry respond to the considerable global medical device market expansion that is expected in the coming years [2]." According to Industry Canada's Medical Device Industry Profile the Canadian medical devices market was valued at \$7.5 billion in 2008, up from \$5 billion in 2000, and employment rose from 22,000 in 2000 to 26,000 in 2005 [3]. The diverse range of medical devices for diagnosis, prevention and treatment of diseases, disabilities and other ailments which Canadians and those abroad rely on could not have been possible without the scientific and technological advancements of recent years. Design and development of medical devices is a multidisciplinary research area involving many scientific and engineering disciplines. Advancements in the fields of biotechnology, advanced materials, telecommunications, software and informatics, and microelectronics have all contributed to the exponential increase in the number of new devices being developed.

In recent years, the aggressive scaling of Complementary Metal-Oxide Semiconductor (CMOS) technology has allowed for not only the reduction in the physical size on an integrated circuit (IC), but also the ability to include many more components onto a single die. These devices, known as System-on-Chip (SoC), can hold a combination of analog (i.e. filters, signal conditioning, ADC), digital (memory, DSP, DAC), and RF (transmitter, receiver, antenna) components. These advances have allowed for the development of new devices such as handheld devices. In cell phones and PDAs, increasing capabilities are not accompanied by increasing sizes. Using high density solid state memory instead of miniature hard drives has allowed for increased storage in MP3 players. Similarly in medical electronics the miniaturization of devices for patient monitoring and treatment has created a new class of electronics: implantable medical devices (IMDs). This thesis will focus on the latter, specifically wireless IMDs for biotelemetry, which is defined as the measurement and transmission of physiological signals.

Implantable medical devices have evolved greatly since the first pacemaker was designed in the 1950s. The current generation of IMDs are capable of replacing damaged or malfunctioning organs, and are designed for long-term patient care. Cochlear implants, which differ greatly from hearing aids, convert received audio signals to electrical impulses and are capable of bypassing damaged parts of the ear and interfacing directly with auditory nerves [4]. Microstimulators for neuromuscular stimulation can restore functionality to paralysed limbs. Implantable drug administration devices can deliver precise amounts of a drug, such as insulin for diabetics, at particular intervals, replacing the need for regular injections. Wireless IMDs designed for biotelemetry applications include implantable ECG and EEG recording, intra-ocular pressure sensing and wireless endoscopy capsules. More examples of IMDs are shown in Fig. 1.1.

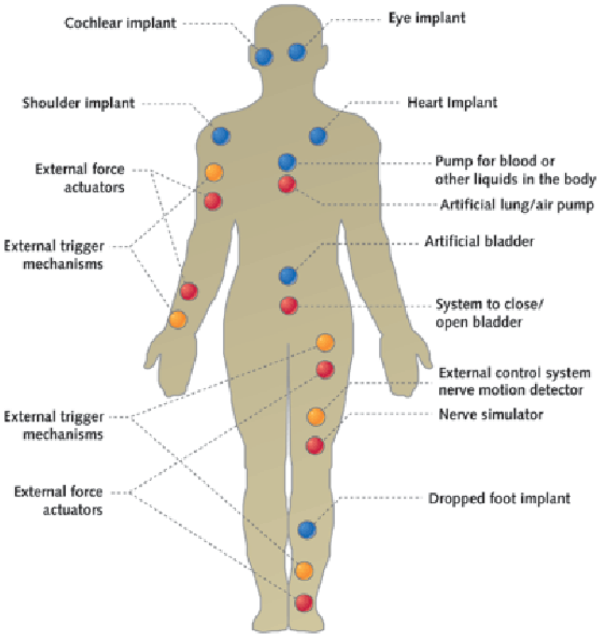
Cochlear implant
Eye implant
Shoulder implant
Heart Implant
External force actuators
Pump for blood or other liquids in the body
Artificial lung/air pump
External trigger mechanisms
Artificial bladder
System to close/ open bladder
External control system nerve motion detector
Nerve simulator
External trigger mechanisms
External force actuators
Dropped foot implant

Figure 1.1: Examples of patient health monitoring using implantable devices [5].

There are numerous benefits of these IMDs in the health care industry. Since the devices can provide real-time, continuous monitoring of physiological parameters, patient mobility increases since they no longer need to be tied to the monitoring equipment. For example, when a heart patient requires constant, long term monitoring of the ECG signal, the data can be transmitted wirelessly rather than the patient having to wear ECG measurement leads and having some external device to monitor and collect data. As well, they can save the patient from undergoing an uncomfortable and invasive procedure. The wireless endoscopy capsule is an ingestible pill camera which wirelessly transmits the observed data to an external receiver, a welcomed alternative to traditional endoscopy which involves the insertion of a long tube down the throat of a patient. Since all the data can be transmitted wirelessly to a central monitoring station such as a nurses station in a hospital, monitoring of patient vitals can be performed less frequently since all the data is being collected in real-time providing easy access for doctors and nurses.

Implantable medical devices can be split into two categories: passive and active. Passive devices are designed with the sole purpose of monitoring a particular physiological parameter, while active devices are able to perform some action in response to a change in the physiological parameter being measured. For example, visual and hearing aids are considered as passive devices and drug pumps for insulin delivery and cardiac rhythmic management systems are active devices [6].

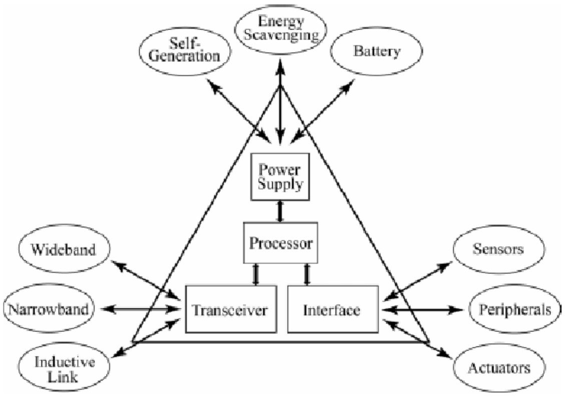

Figure 1.2: General block diagram for an implantable medical device [7].

Figure 1.2 shows the block diagram for an arbitrary wireless IMD. Inside the triangle are the core components of the IMD, namely the power supply, processor, interface and transceiver.

1.2 Medical Implant Communication Service

1.2.1 Overview

The Medical Implant Communication Service (MICS) was established in 1999 (Proposed Feb 12; Adopted November 19) to provide a dedicated frequency spectrum for ultra-low power (ULP) implantable medical devices (IMDs) that would overcome the shortcomings of existing spectra available for these devices. Existing IMDs were typically magnetically coupled to the external control devices, which required very close spacing between the implant and external device to allow for reliable operation. Additionally, the magnetically-coupled devices suffered from low data transmission rates. The proposed MICS spectrum would allow for devices to enjoy the benefits of the advances in wireless technology and communications. RF transmission would afford the patient increased mobility since they no longer need to sit in uncomfortable positions to achieve optimal magnetic coupling to the reader, and increased data rates would reduce the data collection time and give physicians quicker access to physiological data for faster diagnosis.

The MICS band was proposed to operate in the 402 MHz to 405 MHz UHF spectrum for several reasons. Firstly, the spectrum exhibits favourable propagation characteristics through the human body compared to other spectra that have been allocated for use by physicians and health care providers. These bands are also at risk for interference from high power carriers operating in the same spectrum. Secondly, the spectrum is available worldwide, unlike the ISM UHF bands which require dual band operation to satisfy international regulations, complicating the design of the device. Finally, the operating frequency allows for the device to use an integrated antenna whose dimensions are suitable for implantable devices.

The MICS band shares its spectrum with METAIDS meteorological devices operating in the 401 MHz to 406 MHz band, and therefore has been designated to operate on a secondary, shared basis. Since the radiated power from the IMD is small and confined to small distances, the probability that an MICS device will interfere with a METAIDS device is very low. However MICS devices must accept interference from METAIDS devices, therefore designers must be careful to make IMDs robust to noise.

The types of devices which are permitted to operate in the MICS band are those which are used for therapeutic and diagnostic purposes, and they can only be used to transmit non-voice data. These devices include implantable cardiac defibrillators (ICDs), pace makers, blood glucose monitors, implantable vagus nerve stimulators and deep brain stimulators.

Operating guidelines for the MICS standard have been established by several international regulatory authorities such as the United States FCC [8], Industry Canada Spectrum Management and Telecommunications [9], the Australian Communications and Media Authority [10], and the European Telecommunications Standards Institute [11], and an overview of these regulations is provided in the next section.

1.2.2 Technical specifications

As mentioned previously, favourable propagation characteristics, international availability and low probability of interference are the reasons for choosing the 402 MHz to 405 MHz spectrum for the MICS band. Although there is no fixed channel arrangement for the MICS band, an MICS channel is permitted to have an emission bandwidth between 25 kHz and 300 kHz. An example channel arrangement with ten 300 kHz channels is shown in Fig. 1.3. The maximum equivalent isotropically radiated power (EIRP) for each channel is limited to 25 μW (-16 dBm), and the power at the band edges should be attenuated by 20 dB from the carrier signal. The typical transmission range for IMDs is approximately 2 m. The transmitter data is collected by a medical implant programmer/controller which is operated by a “duly authorized health care professional” such as a physician. The US FCC has specified the following operating guidelines for MICS transmitters:

- Frequency agility: Before transmission takes place, the transceiver should perform Clear-Channel Assessment (CCA) to determine which available channel has the lowest ambient noise, and begin transmission once the best channel is found.
- A MICS communication session must be initiated by an external medical implant programmer/controller transmitter or in response to a medical implant event. During a medical implant event, the

transceiver may begin transmission on the first available channel regardless of its noise characteristics.

To satisfy regulatory and power saving requirements, MICS transmitters are not intended to be used for continuous data transmission. In order to extend the battery life of the IMD, circuitry should be powered down when not transmitting. A low power wake-up receiver such as the one used in [12] is needed to detect when a communication session is being requested. Regulations state that an MICS transmitter is permitted to transmit only at the request of an external programmer/controller operated by a duly authorized health care processional or in response to a "medical implant event" – that is, an unwanted change in the physiological parameter being observed which requires immediate transmission of data to protect the safety and well being of the patient, detected either by a duly authorized health care provider or by the implant itself.

Before the MICS transmitter begins to transmit, it must scan all available channels to find the unused channel with the lowest ambient noise. This type of frequency monitoring is called Adaptive Frequency Agility/Listen Before Talk (AFA/LBT). In order for a channel to be usable for transmission, the ambient noise should not exceed the monitoring threshold given by

$$10\log_{10}\mathrm{B}\ (\mathrm{Hz})\ -\ 150\ (\mathrm{dBm/Hz})\ +\ \mathrm{G}\ (\mathrm{dBi}), \tag{1.1}$$

where B is the bandwidth and G is the MICS programmer/controller antenna gain relative to an isotropic antenna.

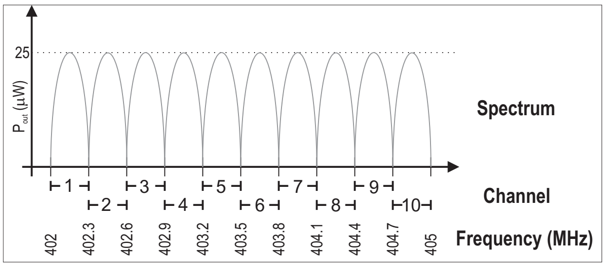

Figure 1.3: Allocated frequency spectrum for Medical Implant Communication Service.

In 2009, the 402 MHz to 405 MHz MICS band was expanded to accommodate new types of implantable and external medical devices. The two "wing" bands, 401 MHz to 402 MHz and 405 MHz to 406 MHz were added to the spectrum, and the band was renamed to the Medical Device Radiocommunication Service (MedRadio) [13], [14]. While the "core" 402 MHz to 405 MHz spectrum retains its original purpose (AFA/LBT IMDs for time-sensitive, life critical applications), the wing bands may be used for body worn devices which were not previously allowed to operate in the core band. Specifically, the devices can employ Low Power, Low Duty Cycle (LP-LDC) spectrum access with a reduced carrier power of 250 nW EIRP and occupy a maximum bandwidth of 100 kHz per channel. This allows for an additional 20 devices to operate in the new spectrum. The wing bands have been deemed more suitable for devices that might not have the same quality of service demands as those life critical implants operating in the core band. These external devices, which do not have stringent requirements on power consumption, can use a narrower bandwidth and more transmissions of greater duration with the possibility of retransmits without significantly compromising patient care or safety. The existing core band is more suitable for short-duration, high speed, data-intensive transmission, which conforms with the battery saving measures used for implanted devices. A summary of the operating specifications for the new MedRadio frequency band is given in Table 1.1.

Frequency Band	Minimum Bandwidth	Maximum Bandwidth	Maximum Transmit Power	Spectrum Access Method	Type of Device
401 MHz to 402 MHz	25 kHz	100 kHz	250 nW[1]	LP-LDC	External
402 MHz to 405 MHz	25 kHz	100 kHz	25 μW	AFA/LBT[2]	Implantable
405 MHz to 406 MHz	25 kHz	100 kHz	250 nW	LP-LDC	External

Table 1.1: MedRadio operating specifications

As with the original MICS specifications, the MedRadio band does not have a fixed channel arrangement. An example of a fully occupied spectrum is shown in Fig. 1.4.

In order to ensure that the MICS transmitter satisfies all regulatory requirements in regards to emission limits, the IMD is tested inside a test fixture modelling the human torso. The test fixture, shown in Fig. 1.5, is made from a plexiglass cylinder measuring 30 cm by 76 cm, and a sidewall thickness of 0.635 cm. The test fixture is filled with a fluid whose permittivity and conductivity match those of human muscle tissue at 403.5 MHz. The implant is centred vertically and placed 6 cm from the sidewall of the container, and is 1.5 m from the ground level.

1.2.3 Existing work

Although it was officially established in 1999, the MICS band did not receive significant attention from the academic and research communities until almost 2006. Taking into consideration the main design constraints of IMDs, namely ultra-low power consumption to increase battery life and maintaining acceptable RF performance (phase noise, spurious tones, bandwidth and transmit power), several designs for transmitters, receivers, antennas [16], [17], low-noise amplifiers [18], [19], voltage-controlled oscillators and PLL frequency synthesizers have been proposed which attempt to address these criterion. The scope of this work is limited to the voltage-controlled oscillator and PLL frequency synthesizer, and an overview of recent publications in this area will be discussed. However, the reader is encouraged to refer to the above-mentioned references in order to obtain a more complete picture of the state of the art research in MICS transceivers.

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[1] A 150 kHz channel occupying 401.85 MHz to 402 MHz can have an output power of 25 μW.

[2] A 300 kHz channel centred at 403.65 MHz can use LP-LDC spectrum access at a reduced output power of 100 nW.

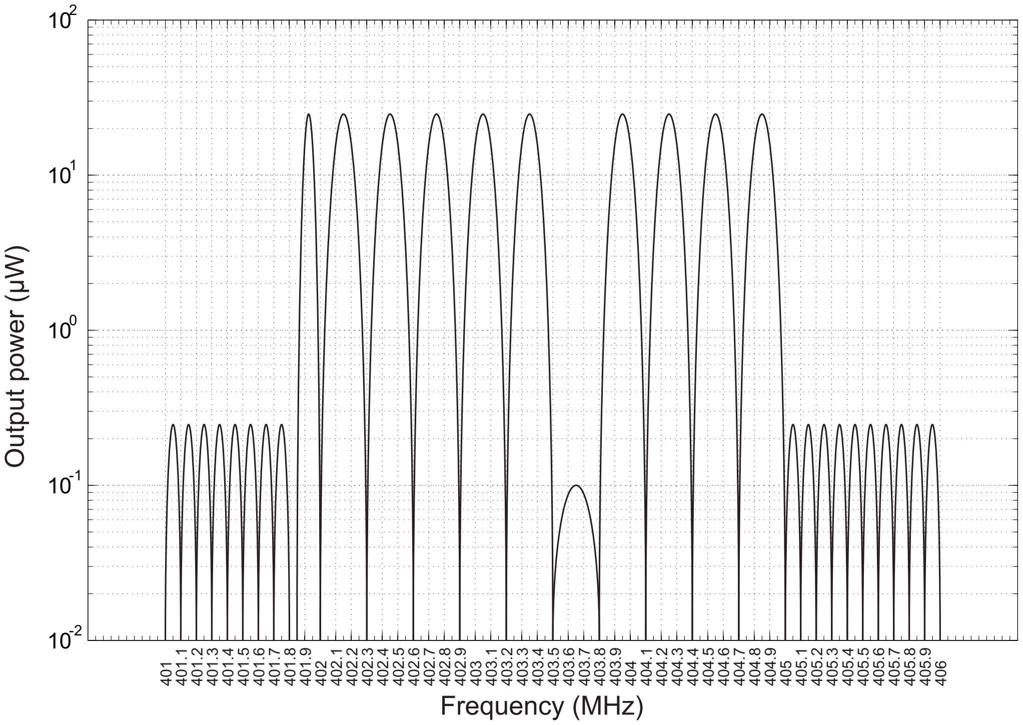


Figure 1.4: Allocated frequency spectrum for Medical Device Radiocommunication Service.

The *LC* VCO presented in Chapter 2 has been used in several previously published works. In [20], the authors proposed an MICS transceiver front-end whose LO is produced using an integer-n frequency synthesizer with quadrature outputs. Implemented in a 130nm CMOS process, the entire PLL consumes 1.2 mW from a 1.2 V power supply. The authors of [21] studied three different MICS VCO architectures designed in a 180 nm CMOS process, two of which used *LC* VCOs. The first operated in the MICS frequency band and used a polyphase filter to produce quadrature outputs, the second operated at twice the MICS frequency and used a master-slave divide-by-2 to produce quadrature outputs. Results showed that the first method consumed 1.2 mW from a 1.5 V supply, while the second consumed 3.3 mW from a 1.5 V supply. The authors of [21] used a dual band VCO in proposed transceiver, operating at 1 GHz and 400 MHz for the transmitter and receiver respectively, but did not reveal specific performance details.

A modification to the *LC* VCO used in several proposed designs is called a digitally controlled oscillator (DCO) [22]. In this topology the *LC* tank is modified to include an array of binary-weighted capacitors which can be enabled or disabled by a control bit. Rather than use an analog control voltage as an *LC* VCO does, the DCO uses an n-bit control word and by changing the control word the resonant frequency of the tank will change. The authors of [23], [24] and [25] used DCOs in their MICS designs, consuming 600 μW, 500 μW and 300 μW, respectively.

Ring oscillators are part of another family of oscillators called phase-shift oscillators. Although they

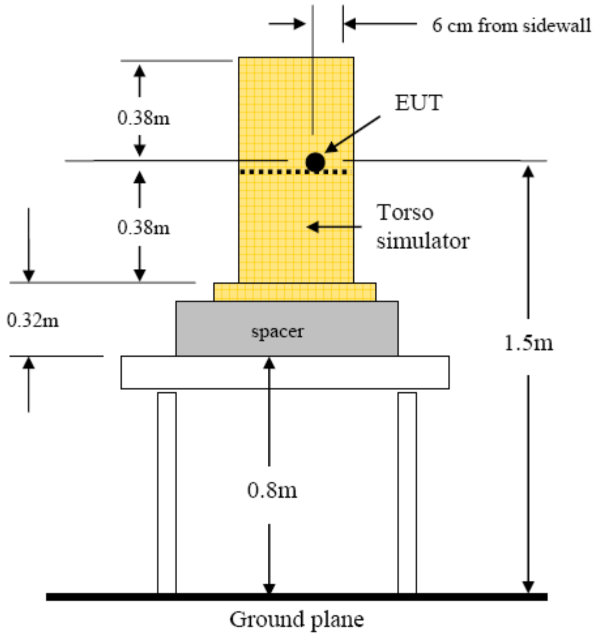


Figure 1.5: Medical Implant Communication Service implant torso simulator [15].

consume a small fraction of the area compared to resonator oscillators, such as the *LC* VCO, they demonstrate poor phase noise performance because of the number of active devices used to implement the oscillator. Nevertheless, the authors of [26] used a four stage differential ring oscillator. Despite citing power saving as the reason for choosing this topology, the ring oscillator consumed 1.1 mW from a 1.5 V supply, more than the previously presented *LC* VCOs and DCOs. As part of their investigation, the authors of [21] implemented a similar four stage ring oscillator. Although in this case it did consume less power than the two *LC* VCOs in the same study, it showed significantly worse phase noise performance in comparison.

A fairly unknown modification to the traditional *LC* VCO is the single-ended cross-coupled oscillator, which uses the half-circuit of a complementary *LC* VCO (which consists of both NMOS and PMOS negative resistance pairs). By virtue of requiring half the bias current, the implementation proposed in [27] consumes less power than those oscillators presented previously (230 μW from 1.5 V supply) but it lacks differential signals which are crucial for common mode noise rejection. This idea was extended by the authors of [28], who proposed an injection-locked single-ended cross-coupled oscillator. The design demonstrates very good phase noise performance, but at the expense of high power consumption (1.2 mW from a 1.2 V power supply).

A full summary of the performance of the designs presented in this section will be given in Chapter 4 when comparing the existing works with the design proposed in this thesis.

1.3 Project objective and target applications

The objective is to design an ultra-low power CMOS integer-n frequency synthesizer for use in a wireless implantable medical device operating the the 402 MHz to 405 MHz Medical Implant Communication Service spectrum. The synthesizer must have the following characteristics:

- Integrability: The synthesizer should utilize as few off chip components as possible (ideally none) to achieve the required specifications and functionality, and to decrease its physical size and cost.
- Flexibility: It should be possible to implement the frequency synthesizer in various wireless implantable medical devices which include sensors and transducers to transmit and receive physiological information, provided that the appropriate signal conditioning is included.
- Reliability: Since the device is to be implanted into a human body, manual adjustments to components cannot be made (i.e. potentiometers, biasing). Thus the synthesizer should be as insensitive as possible to process variations and temperature in order to provide accurate and stable carrier frequencies for data transmission under all conditions. Additionally, a stable power supply and biasing source is necessary. However the design of such circuitry is beyond the scope of this paper.
- Ultra-low power consumption: In order to achieve long battery life, measures should be taken to ensure that power consumption is minimized resulting in maximum lifetime of the device.

1.4 Contributions

In this thesis, several novel circuits for a 402 MHz to 405 MHz integer-n frequency synthesizer are proposed, implemented and tested to ensure they conform to the design objectives stated above. The major contributions of this work are:

- A current reuse quadrature voltage controlled oscillator. The proposed topology consumes half the power of conventional quadrature oscillators while improving phase noise performance and is compatible with low supply voltage operation.
- A design methodology for low power voltage controlled oscillators. By exploiting the MOS EKV model and the g_m/i_D methodology, the proposed design methodology provides a systematic procedure for various oscillator topologies and is suitable for hand analysis. The methodology is applied to the proposed current reuse quadrature voltage controlled oscillator, however it can be used for most CMOS LC oscillator topologies.
- An ultra-low power programmable frequency divider using subthreshold source-coupled logic. The power consumption has been reduced significantly compared to existing programmable dividers. A novel D-latch with clear and preset functionality is proposed as existing designs either don't perform clear and preset functions simultaneously or they are not conducive to low voltage applications.

- Based on the novel clear/preset D-latch, a subthreshold source-coupled logic phase/frequency detector is implemented.

1.5 Organization of report

This thesis focuses on the topic of ultra-low power frequency synthesis for use in Medical Implant Communication service transceivers.

Chapter 2 (Oscillators and Frequency Synthesis): provides a summary of CMOS oscillators and phase-locked loop frequency synthesizer fundamentals. *LC* VCO fundamentals are introduced, covering *LC* tanks, start-up conditions, steady-state operation, and phase noise. Spectral purity is explored in terms of phase noise, where two popular models for phase noise analysis are presented. Quadrature signal generation for image-reject transceiver architecture is presented, followed by similar analysis provided for the *LC* VCO. To support our discussion, the main building blocks are briefly described.

Chapter 3 (Medical Implant Communication Service): provides an introduction to the frequency band of interest, the 402 MHz to 405 MHz Medical Implant Communication Service. A brief history of the frequency band is given, followed by the regulatory requirements for implantable medical devices including their operation and testing. A brief literature survey summarizing state-of-the-art designs for Medical Implant Communication Service concludes the chapter.

Chapter 4 (The Proposed Subthreshold 402 MHz to 405 MHz Integer-N Frequency Synthesizer): introduces *the proposed* design of an integer-n frequency synthesizer, with particular attention to the current-reuse quadrature voltage-controlled oscillator and subthreshold source-coupled logic programmable frequency divider. A design methodology for low power oscillators based on the MOS EKV model and the g_m/i_d design methodology is presented. A novel D-latch is proposed to address the need for clear and preset functionality in the programmable divider and phase/frequency detector.

Chapter 5 (Results): presents the simulation results for each of the designed circuits using Cadence Spectre circuit simulator, as well as some measurement results from fabricated prototypes. A comparison between existing designs and the proposed design is provided.

Chapter 6 (Conclusion): summarizes the contributions of this research and suggests future directions.

Chapter 2

Oscillators and frequency synthesis

2.1 Overview

Due to their importance in transmitter and receiver architectures for wired and wireless applications, oscillators and phase-locked loops have received extensive attention in literature and academic research. The depth and breadth of this discussion is limited to those topics and topologies that provide a fundamental understanding of the work proposed in this thesis. References to material on topics outside those covered in this chapter will be given when necessary, and the reader is encouraged to review those references to obtain a thorough understanding of oscillators and phase-locked loops in RF systems.

2.2 CMOS Oscillators

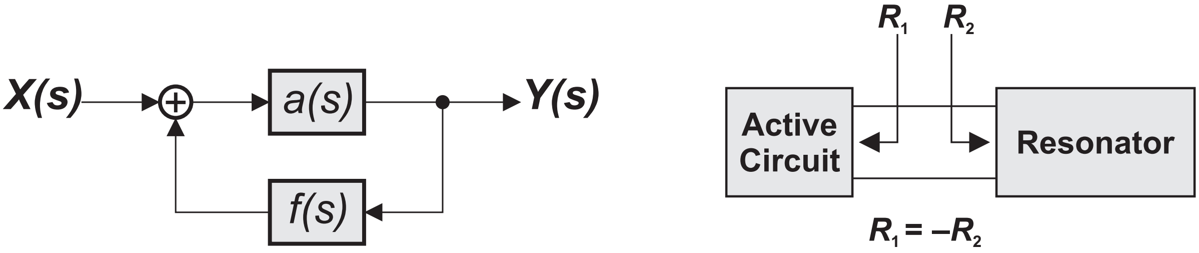
2.2.1 General considerations

Oscillators are autonomous circuits which produce a periodic output signal from a DC power supply. They are an essential component of many electronic communication systems. There are a wide variety of oscillator topologies, each suitable for different applications. Example of oscillator applications include carrier signal generation for wireless RF transmitters, and clock generation for microprocessors. The forthcoming discussion will focus on topics related to the former, and the implementation of interest will be the LC-tank oscillator.

As shown in Fig. 2.1, oscillators can be represented as either a one-port network, known as the negative resistance model, or a two-port network, known as the feedback model. The conditions for oscillation can be determined by analysing either of these models.

First consider the positive feedback model in Fig. 2.1a, which has a forward gain $a(s)$ and feedback factor $f(s)$. The output signal of the summing block, denoted $e(s)$, is given by

$$e(s) = X(s) + f(s) \cdot Y(s). \tag{2.1}$$



(a) Feedback model.

(b) Negative resistance model.

Figure 2.1: Oscillator models.

The output signal $Y(s)$ is given by

$$Y(s) = a(s) \cdot e(s). \tag{2.2}$$

From (2.1) and (2.2) the transfer function of the two-port network can be obtained:

$$\frac{Y(s)}{X(s)} = \frac{a(s)}{1 - a(s) \cdot f(s)}. \tag{2.3}$$

In order for this system to oscillate at a frequency ω_0, it must satisfy the Barkhausen criterion [29]. The conditions that must be met are that the loop gain at frequency ω_0 must be unity and the total phase shift around the loop must be an integer multiple of 2π.

- $|H(j\omega_0)| = 1$.
- $\angle H(j\omega_0) = 2n\pi, n \in \mathbb{N}$.

Note that if the network employs negative feedback, the second condition of the Barkhausen criterion changes such that the total phase shift around the loop must be an odd multiple of π.

- $\angle H(j\omega_0) = (2n+1)\pi, n \in \mathbb{N}$.

The one-port oscillator model of Fig. 2.1b consists of two circuits – a frequency selective network such as a resonator that exhibits some loss and an active circuit which compensates for the loss in the resonator. The quality factor, Q, of a resonant circuit is defined as the ratio of the energy stored per cycle to the energy dissipated per cycle.

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy dissipated}}. \tag{2.4}$$

Ideal resonators have infinite Q and resonate forever, however passive devices implemented in integrated circuit resonators have finite values of Q and can not sustain oscillations (as a rough approximation, the resonator will only oscillate at frequency ω_0 for Q cycles). In order to produce sustained oscillations a "negative resistor," which has an energy restoring mechanism, can be added to the tank.

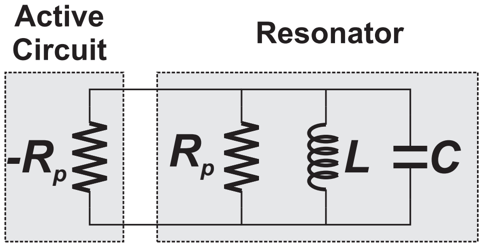


Figure 2.2: LC resonator with loss compensation.

This is illustrated in Fig. 2.2, where R_p is a lumped element consisting of the series losses of the inductor and capacitor defined as

$$R_p = \omega_0 L Q. \tag{2.5}$$

It can be shown that at resonance, the input impedance of the tank at resonance is R_p. Since the tank components are in parallel, one can also consider the admittance of the tank and take the inverse to obtain the impedance. Knowing that the capacitor has a quality factor equal to $\omega_0 R_p C$ and the inductor has a quality factor equal to $R_p/(\omega_0 L)$, the admittance can be written as

$$\begin{aligned} Y_{tank}(j\omega) &= \frac{1}{R_p} + j\omega C + \frac{1}{j\omega L} && (2.6)\\ &= \frac{1}{R_p} + \frac{Q}{R_p}\left(\frac{j\omega}{\omega_0} + \frac{\omega_0}{j\omega}\right) && (2.7)\\ &= \frac{1}{R_p}\left[1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right]. && (2.8) \end{aligned}$$

This yields an input impedance of

$$Z_{tank}(j\omega) = \frac{R_p}{1 + jQ\left(\dfrac{\omega}{\omega_0} - \dfrac{\omega_0}{\omega}\right)}. \tag{2.9}$$

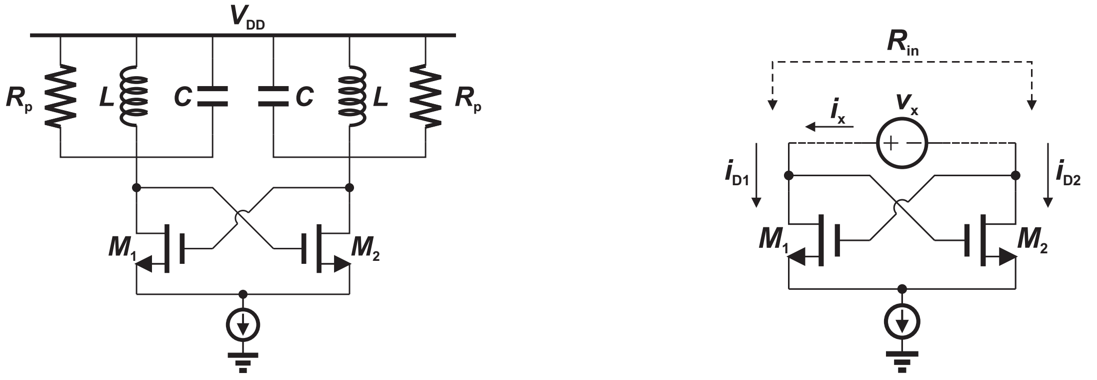
It can be seen from (2.9) that when $\omega = \omega_0$, the tank impedance consists only of the loss component R_p. This conclusion will help develop the oscillator circuit that will be discussed in the following section.

2.2.2 Negative-g$_m$ LC-tank oscillators

Basic topology and analysis

The LC-tank oscillator is the most popular circuit in RF applications because of its superior phase noise performance and the ability to be fully integrated on chip (no external components). Referring to the one-port oscillator model, the LC-tank serves as the resonator. The active circuit which compensates for the parasitic losses at resonance is implemented using the cross-coupled differential pair shown in

Fig. 2.3a. It can be shown that this configuration presents a negative input resistance, which when the transistors are properly sized, can cancel out the losses of the *LC*-tank.



(a) Conventional topology with losses.

(b) Negative impedence measurement.

Figure 2.3: Negative-g$_m$ LC-tank oscillator.

The test circuit for calculating the input impedance is shown in Fig. 2.3b. The input impedance is obtained by applying a test voltage, v_x, across the two terminals of the differential pair and calculating the current, i_x, flowing through the circuit. By recognizing that $v_x = v_{gs_2} - v_{gs_1}$ and $i_x = i_{d_2} = -i_{d_1}$, small signal analysis shows that

$$\frac{v_x}{i_x} = \frac{-2}{g_m}, \tag{2.10}$$

and it can be concluded that for the circuit in Fig. 2.3a, oscillations are sustained when

$$R_p = \frac{1}{g_m}. \tag{2.11}$$

The devices in CMOS processes are subjected to variations due to process, supply voltage and temperature (PVT) which may cause the device transconductance to be less than required to guarantee oscillator startup. To combat these variations, the device transconductance is usually designed to be a factor of β greater than what is required by (2.11), where $\beta \geq 2$.

$$R_p = \frac{\beta}{g_m}. \tag{2.12}$$

The circuit can also be analysed using the feedback model. The transfer function of the circuit in Fig. 2.3a is

$$H(s) = (-g_m Z_{tank}(s)) \cdot (-g_m Z_{tank}(s)). \tag{2.13}$$

As shown by (2.9), at resonance $Z_{tank}(j\omega_0) = R_p$ and the transfer function becomes

$$H(j\omega_0) = (g_m R_p)^2. \tag{2.14}$$

The total phase shift around the loop should be 0° and to obtain a loop gain of unity

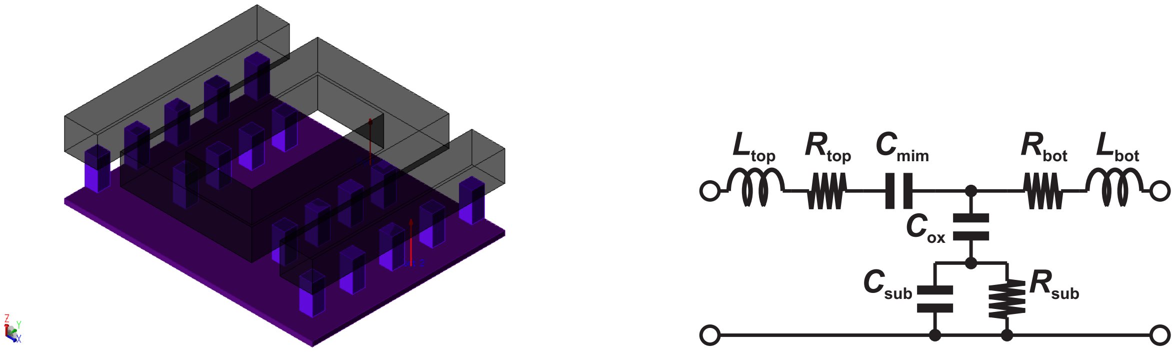
$$R_p = \frac{1}{g_m}. \tag{2.15}$$

Passive devices in CMOS processes

In previous generations of integrated circuits, passive devices (inductors, capacitors, resistors) were implemented off-chip and connected to the circuit using bond wires. In modern CMOS processes, passive devices can be integrated on the same die as the active circuitry. This is a major benefit in modern CMOS processes because it decreases the total cost of the design. The drawback is that inductance, capacitance and quality factors of on-chip passive devices is much less than their off-chip counterparts. However, the values obtained on-chip are usually sufficient for most applications. Passive devices are used extensively in analog and radio frequency integrated circuits for applications such as filtering, impedance matching, AC coupling, and as the tuned resonator in LC oscillators.

Integrated capacitors are typically implemented using the metal-insulator-metal (MIM) topology. The MIM capacitor is a parallel plate capacitor formed using two of the upper metal layers and a thin oxide layer with a high dielectric constant. The capacitance density of a MIM cap is defined in the same way as a transistor – $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ – where ϵ_{ox} is the dielectric constant of the oxide and t_{ox} is the oxide thickness. Standard metal layers used for signal routing can be spaced far apart (a few micrometers) which results in a large oxide thickness and therefore low capacitance density. To remedy this, additional layers specifically for MIM capacitors exist in between the standard metal layers which are closely spaced to reduce the oxide thickness. An example of a MIM capacitor is shown in Fig. 2.4a. MIM capacitors suffer from parasitic losses as with all integrated devices. The top and bottom metal plates have both inductive (L_{top}, L_{bot}) and resistive (R_{top}, R_{bot}) losses, and the bottom plate of the MIM capacitor has a parasitic capacitance (C_{ox}) that exists between itself and the substrate which has a thick dielectric in between. The substrate layer iself exhibits resistive (R_{sub}) and capacitive (C_{sub}) losses, which decrease the quality factor of the MIM capacitor. The equivalent circuit for a MIM capacitor used for circuit simulation is shown in Fig. 2.4b.

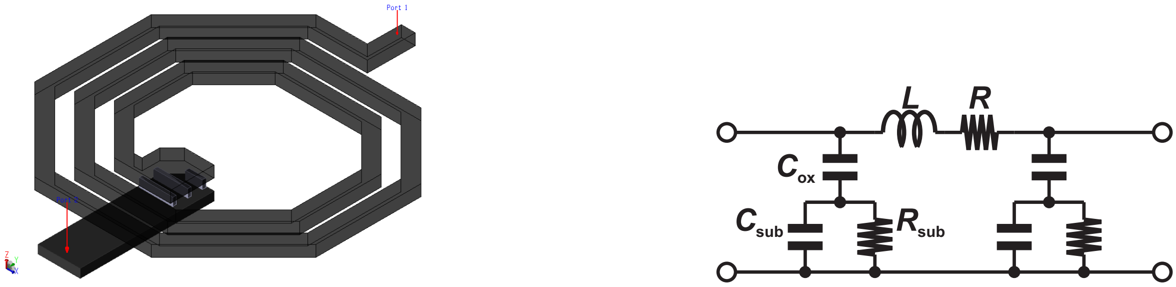
Square spiral inductors are the most popular planar inductor geometries, but many recent processes allow more optimal geometries such as octagonal and circular inductors. Spiral inductors are wound on the top metal layer and a second layer is used to connect the innermost winding to the outside. As shown in Fig. 2.5a, planar spiral inductors are wound on the top metal layer to increase their self-resonant frequency by decreasing the capacitance to the substrate and a second layer is used to connect the innermost winding to the outside. Spiral inductors get their name because they spiral inward by adding loops inside each successive loop, forming a spiral. The important geometric parameters of a spiral inductor are the number of turns, trace width, trace spacing, trace length, inner diameter and outer diameter. The equivalent circuit of the planar spiral inductor is shown in Fig. 2.5b, where L is the inductance of the spiral, R is the winding loss, C_{ox} is the capacitance existing between the spiral



(a) Three dimensional view. (b) Equivalent circuit.

Figure 2.4: Metal-insulator-metal capacitor.

and the oxide layer, and C_{sub} and R_{sub} are substrate loss components.



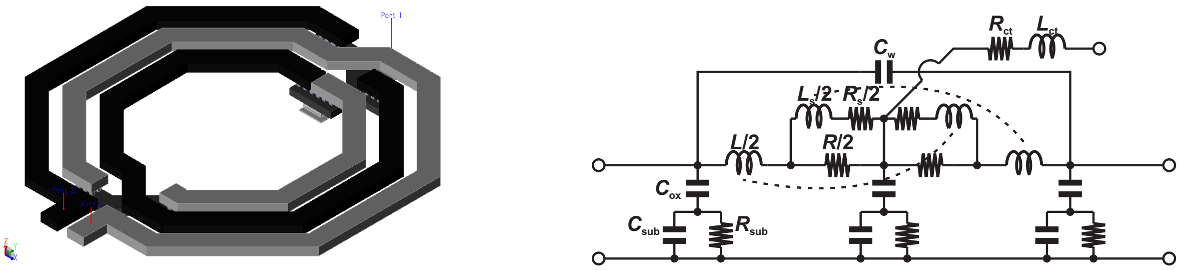
(a) Three dimensional view. (b) Equivalent circuit.

Figure 2.5: Octagonal spiral inductor.

The planar spiral inductor in Fig. 2.5a has several drawbacks. The inductor is not suitable for differential excitation in applications such as the LC oscillator because the electrical center of the structure is not well defined. As a result, applying a bias potential (i.e. V_{DD} for an LC oscillator) cannot be made with certainty. One way to resolve this is to connect two spiral inductors in series, using the outer ports for differential excitation and the inner ports as the electrical center. Although the electrical center is now well defined (same as the geometric center), the use of two spirals consumes twice as much silicon area. A better approach is to use a symmetric inductor layout, such as the one in Fig. 2.6a, consisting of two interwound coils. In addition to having a clearly defined electrical center and occupying less area, the symmetric inductor benefits from the mutual coupling between the two coils. If the two inductors are identical with inductance L and mutual inductance M, and the coupling factor that exists between them is k, the total differential inductance of the symmetric inductor is

$$
\begin{aligned}
L_{diff} &= L + L + 2M, && (2.16)\\
&= 2L + 2k\sqrt{L \times L}, && (2.17)\\
&= 2L(1 + k). && (2.18)
\end{aligned}
$$

The equivalent circuit of the symmetric inductor is shown in Fig. 2.6b, where the dashed lines indicate coupling between two inductors [30].



(a) Three dimensional view.

(b) Equivalent circuit.

Figure 2.6: Symmetric spiral inductor.

Since the two resonators in Fig. 2.3a are connected in series, they can be merged into a single tank as shown in Fig. 2.7. The inductor is replaced with a differential symmetric inductor with its center-tap connected to V_{DD}.

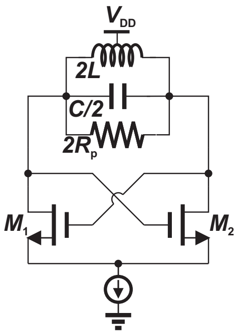


Figure 2.7: Negative-g$_m$ LC-tank oscillator with merged tanks.

Transient behaviour

Once the oscillator has reached steady state oscillations, the switching transistors M_1 and M_2 in Fig. 2.3a behave as ideal current sources. The drain current waveforms can be approximated as square waves, since the entire bias current flows through each transistor for half a cycle. The Fourier series of the drain current waveform is

$$I_{DS} = \frac{1}{2} I_{bias} \left(1 + \frac{4}{\pi} \sin \omega_0 t + \frac{4}{3\pi} \sin 3\omega_0 t + \dots \right). \tag{2.19}$$

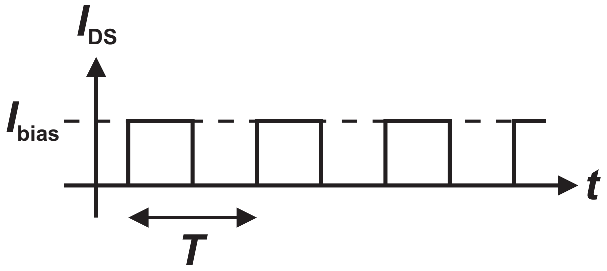


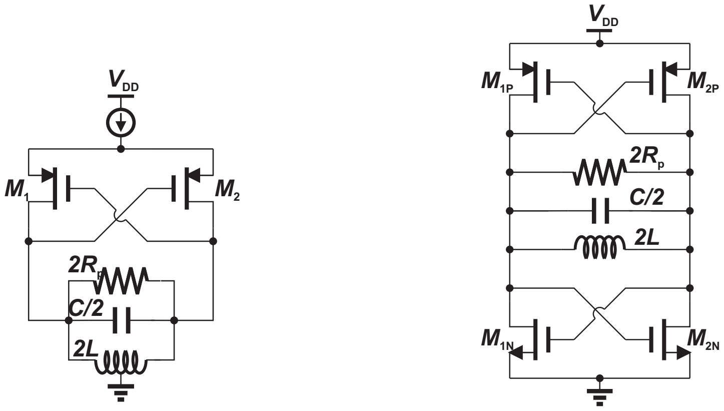
Figure 2.8: Drain current for switching transistor.

Assuming the tank quality factor is high enough to attenuate the higher order harmonics, the oscillation amplitude can be approximated as

$$\hat{V_0} = \frac{2}{\pi} I_{bias} R_p, \tag{2.20}$$

where I$_{bias}$ is the bias current and R$_p$ is impedance of the parallel *LC* tank at resonance.

The negative-g$_m$ oscillator can be modified to use PMOS transistors (Fig. 2.9a) or both NMOS and PMOS transistors (Fig. 2.9b) to generate the negative resistance required to sustain oscillations. The latter is commonly referred to as the CMOS oscillator since it uses both NMOS and PMOS cross-coupled transistors. The behaviour of the CMOS oscillator is different than the NMOS-only and PMOS-only oscillators – the total negative conductance and output oscillation amplitude are twice that of NMOS-only and PMOS-only oscillators.



(a) PMOS oscillator.

(b) CMOS oscillator.

Figure 2.9: Variations of the negative-g$_m$ topology.

2.2.3 Voltage-controlled oscillators

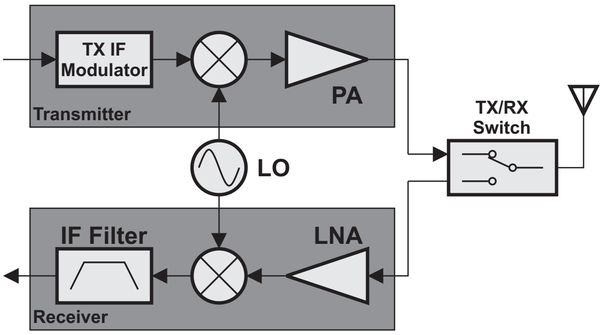


Figure 2.10: Simple transceiver.

Consider the simple transceiver architecture of Fig. 2.10. The transmitter consists of a baseband modulator, a frequency mixer which up-converts the baseband data to the carrier frequency, and a power amplifier. The receiver consists of a low-noise amplifier, a frequency mixer to down-convert the RF signal to an intermediate frequency (IF), and a filter. The mixer produces tones at $(f_{in_1} + f_{in_2})$ and $(f_{in_1} - f_{in_2})$, where one of the frequencies is produced by the local oscillator (LO). The transceiver must be able to operate on one of many channels available in the allocated frequency band since each channel can only be occupied by one user. When operating in transmit mode, the modulated data would be transmitted on a channel which is not in use and has acceptable noise characteristics.

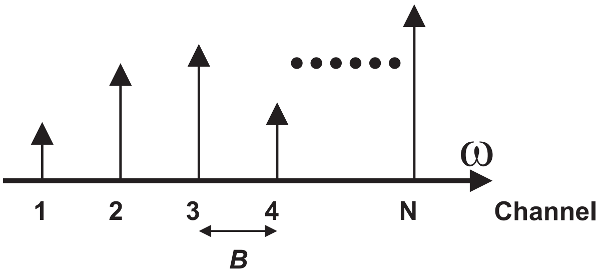
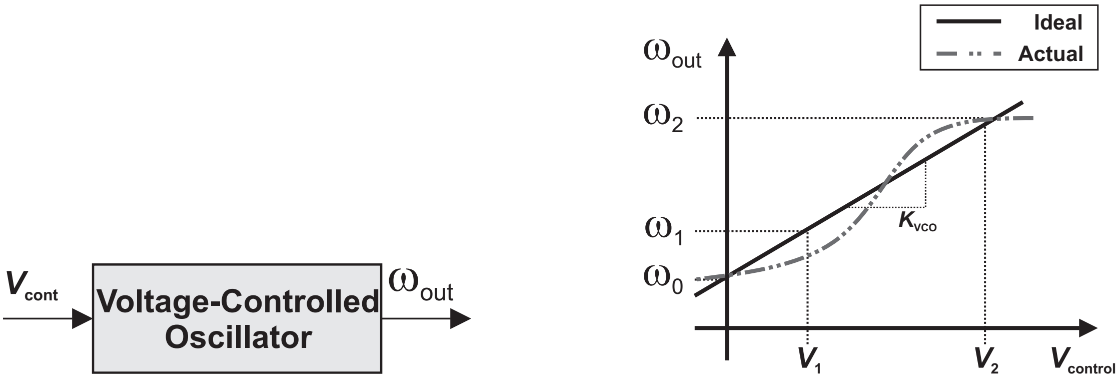


Figure 2.11: Arbitrary spectrum for example transceiver.

If the transceiver can operate on the arbitrary spectrum of Fig. 2.11 which contains N channels spaced B Hz, the transmitter should be capable of operating on any of those frequencies. In order to achieve this behaviour, the LO must be tunable so that the up-converted frequency $(f_{BB} + f_{LO})$ is equal to the desired carrier frequency. For the receiver, in order to use a fixed IF filter the incoming RF signal must be downconverted to the IF. This means that the LO must be tuned so that the down-converted frequency $(f_{RF} - f_{LO})$ is equal to the IF frequency. The tunable LO is implemented using a voltage-controlled oscillator (VCO). A VCO is an oscillator whose output frequency is directly proportional to an input voltage, known as the "control voltage" V_{cont}. The relationship between a VCO's control voltage and output frequency, ω_{out}, is

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}, \tag{2.21}$$

where ω_0 is the free-running VCO frequency when no control voltage is applied and K_{VCO} is the VCO gain. The conceptual VCO block diagram and its tuning characteristics are shown in Fig. 2.12b.



(a) Block diagram.

(b) Tuning characteristics.

Figure 2.12: Voltage-controlled oscillator.

The amount of frequency variation is known as the tuning range, and is typically determined by the requirements of the desired application. The gain of the VCO is the ratio of the tuning range to the usable control voltage (i.e. the slope of the tuning curve),

$$K_{VCO} = \frac{\omega_2 - \omega_1}{V_2 - V_1}. \tag{2.22}$$

Ideally the tuning characteristics shown in Fig. 2.12b are linear, but since there are no ideal elements in CMOS processes there is always some nonlinearity as demonstrated by the dashed line in the figure. In addition to nonidealities in the VCO components that contribute to the nonlinearity of the tuning characteristics, the VCO is susceptible to noise on the control voltage. When this noise is added to the control voltage the noise is amplified by K_{VCO}, causing random variations to the VCO frequency. In order to reduce the effect of noise the VCO gain should be minimized, ensuring that the tuning range requirements are still satisfied. By maximizing the amplitude of oscillations, the sensitivity to noise is decreased but at the expense of increased power consumption, $V_{DD} \times I_{bias}$. This is an important consideration for ultra-low power oscillators where minimization of power consumption is an important design criterion.

The VCO topologies shown in Fig. 2.3 are capable of tuning since the resonator uses passive components with fixed values. In order to implement a VCO in a CMOS process, the negative-g$_m$ oscillator is modified by adding a tunable element to the resonator which changes the resonant frequency of the tank in response to a control voltage. The most popular tuning element is the MOS varactor. The structure of the MOS varactor shown in Fig. 2.13 is known as an "NMOS-in-nwell" varactor. By shorting the drain and source terminals together, a capacitor is formed between the gate and drain/source terminals whose value is controlled by the voltage V_{g-sd}. Although other MOS varactor topologies are available, it has been shown the NMOS-in-nwell exhibits the lowest phase-noise and power consumption [31].

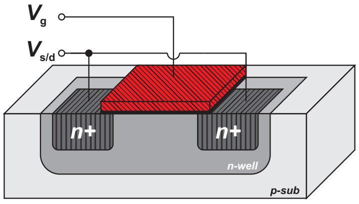
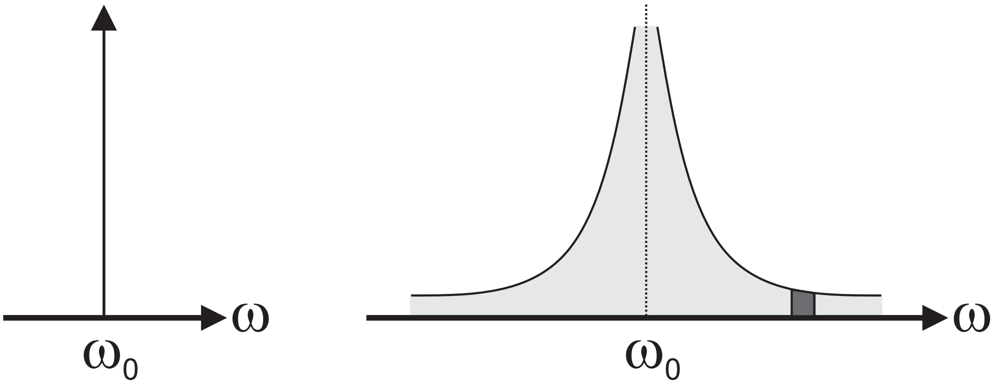


Figure 2.13: Cross-section of MOS varactor.

2.2.4 Phase noise in oscillators

An ideal oscillator produces a signal which is described by $x(t) = \hat{V_0}\cos(\omega_0 t + \phi)$, where $\hat{V_0}$ is the VCO amplitude, ω_0 is resonant frequency, and ϕ is a fixed excess phase. The output spectrum of an ideal oscillator is a delta function at frequency ω_0, as shown in Fig. 2.14a. Real oscillators are subjected to phase noise, which is a random variation in the excess phase, as well as amplitude noise. Taking these nonidealities into account, the output waveform can then be described by $x(t) = \hat{V_0}(t)\cos(\omega_0 t + \phi(t))$. The amplitude noise is typically disregarded because of the amplitude limiting mechanism provided by the fixed bias current in the oscillator, therefore the noise at the output is dominated by phase noise. The frequency domain representation of the waveform is no longer an impulse, rather the spectrum has a finite width centered at ω_0 as shown in Fig. 2.14b.



(a) Ideal.
(b) Actual.

Figure 2.14: Voltage-controlled oscillator output spectrum.

Phase noise is measured in units of dBc/Hz, which is how much power the signal contains at an offset frequency relative to the carrier within a 1 Hz measurement bandwidth. The negative effects of phase noise can be seen in both the transmitter and receiver. Consider again the abitrary spectrum presented previously, but this time in the presence of phase noise. If the LO of the transmitter is noisy the noise spectrum can leak into adjacent channels, corrupting that channel's carrier signal. If the receiver's LO is noisy, any signal which is at a small offset from the incoming carrier will also get downconverted and corrupts the IF band because of the finite width of the LO spectrum which provides "parasitic LO's" to adjacent signals.

Phase noise is quantified by the ratio of the single-side band power at an offset $\Delta\omega$ from the carrier within a measurement bandwidth of 1 Hz to the power of the carrier signal,

$$\mathcal{L}\{\Delta\omega\} = 10\log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega,\, 1\text{ Hz})}{P_{carrier}}\right]. \tag{2.23}$$

One of the most famous phase noise models, which has been the driving force behind modern phase noise analysis, is the Leeson-Cutler model [32]. This semi-empirical model is based on linear, time-invariant (LTI) analysis of the oscillator and predicts the phase noise as

$$\mathcal{L}\{\Delta\omega\} = 10\log\left\{\frac{2FkT}{P_{carrier}}\left[1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1 + \frac{\Delta\omega_{\frac{1}{f^3}}}{|\Delta\omega|}\right)\right\}, \tag{2.24}$$

where F is called the noise factor, k is the Boltzmann constant, and $\Delta\omega_{\frac{1}{f^3}}$ is approximated as the device $\frac{1}{f}$ noise corner. Graphically the Leeson model is illustrated in Fig. 2.15.

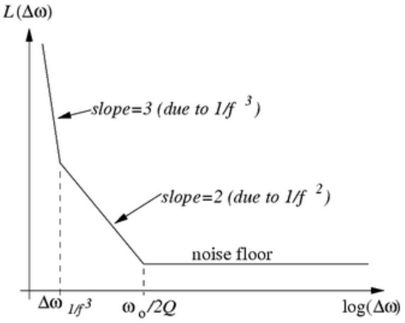


Figure 2.15: Predicted phase noise spectrum.

Several important qualities can be observed from this model [33]:

- $\mathcal{L}\{\Delta\omega\}$ always has a $\frac{1}{f^3}$ region.
- $\mathcal{L}\{\Delta\omega\}$ has a $\frac{1}{f^2}$ region from $\Delta\omega_{\frac{1}{f^3}}$ to $\frac{\omega_0}{2Q}$, but only if $\Delta\omega_{\frac{1}{f^3}} < \frac{\omega_0}{2Q}$.
- $\mathcal{L}\{\Delta\omega\}$ has a $\frac{1}{f}$ region from $\frac{\omega_0}{2Q}$ to $\Delta\omega_{\frac{1}{f^3}}$, but only if $\frac{\omega_0}{2Q} < \Delta\omega_{\frac{1}{f^3}}$.
- $\mathcal{L}\{\Delta\omega\}$ has a white noise region at starting at the larger of $\omega = \Delta\omega_{\frac{1}{f^3}}$ or $\omega = \frac{\omega_0}{2Q}$.

There are several shortcomings in the predictive power of this model [34]. Firstly the noise factor F was added as a fitting parameter to account for the excess noise contribution of the energy restoring mechanism and can only be determined through measurement. Secondly the transition from the $\frac{1}{f^3}$ region to the $\frac{1}{f^2}$ region does not occur at the device $\frac{1}{f}$ noise corner, and must also be considered as an empirical fitting parameter. Lastly, $\mathcal{L}\left\{\Delta\omega\right\}$ does not always flatten out at $\omega = \Delta\omega_{\frac{1}{f^3}}$ or $\omega = \frac{\omega_0}{2Q}$. Despite these shortcomings, an important conclusion that can be drawn from this model is that phase noise can be minimized by maximizing the tank quality factor and the carrier signal power. The drawback of the latter is the increase in oscillator power consumption.

In order to address the flaws in the Leeson model, a new linear, time-varying (LVT) phase noise model was proposed by Hajimiri and Lee [35], [36]. The authors sought to investigate how noise injected into an LC tank affects the phase and amplitude of oscillation. The important conclusion describes how the time at which the charge is injected changes the oscillation amplitude and phase. If the charge is injected at a peak of oscillation, the amplitude will increase in response to the energy added to the tank, however the phase does not change. On the other hand if the disturbance occurs at a zero crossing, both the amplitude and phase of oscillation changes. In order to describe this behaviour, the authors proposed the following unit impulse response for excess phase,

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0 t)}{q_{max}} u(t-\tau), \tag{2.25}$$

where q_{max} is the maximum charge displacement across the capacitor, $u(t-\tau)$ is the unit step function occurring at $t = \tau$, and $\Gamma(\omega_0 t)$ is a periodic function called the Impulse Sensitivity Function (ISF) describing how much phase shift results by applying a unit impulse at $t = \tau$. Examples of the ISF for common oscillator output waveforms is shown in Fig. 2.16 [35]. The phase offset caused by an impulse current can be calculated using the superposition integral

$$\begin{aligned} \phi(t) &= \int_{-\infty}^{\infty} h_\phi(t) i(t-\tau) d\tau, & (2.26)\\ &= \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0 t) i(\tau) d\tau. & (2.27) \end{aligned}$$

A full derivation of the integral and assumptions made therein is given in [34], [35], [36]. From the result of the expression, the authors further explore how this excess phase affects the output voltage, and it was found that noise components near integer multiples of the carrier frequency all fold in to the noise near the carrier itself. Minimization of the ISF is instrumental in reducing phase noise.

This model is a significant step in understanding the mechanisms of phase noise, as the authors have described many important aspects such as the conversion of current noise into excess phase, excess phase into output voltage, sideband noise power, as well as equations describing the phase noise spectrum in the $\frac{1}{f^3}$ and $\frac{1}{f^2}$ regions, and the corner frequency between those regions.

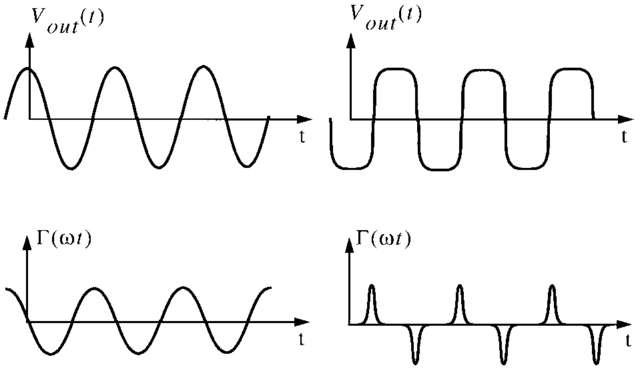


Figure 2.16: Waveforms and ISFs for (a) a typical LC oscillator and (b) a typical ring oscillator.

2.2.5 Quadrature oscillators

The *LC* VCO produces differential outputs, that is the outputs are 180°out of phase. Modern transceiver architectures that use image rejection to remove undesired tones whose distance from the LO is equal to the intermediate frequency of the transceiver employ complex mixers which are driven by a quadrature local oscillator, which produces four output signals whose phases are 90°apart. One of the most popular methods for quadrature signal generation was proposed in [37]. The authors observed that by cross coupling two *LC* oscillators that operate at a common frequency, the output phases are in precise quadrature. The quadrature *LC* tank oscillator is shown in Fig. 2.17.

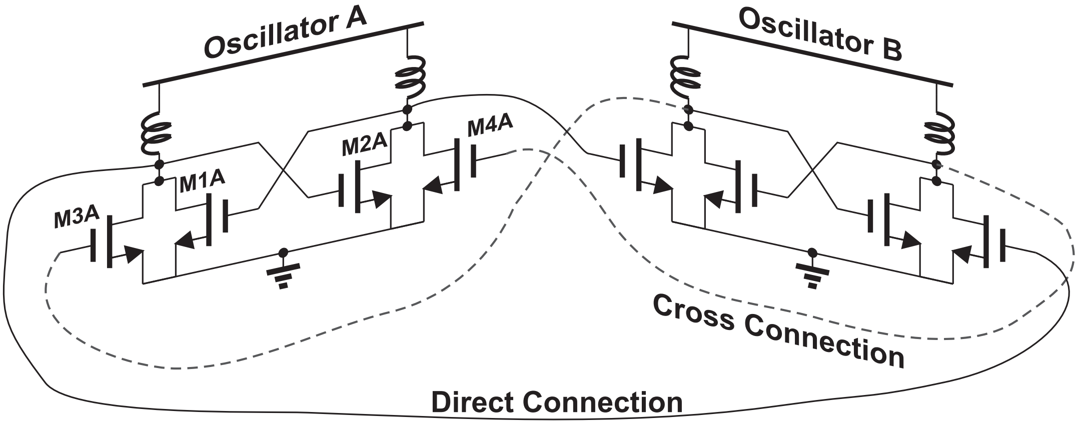


Figure 2.17: Original quadrature *LC* oscillator (omitting bias).

In the design proposed in [37], the *LC* tank is modified by adding coupling transistors (M3A, M4A) in parallel with the switching transistors (M1A, M2A). The outputs of Oscillator A are directly coupled to Oscillator B's coupling transistors, and the outputs of Oscillator B are cross-coupled to Oscillator A's coupling transistors. As in the previous discussion about *LC* oscillators, adding a frequency tuning element such as a varactor will produce a quadrature *LC* VCO (QVCO). In [38], the authors used symmetry to conclude that the two oscillators will have identical oscillation frequency and amplitude if their output voltages are in quadrature. They further demonstrate that the oscillators will synchronize at a frequency greater than the tank resonant frequency. Using a linearized model of the QVCO, the authors of [39] showed that the transfer function of the loop that exists between the positive output nodes of Oscillators A and B is given by

$$\frac{V_B^+}{V_A^+} = -j\frac{\omega_0 C\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)}{G_{M_c}}, \tag{2.28}$$

where G_{M_c} is the effective large signal transconductance of the coupling transistors. This equation verifies that the two tanks can not synchronize at the resonant frequency since when $\omega = \omega_0$, the tank voltage becomes zero. In the original QVCO topology, commonly referred to as the parallel QVCO (PQVCO) because of the location of the coupling transistors, the switching and coupling transistors were sized equally. In more general cases, the transistors are not all sized the same. The ratio of the width of the coupling transistor to the width of the switching transistor is called the coupling factor, and denoted as α.

$$\alpha = \frac{W_{cpl}}{W_{sw}}. \tag{2.29}$$

This parameter has an important role in the QVCO performance. In [40] the authors showed that for the PQVCO a coupling factor of unity provides the best phase error, and reducing the coupling between the two oscillators (by decreasing α) increases the phase error. However, phase noise improves as α decreases. A trade-off exists between phase noise and phase error, and the selection of α is important for optimizing both of these parameters. Further analysis by the authors showed that by varying the coupling factor the amount of bias current flowing through the switching and coupling transistors changes. When steered entirely into one branch (M1A, M3A or M2A, M4A), the bias current I_{bias} has two components: I_{sw} flowing through the switching transistor and I_{cpl} flowing through the coupling transistor,

$$I_{sw} = (1-\delta)I_{bias}, \tag{2.30}$$

$$I_{cpl} = \delta I_{bias}, \tag{2.31}$$

where δ is defined for compactness,

$$\delta = \frac{W_{cpl}}{W_{sw} + W_{cpl}} = \frac{\alpha}{1+\alpha}. \tag{2.32}$$

By analysing the drain current waveforms during a cycle of oscillations, the oscillation amplitude is given by

$$\hat{V_0} = \frac{2}{\pi}(1-\delta)I_{bias}R_p, \tag{2.33}$$

which shows that only the current flowing through the switching transistors contributes to the oscillation amplitude. A weaker coupling factor gives rise to a larger oscillation amplitude, which improves the phase noise at the expense of phase error. Another way to increase the oscillation amplitude is to increase the bias current, however this also increases the power consumption of the oscillator and the increase is compounded by the fact the there are now two oscillation cores each drawing their own bias current.

The work presented in [37] has motivated a significant amount of research into the design of QVCOs and analysis of their behaviour and phase noise performance, as well as modifications to the original topology to improve phase noise, power consumption and quadrature accuracy. Some notable modifications include

- The disconnected-source QVCO (DS-QVCO) [41], where the switching and coupling transistors or the PQVCO are biased independently,
- The series QVCO (SQVCO) [39], where the coupling transistors are placed in series with the switching transistors.
- The phase-tunable QVCO (PT-QVCO) [42], which is capable of correcting phase errors in the quadrature outputs,
- The transformer-coupled QVCO (TC-QVCO) [43], in which two *LC*-VCOs are cross-coupled passively by on-chip transformers instead of actively by coupling transistors as in conventional *LC*-QVCOs to generate quadrature signals.

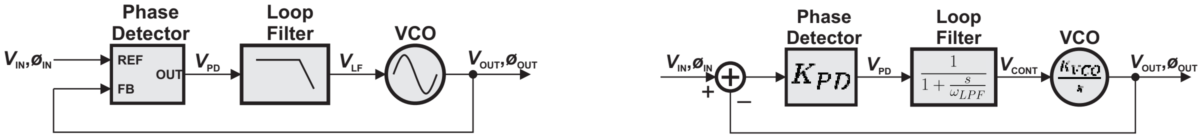
However, the most common QVCO implementations in recent literature are the PQVCO and the SQVCO. Like the *LC* VCO, the QVCO can be implemented as NMOS-only, PMOS-only, or complementary oscillators.

2.3 Phase locked loops and frequency synthesizers

In order to generate the tunable LO signal for a transmitter or receiver chain, the *LC* VCO is not sufficient because oscillators, like all other circuits implemented in a CMOS process, are subjected to variations due to process, supply voltage and temperature (PVT). This means that if an entire wafer of the same VCO was fabricated and tested, one would observe variations in the criteria which describe an oscillator (ω_0, $\hat{V}_0$, power consumption, tuning range, phase noise). If the tuning characteristics of a VCO were predictable and constant across all dies, the voltages to tune to a particular frequency could be stored in a ROM on chip for fast frequency tuning. Referring to Fig. 2.12b, the tuning curve may shift vertically or horizontally, or the slope may become steeper or shallower, therefore the tuning characteristics would no longer be predictable. To produce a stable LO signal, the oscillator is placed in a closed-loop feedback system called a phase-locked loop (PLL). The function of a PLL is to align the output phase of the VCO with the phase of a stable reference clock, such as a crystal oscillator.

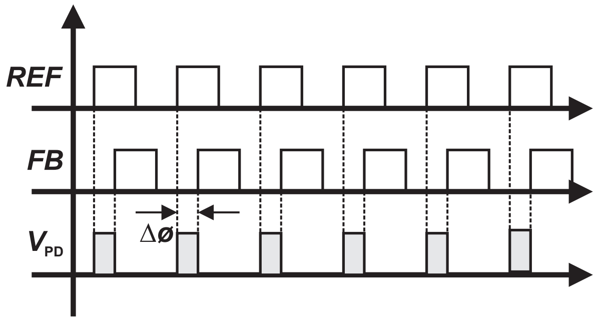
2.3.1 Simple phase-locked loop

The simple PLL consists of a VCO and a phase detector in a closed loop as shown in Fig. 2.18a. The phase detector compares the phase of the VCO output signal with that of an input reference, and



(a) Block diagram.

(b) Linear model.



(c) Phase detector waveforms.

Figure 2.18: Simple phase-locked loop.

produces an output whose average value is proportional to the phase difference, $\Delta\phi$,

$$\overline{V}_{pd} = K_{pd}\Delta\phi. \tag{2.34}$$

The slope of the $\overline{V}_{pd}$–$\Delta\phi$ curve is called the phase detector gain and is denoted K_{pd}. Consider the waveform in Fig. 2.18c where the input reference leads the output. The phase detector produces an output from when the input signal is high to when the output signal is high. Recalling that the phase is the integral of frequency, in order for the phases to be aligned the output signal must accumulate phase faster, which necessitates a temporary increase in frequency until the phases are aligned. This process is known as phase-locking. The phase detector output can not be connected directly to the VCO because the control voltage should be the average value of the phase detector output. In order to extract the DC component from the phase detector output, a low pass filter, commonly referred to as the loop filter, is placed between the phase detector and the VCO. To simplify the analysis, the loop filter is assumed to be a first order RC filter.

Ideally in locked condition the phase error is zero, but in practical situations the PLL reaches the locked condition when the phase error is a constant, small value. That is,

$$\frac{\mathrm{d}\phi_{out}}{\mathrm{d}t} - \frac{\mathrm{d}\phi_{in}}{\mathrm{d}t} = 0. \tag{2.35}$$

Again recalling that the frequency is the derivative of phase, we have

$$\omega_{in} = \omega_{out}, \tag{2.36}$$

implying that in the locked state, the input and output signals have the same phase and frequency.

The PLL can be analysed using the linear model of Fig. 2.18b [29]. The phase detector is modelled as a subtractor whose output, the phase difference between the input and output waveforms, is “amplified” by K_{pd}. The first order lowpass filter has a transfer function $\frac{1}{1+\frac{s}{\omega_{LPF}}}$. The output waveform of a VCO can be described by $x(t) = \hat{V_0}\cos(\omega_{out}t)$ and $\omega_{out} = \omega_0 + K_{VCO}V_{cont}$. Since frequency is the derivative of phase, the phase of a sinusoid can be expressed as

$$\phi = \int \omega dt + \phi_0, \tag{2.37}$$

where ϕ_0 is the initial phase and usually assumed to be zero [29]. Substituting this result into $x(t)$ yields

$$x(t) = \hat{V_0}\cos\left(\int \omega_{out}dt\right). \tag{2.38}$$

$$= \hat{V_0}\cos\left(\omega_{out}t + K_{VCO}\int V_{cont}dt\right). \tag{2.39}$$

For the purpose of phaselocking, only the excess phase of the cosine argument is important. We use this term to obtain the transfer function of the VCO.

$$\phi_{ex} = K_{VCO}\int V_{cont}dt. \tag{2.40}$$

$$\frac{\Phi_{ex}}{V_{cont}}(s) = \frac{K_{VCO}}{s} \tag{2.41}$$

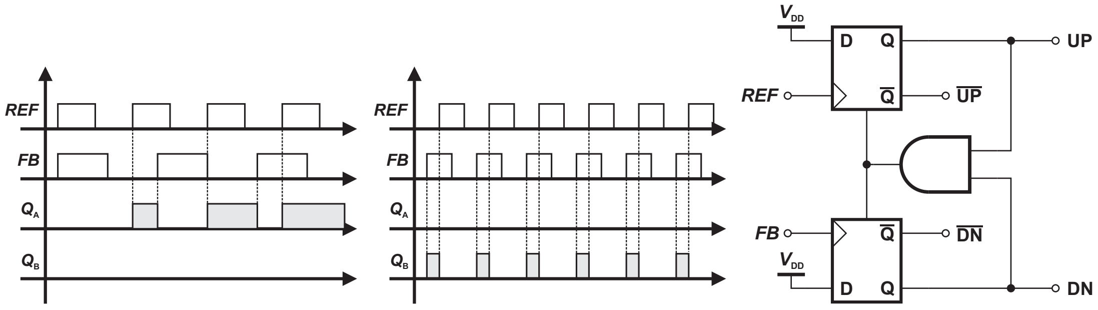
From (2.41) it is clear that the VCO operates as an ideal integrator. The open-loop and closed loop transfer functions for the simple PLL can be computed as:

$$H_{ol}(s) = \frac{\Phi_{out}}{\Phi_{in}} = K_{pd}\cdot\frac{1}{1+\frac{s}{\omega_{LPF}}}\cdot\frac{K_{VCO}}{s}, \tag{2.42}$$

$$H_{cl}(s) = \frac{K_{pd}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{pd}K_{VCO}}. \tag{2.43}$$

Further analysis of the simple PLL given in [29] shows that it suffers from two main drawbacks: (1) narrow lock acquisition range (2) tradeoffs between the settling time, control voltage ripple, phase error and stability. The range of frequencies over which the PLL can achieve phase lock is called the acquisition range, and is approximately limited to the bandwidth of the loop filter. In order to overcome this problem, the simple PLL must be modified. Specifically, the phase detector must be replaced with a block which can pull the output frequency within the acquisition range of the PLL, then perform phase locking as usual. This block is known as the phase/frequency detector, and will be discussed in the context of charge-pump phase lock loops described in the next section.

2.3.2 Charge-pump phase-locked loop



(a) $\omega_{REF} > \omega_{FB}$. (b) $\phi_{REF} < \phi_{FB}$. (c) Implementation.

Figure 2.19: Phase/frequency detector.

Before introducing the entire charge-pump phase-locked loop (CP-PLL), an overview of the new components will be given. As mentioned previously the phase detector is replaced with a circuit which can detect both phase and frequency differences of its input signals. The phase/frequency detector (PFD) has two inputs: REF and FB, and two outputs: UP and DN. The UP signal is high when the REF signal leads the FB signal in either phase or frequency. Likewise, the DN signal is high when the FB signals leads the REF signal in either phase or frequency. When a frequency error exists, such as in Fig. 2.19a, the UP signal is high between the rising edge of the REF signal to the rising edge of the FB signal. Similarly when a phase error exists, such as in Fig. 2.19b, the DN signal is high between the rising edge of the FB signal to the rising edge of the REF signal. In both cases, the output is proportional to either the phase or frequency difference between the inputs. The conventional implementation of the PFD consisting of two D-flip flops and an AND gate is shown in Fig. 2.19c.

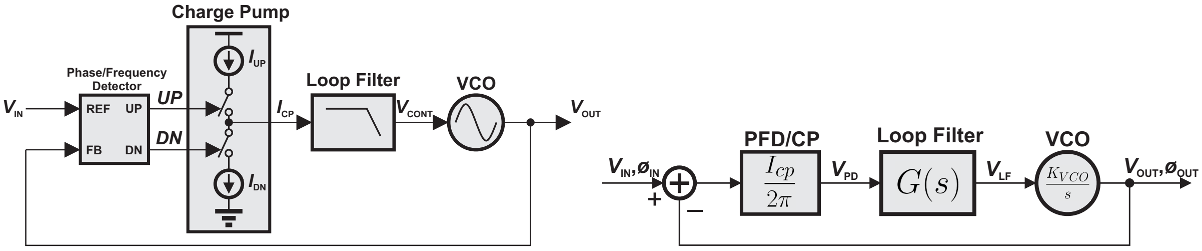
Unlike the simple PLL, the PFD output does not get filtered by the loop filter directly. Instead, the UP and DN outputs are used to drive a charge pump (CP), which consists of two switched current sources that add or subtract charge from the loop filter. A capacitor can be used as the loop filter since the purpose is for storing charge. The conceptual CP-PLL and its linear model are shown in Fig. 2.20.

In Fig. 2.20c the behaviour of the PFD/CP is shown. When UP is high, the top current source is enabled and dumps charge onto the loop filter capacitor until it goes low. The average value of the charge pump output, $\overline{I}_{CP}$, is proportional to the phase difference between REF and FB. Assuming that I_{UP}=I_{DN}=I, the average output current can be written as

$$\overline{I}_{CP} = I\frac{\Delta\phi}{2\pi}. \tag{2.44}$$

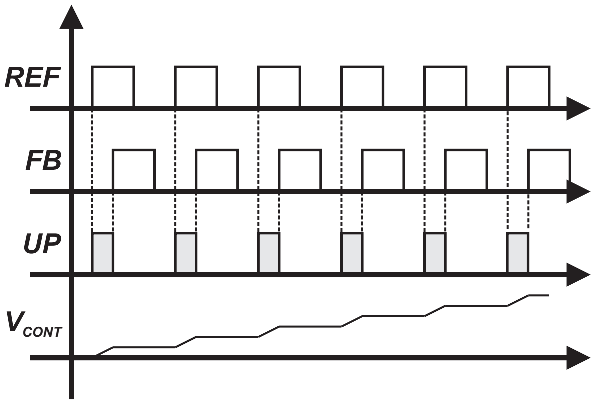
The gain of the PFD/CP combination, K_{pd}, is defined as the average charge pump output current for a given phase difference at the input of the PFD, and can be expressed as

$$K_{pd} = \frac{\overline{I}_{CP}}{\Delta\phi} = \frac{I}{2\pi}. \tag{2.45}$$


Charge Pump
Phase/Frequency Detector
V_{IN}
REF
UP
FB
DN
UP
DN
I_{UP}
I_{DN}
I_{CP}
Loop Filter
V_{CONT}
VCO
V_{OUT}
PFD/CP
V_{IN},ø$_{IN}$
+
−
$\frac{I_{cp}}{2\pi}$
V_{PD}
$G(s)$
V_{LF}
$\frac{K_{VCO}}{s}$
V_{OUT},ø$_{OUT}$

(a) Block diagram.

(b) Linear model.


REF
FB
UP
V_{CONT}

(c) Waveforms.

Figure 2.20: Charge-pump phase-locked loop.

Following the previous assumption that the loop filter is a single capacitor the loop filter transfer function, $G(s)$, is

$$G(s) = \frac{1}{sC_1}. \tag{2.46}$$

The open-loop and closed loop transfer functions for the CP-PLL can be computed,

$$\begin{aligned} H_{ol}(s) &= \frac{\Phi_{out}}{\Phi_{in}}, && (2.47)\\ &= \frac{I}{2\pi} \cdot \frac{1}{sC_1} \cdot \frac{K_{VCO}}{s}. && (2.48) \end{aligned}$$

$$H_{cl}(s) = \frac{\frac{K_{VCO}I}{2\pi C_1}}{s^2 + \frac{K_{VCO}I}{2\pi C_1}}. \tag{2.49}$$

Since the loop gain has two poles at the origin, each contributing 90° phase shift, the loop is unstable. Stabilization is realized by adding a resistor, R_1 in series with the capacitor, thus adding a zero to the loop gain. This resistor causes voltage drops on the control voltage whenever the charge pump injects/draws current to/from the loop filter, leading to frequency instability of the VCO. To resolve this a second capacitor, C_2 is placed in parallel with R_1 and C_1, whose value is approximately $\frac{1}{10}C_1$ as to not create stability problems.

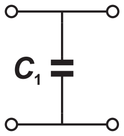
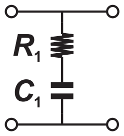
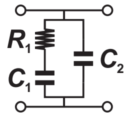
Configuration	Transfer Function
 (a)	$\frac{1}{sC_1}$
 (b)	$\frac{1+sR_1C_1}{sC_1}$
 (c)	$\frac{sR_1C_1+1}{s(C_1+C_2)\left[1+s(C_1\|\|C_2)\right]}$

Table 2.1: Loop filter topologies.

So far we have seen why VCOs are needed in transmitters and receivers, and why the nonidealities caused by PVT variations in CMOS processes require placing the VCO in a PLL configuration to generate a stable output frequency. The question now arises: knowing that the output frequency is equal to the input frequency in the locked condition, how can the PLL produce a multitude of output frequencies to operate within the desired spectrum? Recall Fig. 2.11 and assume the frequency at the lower end of the spectrum is f_0. To operate on the i^{th} channel of the spectrum, the PLL output frequency must be f_0+(i-1)B. In accordance with (2.37), one might think that in order to change the output frequency, the input frequency must be changed. This is not a practical solution for integrated circuit transmitters and receivers because the input frequency is generated by a highly stable crystal oscillator, and putting multiple crystals on chip corresponding to each output frequency is even less practical. Instead, a new block is inserted in the feedback path which allows a programmable constant of proportionality between the input and output frequencies. Producing multiple output tones from a single fixed reference frequency is called frequency synthesis. Although there are several frequency synthesizer architectures, the one which will be the focus of the following section is the integer-n architecture.

2.3.3 Integer-N frequency synthesizer

As shown in Fig. 2.21 an integer-n frequency synthesizer consists of a single high spectral purity quartz crystal oscillator as the reference for a PLL, and a frequency divider in the feedback path. The output frequency of the voltage-controlled oscillator (f_{OUT}) is an integer multiple of the reference frequency

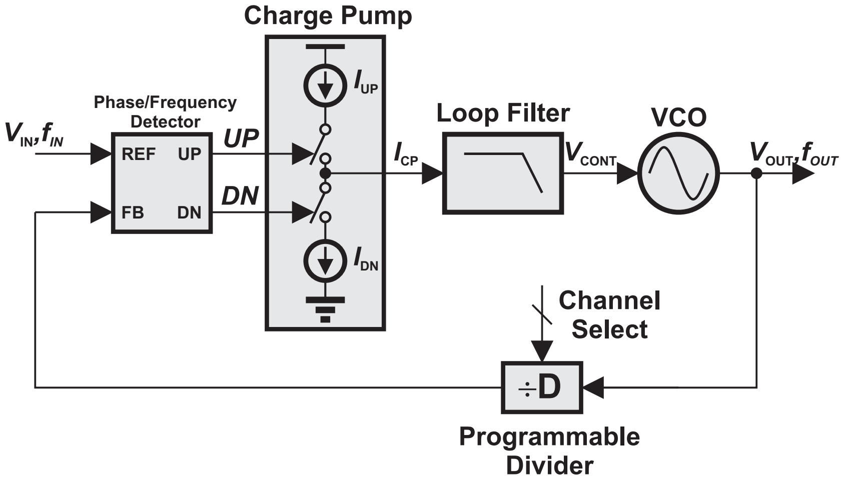
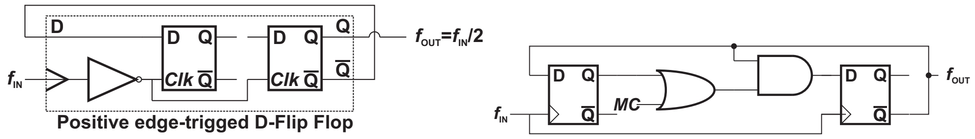

Charge Pump
I_{UP}
Phase/Frequency Detector
V_{IN}, f_{IN}
REF
UP
FB
DN
UP
DN
I_{CP}
Loop Filter
V_{CONT}
VCO
V_{OUT}, f_{OUT}
I_{DN}
Channel Select
÷D
Programmable Divider

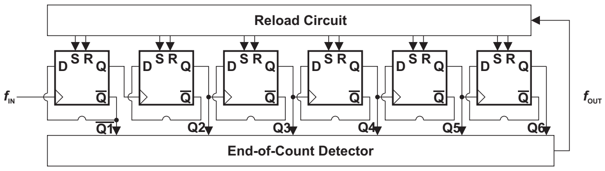
Figure 2.21: Integer-n frequency synthesizer block diagram.

(f_{IN}), yielding the relationship $f_{OUT} = D \times f_{IN}$. To generate frequencies given by f_{OUT}=f_0+(i-1)B, a frequency divider with variable modulus can be used. This can be achieved by using a programmable frequency divider whose modulus can be varied between D_L and D_H. By changing the division ratio of the divider, the RF carrier frequency will increase or decrease so that the relationship between f_{REF} and f_{IN} is satisfied. If $D \times f_{IN}$ has to equal f_0+(i-1)B, for the first channel (i=1) we have $D_L \times f_{IN}$=f_0, which implies that B=f_{IN}. For integer-n synthesizers, f_{IN} must be equal to the required channel spacing [44]. The three types of frequency dividers shown in Fig. 2.22 are used to design the programmable divider.


D
D Q
Clk Q
D Q
Clk Q
Q
Q
$f_{OUT}=f_{IN}/2$
f_{IN}
Positive edge-trigged D-Flip Flop
D Q
Q
MC
D Q
Q
f_{IN}
f_{OUT}

(a) Divide by 2.

(b) Divide by 2/3.


Reload Circuit
D S R Q
Q
f_{IN}
Q1
Q2
Q3
Q4
Q5
Q6
f_{OUT}
End-of-Count Detector

(c) Programmable counter.

Figure 2.22: Types of frequency dividers.

As given by its name, static modulus dividers are only capable of dividing by a fixed value, the simplest being divide-by-2 (Fig. 2.22a). Typically these dividers operate at high speeds and are useful for reducing the frequency so that subsequent logic which operates at lower frequencies can be used. When cascaded, these dividers can achieve a division ratio of 2^k, where k is the number of divide-by-two cells in cascade. By combining the divide-by-two circuit with some additional logic, a dual-modulus prescaler (DMP) with division ratio of M or $M+1$ is formed (Fig. 2.22b). The modulus control signal (MC) determines what value the divider divides by. Typical values of dual modulus dividers are 2/3, 4/5, 8/9, 15/16 and 32/33. A programmable divide-by-N counter (Fig. 2.22c) is a down counter consisting of cascaded asynchronous divide-by-2 stages, an end-of-counter (EOC) detector and a reload circuit. The value of N is determined by a control word which presets or clears each stage accordingly. Once the counter reaches the null state, a reload signal is produced and the countdown begins again. Since the reload signal is produced every N cycles, its frequency is f_{in}/N, where N can be programmed between 2 and 2^k-1 and k is the number of divide-by-2 stages in the counter.

The conventional programmable frequency divider is shown in Fig. 2.23. It consists of a dual-modulus prescaler and two programmable counters, referred to as the Pulse counter and Swallow counter. The programmable divider operates as follows: When a CLK_{OUT} pulse is generated by the Pulse counter, both counters reload to their initial states and the MC signal goes high. The initial states are determined by the S and P control words. The DMP divides CLK_{IN} by $(M+1)$ until the swallow counter has counted down to 0. The Swallow counter generates a CLK_{OUT} pulse which changes the MC to low and the DMP divides CLK_{IN} by M until the Pulse counter has counted down to 0. The Pulse counter generates a CLK_{OUT} pulse and the process repeats. Since the DMP divides by $(M+1)$ S times and by M $(P-S)$ times, the division ratio, D, of the programmable divider is given by

$$D = (M+1)S + (P-S)M, \tag{2.50}$$

$$= MP + S. \tag{2.51}$$

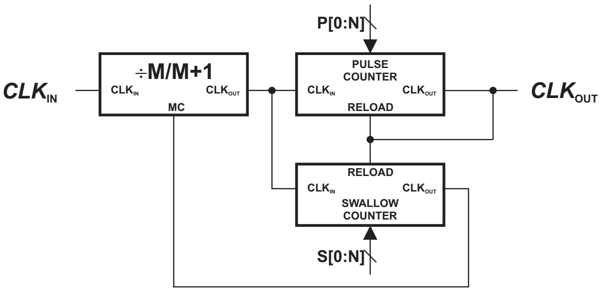


Figure 2.23: Block diagram of programmable frequency divider.

Channel selection can be performed by changing either the S or P control words. Typically the P counter is fixed and S is varied to allow selection of successive values.

It is evident from Fig. 2.22 that the D-flip flop (DFF) is a fundamental component in the presented types of frequency dividers. A popular implementation of the DFF is the master-slave D-latch configuration shown in Fig. 2.24.

D-latches can be implemented using many logic families as shown in Fig. 2.25, however the most common logic families are true single-phase clocked (TSPC) [45] and source-coupled logic (SCL) [46].

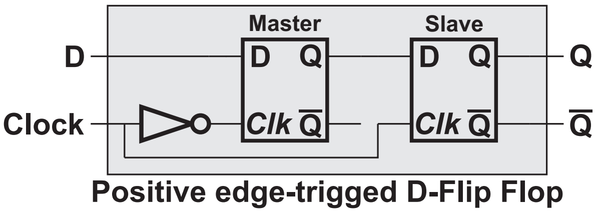
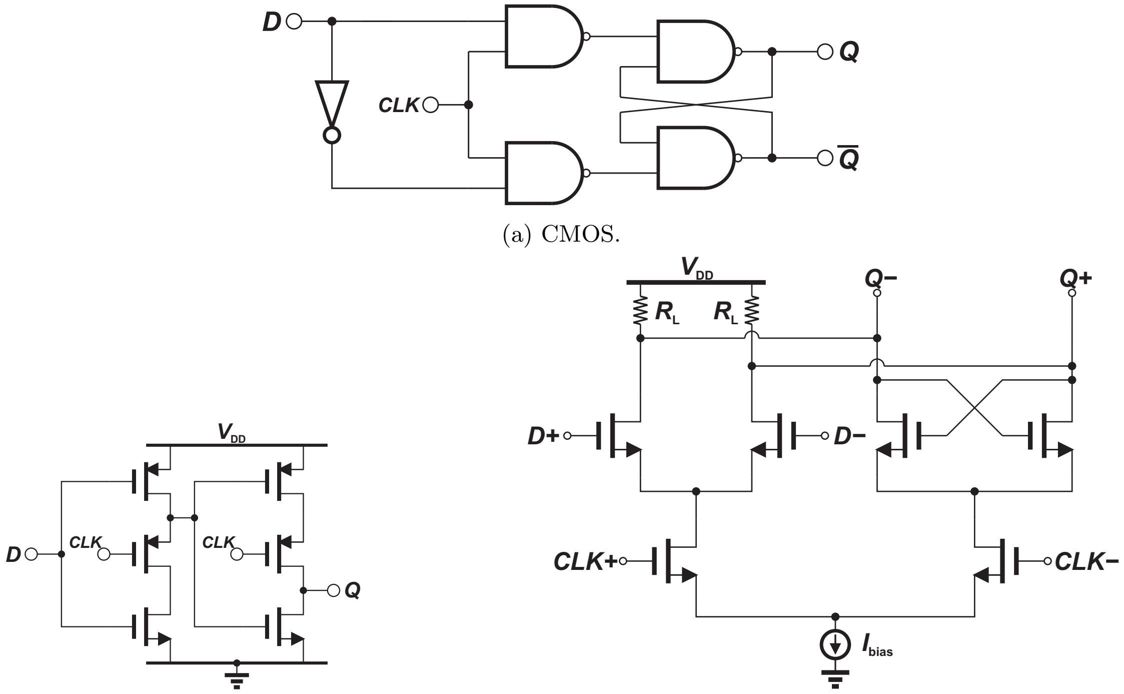


Figure 2.24: Master-slave d-flip flop.



(a) CMOS.

(b) TSPC.

(c) SCL.

Figure 2.25: Types of d-latches.

2.4 Summary

In this chapter, we have examined oscillators at the system and circuit level. Two approaches for oscillator analysis, the feedback model and the negative resistance model, were used to establish the conditions for oscillation. Using the conventional LC-tank oscillator as a starting point, we provided analysis and design criterion for the voltage-controlled oscillator and quadrature voltage-controlled oscillator. An important design metric, phase noise, was discussed and two important models for phase noise analysis, the Leeson model and Hajimiri-Lee model, were presented. Noting that an integrated circuit oscillator alone cannot produce a stable frequency due to process, supply voltage, and temperature variations, the phase-locked loop was introduced and system level analysis of a simple phase-locked loop and the charge-pump phase-locked loop were provided. To address the need for producing multiple tones from the phase-locked loop, the integer-n frequency synthesizer was introduced. The concepts presented in this chapter are fundamental to the understanding of the work proposed in this thesis.

Chapter 3

The Proposed Subthreshold 402 MHz to 405 MHz Integer-N Frequency Synthesizer

In this chapter, several novel circuits are proposed for use in an ultra-low power integer-n frequency synthesizer (Fig. 2.21) operating in the 402 MHz to 405 MHz MICS frequency band. Namely, a current-reuse quadrature voltage controlled oscillator, subthreshold source-coupled logic programmable divider with clear/preset d-latch, and subthreshold source-coupled logic phase/frequency detector are proposed. The evolution of each circuit from the conventional implementation to the proposed design is discussed.

3.1 Design specifications

Implantable medical devices are typically powered by batteries, which inherently have finite lifetimes. In order to maximize the lifetime of the implantable battery, IMDs must be designed to consume as little power as possible, since it is impractical to subject the patient to a medical procedure, such as surgery, to replace the battery. Measures must be taken at both the system level, such as power-off/wake-up circuitry for when the device is not transmitting or receiving data, and at the circuit level, by using novel circuits which reduce static power consumption of conventional designs. By recognizing that the fundamental definition of power consumption is $P = V \times I$, the power consumption can be reduced by minimizing the supply voltage, the bias current, or both simultaneously. The principal design approaches used to develop the proposed circuits are summarized as follows.

Current reuse: This can be achieved when two circuits consume the same bias current. Rather than biasing two circuits independently, the circuits are connected in a stacked topology between the supply rails and have a single bias current flowing through them. Conceptually this is illustrated in Fig. 3.1. This technique has been used successfully in [47] where the authors implemented a stacked quadrature Gilbert cell downconversion mixer and cascode low-noise amplifier, consuming 11.3 mW from a 2.5 V supply. Although this particular design does not provide ultra-low power consumption, it demonstrates the viability of this concept. In order to effectively employ this power saving technique, the supply voltage must be sufficient to keep all transistors in their desired region of operation.

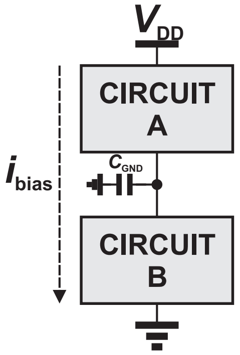


Figure 3.1: Current reuse between two stacked circuits.

Supply voltage scaling: The scaling of CMOS transistor minimum feature size (device length) has typically been accompanied with lower supply voltages (for example, 3.3 V for 350 nm, 2.5 V for 250 nm, 1.8 V for 180 nm, 1.2 V for 130 nm). However, as minimum feature sizes are scaled further into the tens of nanometers the supply voltage no longer scales at the same rate. This is caused in part by the reverse short channel effect, which is a separate discussion beyond the scope of this work. In order to provide sufficient voltage headroom to keep the devices in the strong inversion region, nanoscale processes do not scale the supply voltage at the same rate (for example, 1 V for 65 nm and 45 nm). If the supply voltage is scaled to the point where the device operates in the moderate or weak inversion regions, there are benefits from a power consumption point of view. The rationale for doing so will be discussed in the following section.

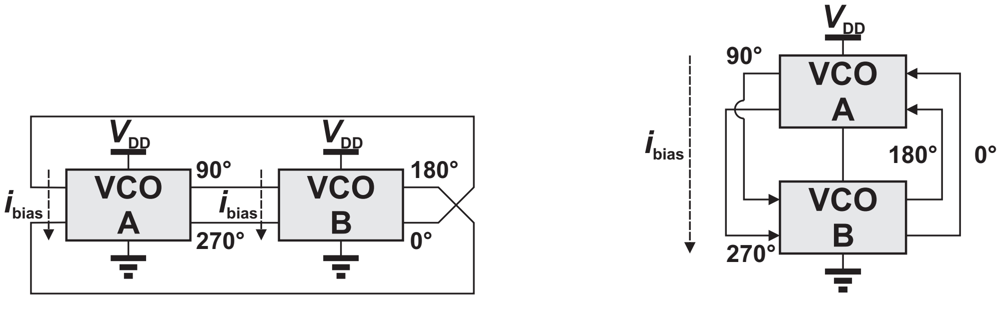
Weak inversion operation: It is well known that when the gate voltage of a device drops below its threshold voltage, current does not immediately stop flowing through the device. Rather, the device enters the weak inversion region, where the current-voltage relationship is exponential as opposed to the square-law relationship in strong inversion. Weak inversion operation bears a strong resemblance to bipolar transistor operation. It has been shown that the weak inversion region provides the highest "transconductance efficiency", g_m/i_d, which is the capability to translate current into transconductance [48]. By exploiting this property, a device operating in the weak inversion region is capable of producing the same transconductance as a device operating in strong inversion while consuming significantly less current, provided the transistor is sized correctly.

Using a combination of these power-saving techniques, novel circuits for an ultra-low power integer-n frequency synthesizer operating in the 402 MHz to 405 MHz MICS frequency band will be presented.

Development of these circuits, methods for achieving ultra-low power consumption, and design methodologies will be discussed. The synthesizer will satisfy the channel selection requirements of the MICS band, that is, it can tune to one of the ten channels which are spaced 300 kHz apart. Operation in the 401 MHz to 402 MHz and 405 MHz to 406 MHz wing bands designated in the MedRadio specifications will not be covered, the proposed design will operate only in the core MICS band. Since there are no set requirements for power consumption, the objective will be to provide lower power consumption and comparable or better performance than previously proposed designs.

3.2 Proposed current-reused quadrature voltage-controlled oscillator

Existing QVCO topologies consume significant amounts of power, making them unsuitable for ultra-low power applications such as IMDs. Increasing the quality factor of the tank to achieve high oscillation amplitude for small bias currents has its limits, since the quality factor of inductors in CMOS processes is typically between 10 to 20. Therefore, it is necessary to explore other means to reduce power consumption of the QVCO. One of the salient properties of the QVCO is that its power consumption is double that of the standard *LC* VCO, as shown in Fig. 3.2a. When stacking two different circuits, the performance of one circuit may be compromised because it may have better performance when biased independently. However in the QVCO both oscillator cores are ideally identical, thus current reuse is viable and will provide a 50% improvement in power consumption. The conceptual QVCO with current-reuse (CR-QVCO) is shown in Fig. 3.2b, where two coupled *LC* tank oscillators are stacked between the supply rails.



(a) Conventional QVCO.

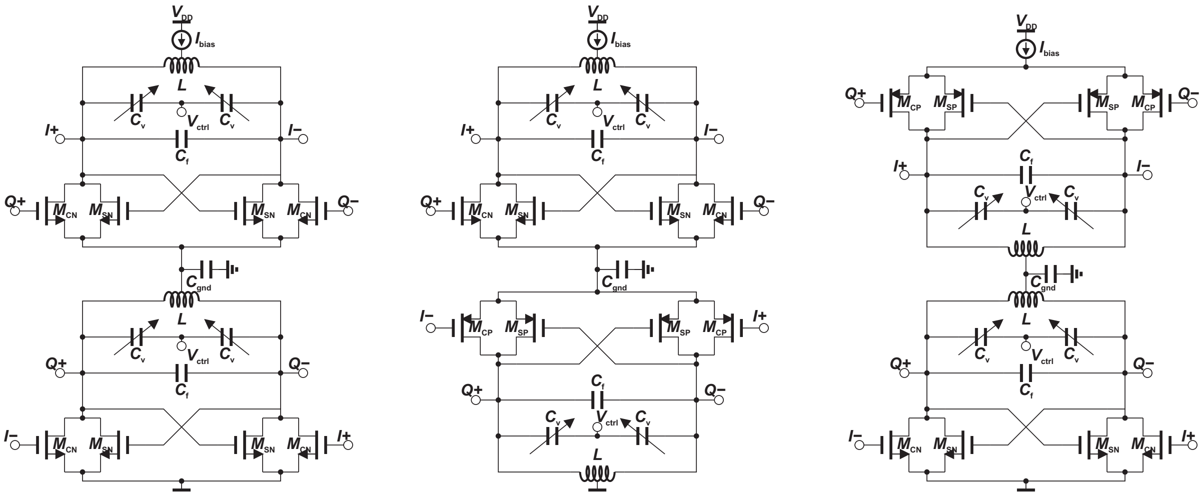
(b) Proposed QVCO with current-reuse.

Figure 3.2: Quadrature VCO block diagram.

Going back to the types of *LC* VCOs and QVCOs discussed in Chapter 2, the choice of oscillator topology for the CR-QVCO cannot be made arbitrarily. The ideal oscillator core is conducive to low voltage operation and provide minimum “challenges” for the designer. Firstly, the choice of coupling topology should be made. Since low voltage operation is one of the design criterion, the number of transistors which can be stacked between the supply rails must be kept to a minimum. For this reason, the SQVCO is not a suitable option because there would be five transistors connected between the supply rails – two from each oscillator core and one to provide the bias current. Both the PQVCO and the DS-QVCO would only have three transistors between the supply rails since the switching and coupling transistors are connected in parallel in both topologies. However, the authors of [41] showed that the PQVCO is a more robust topology than the DS-QVCO since it is less sensitive to mismatch in the tank components which lead to amplitude and phase errors.

Now that the QVCO topology has been selected, the implementation of each oscillator core must be determined. The complementary *LC* VCO can immediately be ruled out for the same reason as the SQVCO, leaving only three options:

- VCOs A and B are both NMOS or both PMOS (Fig. 3.3a).
- VCO A is NMOS, VCO B is PMOS (Fig. 3.3b).
- VCO A is PMOS, VCO B is NMOS (Fig. 3.3c).



(a) NMOS top and bottom. (b) NMOS top, PMOS bottom. (c) PMOS top, NMOS bottom.

Figure 3.3: Possible topologies for the proposed CR-QVCO.

By examining the potential CR-QVCO topologies shown in Fig. 3.3, the implementation which best suits the design specifications can be determined. We can observe some design challenges which complicate the circuit design in Fig. 3.3a and Fig. 3.3b. Firstly, the oscillator nodes (I+, I-, Q+, Q-) are at different potentials, therefore the coupling transistors of one oscillator can not be directly connected to the oscillator nodes of the other oscillator since they are biased at different voltages. A circuit to provide the correct bias voltages for the coupling transistors for each oscillator core is needed. One possibility is using a source follower amplifier which provides a level shift but has a gain of less than unity. Another option is to use a bias network such as the one shown in Fig. 3.4, where the capacitor

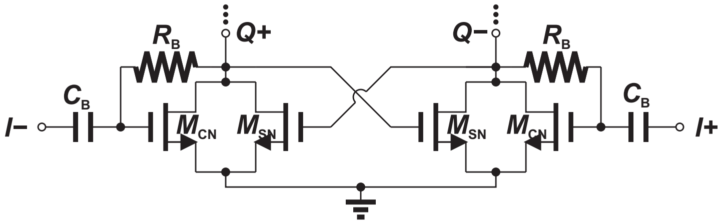


Figure 3.4: Modified oscillator core.

C$_b$ blocks the DC of the signal applied to the coupling transistor, and the resistor R$_b$ sets the DC bias of the coupling transistor to the same level as the oscillator node.

Furthermore, one or both cores will experience *body effect*, which occurs when $|V_{SB}| \neq 0$ and the threshold voltage of the transistor changed from its nominal value according to

$$V_{th} = V_{th0} + \gamma \left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F} \right), \tag{3.1}$$

where V_{th0} is the nominal threshold voltage, γ is the body effect parameter, and ϕ_F is the Fermi potential. Again the biasing problem arises since the switching transistors will be on and off during different parts of the oscillation period.

As mentioned above the oscillator nodes are at different potentials, therefore the control voltage can not be applied to the varactors directly. This is because the voltage across the varactor in each core will be different, and each core's tank will have a different resonant frequency. A "frequency tuning circuit" can be added to each tank to ensure the varactors have the same voltage across them. However the frequency tuning circuit also degrades the phase noise due to the thermal noise generated by biasing resistors.

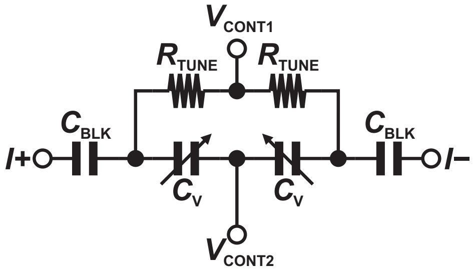


Figure 3.5: Varactor frequency tuning circuit.

This leaves the circuit in Fig. 3.3c, with PMOS transistors in the top oscillator core and NMOS transistors in the bottom oscillator core. In this topology, the oscillator nodes for both cores are at the same DC level (ignoring the losses across the inductors), eliminating the need for DC level shifting of the coupling transistor inputs and the use of a frequency tuning circuit for the varactors. For these reasons, this topology will be used for implementing the proposed CR-QVCO.

The capacitor, C$_{GND}$, at the intermediate node provides AC ground for both oscillators, and allows the cores to be decoupled for analytical purposes. The analysis is similar to the previously discussed PQVCO, however modifications must be made to the oscillation amplitude equation as it did not account for two important properties of the CR-QVCO. Firstly, the startup conditions for the CR-QVCO are not what was given in (2.11). In their analysis of the PQVCO, the authors of [38] noted that by adding the coupling transistors to the oscillator core, the loading effect decreases the input impedance of the cross-coupled transistors by a factor of $\frac{1}{\sqrt{2}}$. Thus for the same bias current, the oscillation amplitude decreases by a factor of $\frac{1}{\sqrt{2}}$ as well,

$$\hat{V_0} = \frac{2}{\sqrt{2}\pi}(1-\delta)I_{bias}R_p. \tag{3.2}$$

In order to achieve the same oscillation amplitude as predicted by (2.33), the bias current must be increased by a factor of $\sqrt{2}$. Furthermore, the equations describing oscillator amplitude all referred to oscillators using the topology of Fig. 2.3a, which uses two planar spiral inductors as shown in Fig. 2.5a. However, the design proposed uses a differential spiral inductor of Fig. 2.6a to improve symmetry in the tank. Although the tank resonant frequency is defined as $\frac{1}{\sqrt{LC}}$, the bias current is injected through the center tap and during each half-cycle flows through $\frac{L}{2}$. As a result, the bias path for the transistor includes only half the total inductance, and the equivalent parallel resistance that the bias current flows through becomes

$$R_p = \omega_0 \frac{L}{2} Q, \tag{3.3}$$

which is half of the expected tank parallel resistance, which further reduces the oscillation amplitude to

$$\hat{V_0} = \frac{2}{\sqrt{2}\pi}(1-\delta)I_{bias}\frac{R_p}{2}. \tag{3.4}$$

Taking these two modifications into consideration, the oscillation amplitude of the CR-QVCO using a differential, center-tapped inductor is

$$\hat{V_0} = \frac{1}{\sqrt{2}\pi}(1-\delta)I_{bias}R_p. \tag{3.5}$$

With respect to supply voltage scaling, if the CR-QVCO is to be designed for weak inversion (subthreshold) operation the supply voltage can be approximated as

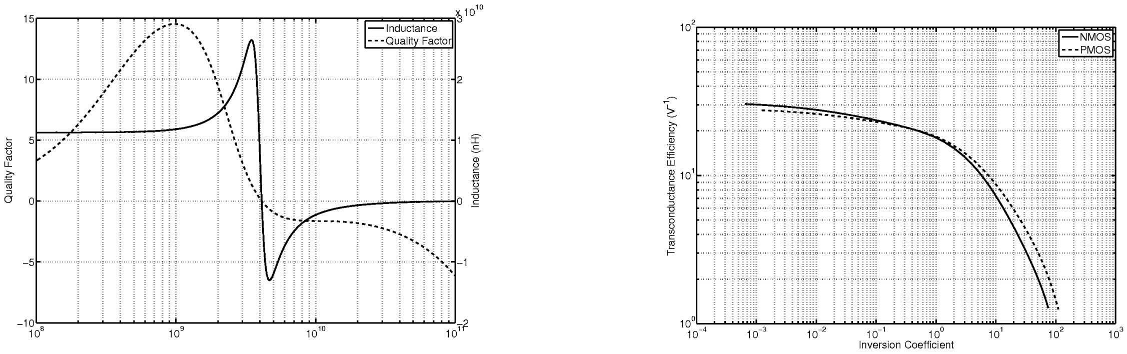
$$V_{DD} = V_{thn} + |V_{thp}| + V_{DSAT}, \tag{3.6}$$

where V_{thn} and V_{thp} are the threshold voltages of the NMOS and PMOS transistors respectively, and V_{DSAT} is the saturation voltage of the current source transistor. Since the transistors are biased in the subthreshold region, the supply voltage can be lower than this value because the DC bias points of the switching transistors will be less than $V_{thn,p}$.

3.2.1 Proposed low power VCO design methodology

Now that we have developed equations describing various *LC* VCO topologies, we present a design methodology for sizing the switching transistors (and coupling transistors for QVCOs) based on the MOS EKV Model, a charge based model that accurately describes transistor behaviour in all three levels of inversion, and the g_m/i_d design methodology, which has previously been used in the design of output transconductance amplifiers (OTAs). For this methodology, the g_m/i_d design methodology is modified to consider the important criteria of *LC* VCOs rather than OTAs. The reader should first refer to Appendix A for an overview of the MOS EKV Model and g_m/i_d design methodology if they are not already familiar with these concepts.

First some information needs to be obtained about the devices used in the design which are used as inputs in the proposed methodology. It is assumed that the inductor has been selected to provide the maximum inductance and quality factor, and therefore maximum equivalent parallel resistance, at the frequency of interest. This data can be obtained from the documentation of the semiconductor foundry's process design kit, or by electromagnetic simulation using a tool such as ASITIC or Cadence Virtuoso Passive Component Designer. An example of the inductance and quality factor vs. frequency graph is shown in Fig. 3.6a. The graph of transconductance efficiency vs. inversion coefficient (g_m/i_d vs. IC) can be obtained from measurement of a fabricated device or by simulation provided that the MOS model provides a continuous representation of the transistor current and small signal parameters in all regions of operation. The inversion coefficient is defined by parameters in the MOS EKV model, and is used to obtain the required transistor aspect ratio ($\frac{W}{L}$) to satisfy the oscillator design criteria. An example of the transconductance efficiency vs. inversion coefficient graph extracted from 130 nm NMOS and PMOS transistors using the BSIM4 transistor model is shown in Fig. 3.6b.



(a) Inductance and quality factor vs. frequency.

(b) Transconductance efficiency vs. inversion coefficient.

Figure 3.6: Necessary graphs for proposed design methodology.

The flow chart of the proposed design methodology is shown in Fig. 3.7. The methodology starts with the desired specifications of the VCO as inputs, namely the inductance (L) and quality factor (Q) of the inductor, oscillation amplitude ($\hat{V_0}$), the free running frequency (ω_0), the tuning range (TR), the startup factor (β), and in the case of quadrature oscillators the coupling factor (α). Using these parameters the intermediate parameters are calculated and from Fig. 3.6b the transistor aspect ratios can be obtained.

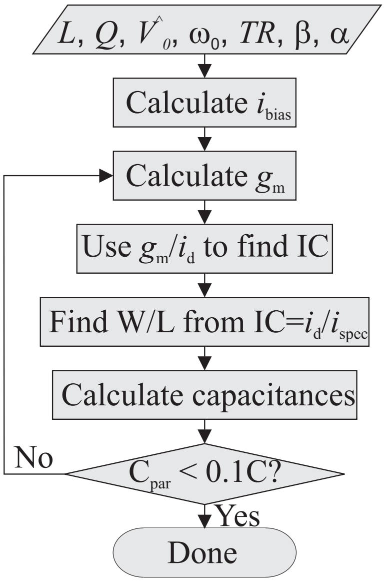


Figure 3.7: Proposed VCO design methodology.

The first step is to calculate the total bias current for the VCO. The relationship between bias current for the VCO topologies discussed so far and the input parameters of the design methodology are summarized below:

$$\hat{V_0} = \begin{cases} \frac{2}{\pi} I_{bias} R_p & \text{Fig. 2.3a, Fig. 2.9b} \\ \frac{1}{\pi} I_{bias} R_p & \text{Fig. 2.7} \\ \frac{2}{\pi}(1-\delta) I_{bias} R_p & \text{Fig. 2.17} \\ \frac{1}{\sqrt{2}\pi}(1-\delta) I_{bias} R_P & \text{Fig. 3.3c} \end{cases} \tag{3.7}$$

To ensure oscillator startup, the transconductance can be calculated using (2.12) taking into account the startup factor β. With the transconductance and bias current at hand, the transconductance efficiency for the switching transistors (and coupling transistors for a QVCO) can be calculated. It is important to note that since the transconductance efficiency is a parameter for a single device, the drain current to be used is the amount of DC current flowing through each device. Looking back to (2.19), the DC component of the drain current is equal to $\dfrac{1}{2} I_{bias}$ and therefore the transconductance efficiency for each transistor is $g_m / \frac{1}{2} I_{bias}$. For a PQVCO, the bias current has to be scaled further since each half of the current is shared by the switching and coupling transistors as per (2.31). Once the transconductance efficiency has been computed, the corresponding inversion coefficient can be obtained from Fig. 3.6b. Finally the definition of the inversion coefficient is rearranged to solve for the transistor aspect ratio,

$$\left(\frac{W}{L}\right) = \frac{i_d}{2n\mu_0 C'_{ox} U_t^2 IC}, \tag{3.8}$$

where n is the subthreshold slope parameter of the device, μ_0 is the carrier mobility, C'_{ox} is the gate oxide capacitance density, U_t is the thermal voltage and IC is the inversion coefficient. These parameters are described in Appendix A.

The device aspect ratio varies significantly depending on the region of inversion that the transistor operates in. As the device goes from strong inversion to weak inversion, the aspect ratio increases, which gives rise to increases in the gate capacitance of the device. This poses a problem since the gate capacitance is inversely proportional to the device unity gain frequency, ω_T, which is defined by

$$\omega_t = \frac{g_m}{C_G} = \frac{g_m}{C_{Gi} + C_{Go}} = \frac{g_m}{\underbrace{C_{GSi} + C_{GDi} + C_{GBi}}_{C_{Gi}} + \underbrace{2WL_{ov}C_{ox}}_{C_{Go}}}. \tag{3.9}$$

All of the device capacitances are summarized in Appendix A.

In weak inversion the intrinsic gate capacitance is dominated by the gate-to-bulk capacitor, and the unity gain frequency can be approximated as

$$\omega_t = \frac{g_m}{C_{GBi} + 2WL_{ov}C_{ox}} = \frac{g_m}{WC_{ox}\left(\dfrac{n-1}{n} + 2L_{ov}\right)}. \tag{3.10}$$

In order to ensure the oscillator exhibits the desired behaviour the unity gain frequency must be greater than oscillation frequency, otherwise the circuit will not oscillate. The large capacitances also have another negative effect on the oscillator. The large, nonlinear capacitors of the device are added to the capacitance of the LC tank, which affects both the free-running frequency and the tuning range of the oscillator. The total tank capacitance is now comprised of the fixed capacitor, the varactor, and the device capacitances. In order to limit the effects of these unwanted capacitances, they must account for less than 10% of the total tank capacitance. If these criteria are satisfied, the design methodology is complete.

As illustrated in Chapter 2, phase noise expressions are very complicated and depend on parameters which can only be obtained through measurement. Therefore it cannot be used as part of the hand-analysis portion of the design methodology and must be obtained through simulation. If the simulated phase noise does not meet the desired specifications, the input parameters of the methodology must be adjusted accordingly.

3.3 A subthreshold source-coupled logic programmable divider

The pulse-swallow frequency division architecture described in Section 2.3.3 is used in the proposed design. The synthesizer must be able to operate on one of the 10 channels in the 402 MHz to 405 MHz spectrum, with each channel spaced 300 kHz apart. Intuitively one would design the divider so that the output frequency of the i^{th} channel is

$$f_{OUT} = 402 \text{ MHz } + \text{ (i-1)300 kHz}, \tag{3.11}$$

but referring to Fig. 1.3 this would lead to the frequency synthesizer tuning to the *channel edges* rather than the *center frequency* of the channel (and there are 11 values of i which satisfy (3.11), not 10). The channel selection scheme must therefore be modified so that the center frequency of the channel is selected. If we continue to use 300 kHz as the reference frequency, we will have the division ratios in Table 3.1.

Channel #	f_{out}	D
1	402.15 MHz	1340.5
2	402.45 MHz	1341.5
3	402.75 MHz	1342.5
4	403.05 MHz	1343.5
5	403.35 MHz	1344.5
6	403.65 MHz	1345.5
7	403.95 MHz	1346.5
8	404.25 MHz	1347.5
9	404.55 MHz	1348.5
10	404.85 MHz	1349.5

Table 3.1: Division ratios for integer-n frequency synthesizer with 300 kHz reference frequency.

However these values of D listed in Table 3.1 cannot be used because they are not integers. Reorganizing the relationship between the input and output frequencies of the frequency synthesizer, we have

$$D = \frac{f_{OUT}}{f_{IN}}, \tag{3.12}$$

which means we can obtain an integer value of the division ratio by either doubling the output frequency, which means running the VCO at twice the desired output frequency, or using half the value of the reference frequency. In the former, a divide-by-two block would be added outside the frequency synthesizer loop to achieve the desired output frequency. In the latter, the reference frequency changes from 300 kHz to 150 kHz. In either case the same division ratios will apply, as shown in Table 3.2.

Now that an integer value of D has been obtained, the dual-modulus divider, pulse counter and swallow counter values must be obtained to satisfy (2.51). By using a divide-by-32/33 dual-modulus divider (M=32), the values of the pulse (P) and swallow (S) counters can be obtained by assuming a value for P and solving for the range of values for S. For P=82,

Channel #	f_{OUT}	D
1	804.3 MHz	2681
2	804.9 MHz	2683
3	805.5 MHz	2685
4	806.1 MHz	2687
5	806.7 MHz	2689
6	807.3 MHz	2691
7	807.9 MHz	2693
8	808.5 MHz	2695
9	809.1 MHz	2697
10	809.7 MHz	2699

(a) Doubling VCO frequency.

Channel #	f_{OUT}	D
1	402.15 MHz	2681
2	402.45 MHz	2683
3	402.75 MHz	2685
4	403.05 MHz	2687
5	403.35 MHz	2689
6	403.65 MHz	2691
7	403.95 MHz	2693
8	404.25 MHz	2695
9	404.55 MHz	2697
10	404.85 MHz	2699

(b) Halving reference frequency.

Table 3.2: Division ratios for integer-n frequency synthesizer with new division ratios.

$$\begin{aligned} S &= D - MP \qquad (3.13) \\ &= 2681 - (32)(82) \qquad (3.14) \\ &= 2681 - 2624 \qquad (3.15) \\ &= 57, \qquad (3.16) \end{aligned}$$

and so on for other values of D. Using these values, the range of S is [57, 59, ... 75], therefore both the P and S counters must be 7-bit down counters. If we assume P=83,

$$\begin{aligned} S &= D - MP \qquad (3.17) \\ &= 2699 - (32)(83) \qquad (3.18) \\ &= 2699 - 2656 \qquad (3.19) \\ &= 43, \qquad (3.20) \end{aligned}$$

and so on for other values of D. Using these values, the range of S is [25, 27, ... 43], therefore only the P counter must be 7-bits and the S counter can be a 6-bit counter. As specified previously, the pulse counter has a fixed modulus and its control bits can be set on-chip, but the swallow counter must be programmable – either off-chip or by separate control logic. Consider the control word $S[5:0] = S_5S_4S_3S_2S_1S_0$, the control bits are assigned as shown in Table 3.3.

If the swallow counter is programmed off-chip, six additional inputs would be required for the test fixture. By analysing the truth table of Fig. 3.3 we can observe that $S_5 = \overline{S_4}$ and $S_0 = 1$. The number of inputs can therefore be reduced to four by inverting S_5 to obtain S_4 and forcing the state of S_0 to a logic 1. The gate-level diagrams of the 7-bit pulse counter, the 6-bit swallow counter and divide-by-32/33 DMP are shown below. The DMP divides by 32 when MC is logic 0 and by 33 when MC is logic 1.

Decimal	S_5	S_4	S_3	S_2	S_1	S_0	Division Ratio
25	0	1	1	0	0	1	2681
27	0	1	1	0	1	1	2683
29	0	1	1	1	0	1	2685
31	0	1	1	1	1	1	2687
33	1	0	0	0	0	1	2689
35	1	0	0	0	1	1	2691
37	1	0	0	1	0	1	2693
39	1	0	0	1	1	1	2695
41	1	0	1	0	0	1	2697
43	1	0	1	0	1	1	2699

Table 3.3: Control bits for the swallow counter.

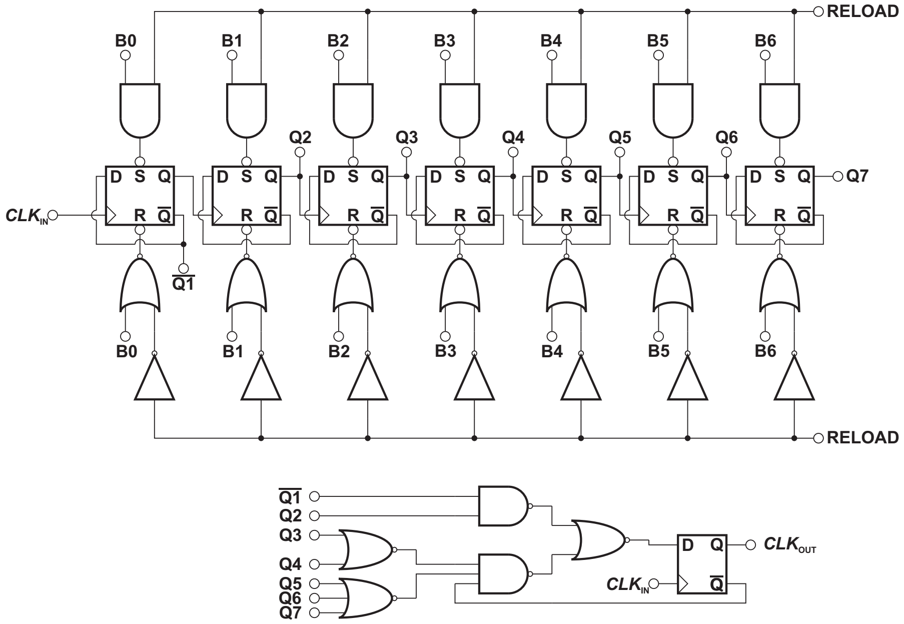


Figure 3.8: Block diagram of pulse counter.

Previously proposed low power programmable frequency dividers were implemented using true single-phase clocked (TSPC) logic [49], [50], [51]. Although TSPC logic occupies small silicon area, it suffers from drawbacks such as generation of switching noise, charge leakage at low frequencies, and requires rail-to-rail input signal swing [52]. These drawbacks can be avoided by using source-coupled logic (SCL) at the expense of increased silicon area. Additionally these implementations were designed for saturation region operation and therefore their power consumption is high relatively compared to ultra-low power requirements. The general circuit implementation of an SCL gate is shown in Fig. 3.11.

SCL gates are implemented by properly stacking NMOS differential pairs to achieve a particular logic function. The bias current, I_{bias}, is steered to one of the two load resistors, R_L, by the NMOS

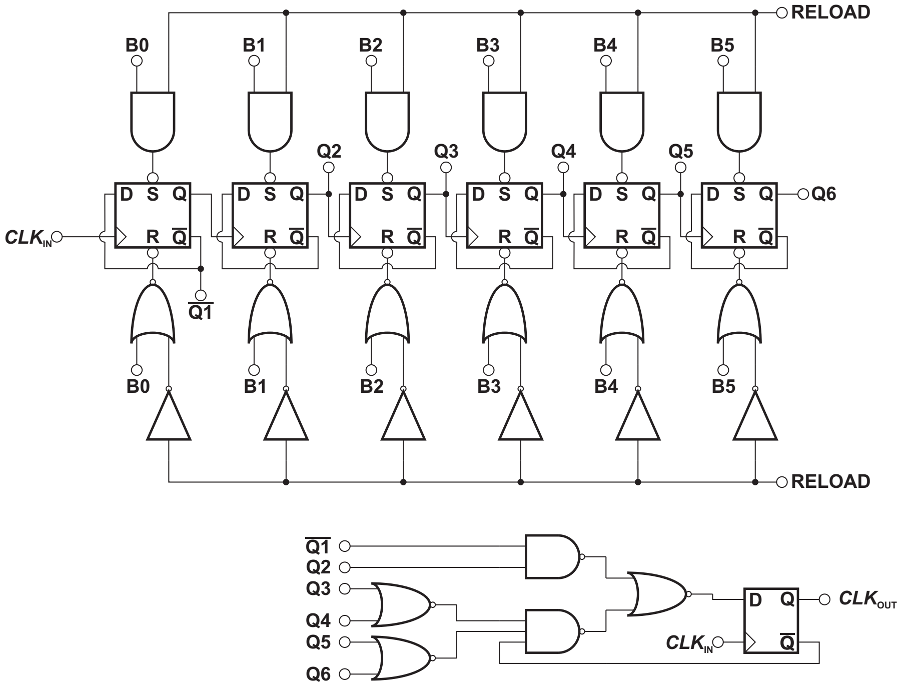

RELOAD
B0
B1
B2
B3
B4
B5
Q2
Q3
Q4
Q5
Q6
D S Q
R Q̄
CLK_IN
Q̄1
RELOAD
Q̄1
Q2
Q3
Q4
Q5
Q6
D Q
Q̄
CLK_IN
CLK_OUT

Figure 3.9: Block diagram of swallow counter.

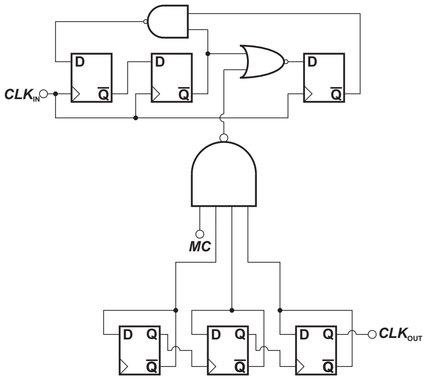

CLK_IN
D
Q̄
MC
D Q
Q̄
CLK_OUT

Figure 3.10: Block diagram of dual modulus prescaler.

differential pair network according to its input signal values. SCL has several advantages when compared to static CMOS logic. Firstly, CMOS gates consume dynamic power but no static power, and SCL gates consume static power but no dynamic power. This feature means that SCL gates do not generate switching noise like static CMOS gates do. Static CMOS logic conventionally uses negative logic, but SCL gates have complementary outputs, eliminating the need for extra inverters to produce positive logic gates. Additionally, by virtue of De Morgan's Law, 2-input AND/NAND and OR/NOR functions can be implemented using a single gate simply by swapping the positive and negative inputs and outputs of the 2-input gate [53]. The "universal gate" which implements both the AND/NAND and OR/NOR

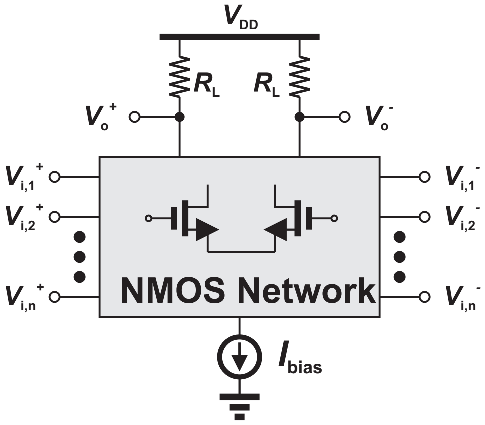
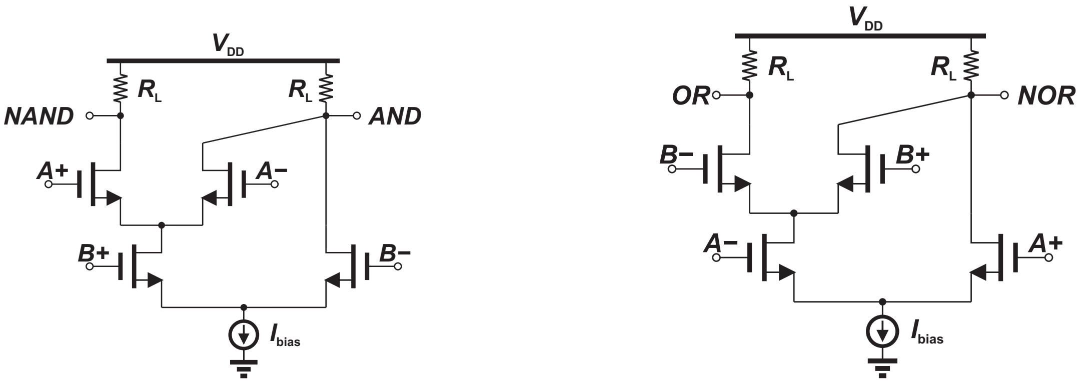


Figure 3.11: General topology of an SCL gate.

functions is shown in Fig. 3.14.



(a) AND/NAND.

(b) OR/NOR.

Figure 3.12: SCL 2-input universal gate.

As mentioned previously, the D-latch is an integral component in the programmable divider. The SCL D-latch shown in Fig. 2.25c replaces the load resistances with PMOS devices operating in the triode region. This implementation of the D-latch is not suitable for use in the programmable counter for two reasons. Referring to Fig. 3.8 and Fig. 3.9 the D-flip flop, which is implemented using the master-slave topology of Fig. 2.24, requires clear and preset capability in order to initialize the counter values when a reset occurs. As well, the PMOS load device cannot achieve a high resistance value, thus if the device is biased in the subthreshold region and consumes only a few microamps a load resistance on the order of tens to hundreds of kilo-ohms would be needed to generate a usable output voltage swing. In the following section, a novel D-latch which addresses both these design issues is proposed.

3.3.1 Proposed D-latch with clear and preset functionality

Previously proposed latches presented in literature are not suitable for low power, low voltage applications such as implantable medical devices because they required too many stacked transistors [54], [55] or do not perform both clear and preset functions [56], [57]. In order to correctly implement the programmable counters, the clear and preset functions are required for the D-latches to build master/slave D-flip flops with clear and preset functions. To this end, a novel D-latch with clear and preset is proposed. The power consumption of the proposed design is reduced by using the load device presented in [58]. The authors demonstrated that a high resistance load device can be obtained by shorting the bulk of a minimum sized PMOS transistor to its drain (rather than its source), reducing the amount of bias current required to achieve an output voltage sufficient to drive subsequent gates. The proposed design is shown in Fig. 3.13.

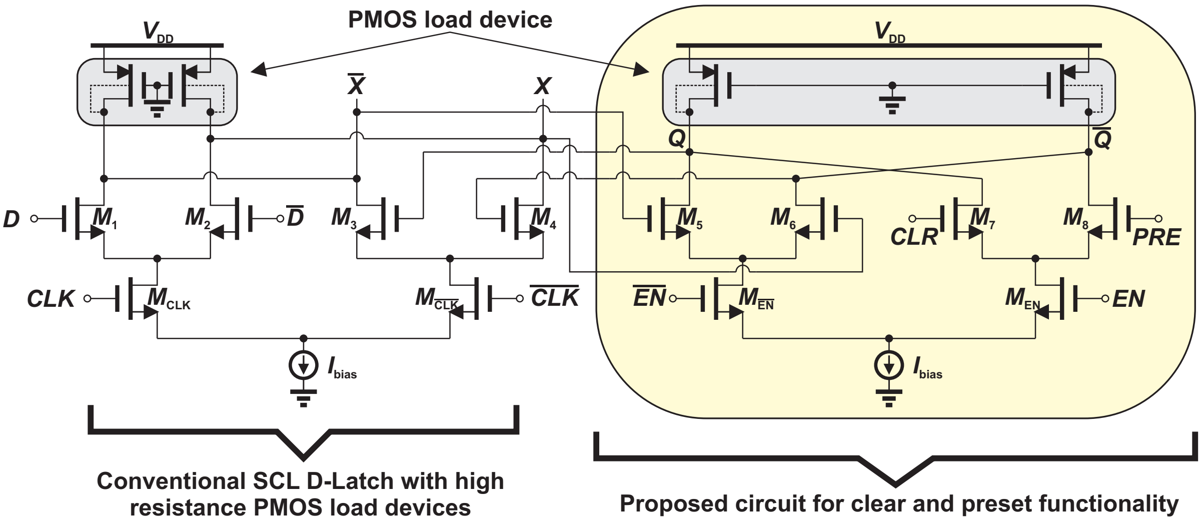
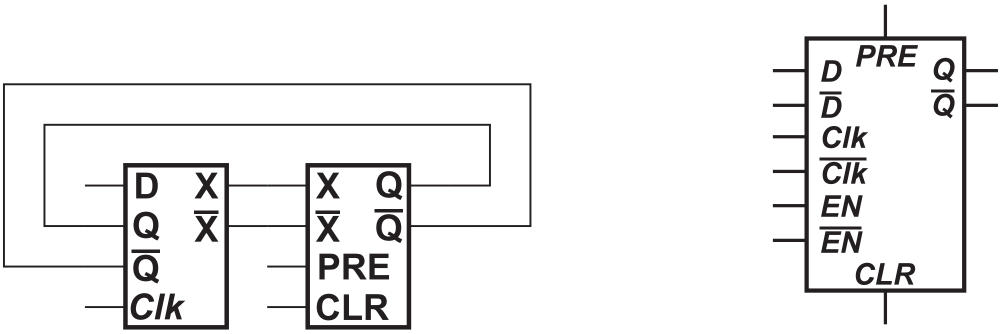

V_{DD}
PMOS load device
V_{DD}
$\overline{X}$
X
Q
$\overline{Q}$
D
M_1
M_2
$\overline{D}$
M_3
M_4
M_5
M_6
CLR
M_7
M_8
PRE
CLK
M_{CLK}
$M_{\overline{CLK}}$
$\overline{CLK}$
$\overline{EN}$
$M_{\overline{EN}}$
M_{EN}
EN
I_{bias}
I_{bias}
Conventional SCL D-Latch with high resistance PMOS load devices
Proposed circuit for clear and preset functionality

Figure 3.13: Proposed D-latch with clear and preset.


D
Q
$\overline{Q}$
Clk
X
$\overline{X}$
X
$\overline{X}$
PRE
CLR
Q
$\overline{Q}$
D
$\overline{D}$
Clk
$\overline{Clk}$
EN
$\overline{EN}$
PRE
CLR
Q
$\overline{Q}$

(a) Proposed D-latch (conceptual).

(b) Symbol of proposed D-latch.

Figure 3.14: Representations of proposed D-latch.

The proposed D-latch consists of two stages and requires an additional input to enable the clear and preset circuit. The first stage is a D-latch where the sensing pair ($M1, M2$) is active while CLK is high and the latching pair ($M3, M4$) is active while CLK is low. Instead of cross coupling the outputs of the sensing pair via the latching pair as in a conventional SCL D-latch, the intermediate outputs ($X, \overline{X}$) are routed to the second stage. Devices $M5, M6$ act as a buffer when EN is low, and the outputs are fed back to the latching pair. When EN is high, the Set/Reset latch ($M7, M8$) is active and the latch is initialized according to the state of CLR and PRE. The complementary enable signals can be generated by

$$EN = CLR \oplus PRE, \tag{3.21a}$$

$$\overline{EN} = \overline{CLR \oplus PRE}. \tag{3.21b}$$

This comes at the cost of an additional XOR/XNOR gate, since SCL gates produce complementary outputs. However in this application EN can be obtained from the $RELOAD$ signal generated by the pulse counter, eliminating the need for the additional logic gate.

3.4 A subthreshold source-coupled logic phase/frequency detector, modified current-steering charge pump and loop filter

The phase/frequency detector (PFD) uses the architecture of Fig. 2.19c. The proposed D-latch with clear preset are is to implement the master-slave D-flip flops in the PFD. The outputs of the 2-input SCL AND/NAND gate drives the EN and $\overline{EN}$ signals in the proposed D-latch. In order to perform the required function, the CLR signal is tied to the positive supply and the PRE signal is tied to the negative supply. The block diagram of the PDF is shown in Fig. 3.15

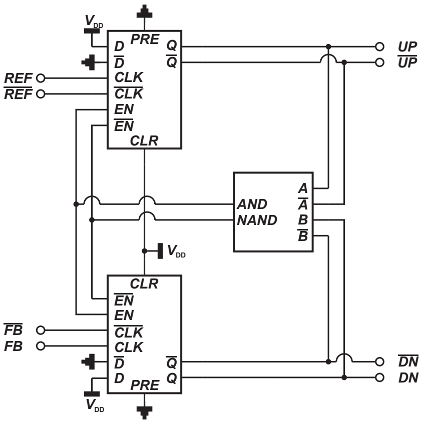

V_{DD}
PRE
D
$\overline{D}$
Q
$\overline{Q}$
REF
$\overline{REF}$
CLK
$\overline{CLK}$
EN
$\overline{EN}$
CLR
UP
$\overline{UP}$
AND
NAND
A
$\overline{A}$
B
$\overline{B}$
V_{DD}
CLR
$\overline{EN}$
EN
$\overline{FB}$
FB
$\overline{CLK}$
CLK
$\overline{D}$
D
$\overline{Q}$
Q
PRE
$\overline{DN}$
DN
V_{DD}

Figure 3.15: Phase/frequency detector using proposed clear/preset D flip-flop.

The charge-pump used in this work is a modification of the low voltage charge pump circuit proposed in [59]. The circuit consists of a wide-swing current mirror and symmetric charge pumps to provide I_{UP} and I_{DN}. Each charge pump is controlled by a differential input pair biased with a tail current source, a current mirror load and a diode connected load. In the "pump up" circuit, when UP is high the bias current flows through M_1 and is mirrored to the output through the current mirror $M_{5,16}$. A pull-up transistor M_9 is added to immediately bring the gate of the current mirror transistors to V_{DD} when UP is low in order to shut off the current mirror and prevent any current from leaking into the output. The "pump down" circuit can be analysed in the same fashion. The wide-swing current mirror M_{11-14} mirrors the pump down current to the output of the charge pump. The loop filter is a 3rd order passive filter as shown in Table 2.1c.

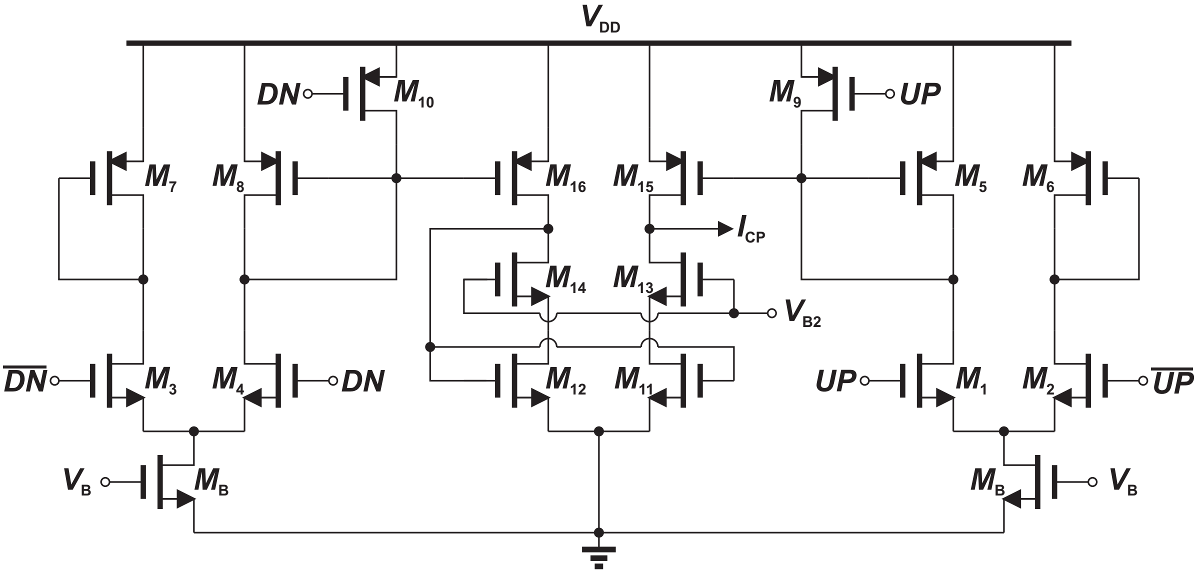


Figure 3.16: Current-steering charge pump.

3.5 Summary

In this chapter, we proposed a current reuse QVCO, a design methodology for low-power VCOs, a subthreshold source-coupled logic pulse/swallow counter using a novel D-latch with clear and preset functionality, and a modified current-steering charge pump. Current reuse, supply voltage scaling and subthreshold operation were introduced as means to reduce the power consumption of the QVCO. The clear/preset D-latch was designed to be conducive to low voltage operation, which was not possible with previously published designs. The proposed circuit designs will be used to implement an integer-n frequency synthesizer that operates in the 402 MHz to 405 MHz Medical Implant Communication Service frequency spectrum. The block diagram of the proposed frequency synthesizer is shown in Fig. **??**. In the following chapter, the simulation and measurement results of the proposed designs are presented, along with comparisons to existing designs.

Chapter 4

Results

4.1 IBM CMRF8SF 130 nm CMOS Technology

The proposed designs are implemented using the IBM CMRF8SF 130 nm CMOS process design kit (PDK). This PDK is provided through MOSIS Integrated Circuit Fabrication Service and access to fabrication is provided through Canadian Microelectronics Corporation (CMC). Although this technology offers several metallization options, the option which is available for integrated circuit fabrication through MOSIS/CMC is:

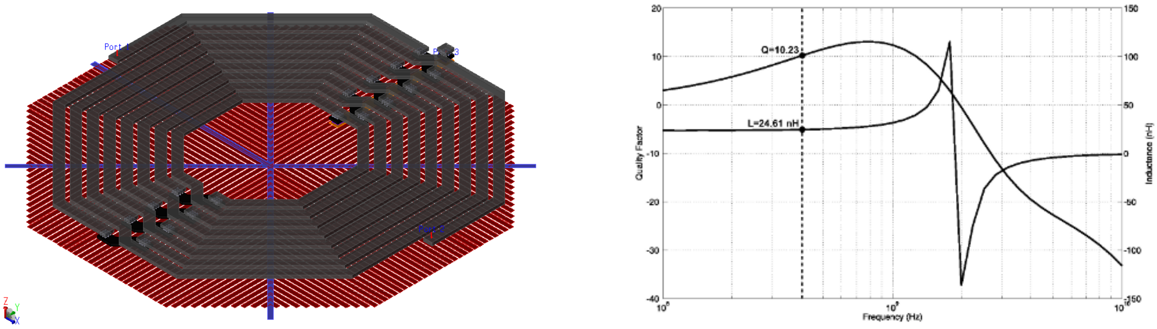
DM-topmetal: M1/V1/M2/V2/M3/VL/MQ/VQ/MG/FY/LY/FT/E1/F1/MA/DV

This is the so-called "3-thin, 2-thick, 3-RF" wirebond variant. The kit includes thin and thick oxide NMOS and PMOS transistors with nominal, high and low threshold voltages, and several inductor, resistor and capacitor topologies. Schematic entry, simulation, analysis, layout and verification are performed using the Custom Integrated Circuit Design suite of tools from Cadence Design Systems.

4.2 Current reuse quadrature VCO

The CR-QVCO was designed according to the methodology proposed in Section 3.2.1. To reduce the current drawn by the CR-QVCO, an inductor with high inductance and quality factor should be used. The inductors provided with the PDK did not provide high quality factors at low frequencies (> 1 GHz), which required the use of a custom spiral inductor. Cadence Virtuoso Passive Component Designer was used to synthesize a symmetrical octagonal inductor with high inductance and quality factor at the center frequency of the MICS band. The inductor was formed over an M1 groundplane to decrease substrate coupling and raise the quality factor [60]. The layout of the synthesized inductor and its simulated inductance and quality factor are shown in Fig. 4.1.

The inputs for the proposed low power VCO design methodology are summarized in Table 4.1.



(a) Three dimensional view.

(b) Simulated inductance and quality factor

Figure 4.1: Synthesized spiral inductor for current-reuse quadrature VCO.

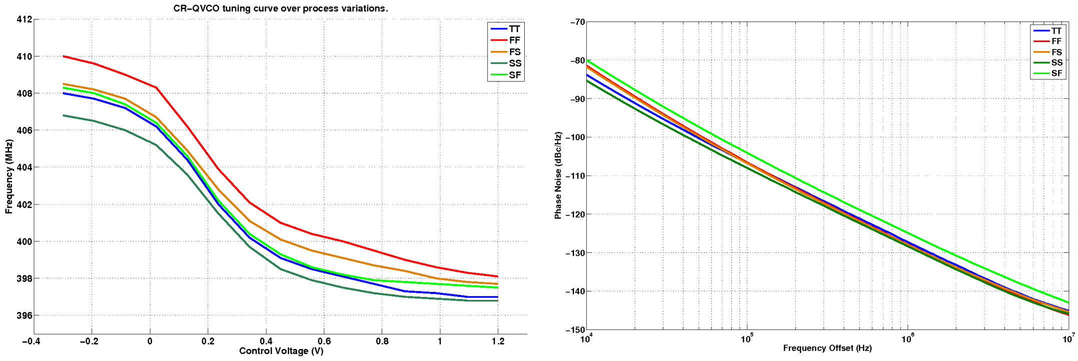
Parameter	Symbol	Value
Inductance	L	24.61 nH
Quality Factor	Q	10.23
Oscillation Amplitude	$\hat{V}_0$	100 mV
Resonant Frequency	ω_0	403.5 MHz
Tuning Range	TR	398 MHz to 410 MHz
Oscillator Startup Factor	β	3
Quadrature Coupling Factor	α	0.5

Table 4.1: Low power VCO design methodology input parameters.

As mentioned in Section 3.2, the CR-QVCO in Fig. 3.3c does not suffer from body effect. This is because the NMOS transistors can have their bulk and source terminals at the same potential, and all the PMOS transistors exist in their own n-wells which can be connected to the same potential as their respective sources. For both oscillator cores, the source terminals are not oscillator nodes so the threshold voltage stays constant during oscillation. The bias current was provided using the PMOS transistor. The upconversion of flicker noise generated by the current source transistor is a known contributor to the phase noise of the oscillator. To combat this effect, the bias transistor was sized to have long channel length and width as flicker noise is inversely proportional to the area of the active device. NMOS varactors were used as the frequency tuning element in the tank, and a fixed metal-insulator-metal (MIM) capacitor was used to set the tuning range around the frequency band of interest. Existing CR-QVCOs require the use of a frequency tuning circuit that accounted for the different DC voltages between the differential output nodes, which resulted in different voltage drops across the varactors in each tank. By designing the CR-QVCO such that the top tank is PMOS only and the bottom tank is NMOS only, a frequency tuning circuit was not necessary as the DC voltage of the quadrature outputs was almost the same (within a few mV). The small DC offset can be attributed to series resistance of the inductors. Omitting the frequency tuning circuit also improves the phase noise as the thermal noise generated by biasing resistors is not present.

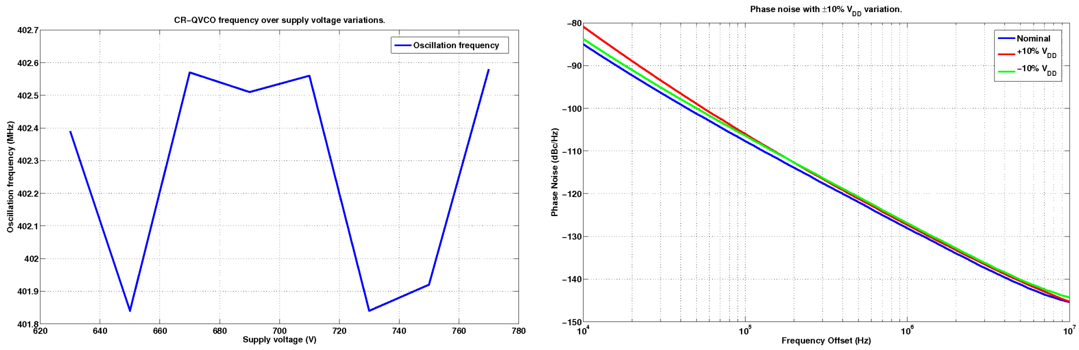
4.2.1 Simulation

As mentioned in Section 2.3, VCOs are subjected to variations due to process, supply voltage and temperature which cause the oscillation frequency to drift from the nominal value. In order to ensure the CR-QVCO can operate on across the MICS frequency band, simulations were performed to predict its oscillation frequency. The results of corner analysis and supply voltage sensitivity are shown in Fig. 4.2 and Fig. 4.3 respectively (biasing adjusted for each simulation to achieve same oscillation amplitude).



(a) Tuning range. (b) Phase noise.

Figure 4.2: CR-QVCO simulated over process variations.

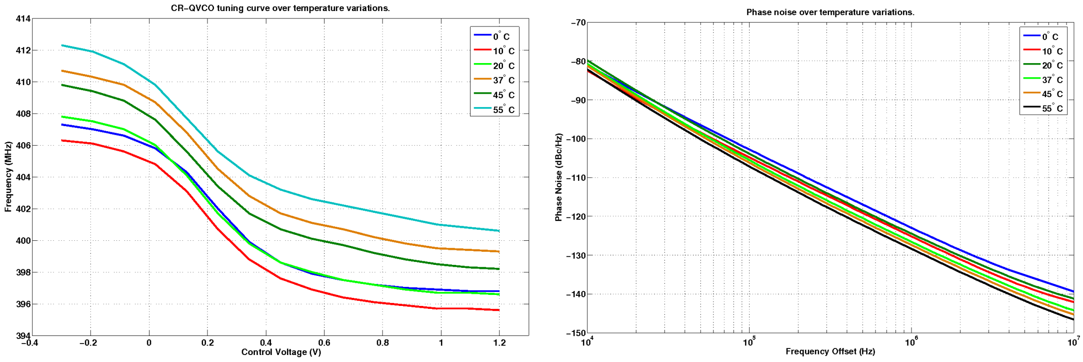


(a) Free-running frequency. (b) Phase noise.

Figure 4.3: CR-QVCO simulated over ± 10% supply voltage variations.

As per the requirements of the MICS frequency band, the IMD must be tested over temperature variations from 0° C to 55° C. Although the proposed work is not a complete IMD, the CR-QVCO performance at different temperatures in the required range was simulated to predict that the operating frequency and phase noise do not degrade significantly. The graphs in Fig. 4.4 show the tuning curves and phase noise plots for simulations at 0° C, 10° C, 20° C, 37° C, 45° C and 55° C.

The simulated CR-QVCO consumed 600 μW from a 0.7 V supply, and the phase noise was -127.2 dBc/Hz. The simulation results of the proposed CR-QVCO were compared with the existing designs



(a) Tuning range.

(b) Phase noise.

Figure 4.4: CR-QVCO simulated over temperature variations.

discussed in Section 1.2.3, and are summarized in Table 4.2.

Reference (Technology)	Tuning Range [MHz]	V_{DD} [V]	Power [mW]	Phase Noise [dBc/Hz]	Topology
This work (0.13 μm)	**398 to 410**	**0.7**	**0.42**	**-127.2 @ 1 MHz**	**Current-reuse quadrature oscillator**
[20] (0.13 μm)	401 to 406	1.2	0.72	-96 @ 1 MHz	LC tank VCO
[26] (TSMC 0.18 μm)	——	1.5	1.11	——	Differential ring VCO
[23] (TSMC 0.18 μm)	402	1.3	0.78	——	6-bit digitally controlled oscillator
[25] (0.18 μm)	398 to 408	0.7	0.21	-118 @ 1 MHz	7-bit digitally controlled oscillator
[24] (0.09 μm)	391 to 415	0.7	0.46	-108 @ 100 kHz	Digitally controlled oscillator
[61] (TSMC 0.18 μm)	——	1.5	——	——	Dual band LC tank VCO
[21] (TSMC 0.18 μm)	——	1.5	1.2	-98 @ 160 kHz	LC tank VCO
[28] (0.13 μm)	380 to 440	1.2	1.2	-107 @ 100 kHz	Injection-locked oscillator
[27] (0.18 μm)	440	1.5	0.231	-103 @ 100 kHz	Single-ended cross-coupled oscillator

Table 4.2: Comparision of existing MICS VCOs

As shown in the comparison results, the simulated CR-QVCO predicts improved power consumption and phase noise performance. Although both [25] and [27] have lower power consumption, it is important to note that these designs do not produce quadrature signals. If the VCOs in these works were used to implement a PQVCO to produce quadrature signals, the power consumption would at least double.

Furthermore the VCOs use off-chip inductors with high Q values. Although off-chip inductors are a valid method of reducing power consumption, their use violates one of the objectives of this work in this thesis which is to eliminate the need for off-chip components to lower the size and cost of the frequency synthesizer.

4.2.2 Measurement

The proposed CR-QVCO was fabricated using a 130 nm CMOS process from IBM through MOSIS Integrated Fabrication Service to provide validation of the design's simulation results. Testing of the integrated circuit was performed in the Ryerson Integrated Circuits and Systems laboratory using wafer probing on a Cascade Microtech IC probe station. Each of the four positioners on the probe station is capable of holding a different set of probes for applying and measuring signals to and from the device under test. The available probe configurations were

- 3 × Ground-Signal-Ground (GSG) operating at up to 40 GHz,
- 2 × Signal-Ground-Signal-Signal-Ground-Signal (SGSSGS) "wedge" operating up to 100 MHz,
- 2 × DC needle.

The wafer probe station and probe pad configuration diagrams are shown in Fig. 4.5 and Fig. 4.6 respectively. The square probe pads have side lengths of 100 μm and a pitch of 150 μm.

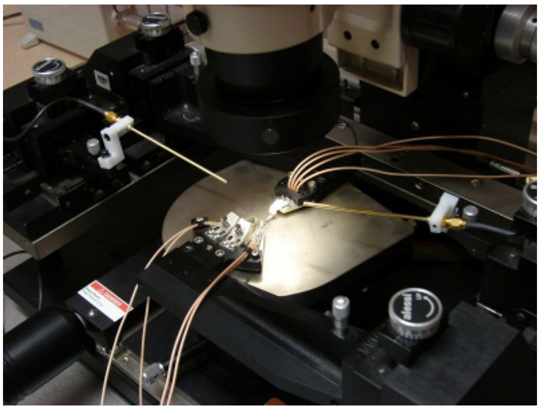
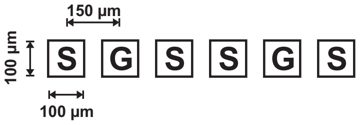
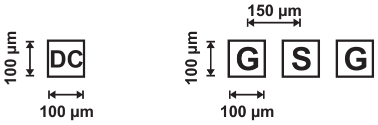


Figure 4.5: Wafer probe station



(a) SGSSGS.

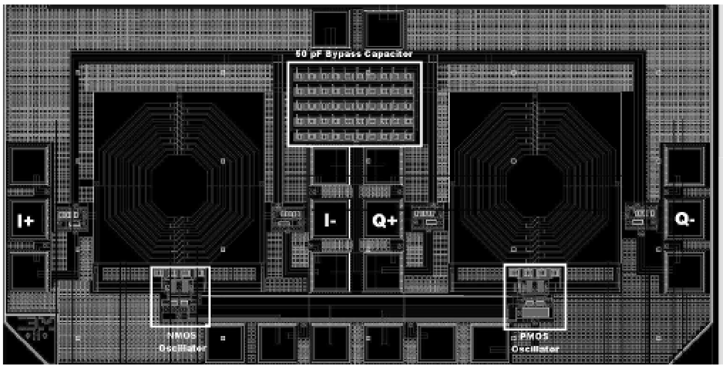


(b) DC needle.

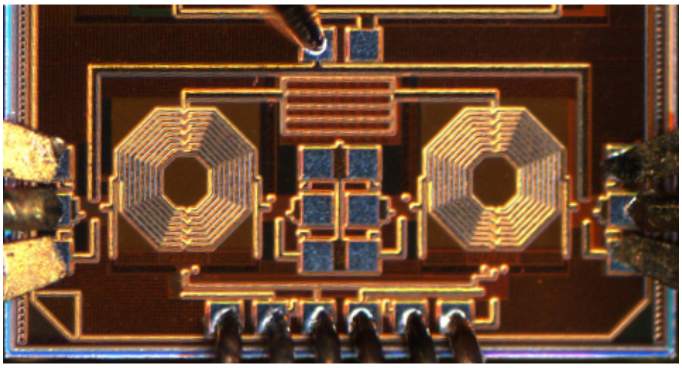
(c) GSG.

Figure 4.6: Probe configurations

The CR-QVCO had four RF outputs ($I+$, I-, $Q+$, Q-) and four DC bias voltages (core V_{DD}, V_{cont}, V_{bias}, and buffer V_{DD}). To implement the required input and output configuration four sets of probe pads for the GSG probes were used (only two could be probed at a time), a DC needle was used for the output buffer supply voltage and the SGSSGS wedge was used for the remaining DC signals. The layout and die photo of the CR-QVCO are shown in Fig. 4.7. The total silicon area occupied by the CR-QVCO including bond pads was 2 mm × 1 mm.



(a) CR-QVCO layout.



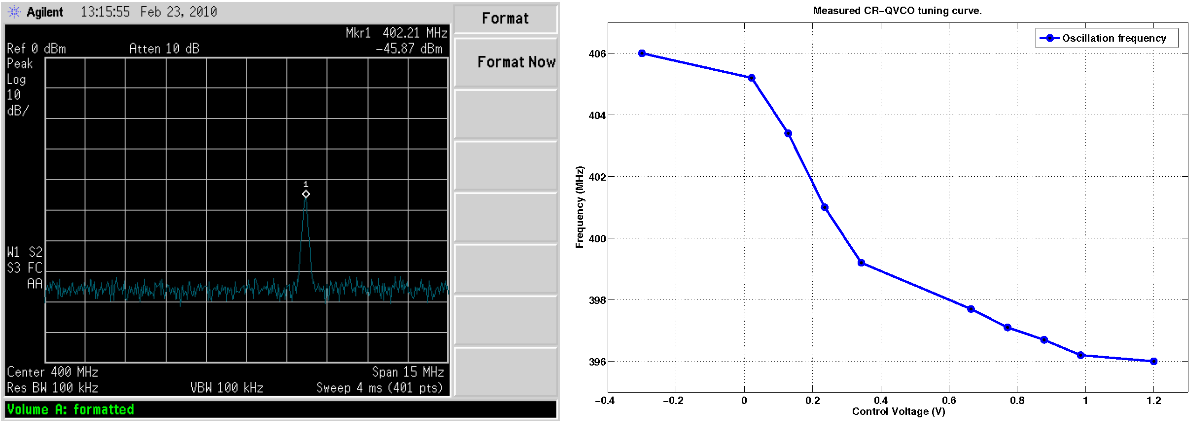
(b) CR-QVCO die photo.

Figure 4.7: Physical implementation of current-reuse quadrature VCO.

Measurement results for the CR-QVCO output spectrum and tuning range were obtained using an Agilent 4407B spectrum analyser, and power and bias voltages were provided using two high precision DC sources. The measured output spectrum and control voltage are shown in Fig. 4.8. The tuning curve was obtained by adjusting the control voltage across the desired range and observing the change in the output spectrum. Although the frequency range of the MICS is covered, the total tuning range is narrower than the desired range and is likely due to parasitics and other variations in the fabrication process such as increased capacitance density of the MIM capacitors or reduced tuning range of the varactors.

4.2.3 Fabrication challenges

Several challenges arose during the layout and fabrication process. Firstly, this was the first fabrication using the IBM 130 nm CMOS design kit since it became available to the Ryerson Electrical & Computer Engineering department. The support engineers from MOSIS were instrumental in overcoming many of the software-related issues to ensure the submitted designs satisfied all manufacturability checks. Additionally the spectrum analyser provided by Canadian Microelectronics Corporation was not capable of measuring phase noise it did not contain the additional firmware needed to perform these measure-



(a) Output spectrum.

(b) Tuning range.

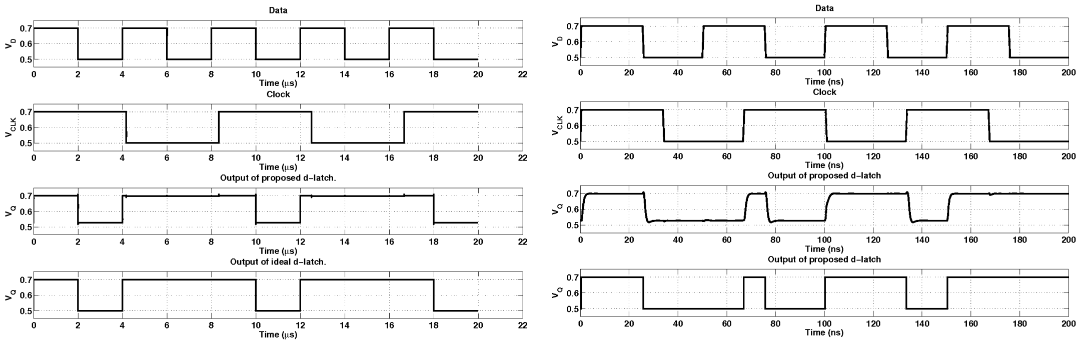
Figure 4.8: Measurement results of CR-QVCO.

ments. At the time measurements were performed, transient waveforms could not be obtained as an oscilloscope which operated in the UHF frequency range was not available. However the results serve as proof-of-concept for both the functionality of the proposed CR-QVCO and the proposed low-power VCO design methodology.

4.3 Subthreshold source-coupled logic programmable divider

4.3.1 Clear/preset D-latch simulation

The proposed D-latch was simulated along with an ideal D-latch written in Verilog-A to predict that the proposed design produces the correct output. The latch was simulated for two cases to predict that it can operate over the required frequency range. In Fig. 4.9a, the frequency of the data and clock inputs are 250 kHz and 120 kHz respectively, and in Fig. 4.9b they are 20 MHz and 15 MHz respectively.



(a) D=250 kHz, CLK=120 kHz.

(b) D=20 MHz, CLK=15 MHz.

Figure 4.9: Transient simulation of proposed D-latch and ideal D-latch.

To demonstrate the clear and preset functionality, the proposed D-latch was connected in a master-slave D-flip flop divide-by-two configuration and alternating PRE and CLR signals were applied every 20 ns. As shown in Fig. 4.10 the output signal (V$_{CLKOUT}$) is pulled high when V$_{PRE}$ is applied, and pulled low when V$_{CLR}$ is applied.

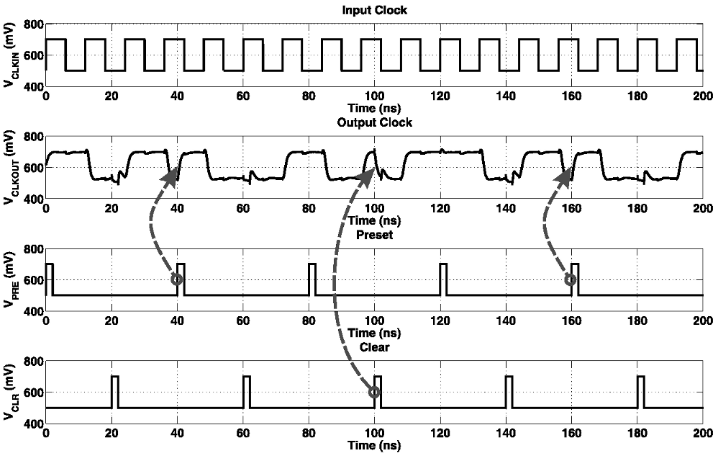


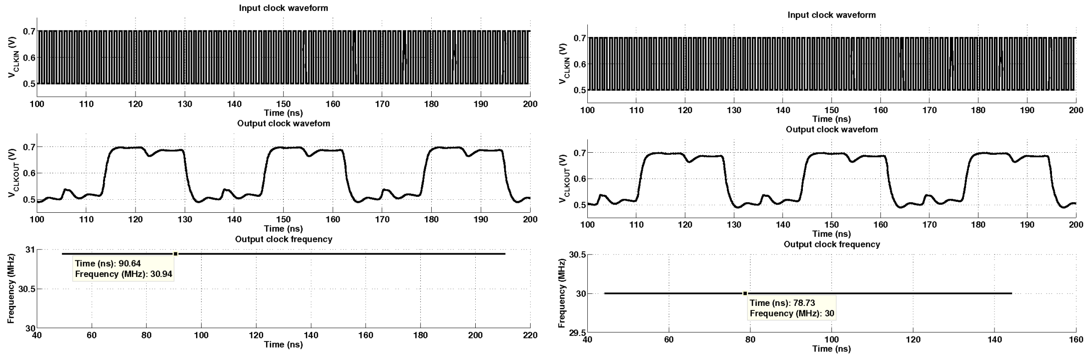
Figure 4.10: Simulation of D-flip flop with clear and preset.

4.3.2 Dual-modulus prescaler simulation

The divide-by-32/33 dual modulus prescaler in Fig. 3.10 was implemented using subthreshold source-coupled logic gates. The resistors in the SCL universal 2-input gate in Fig. 3.14 were replaced with the PMOS load device proposed in [58]. Since clear and preset functionality were not needed for the DMP the D-latch in Fig. 2.25c was used, and the load resistors were replaced with the PMOS load device. The divide-by-32 and divide-by-33 operations were simulated using a 990 MHz input signal, and the results are shown in Fig. 4.11. As shown in the figure the divider output frequency is 30.9375 MHz when dividing by 32, and 30 MHz when dividing by 33.

4.3.3 Programmable down counter simulation

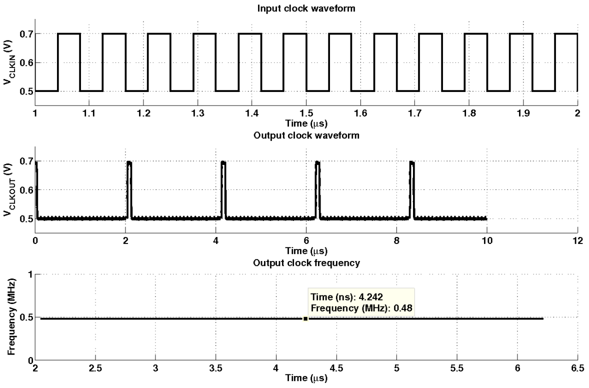
Transient simulations of the 6-bit and 7-bit programmable counters were performed to verify the desired behaviour of the down counters. The control word for the 6-bit counter was set to $S[5:0] = S_5S_4S_3S_2S_1S_0 = 011001$ and for the 7-bit counter it was $P[6:0] = P_6P_5P_4P_3P_2P_1P_0 = 1010011$. The simulation results in Fig. 4.12 show that the 6-bit down counter starts from 25 and counts down as expected. Likewise for the 7-bit counter, the results in Fig. 4.13 show that the count down starts from 83, as expected.



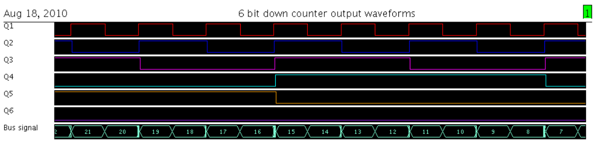
(a) Divide by 32.

(b) Divide by 33.

Figure 4.11: Transient simulation of dual-modulus prescaler.

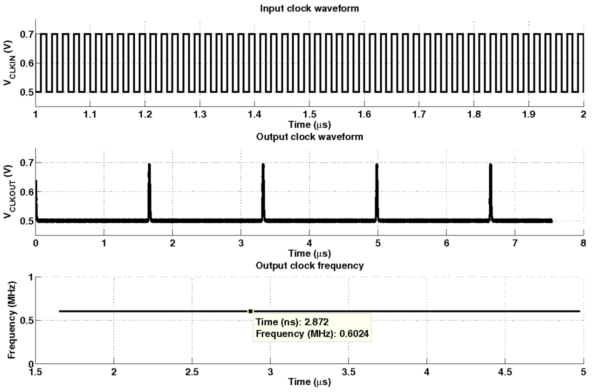


(a) Input and output waveforms.

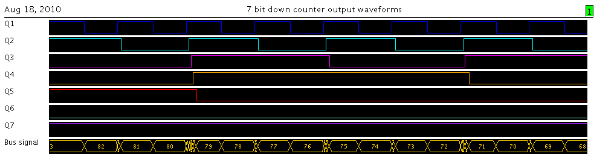


(b) Programmable counter outputs.

Figure 4.12: Transient simulation of 6-bit down counter.



(a) Input and output waveforms.



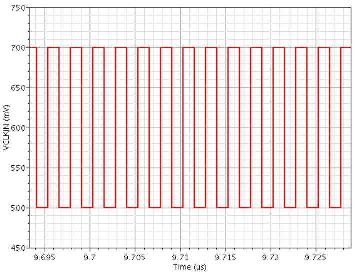
(b) Programmable counter outputs.

Figure 4.13: Transient simulation of 7-bit down counter.

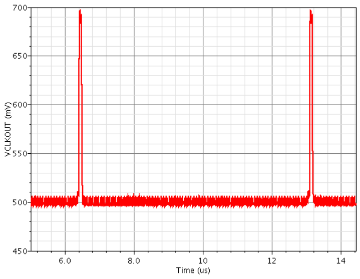
4.3.4 Programmable divider simulation

Once the major blocks of the proposed programmable divider were analysed in simulation, the divider itself was implemented and simulated to predict it could produce the correct output frequency which would server as the FB input for the phase/frequency detector. The frequency for each MICS channel was used as the input for the divider, and the control word of the Swallow Counter was adjusted so that the corresponding division ratio was used. Simulation results showed that for each channel, the corresponding division ratio produced an output frequency of 150 kHz. The simulation waveforms in Fig.

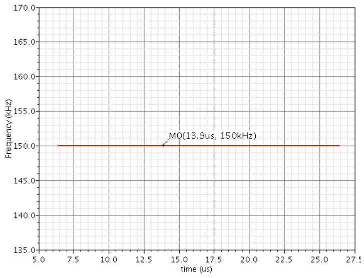
4.14 and Fig. 4.15 show the input waveform, output waveform and output frequency of the programmable divider when the input frequency is 402.15 MHz (channel 1) and 404.85 MHz (channel 10) respectively.



(a) Input voltage waveform

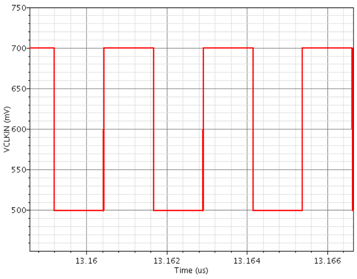


(b) Output voltage waveform

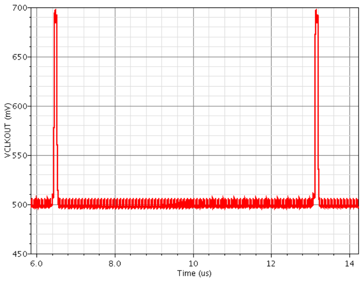


(c) Output frequency

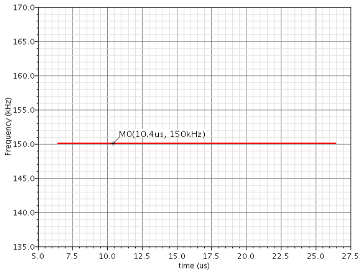
Figure 4.14: Programmable divider output when f$_{in}$ = 402.15 MHz



(a) Input voltage waveform



(b) Output voltage waveform



(c) Output frequency

Figure 4.15: Programmable divider output when f$_{in}$ = 404.85 MHz

A comparison between the proposed subthreshold programmable divider and recently published programmable dividers is given in Table 4.3. The figure of merit used to compare the results is the power consumption at the operating frequency, given in μW/MHz.

The programmable divider was submitted for fabrication as part of an MICS band frequency synthesizer. The layout of the programmable divider is shown in Fig. 4.16. Measurement results were not available at the time of writing as the design was still being fabricated. The total simulated power consumption of the proposed programmable divider was 200 μW. A summary of the simulated power consumption for each of the major blocks is given in Table 4.4.

Reference (Technology)	Frequency [MHz]	V_{DD} [V]	Power [mW]	FOM [μW/MHz]
This Work (0.13μm)	**200 to 1000**	**0.7**	**0.21**	**0.247**
[49] (0.18μm)	2400 and 5000	1.8	2.6	1.08
[50] (0.18μm)	5141 to 5860	1.5	4.8	0.934
[51] (0.18μm)	500 to 3500	1.8	3.01	0.86
[62] (0.18μm)	1600	1.2	0.475	0.296
[63] (0.18μm)	3000	1.5	3.58	1.19
[64] (0.18μm)	1700	1.5	3.2	1.88
[65] (0.18μm)	440	1.8	0.54	1.23

Table 4.3: Comparison of low power programmable dividers

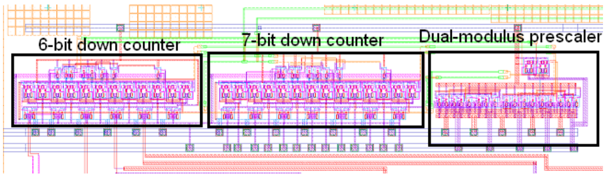


Figure 4.16: Programmable frequency divider layout.

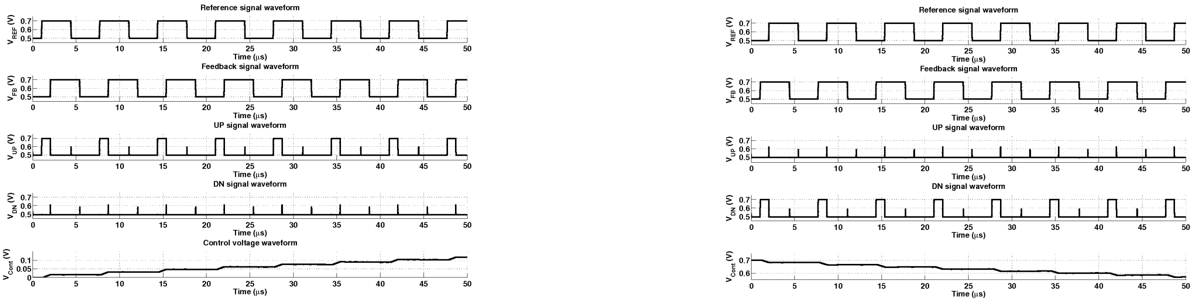
Block	Power consumption [μW]
Dual modulus prescaler	30
6-bit programmable counter	76
7-bit programmable counter	89
Pulse-swallow programmable divider	200

Table 4.4: Power consumption of programmable divider components.

4.4 Phase/frequency detector, charge pump and loop filter

The simulation results of the proposed subthreshold source-coupled logic phase/frequency detector, current-steering charge pump and loop filter are presented in Fig. 4.17. In Fig. 4.17a, the reference signal phase leads the feedback signal phase and the control voltage increases as expected. Similarly in

Fig. 4.17b, the reference signal phase lags the feedback signal phase and the control voltage decreases. It should be noted that an initial voltage was placed on the loop filter capacitor for the simulation in Fig. 4.17b because when the simulator starts the initial control voltage would be zero and the charge pump cannot remove any more charge from the capacitor.

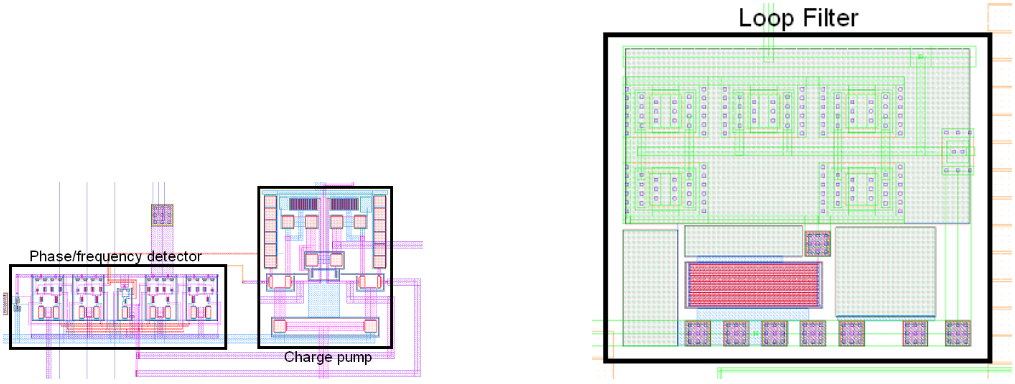


(a) Reference leads feedback.

(b) Reference lags feedback.

Figure 4.17: Transient simulation of PFD/CP/LF.

The PFD/CP/LF was submitted for fabrication as part of the previously mentioned MICS band frequency synthesizer, and measurement results are not currently available. The layout of the PFD/CP/LF is shown in Fig. 4.18. The CP was designed to have I_{UP}=I_{DN}=1 μA. The entire PFD/CP/LF consumes under 20 μW of power, most of which is consumed by the PFD.



(a) Phase/frequency detector and charge pump.

(b) Loop filter.

Figure 4.18: Phase/frequency detector, charge pump and loop filter layouts.

4.5 402 MHz to 405 MHz integer-n frequency synthesizer

4.5.1 Simulation

The frequency synthesizer in Fig. **??** was simulated to verify the locking behaviour. Simulation results predict that the synthesizer reaches the lock stated in 250 μs, and the total power consumption is 700 μW. The chip layout of the entire subthreshold integer-n frequency divider is shown in Fig. 4.20.

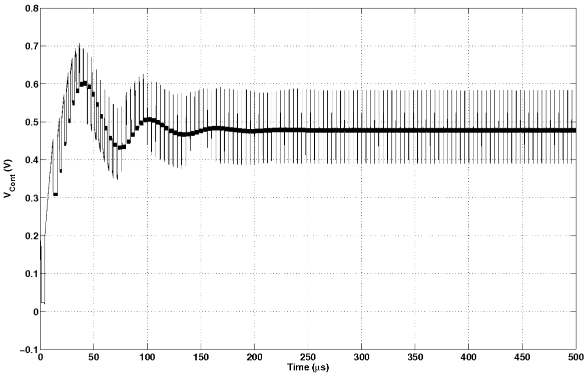


Figure 4.19: Frequency synthesizer control voltage.

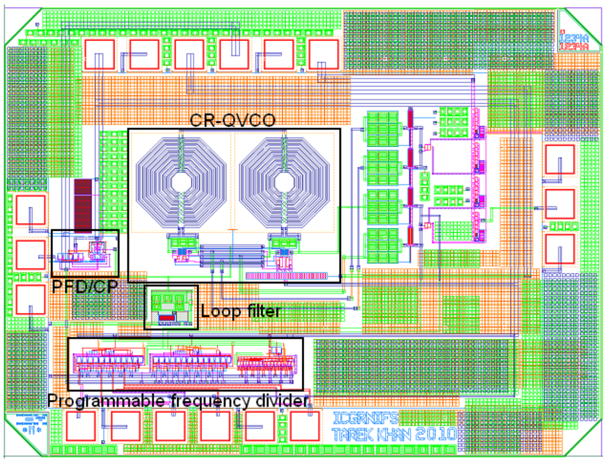


Figure 4.20: Frequency synthesizer layout.

4.5.2 Fabrication challenges

Many of the challenges faced in this fabrication were previously resolved during the first fabrication, but new issues came up at both the simulation and physical implementation levels. Phase-locked loop frequency synthesizers require a significant amount of time and computing power to simulate, with each simulation lasting anywhere from one to three days. It may take hours before it is apparent that the frequency synthesizer will not reach the locked state, at which point modifications must be made to different parts of the circuit to resolve the locking issue.

With regards to the physical implementation, the amount of silicon area was not sufficient to implement the proposed frequency synthesizer. With only 2 mm × 1.5 mm available for the entire synthesizer including bondpads, changes needed to be made to accommodate the entire design. It was mentioned in Section 3.3 that in order to tune to the correct channel, the VCO frequency could be doubled while using a 300 kHz reference frequency and adding a divide-by-2 circuit outside the loop. By adopting this approach, a higher resonant frequency was achieved by using smaller inductance and capacitance values, and consequently smaller inductors and capacitors, which occupy less silicon area.

Compromises had to be made for the inputs and outputs due to the available probe configurations. The frequency synthesizer required four inputs for the control word of the programmable divider, which uses up an entire SGSSGS wedge. The remaining DC wedge was used for DC biasing, however there were more bias voltages than there were signal pads available. The CR-QVCO, output buffer, charge pump, and all of the logic circuits that make up the phase/frequency detector and programmable divider needed bias voltages. This required designing all of the logic circuits to be biased by the same voltage. In practice bias voltages may be generated on chip using bandgap voltage references, but the design of such circuits was beyond the scope of this research and biasing voltages had to be applied off chip. Another way to allow for more inputs and outputs was to use ceramic flat packaging (CFP), however the cost for packaging makes prototyping prohibitively expensive.

4.6 Summary

In this chapter, the CR-QVCO, ST-SCL programmable divider and phase detector which were proposed in Chapter 3, and a modified current-steering charge pump were implemented using the IBM CMRF8SF 130 nm CMOS process. Simulation were performed using Cadence Spectre circuit simulator, which showed that both the CR-QVCO and ST-SCL programmable divider demonstrate improved performance compared to existing designs. Measurement results from a fabricated CR-QVCO designed according to the proposed low power VCO design methodology were in agreement with simulation results, however the tuning range was slightly narrower. A second fabrication for the subthreshold integer-n frequency synthesizer operating in the MICS frequency band has been submitted, pending measurement results. Simulations show that the frequency synthesizer reaches the locked state after 250 μs.

Chapter 5

Conclusion and future work

5.1 Thesis summary

In this research, novel circuits and design methodologies were presented for the design and implementation of an ultra-low power integer-n frequency synthesizer operating in the 402 MHz to 405 MHz Medical Implant Communication Service band of frequencies. Prior to introducing the proposed circuit designs, an overview of the theory and design metrics of oscillators and frequency synthesizers was given to provide readers with a sufficient understanding of these topics. The regulatory and design aspects of the Medical Implant Communication Service were discussed as well as a survey of previously published work in this field. The principal design concepts to achieve ultra-low power operation were introduced, namely current reuse, supply voltage scaling and subthreshold operation. Using these techniques, several novel circuits for use in the ultra-low power integer-n frequency synthesizer were proposed, namely:

- A current reuse quadrature voltage-controlled oscillator.
- A design methodology for the design of low power CMOS VCOs using the MOS EKV model and g_m/i_d methodology.
- A novel clear/preset SCL D-latch.
- A subthreshold SCL programmable divider and phase/frequency detector based on the proposed clear/preset SCL D-latch.

Using IBM CMRF8SF 130 nm CMOS technology, the proposed circuits were used to implement an integer-n frequency synthesizer. Simulations predict that the proposed CR-QVCO, ST-SCL programmable divider and ultra-low power frequency synthesizer achieve better performance than existing designs. The CR-QVCO was submitted for fabrication and measurement results of the fabricated prototype verified proposed design as well as the proposed low-power VCO design methodology.

5.2 Future work

As mentioned Chapter 4, the ultra-low power interger-n frequency synthesizer was being fabricated at the time of writing and measurement results were not available. Once the fabricated chip is returned, testing will be performed to verify the design. By continuing research in wireless IMDs, the work proposed in this thesis could be implemented in a complete implantable medical device operating in the Medical Implant Communication Service. As shown in Fig. 1.2, the wireless IMD consists of the power supply, processor, interface and transceiver. The work proposed in this thesis is only one block of the transceiver shown in Fig. 2.10. Each of the wireless IMDs shown in Fig. 1.1 have a unique set of requirements, particularly for the processor and interface blocks. Possible applications of such a device include passive devices for measuring physiologic signals such as ECG or EKV, or active devices insulin pumps for people with diabetes. Ideally the wireless IMD would receive power through RF wireless power harvesting rather than an implantable battery to eliminate the need for medical procedures to extend the lifetime of the IMD. Design of wireless IMDs requires specialized knowledge of many disciplines including, but not limited to, radio wave propagation, signal processing, circuit design, and biology. With a growing amount of research into the design and development of wireless IMDs, and designers continuously pushing the boundaries of existing technology, both patients and medical professionals will continue to benefit from wireless IMDs.

Appendix A

A brief introduction to the MOS EKV model and the g_m/i_d design methodology

A.1 MOS EKV model

The traditional square law MOS transistor model, which is a threshold based, source referenced model, is not suitable for hand analysis as it fails to caputure the short channel effects in modern deep submicron CMOS processes. The EKV MOS model is a bulk referenced, charge based transistor model suitable for the design and simulation of low voltage, low current, analog, digital and mixed-signal circuits in deep submicron CMOS technologies. The model describes MOSFET behaviour using a single continuous equation valid in all levels of inversion. The model develops continuous equations using nine physical parameters and the charge-sheet approximation, and allows for symmetrical analysis by referring all voltages to the bulk terminal. In this section, the important parameters and equations of the EKV model that are used in the design methodology proposed in Section 3.2.1 are presented. A full derivation of the model can be found in [66], [67].

The cross section of a MOS transistor is shown in Fig. A.1. All potentials are referenced to the bulk of the transistor. The basic assumption of the EKV model is that the entire mobile inversion charge, Q_i, is at the surface potential Φ_s. This is known as the charge sheet aprroximation, and is assumed to be valid since 95% of the inversion charge is at a potential within 3 to 6 times the thermal voltage, U_T below the surface potential. Electron flow occurs when the source and drain voltages are different, and is composed of both drift and diffusion components.

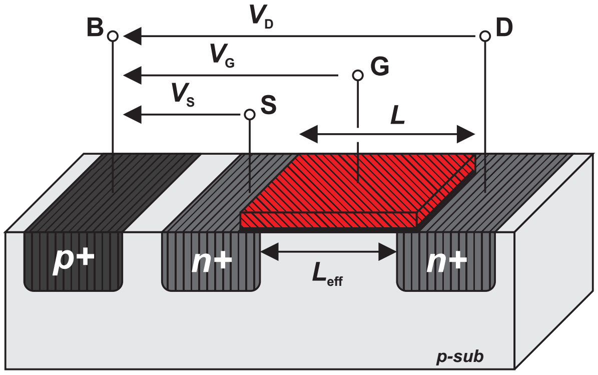


Figure A.1: Cross-section of MOS transistor.

$$I_D = \mu W \left(\underbrace{-Q_i \frac{d\Psi_s}{dx}}_{\text{drift}} + \underbrace{U_T \frac{dQ_i}{dx}}_{\text{diffusion}} \right). \tag{A.1}$$

Integrating the current along the channel and making substitutions for some parameters yields

$$I_D = \beta \int_{V_S}^{V_D} \frac{-Q_i}{C_{ox}} dV, \tag{A.2}$$

where β is the transfer parameter of the transistor depending on the transistor aspect ratio,

$$\beta \triangleq \mu C_{ox} \frac{W}{L}. \tag{A.3}$$

The drain current equation can be rewritten by normalizing the currents and voltages,

$$I_D = I_{spec} \int_{v_s}^{v_d} q_i dv, \tag{A.4}$$

where I_{spec} is the specific current of the transistor defined by

$$I_{spec} = 2n\beta U_T^2. \tag{A.5}$$

where n is the subthreshold slope parameter and U_T is the thermal voltage. Solving this equation provides an expression relating the drain current components with the bias voltages,

$$v_p - v_{s,d} = \sqrt{1 + 4i_{f,r}} + ln(\sqrt{1 + 4i_{f,r}} - 1) - (1 + \ln 2), \tag{A.6}$$

where i_f and i_r are the forward and reverse components of the drain current respectively,

$$i_f = \int_{v_s}^{\infty} q_i dv. \tag{A.7}$$

$$i_r = \int_{v_d}^{\infty} q_i dv. \tag{A.8}$$

$$i_d = i_f - i_r. \tag{A.9}$$

An alternate continuous expression relating the drain current components to the bias voltages is

$$i_{f,r} = \ln^2\left[1 + \exp\frac{v_p - v_{s,d}}{2}\right]. \tag{A.10}$$

$$v_p - v_{s,d} = 2\ln\left(\exp^{\sqrt{i_{f,r}}} - 1\right). \tag{A.11}$$

The drain current can be simplified when the device operates in strong and weak inversion,

$$I_D = \begin{cases} \beta(V_D - V_S)[V_G - V_{T0} - \frac{n}{2}(V_D + V_S)], & \text{linear} \\ \frac{\beta}{2n}(V_G - VT0 - nV_S)^2, & \text{forward saturation} \\ I_{spec}\exp\frac{V_G - V_{T0}}{nU_T}\left(\exp\frac{-V_S}{U_T} - \exp\frac{-V_D}{U_T}\right), & \text{weak inversion.} \end{cases} \tag{A.12}$$

The level of inversion of the device is characterized by the Inversion Coefficient (IC), which is a ratio of the device's drain current to its specific current,

$$IC = \frac{I_D}{I_{spec}}. \tag{A.13}$$

The values of IC corresponding to the levels of inversion are summarized below. It should be noted that moderate inversion is not a precisely defined region. This region exists when the approximations for strong or weak inversion are not sufficient to describe the drain current behaviour.

$$\begin{array}{rc} IC \ll 1 & \text{weak inversion.} \\ IC \cong 1 & \text{moderate inversion.} \\ IC \gg 1 & \text{strong inversion.} \end{array}$$

Changes in the drain current occur in response to changes in the gate voltage. The parameter relating these changes is called the transconductance, G_m, which is defined in each region of operation as follows,

$$G_m = \begin{cases} \beta(V_D - V_S) & \text{linear.} \\ \beta(V_P - V_S) & \text{forward saturation.} \\ \frac{I_D}{nU_T} & \text{weak inversion.} \end{cases} \tag{A.14}$$

An important figure of merit for a transistor is its transconductance to current ratio, also knows as the transconductance efficiency. This parameter is independent of any process parameters, and is a measure of how much transconductance can be obtained for a given current. A continuous expression over all inversion regions is given by

$$\frac{G_m}{I_D} = \frac{1 - \exp(-\sqrt{IC})}{nU_T\sqrt{IC}}. \tag{A.15}$$

The transconductance efficiency varies over the levels of inversion, and tends to the following asymptotes in strong and weak inversion,

$$\frac{G_m}{I_D} = \begin{cases} \frac{2}{nU_T(\sqrt{4i_f+1}+1)} & \text{strong inversion.} \\ \frac{1}{nU_T} & \text{weak inversion.} \end{cases} \tag{A.16}$$

Approximate equations for the intrinsic device capacitances are summarized in Table A.1, and are normalized according to Table A.6.

Capacitor	Strong inversion	Weak inversion
c_{GSi}	$\frac{2}{3}$	q_s
c_{GDi}	0	q_d
c_{GBi}	$\frac{n-1}{3n}$	$\frac{n-1}{n}$
c_{BSi}	$\frac{2}{3}$(n-1)	(n-1)q_s
c_{BDi}	0	(n-1)q_d

Table A.1: Approximation of normalized intrinsic capacitances in strong and weak inversion.

Together with the transconductance, the device capacitances determine the unity gain frequency of the device. This frequency, denoted f_T, is the point where the device current gain falls to unity, and is defined by the ratio of the transconductance to the gate capacitance. The transit frequency is given by

$$\omega_t = \frac{G_m}{C_G} = \frac{G_m}{C_{Gi} + C_{Go}}, \tag{A.17}$$

where

$$C_{Gi} \triangleq C_{OX}(c_{GSi} + c_{GDi} + c_{GBi}) \cong \frac{C_{ox}}{n}(n - 1 + c_{GSi} + c_{GDi}). \tag{A.18}$$

$$C_{Go} \triangleq C_{OX}(c_{GSo} + c_{GDo} + c_{GBo}) \cong 2WL_{ov}C_{ox}. \tag{A.19}$$

Parameter	Description
W	Channel width
L	Channel length
L_{eff}	Effective channel length
t_{ox}	Oxide thickness

Table A.2: Parameters describing MOSFET transistor geometry.

Parameter	Description
U_T	Thermodynamic voltage
V_{T0}	Threshold voltage
V_G	DC gate-to-bulk voltage
V_D	DC gate-to-drain voltage
V_S	DC gate-to-source voltage
V_P	Pinch-off voltage

Table A.3: Voltages.

Parameter	Description
I_D	Drain current
I_S	Source current
I_{spec}	Specific current

Table A.4: Currents.

Parameter	Description
G_m	Gate transconductance
G_{spec}	Specific conductance

Table A.5: Conductances.

Parameter	Description
C_{ox}	Oxide capacitance per unit area
C_{OX}	Total oxide capacitance
C_{GSi}	Intrinsic gate-to-source capacitance
C_{GDi}	Intrinsic gate-to-drain capacitance
C_{GBi}	Intrinsic gate-to-bulk capacitance
C_{GGi}	Total gate intrinsic capacitance
C_{GSo}	Gate-to-source overlap capacitance
C_{GDo}	Gate-to-drain overlap capacitance
C_{GBo}	Gate-to-bulk overlap capacitance
C_{GGi}	Total gate overlap capacitance
C_G	Total gate capacitance

Table A.6: Capacitances.

A.2 g_m/i_d design methodology

In modern deep submicron processes, the validity and predictive power of the square law, threshold based transistor model has diminished. A typical design process may include arbitrary selection of transistor bias currents and obtaining the transistor aspect ratio based on the square law model, the evaluating the remaining parameters such as transconductance, bandwdith, etc. An iterative process may take

Parameter	Description
ω_t	Unity gain frequency
n	Slope factor
β	Transconductance factor

Table A.7: Other parameters.

Parameter	Description	Definition
U_T	Thermodynamic voltage for normalizing voltages	$\frac{kT}{q}$
I_{spec}	Specific current for normalizing currents	$2n\beta U_T^2$
Q_{spec}	Specific charge density for normalizing charges	$-2nC_{ox}U_T$
C_{OX}	Total oxide capacitance for normalizing capacitances	WLC_{ox}
G_{spec}	Specific conductance for normalizing conductances	$\frac{I_{spec}}{U_T}$

Table A.8: Normalizing parameters

Parameter	Description
$v_x \triangleq V_X/U_T$	Normalized voltages
$i_x \triangleq I_X/I_{spec}$	Normalized currents
IC	Inversion coefficient
$q_x \triangleq Q_X/Q_{spec}$	Normalized charges
$c_XYi \triangleq C_XYi/C_{OX}$	Normalized intrinsic capacitance between terminals X and Y
$c_XYo \triangleq C_XYo/C_{OX}$	Normalized extrinsic capacitance between terminals X and Y
$c_J \triangleq C_J/C_{OX}$	Normalized total capacitance
$g_x \triangleq G_X/G_{spec}$	Normalized conductance

Table A.9: Normalizing parameters

place until an aspect ratio is obtained which satisfies the design specifications. Clearly a brute-force trial-and-error approach is not an ideal way to design circuits.

An alternate design approach was proposed in [48] where the authors exploit the transconductance efficiency versus inversion coefficient graph as a means of sizing low-power analog circuits. As identified by the authors, the methodology was developed using the transconductance efficiency for three reasons,

1. It is strongly related to the performance of analog circuits.
2. It gives an indication of the device operating region.
3. It provides a tool for calculating the transistor dimensions.

By providing insight into the transistor level of inversion, the methodology allows the designer to evaluate tradeoffs among gain, transistor size, bandwidth, matching, and any other parameters relevant to the design [68]. The transconductance efficiency is independent the device geometry as shown in (A.16), and the relationship between transconductance efficiency is a unique characteristic of all transistors of the same type in a given process. Recall that the inversion coefficient is defined as $\frac{I_D}{2n\mu C_{ox}\frac{W}{L}U_T^2}$. If the designer knows any two of the desired transconductance, drain current, or transconductance efficiency, the transistor aspect ratio can immediately be obtained from the corresponding inversion coefficient.

The graph of transconductance efficiency versus inversion coefficient is shown in Fig. A.2. As seen from the graph weak inversion offers the highest transconductance efficiency, and in strong inversion the transconductance efficiency decreases proportionately with $1/\sqrt{i_f}$.

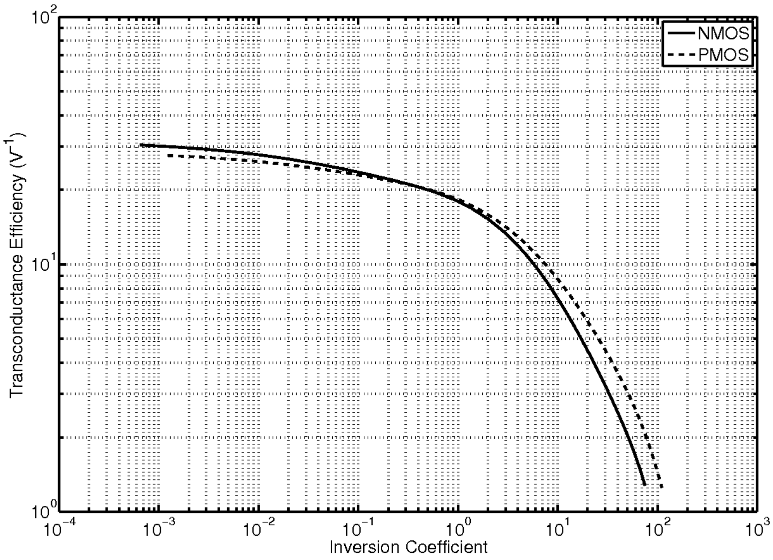


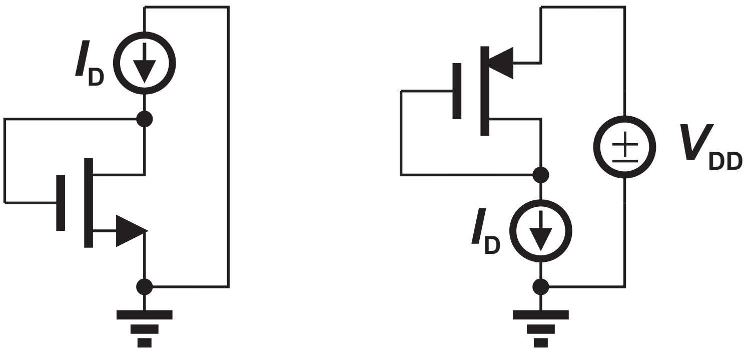
Figure A.2: Transconductance efficiency versus inversion coefficient.

The regions of inversion can be deduced using the relationships specified in (A.1). In weak inversion, the transconductance efficiency is maximized over a few decades of the inversion coefficient. However in order to achieve such small values of the inversion coefficient, the device must be significantly oversized. The penalty for designing in the weak inversion region is increased area and as a consequence, decreased unity gain frequency since the intrinsic capacitances are proportional to transistor width. The transconductance efficiency decreases as the device is pushed further into strong inversion. Although device aspect ratio decreases in this region, more current is required to achieve the same transconductance as when the device is operated in weak inversion. This results in greater power consumption. The moderate inversion region provides a compromise between device size and power consumption, however it is not well modeled which renders hand analysis difficult.

Although simulation is not the ideal way to characterize transistors from a given process, it provides quick, reasonably accurate information about the device's characteristics. Moreover, the EKV model is not yet popular with semiconductor foundries for use in their process design kits (PDKs). This means parameters such as n, I_{spec}, and IC are not calculated in the BSIM4 transistor models that are currently used in PDKs. In order to obtain the waveform of Fig. A.2, these parameters must be derived using the process data from the foundry. If subthreshold slope parameter, n, is not provided the subthreshold slope, S, can be used to derive it. The relationship between these two parameters is

$$\frac{1}{S} = \ln 10 \times n \times U_T. \tag{A.20}$$

The subthreshold slope may be provided by the foundry, or it can be obtained by simulating the I_{DS}-V_{GS} characteristics of a transistor, plotting the current on a logarithmic scale and observing how much change in V_{GS} produces a one decade change in I_{DS}. I_{spec} can be obtained by combining n with β, U_T and $\frac{W}{L}$, and IC is the ratio of the drain current to I_{spec}. One possible testbench for obtaining the waveform of Fig. A.2 is to use a diode-connected transistor and sweep its drain current over several decades (for example, from 10 pA to 10 mA) as shown in Fig. A.3a and Fig. A.3b. The transconductance efficiency is a parameter calculated by BSIM4 models (`gmoverid`), and it can be plotted against IC to obtain Fig. A.2.



(a) NMOS testbench.

(b) PMOS testbench.

Figure A.3: Simulation testbench for obtaining transconductance efficiency versus inversion coefficient graph.

Appendix B

Publications

B.1 Peer reviewed conference papers

T. Khan and K. Raahemifar, "An Ultra-Low Power 200 MHz-1 GHz Programmable Frequency Divider with Novel Clear/Preset D-Latch," 2010 IEEE Mid-West Symp. on Circuits Syst., accepted for publication in May 2010.

T. Khan and K. Raahemifar, "A low power current reused quadrature VCO for biomedical applications," Proc. IEEE Int'l Symp. on Circuits and Systems, pp.669–672, Taipei, May 2009.

B.2 Book chapters

T. Khan and K. Raahemifar, "Subthreshold frequency synthesis for medical implantable transceivers" in *Biomedical Engineering, Trends, Researches and Technologies*, Submitted Sept. 2010.

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