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10-GHz wide tuning-range linear voltage-controlled oscillator

Sameh Soliman
Ryerson University

10-GHz Wide Tuning-Range Linear Voltage-Controlled Oscillator

Sameh Soliman
B.Eng. Ryerson University
Toronto, Ontario

Department of Electrical and Computer Engineering

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School of Graduate Studies
RYERSON UNIVERSITY
Toronto, Ontario

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Abstract

The current high-growth nature of digital communications demands higher speed serial communication circuits. Present day technologies barely manage to keep up with this demand, and new techniques are required to ensure that serial communication can continue to expand and grow.

The goal of this work is to optimize the performance of an essential building block of serial communication circuits, namely, the phase-locked loop (PLL), so that it can cope with today's high-speed communication. Due to its popularity, the optimization has targeted the charge-pump-based implementation of the phase-locked loop.

This goal is achieved by researching, designing, and evaluating high speed serial communication circuits. Research has involved an in-depth study of the state of the art in high-speed, serial communication circuits; high-speed, controlled oscillators; and CMOS technology.

An LC, voltage-controlled oscillator (VCO) is designed in 0.18-micron, mixed-signal, 6-metal-2-poly, CMOS process. A *novel* tuning technique is employed to tune its output frequency. Simulation results shows that it provides quadrature and differential outputs; operates with 10-GHz center frequency, 600-MHz tuning range centered around its center frequency, and phase noise of -95 dBc/Hz at 1-MHz offset from the fundamental harmonic of its output; and draws 10 mA of DC current from a single, 1.8-V power supply. Also, It exhibits a good linearity throughout its tuning range. The new tuning technique increases the tuning range of the VCO to 6% of its center frequency compared to the 1-to-2% typical value.

As its locking performance depends on the characteristic of the employed VCO and to demonstrate the effect of optimizing the tuning range of the VCO, a charge-pump PLL is designed. Simulation results shows that the PLL acquisition range is 300 MHz compared to a maximum value of 100 MHz when a conventional LC VCO is employed. Also, as a measure of its tracking range, the maximum frequency slew rate of its input has improved by 40%.

Acknowledgment

I would like to express my thanks and gratitude to my supervisor, Professor K. Raahemifar. This work would not have been possible without his continuous support and encouragement. I also would like to thank Professor F. Yuan, my co-supervisor, who has provided me with advice, boost, and encouragement.

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IN this chapter, the motivation behind this thesis is presented, as well as a description of the intended application.

1.1 The Necessity of Controlled Oscillators

Most electronic signal processing systems require frequency or time reference signals. To use the full capacity of communication channels, e.g., wireless, wired and optical channels, transmitters modulate the baseband message signal into different parts of the spectrum to exploit better propagation characteristics or to frequency multiplex several messages, and the receivers demodulate them. These operations require accurate frequency reference signals. Digital circuits and mixed mode circuits, e.g., analog-to-digital (A-to-D) and digital-to-analog (D-to-A) converters, pace and synchronize their operations using a clock signal as a time reference signal.

At the lower end of the spectrum, the stable properties of quartz crystals can be used as resonators to build very accurate fixed frequency or time reference signals. On the other hand, at higher frequencies (greater than few hundred MHz) the quality of the crystal resonators degrades due to physical and material-properties limitations. Many communication applications require programmable carrier frequencies and a multitude of crystals would be prohibitive due to the cost and board space. Indirect frequency synthesis techniques based on a phase-locked loop (PLL) [1] are preferred to generate programmable carrier frequencies. As shown in Figure 1.1 a less accurate oscillator whose frequency can be controlled with a control signal is embedded in

a feedback loop and its output frequency is locked to an accurate low frequency reference.

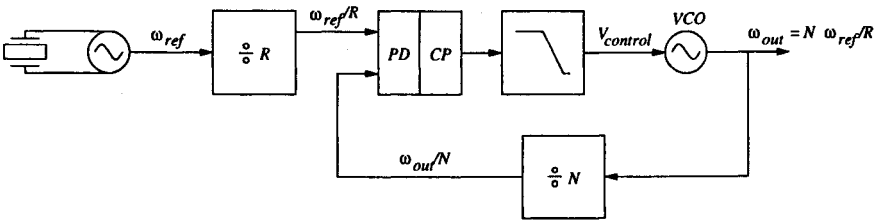


Figure 1.1: A phase-locked loop consists of a voltage-controlled oscillator (VCO), frequency divider, phase detector (PD), charge pump (CP) and lead-lag filter. The VCO output frequency ω_{out} is set to a multiple or sub-multiple of the reference frequency ω_{ref} depending on the divider ratios N and R.

In many data-communication applications, the data rate is accurately standardized. A local clock signal is derived from the incoming data signal with a clock recovery circuit to track small variations in the rate of the sender's clock and to align the phase of the local clock for optimal data recovery [2]. Another important application of controlled oscillators is the modulation or demodulation of frequency or angle modulated carriers. Open loop modulation and demodulation as well as closed loop schemes are very popular for portable wireless handsets [3].

Two main types of controlled oscillators exist: voltage-controlled oscillators (VCO's) with a voltage control signal and current-controlled oscillators (ICO's) with a current control signal. Although VCO's will be mainly referred to in the remainder of this thesis, most of the discussed concepts are equally applicable to ICO's.

1.2 The Necessity of GHz Oscillators

Several evolutions demand the realization of VCO's with center frequencies in the GHz to several GHz range.

In the wireless arena, the better propagation characteristics and the larger available bandwidth in the 1 to 2 GHz range have allowed the standardization and exploitation of digital cellular phone systems worldwide. The fabrication of the wireless phone terminals triggered a large demand for high performance, GHz VCO's. At

higher frequencies, around 2.5 GHz and 5 GHz, new wireless data applications, e.g., domestic short-range automation applications, cable replacement wireless links, etc., have spurred a strong interest and large markets.

With the constant shrinking of feature size in IC technologies and the increase of clock speeds we are very close to the widespread use of digital systems with clock speeds in the 1 GHz range. The distribution and synchronization of these GHz clocks is very challenging and will rely on on-chip PLL clock multipliers. Currently, these techniques are being used at clock frequencies of several hundred MHz [2]. These applications will drive the demand for GHz VCO's.

The same trend exists in data communications where widespread deployment of Gb/s data channels is fueled by the Internet growth and the convergence of data and voice communications. These systems rely on clock recovery architectures and also increase the demand for GHz VCO's.

1.3 The Necessity of Integrated Oscillators

High-volume, IC markets are governed by price, package, performance and power consumption. IC integration reduces production cost since it allows for mass volume production. Integration of the analog components reduces the number of analog pins, hence, it allows for cheaper packaging solutions. However, integration increases the complexity of the part, hence, testing cost can become a limiting factor or the number of I/O pins can become large which are counterproductive for packaging cost reduction. For low-cost and large-volume production post-fabrication trimming is to be avoided. By integrating the VCO on the IC, complex automatic calibration techniques become feasible since there is an abundance of cheap active devices along with sophisticated computing power.

Performance is a key factor. In applications governed by standards, meeting the performance specifications is necessary; without standards compliance, price, package or power consumption is irrelevant. The benefit of integration for performance is less obvious when the analog components are combined with digital ones. The choice of IC technology is driven by the requirements of the majority of the components

which are digital. Therefore, the use of special technology which enables better analog performance is unjustifiable due to its cost. Consequently, integration typically results in a somewhat lower performance for the VCO.

1.4 Intended Application: Fiber-Optic receiver

In recent years there has been a significant research effort in the area of high-speed electronics for communications. Higher speeds are required in order to take full advantage of the broadband capabilities of optical fibers. In particular integrated solutions are sought for practical systems to reduce cost and improve reliability. One of the target bit rates for integrated fiber optic receivers is 10 Gb/s, which is consistent with the SONET hierarchical specification [4]; practical transmission systems at these extremely high data rates will open the way to unexplored territory in networking. Each of these systems will require high-speed, low-cost interface electronics.

A simplified block diagram of a fiber-optic receiver is shown in Figure 1.2. It consists of a photo-detector at the front-end. The low-level signal from the photo-detector is then amplified by a low-noise pre-amplifier, followed by a main amplifier with automatic gain control. A clock extraction and data regeneration circuit recovers the timing information from the random data, and samples the data stream at the appropriate instant. Finally, a serial to parallel converter demultiplexes the re-timed serial data to a lower rate, where it can be processed by other circuitry.

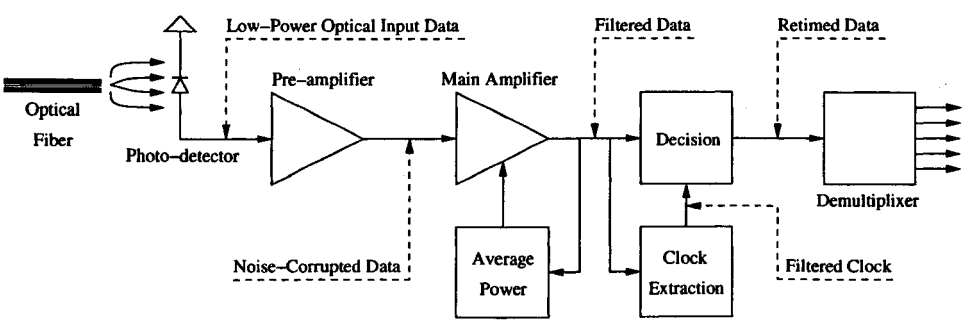


Figure 1.2: Simplified block diagram of a fiber-optic receiver.

The photo-detector is implemented as a $p - i - n$ diode or an avalanche photo-

detector (APD). When light pulses are focused onto it, it absorbs the light energy and generates electron-hole pairs. These electron-hole pairs are swept across the depletion region of the diode, resulting in a current that is proportional to the incident optical power.

To prevent additional processing from adding to the noise current, the low-level signal current from the photo-detector must be amplified. The pre-amplifier is used to convert this current into a voltage for subsequent processing. The sensitivity of the receiver and the signal-to-noise ratio are determined at this stage. Therefore, a very low-noise amplifier is required.

The main amplifier buffers the circuit from process variations and changes in signal strength, and it performs noise shaping. It must contain either a limiter, or an automatic-gain-control circuit to provide the proper signal level to the clock-extraction and data-recovery circuit, regardless of the output power of the pre-amplifier circuit.

Typically, clock-extraction and data-recovery circuit is implemented as a PLL circuit. This approach requires a VCO be controlled by a suitably filtered error signal. Although the PLL has the desirable property of being self adjusting, complications due to non-linear frequency acquisition and tracking make the circuit difficult to design.

1.5 Phase-Locked Loop: An Overview

The basic architecture of the PLL is shown in Figure 1.3. The phase detector (PD) senses the phase difference between the input to the PLL and the output of the voltage-controlled oscillator (VCO)[1]. The loop filter is a low-pass filter (LPF), hence, it averages the output of the PD. This average is used as a control input to the VCO. The VCO generates an output whose frequency is proportional to its control input.

[1] In addition to sensing the phase difference between its inputs, some implementations allow the PD to sense the frequency difference between its inputs as well. Such implementations are referred to as phase and frequency detectors (PFD's).

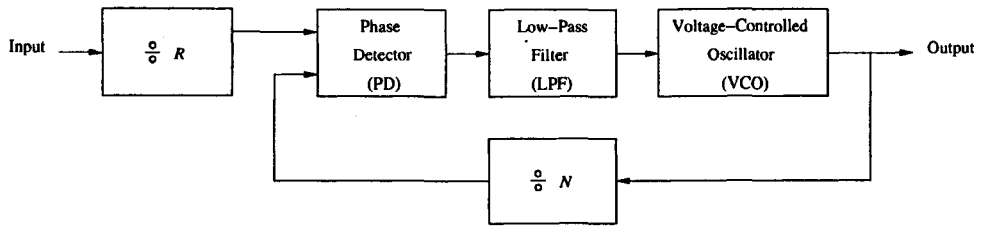


Figure 1.3: The basic architecture of the PLL.

The PLL is locked if the output of the PD has a nearly constant average so that the output frequency of the VCO remains constant.

The frequency divider divides the frequency of its input by a specific factor or a range of factors. The basic architecture of Figure 1.3 utilizes two frequency dividers. They allow the PLL to lock to inputs or generate outputs of different frequencies[2].

1.6 Thesis Contribution

Optimizing the locking performance of the PLL at the 10 Gb/s data-rate relaxes other design trade-offs in the target application. Typically, the locking performance of the PLL is measured by its acquisition and tracking ranges. In the high-frequency region, PLL is usually implemented as a charge-pump PLL. For this implementation, the acquisition and tracking ranges depend on the characteristic of the employed VCO. More specifically, increasing the tuning range of the VCO increases the acquisition and tracking ranges of the charge-pump PLL which allows it to tolerate larger frequency and phase drifts in its input.

In this thesis, a novel approach to tune the output frequency of the conventional LC-oscillator topology is proposed. This approach improves the tuning range of the VCO, hence the acquisition and tracking ranges of the charge-pump PLL where it is employed. The improved VCO utilizes an LC topology and exhibits the following features:

- DC-current consumption of 10 mA from a single, 1.8-V power supply.

[2]Depending on the application and the implementation of the frequency divider, the inputs or the outputs are usually separated by a fixed frequency step.

- Near-sinusoidal, in-phase and quadrature, differential outputs with a fundamental harmonic at 10 GHz.
- Tuning range of 600 MHz centered around the fundamental harmonic of its output.
- Phase noise of -95 dBc/Hz at 1-MHz offset from the fundamental harmonic of its output.
- Output noise of -130 dB at 1-MHz offset from the fundamental harmonic of its output.

The improvement in the locking performance of the charge-pump PLL is demonstrated via a system-level implementation and can be summarized as follows:

- The acquisition range of the charge-pump PLL increased to 300 MHz.
- As a measure of its tracking range, the maximum frequency slew rate of the input of the charge-pump PLL increased by 40%.

1.7 Thesis Outline

This thesis consists of five chapters. Chapter 2 reviews the key design issues and performance parameters of oscillators. Chapter ?? reviews the theory behind the PLL and the system-level design of its charge-pump implementation. Chapter 3 reviews the common topologies used to implement monolithic, high-frequency, CMOS VCO's and presents a strategy for designing them. Chapter 4 describes the transistor-level design of a 10-GHz, wide-tuning-range, linear, CMOS VCO. Also, it presents the simulation results of the designed circuits. As an application example, the VCO is used as a building block in a charge-pump PLL and the improvement in its locking performance is presented via simulation results. Chapter 5 concludes this thesis and presents several future-work plans.

Chapter 2

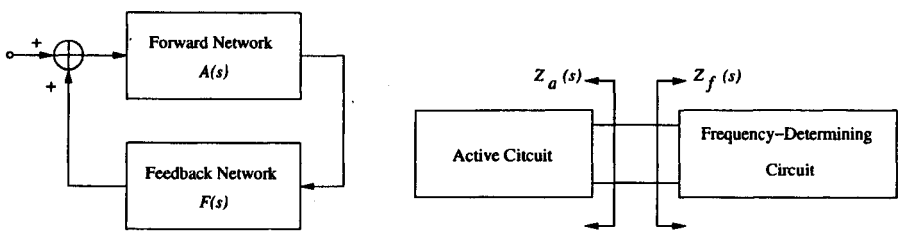
Oscillators: A Background

This chapter reviews the theory behind oscillators. Most of this theory is extensively covered in several text books [5, 6, 7, 8, 9].

2.1 Modeling of Oscillators

Depending on the configuration and characteristic of the oscillator, it can be analyzed using one of two models: the feedback model or the negative-resistance model.

If the oscillator's circuit can be decomposed into a multi-port, forward network and a multi-port, feedback network, the feedback model, shown in Figure 2.1(a), is used.



(a) (b)

Figure 2.1: (a) Feedback and (b) negative-resistance models of an oscillator.

The circuit in Figure 2.1(a) is characterized by its loop transfer function $L(s)$, defined as the product of its forward and feedback transfer functions $A(s)$ and $F(s)$

$$L(s) = A(s)\,F(s). \tag{2.1}$$

Its characteristic equation is given by

$$1 - L(s) = 0, \tag{2.2}$$

from which its poles can be found.

On the other hand, if the oscillator's circuit can be separated into a one-port, active circuit and a one-port, frequency determining circuit, the negative-resistance model, shown in Figure 2.1(b), is used. The function of the active circuit is to produce a small-signal, negative resistance around the operating point of the oscillator and to couple with the frequency-determining circuit in defining the oscillation frequency. Usually, the frequency-determining circuit is a linear, time-invariant circuit and is signal independent.

In Figure 2.1(b), the active and frequency-determining circuits are characterized by the impedance quantities $Z_a(s)$ and $Z_f(s)$, respectively. Alternatively, admittance quantities, $Y_a(s)$ and $Y_f(s)$, may be used for the same purpose. The characteristic equation of the circuit is given by [10]

$$Z_a(s) + Z_f(s) = 0 \quad \text{or} \quad Y_a(s) + Y_f(s) = 0. \tag{2.3}$$

2.2 Start-up Conditions

As a basic requirement for producing a self-sustained, near-sinusoidal oscillation, an oscillator must have a pair of complex-conjugate poles in the right-half of the s plane (RHP)

$$p_{1,2} = \alpha \pm j\beta. \tag{2.4}$$

When excited by an arbitrary input, the RHP poles in Equation (2.4) give rise to a sinusoidal signal with an exponentially growing envelope

$$x(t) = K \exp(\alpha t) \cos(\beta t), \tag{2.5}$$

where K is set by initial conditions. The growth of this signal is eventually limited by nonlinearities in the oscillator.

For a feedback-oscillator circuit, the fulfillment of the following condition indicates that the circuit is unstable around its operating point.

$$\angle L(\omega_z) = 0 \quad \text{and} \quad |L(\omega_z)| \geq 1, \tag{2.6}$$

where ω_z denotes the frequency at which the total phase shift through the forward and feedback networks is zero (or an integer multiple of $\pm 360°$).

For a negative-resistance-oscillator circuit, with the active and frequency-determining circuits characterized by the impedances $Z_a = R_a + jX_a$ and $Z_f = R_f + jX_f$, respectively, the fulfillment of the following condition [10] indicates that the circuit is unstable about its operating point

$$R_a(\omega_x) + R_f(\omega_x) < 0 \quad \text{and} \quad X_a(\omega_x) + X_f(\omega_x) = 0, \tag{2.7}$$

where ω_x denotes the frequency at which the total reactive component $X_a + X_f$ is zero. The underlying assumption in condition (2.7) is that the current entering the active circuit in the steady state is near-sinusoidal.

Alternatively, if the voltage across the active circuit is near-sinusoidal in the steady state, the active and frequency-determining circuits should be modeled in terms of parallel admittances $Y_a = G_a + jB_a$ and $Y_f = G_f + jB_f$ where G and B denote the conductance and susceptance, respectively. The dual start-up condition in this case is

$$G_a(\omega_x) + G_f(\omega_x) < 0 \quad \text{and} \quad B_a(\omega_x) + B_f(\omega_x) = 0. \tag{2.8}$$

It is important to note that conditions (2.6), (2.7), and (2.8) have the following limitations

- Fulfilling any of these conditions does not always imply the existence of RHP poles [2].
- For controlled-oscillator circuits, varying the control signal of the circuit changes the location of its poles[1]. Because these conditions cannot predict the instability

[1]This statement is not rigorous since linear concepts, e.g., poles and zeros, are difficult to apply to nonlinear circuits.

of the circuit throughout its tuning range, the existence of RHP poles throughout this range should be confirmed [2]. As a rule of thumb, these conditions are valid if they hold only at one frequency.

In the high-frequency region, the parasitic elements in the oscillator's circuit can give rise to a multi-oscillation phenomenon, in which more than one oscillation exist simultaneously in steady state. Due to the multiple oscillations, the net steady-state signal is severely distorted, as shown in Figure 2.2, and can cause unwanted spurious effects in many applications.

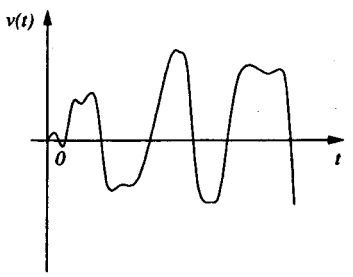


Figure 2.2: Multi-oscillation phenomenon.

The fulfillment of any of the conditions (2.6), (2.7), or (2.8) at more than one frequency indicates a potential multi-oscillation phenomenon and the existence of more than one pair of complex-conjugate poles in the RHP is a strong evidence on the existence of this phenomenon.

2.3 Performance Parameters

Phase noise and frequency tuning range are the key performance parameters of high-frequency oscillators [11]. While the study of frequency tuning range of different oscillator circuits is deferred to Chapter 4, this section provides a detailed analysis of phase noise in oscillators.

2.3.1 Phase Noise

Distinguished by the path into which the noise is injected, phase noise is generated primarily through two mechanisms. A controlled-oscillator circuit includes both a

signal path and a control path. The phase noise observed at its output depends on how much the circuit rejects (or amplifies) noise in these paths. Shown in Figure. 2.3, the injected noise, $x(t)$, in these paths gives rise to distinctly different effects [12, 13].

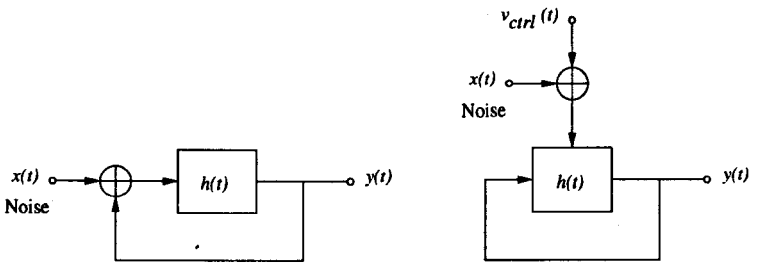


Figure 2.3: Noise in (a) signal path and (b) control path of a controlled-oscillator circuit.

Noise in Signal Path

In the steady state, representing the open-loop circuit in Figure 2.3(a) by a linear transfer function $H_{ol}(j\,\omega)$, its closed-loop transfer function is given by

$$H_{cl}(j\,\omega) = \frac{Y}{X}(j\,\omega) = \frac{H_{ol}(j\,\omega)}{1 - H_{ol}(j\,\omega)}. \tag{2.9}$$

The circuit oscillates at the frequency $\omega = \omega_c$ if Equation (2.9) approaches infinity at this frequency. In the vicinity of this frequency, e.g., $\omega = \omega_c + \Delta\omega$, $H_{ol}(j\,\omega)$ can be approximated by the first two terms of its Taylor expansion

$$H_{ol}(j\,\omega) \approx H_{ol}(j\,\omega_c) + \Delta\omega\,\frac{dH_{ol}(j\,\omega)}{d\omega}. \tag{2.10}$$

Since $H_{ol}(j\,\omega_c) = 1$ and for most practical cases $|\Delta\omega\, dH_{ol}(j\,\omega)/d\omega| \ll 1$, Equation (2.9) can be reduced to

$$H_{cl}(j\,\omega) \approx \frac{-1}{\Delta\omega\,\frac{dH_{ol}(j\,\omega)}{d\omega}}, \tag{2.11}$$

which implies, as shown in Figure 2.4, that the noise spectrum is shaped by

$$|H_{cl}(j\,\omega)|^2 = \frac{1}{(\Delta\omega)^2\left|\frac{dH_{ol}(j\,\omega)}{d\omega}\right|^2}. \tag{2.12}$$

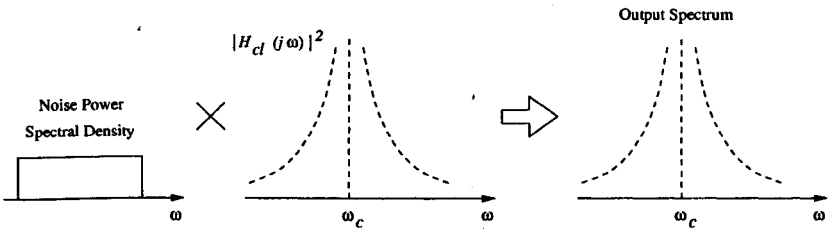


Figure 2.4: Noise shaping in oscillator circuits.

Expressing $H_{ol}(j\,\omega)$ in the polar form $H_{ol}(j\,\omega) = A(\omega)\exp[j\,\Phi(\omega)]$ and substituting for $dH_{ol}(j\,\omega)/d\omega$, Equation (2.12) can be written as

$$|H_{cl}(j\,\omega)|^2 = \frac{1}{(\Delta\omega)^2\left[\left(\frac{dA(\omega)}{d\omega}\right)^2 + \left(\frac{d\Phi(\omega)}{d\omega}\right)^2\right]}. \tag{2.13}$$

Let the open-loop Q^2 of the circuit, which is a measure of the opposition of the closed-loop circuit to variations in frequency, be defined by

$$Q = \frac{\omega_c}{2}\sqrt{\left(\frac{dA(\omega)}{d\omega}\right)^2 + \left(\frac{d\Phi(\omega)}{d\omega}\right)^2}. \tag{2.14}$$

Combining Equations (2.13) and (2.14) results in "Leeson's equation [12]"

$$|H_{cl}(j\,\omega)|^2 = \frac{1}{4Q^2}\left(\frac{\omega_c}{\Delta\omega}\right)^2, \tag{2.15}$$

which reveals the dependence of the output noise on the Q of the circuit, the center (or carrier) frequency, and the offset from the center frequency.

It is interesting to note that ring oscillators exhibit $dA(\omega)/d\omega$ and $d\Phi(\omega)/d\omega$ of the same order at resonance. Thus, phase-noise power of a ring oscillator is typically half the value given by Equation (2.15). On the other hand, LC oscillators exhibit $dA(\omega)/d\omega = 0$ at resonance and Equation (2.14) reduces to the conventional definition of $Q = \omega_c\,(d\Phi(\omega)/d\omega)/2$.

Moreover, phase-noise power compared to carrier power depends on two other parameters: the noise generated by the devices in the circuit, that is, the magnitude of $X(j\omega)$ and the amplitude of the oscillation. Deducing that phase-noise power

[2]The definition of Q of a resonant circuit is reviewed in Appendix A.

of ring oscillators is lower than that of LC ones based on the comparison of their respective Q's may not be correct.

The above linear analysis does not consider the fact that oscillators usually experience amplitude limiting, i.e., nonlinearity, hence folding the noise components. To incorporate the effect of nonlinearity, two types of phase noise need to be identified.

First type is due to noise components that are directly added to the output of the oscillator as shown in Figure 2.4 and formulated by Equation (2.12). It is referred to as additive noise and is predicted by the above linear analysis. The accuracy of this prediction depends on the number of stages in the oscillator and the portion of the oscillation period during which they operate linearly.

To identify the second type, consider a single-stage oscillator whose characteristic is expressed as $v_{out}(t) = \alpha_1 v_{in}(t) + \alpha_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t)$. For an input consisting of the carrier and a noise component, e.g., $v_{in}(t) = A_c \cos(\omega_c t) + A_n \cos(\omega_n t)$, the output of the oscillator exhibits the following important terms

$$v_{out1}(t) \propto \alpha_2 A_c A_n \cos[(\omega_c \pm \omega_n) t], \tag{2.16}$$

$$v_{out2}(t) \propto \alpha_3 A_c A_n^2 \cos[(\omega_c - 2\omega_n) t], \text{ and} \tag{2.17}$$

$$v_{out3}(t) \propto \alpha_3 A_c^2 A_n \cos[(2\omega_c - \omega_n) t]. \tag{2.18}$$

If ω_n is small, $v_{out1}(t)$ appears in band. In a fully differential configuration $\alpha_2 = 0$, hence $v_{out1}(t) = 0$. Also, $v_{out2}(t)$ is negligible because $A_n \ll A_c$, leaving $v_{out3}(t)$ as the only significant cross-product.

This simplified one-stage analysis predicts the frequency of the output components, but not their magnitudes. When noise is injected into the oscillator, the magnitude of the observed response at ω_n and $2\omega_c - \omega_n$ depends on the noise shaping properties of the oscillator.

Since nonlinearity folds all the noise components below ω_c to the region above it and vice versa, these components are referred to as high-frequency multiplicative noise and are important if they fall close to ω_c. This phenomenon is illustrated in Figure 2.5.

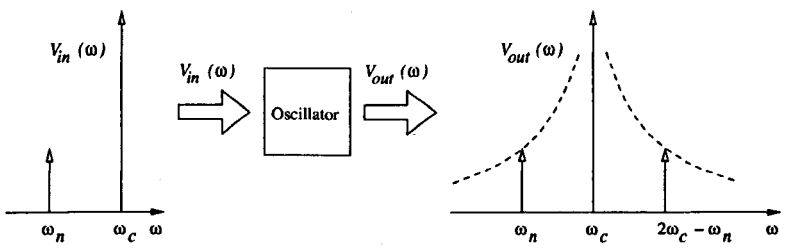


Figure 2.5: High-frequency multiplicative noise.

It should be noted that for highly nonlinear oscillators, the Taylor expansion in Equation (2.10) may need to include higher order terms.

Noise in Control Path

While noise injected into the signal path mixes with the carrier, noise injected into the control path affects the frequency of the oscillator's output by changing its physical properties. Viewed as analog frequency modulation (FM), this effect translates low-frequency noise components in the control path to the region around the carrier as illustrated in Figure 2.6. These components are referred to as low-frequency multiplicative noise.

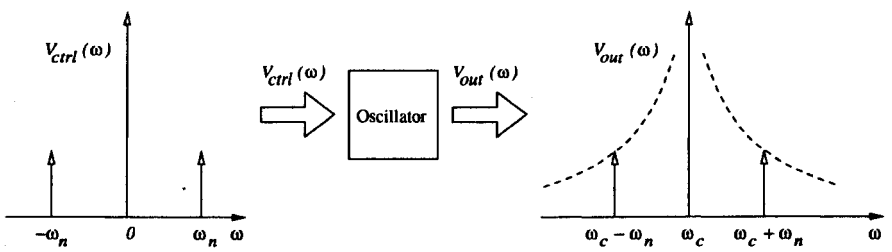


Figure 2.6: Low-frequency multiplicative noise.

Representing the noise per unit bandwidth as a sinusoid $A_n \cos(\omega_n t)$ with the same average power and using the narrowband FM approximation[3]

$$v_{out}(t) \approx A_c \cos(\omega_c t) + \frac{A_c A_n K_{osc}}{2\omega_n} [\cos(\omega_c + \omega_n) t - \cos(\omega_c - \omega_n) t], \qquad (2.19)$$

where K_{osc} is the controlled-oscillator gain. Thus, the noise power at $\omega_c \pm \omega_n$ relative to the carrier power is equal to $(A_n K_{osc}/2\omega_n)^2$. In practice, K_{osc} is proportional

[3]The narrowband FM approximation is reviewed in Appendix B.

to the carrier frequency because for a given control-signal range, the tuning range must be constant percentage of the center frequency to compensate for process and temperature variations. The effect of this type of noise becomes more prominent as ω_n decreases, making $1/f$ noise in the control path particularly detrimental.

It should be noted that low-frequency multiplicative noise arises from any source that can vary the frequency of the output of the oscillator.

The analyses in this section predict that the phase noise decreases indefinitely as the offset of ω_n from ω_c increases. In reality, it reaches a relatively flat floor since the oscillator does not shape the injected noise at high frequency offsets from the carrier.

2.3.2 Noise-Power Trade-off

Oscillators, as other analog circuits, exhibit a trade-off between noise and power dissipation. As shown in Figure 2.7, if the outputs of N identical oscillators are added in phase, the carrier power is multiplied by N^2, whereas the noise power by N (assuming noise sources of different oscillators are uncorrelated).

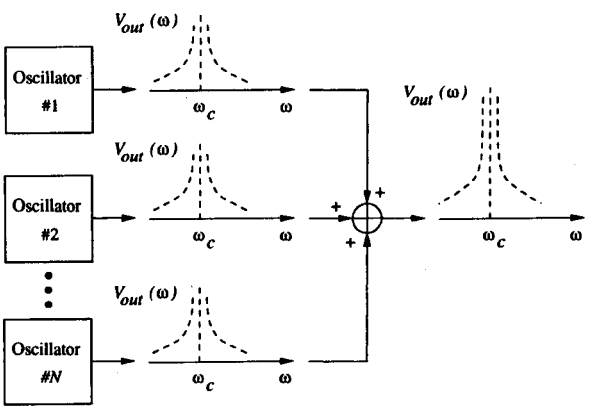


Figure 2.7: Adding the outputs of N identical oscillators.

Thus, the phase noise power relative to the carrier power decreases by a factor N at the cost of a proportional increase in power dissipation.

2.3.3 Effect of Frequency scaling on Phase Noise

Since frequency and phase are related by a linear operator, dividing frequency by a factor N is identical to dividing phase by the same factor. For a nominally periodic sinusoid, $x(t) = A_c \cos[\omega_c t + \phi_n(t)]$, where $\phi_n(t)$ represents the phase noise, a frequency divider divides its total phase by N

$$x_{1/N}(t) = A_c \cos\left[\frac{\omega_c}{N}(t) + \frac{\omega_n}{N}(t)\right], \tag{2.20}$$

where the phase noise contributed by the frequency divider is neglected.

This indicates that the magnitude of the phase noise at a given frequency offset from the carrier is divided by N. Thus, from narrowband FM approximation, the phase noise power is divided by N^2.

Similar reasoning shows that a frequency multiplier multiplies the magnitude of the phase noise by the same factor.

2.3.4 Oscillator Pulling and Pushing

The analysis of phase noise in Section 2.3.1 assumed that the magnitude of the noise injected into the signal path is much less than that of the carrier, thereby arriving at a noise shaping function for oscillators.

Close to the carrier, as the magnitude of the injected noise component becomes comparable to that of the carrier, the carrier frequency may shift toward the noise frequency and eventually locks to this frequency [14, 15]. Referred to as "injection pulling" this effect is shown in Figure 2.8.

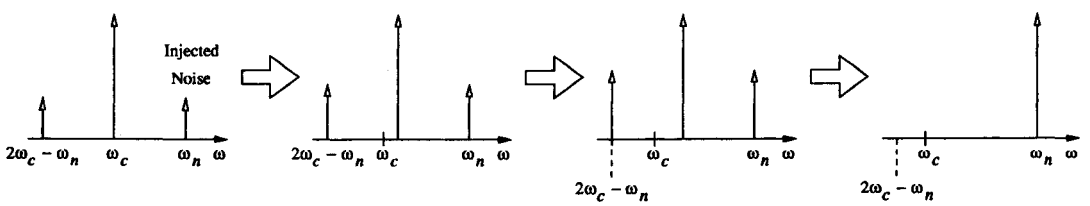


Figure 2.8: Injection pulling of oscillators.

In general, oscillators exhibit a poor supply rejection. If the supply voltage varies, so do the frequency of oscillation. Referred to as "supply pushing" this effect is more

prominent in battery-powered (portable) applications. Owing to the finite output impedance of the battery, the supply voltage may vary by several hundred millivolts.

Chapter 3

Topologies of Monolithic, High-Frequency, CMOS VCO's

In general, oscillators can be categorized into two main categories: linear and non-linear oscillators [26].

Linear oscillators generate a near-sinusoidal output. Their basic topology uses a frequency-tuning network, e.g., an LC tank, in a positive-feedback loop. Although they use a non-linear mechanism to limit the amplitude of the output, they are referred to as linear oscillators to distinguish them from the non-linear ones which can generate a near-sinusoidal output by waveform-shaping techniques.

Oscillators which generate square, triangular, etc. outputs are referred to as non-linear oscillators. Two popular topologies in this category are relaxation and ring oscillators. While the former is a popular topology for bipolar oscillators, the latter is a popular one for CMOS oscillators.

In this chapter, the two main topologies of monolithic CMOS VCO's, namely, LC and ring topologies, are discussed. Also, following an overview of performance metrics of a controlled oscillator, the topologies of high-frequency VCO's are presented.

3.1 LC Oscillator

If a simple LC tank is stimulated by a current impulse, energy reciprocates between its capacitor and inductor in cycles. Every cycle, a portion of the reciprocating energy is lost in the form of heat in its resistor, hence, it responds with decaying oscillations

as shown in Figure 3.1(a). If a resistor with a negative resistance $-R_p$ is placed in parallel with the tank, its net resistance approaches infinity and it responds to the current impulse with indefinite oscillations as shown in Figure 3.1(b).

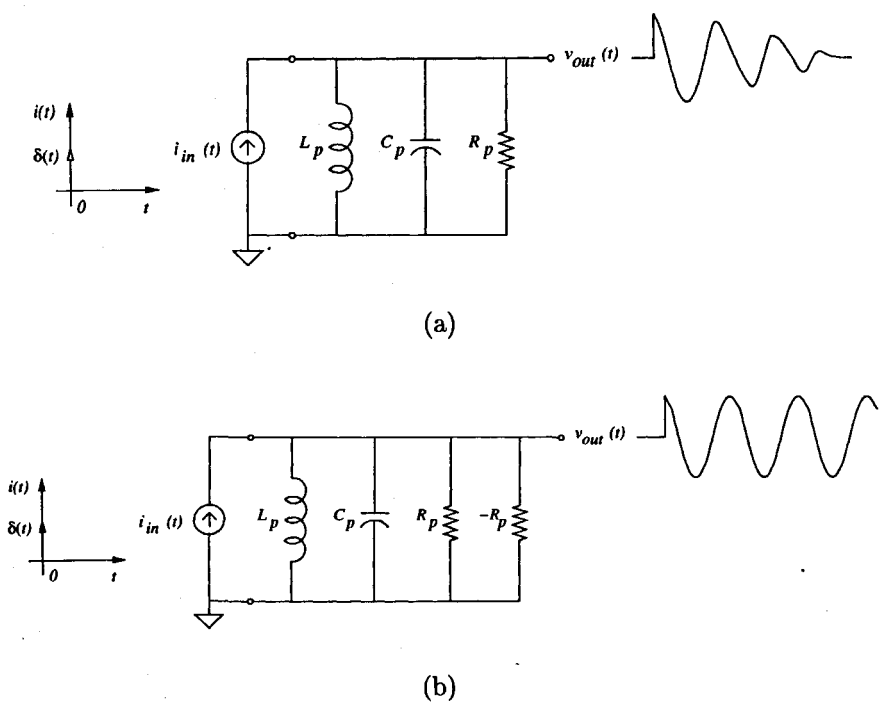


Figure 3.1: The response of (a) an LC tank and (b) the tank in (a) in parallel with a resistor with a negative resistance $-R_p$ to a current impulse.

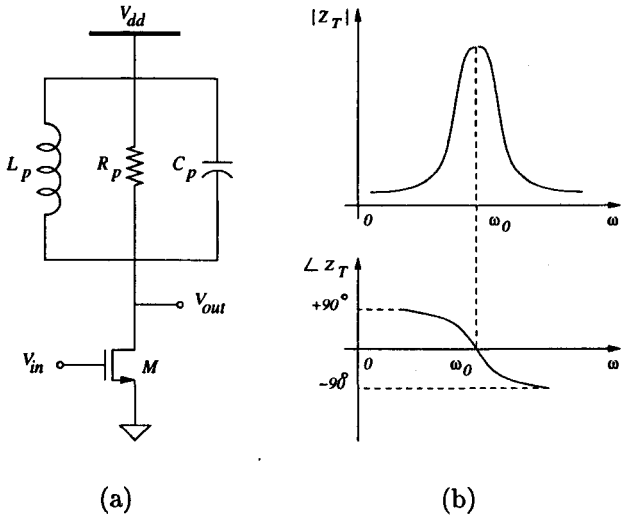
Thus, if a one-port network exhibiting negative resistance[1] is placed in parallel with an LC tank, the combination may oscillate.

A simple *tuned* stage is shown in Figure 3.2 loaded with an LC tank. Also, the magnitude and phase of the impedance of the LC tank, Z_T, as a function of frequency are shown in the same figure.

At resonance, $|Z_T| = R_p$ and $\angle Z_T = 0$. Thus, the magnitude of the gain of the tuned stage is $R_p\, g_m$, where g_m is the small-signal transconductance of the transistor M, and its phase is $\pm 180°$[2].

[1]The negative resistance is an incremental quantity. It indicates that if the applied voltage increases, the current drawn by the network decreases.

[2]This phase is due to the low-frequency phase inversion of the common-source transistor M.



(a) (b)

Figure 3.2: (a) A simple tuned stage; (b) the magnitude and phase of the impedance of an LC tank as a function of frequency.

An LC oscillator is a cascade of N tuned stages. For the cascade to start oscillating, $(R_p\, g_m)^N \geq 1$ and its total phase shift[3] has to be zero. Thus, N has to be an even number.

A differential tuned stage can be implemented by connecting two simple tuned stages as shown in Figure 3.3(a). Since the frequency of oscillation equals $1/\sqrt{L_p\, C_p}$ [16], the output frequency of the LC oscillator can be tuned by varying the inductance or the capacitance of its tank. In monolithic implementations, it is difficult to vary the value of an inductor, hence, the common practice is to vary the value of the capacitance of the tank.

A reverse-biased p/n junction can serve as a voltage-dependent capacitor (also, referred to as a varactor). It can be used to vary the net capacitance of the LC tank as shown in Figure 3.3(b).

[3]Total phase shift = frequency-independent or DC phase shift + frequency-dependent or AC phase shift.

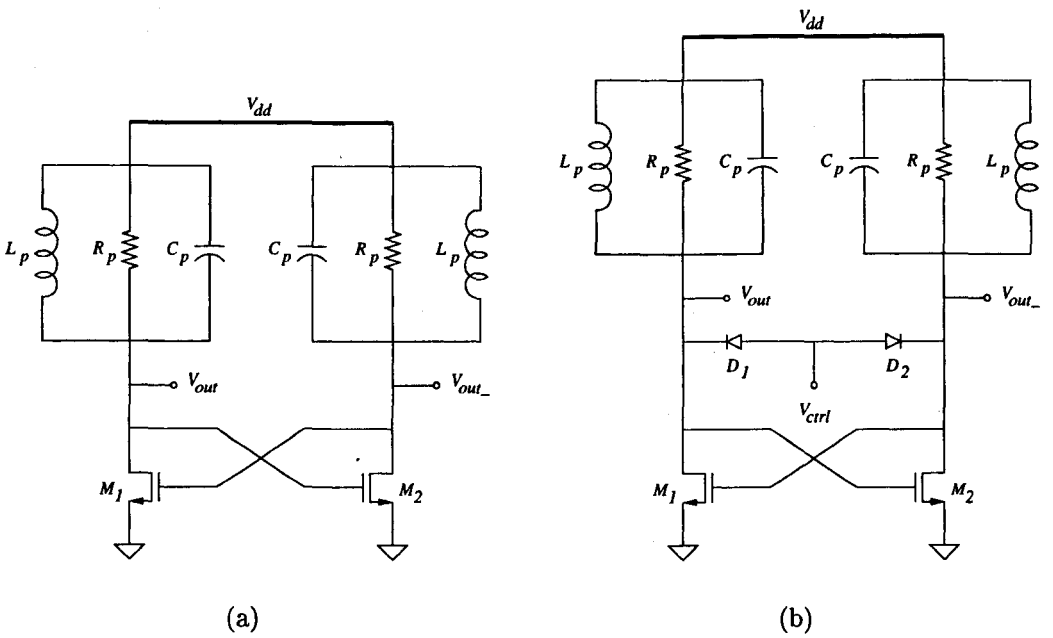


Figure 3.3: (a) A differential tuned stage; (b) using varactor diodes to tune its output frequency.

3.2 Ring Oscillator

As shown in Figure 3.4, a ring oscillator is a cascade of N *gain* stages with a total DC phase shift of 180° in a feedback loop. If the total phase shift around the loop is zero at its unity loop gain, it starts to oscillate with a period of $2\,N\,t_d$ where t_d is the delay of each gain stage with a fanout of one under these conditions.

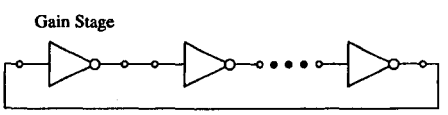


Figure 3.4: The topology of a ring oscillator.

The common implementation of the gain stage is as a simple or differential-pair-based inverter. To achieve a DC phase shift of 180°, N must be an odd number when the simple inverter is used. On the other hand, N can be an even number when the differential-pair-based inverter is used. The required DC phase shift is achieved by swapping the outputs of one of the gain stages.

Tuning the output frequency is achieved by varying the effective number of gain stages or the delay of each one. Delay interpolation, shown in Figure 3.5(a), is the common implementation of the first technique where a fast signal path and a slow one are used in parallel. The total delay is varied by varying the gains, hence the delays, of both paths in complementary fashion.

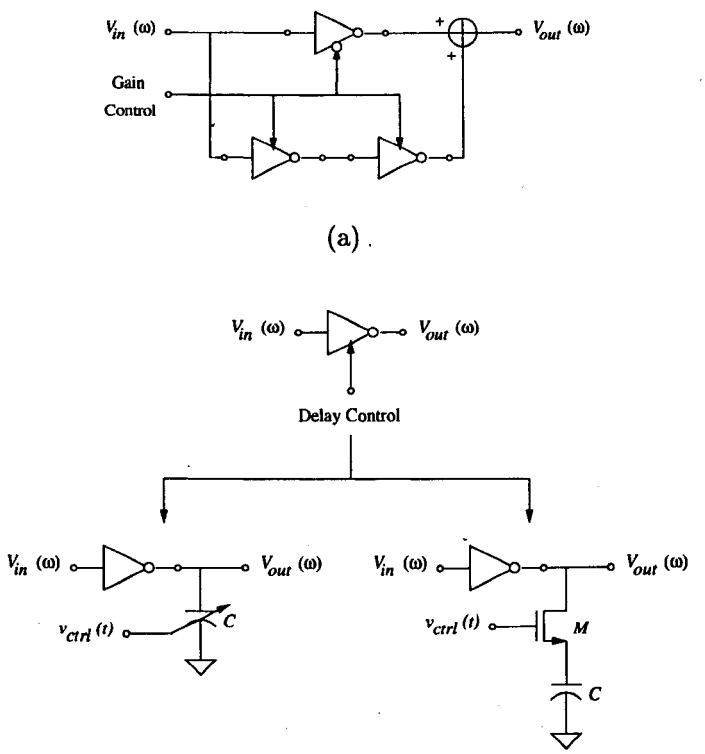


Figure 3.5: Tuning the output frequency of a ring oscillator via (a) delay interpolation (b) delay control.

Varying the delay of each gain stage can be achieved by varying its load capacitance or resistance. As shown in Figure 3.5(b), varying the load capacitance can be achieved by using a voltage-controlled capacitor or a fixed capacitor in series with a voltage-controlled resistor. The main limitations of this approach are the variation of the oscillator's gain and its output swing throughout its tuning range[4]. Moreover, it

[4]These effects can be minimized by varying some other parameters of the gain stage [17].

is susceptible to common-mode noise as it uses single-ended control path.

Although varying the load resistance has the same limitations as changing its capacitance, this approach provides a large, relatively uniform frequency variation and lends itself to differential control [2].

3.3 Performance Metrics

The performance of a controlled oscillator is described by the following metrics:

- *Center frequency*: it is the midpoint of the oscillator's tuning range and is mainly application dependent.

- *Tuning range*: it is the range between the minimum and maximum frequency of the oscillator's output and is mainly dictated by the application and the variation of the oscillator's center frequency with process and temperature. LC oscillators exhibit narrow tuning range compared to ring oscillators.

- *Tuning sensitivity*: it is the change in the output frequency of the oscillator per unit change in its control voltage and is frequently referred to as the oscillator's gain. To tune its output signal frequency, one of the oscillator's circuit parameters must be varied. Depending on the effect of this parameter, the oscillator's gain, hence its output swing, may vary considerably throughout its tuning range. LC oscillators exhibit less gain and output swing variation compared to ring oscillators.

- *Characteristic linearity*: if the oscillator is intended for frequency-synthesis applications, it may exhibit non-linear characteristic (its tuning range can be divided into regions throughout each of which the characteristic is linear). On the other hand, if the oscillator is intended for modulation or demodulation applications, its characteristic must exhibit high linearity. For such applications and as a measure of the linearity of the oscillator's characteristic, the variation of its gain throughout its tuning range must be minimum.

- *Spectral purity*: depending on the application, it can be specified in time domain as jitter or in frequency domain as phase noise.

- *Noise rejection*: when an oscillator share the same substrate with some digital circuit, its sensitivity to substrate and supply noise becomes prominent. Although it is not always possible, the common practice to minimize this sensitivity is to employ differential signal and control paths.

3.4 Topologies of High-Frequency VCO's

Among the different performance metrics of a controlled oscillator, phase noise and tuning range are the most challenging to achieve specifically when operation in the high-frequency region is targeted. During the past few years several techniques to overcome these challenges were reported [18, 19, 20]. In this section a review of these techniques is presented.

The review targeted the recent publications on high-frequency VCO's. a representing examples of the available techniques to implement a 10-GHz VCO is presented.

In [18], a 10-GHz, LC VCO was designed in a 0.25-micron, CMOS process. It achieved a tuning range of 700 MHz. The measured phase noise at 400 kHz offset from the carrier was -101 dBc/Hz at the low end and -87 dB c/Hz at the high end of its tuning range. The circuit drew 2.4 mA from a 2-V power supply. PMOS varactors were used to achieve wide tuning range of the output frequency.

In [19], a 10-GHz, LC VCO was designed in a 0.13-micron, standard-digital, CMOS process. It achieved a tuning range of 3.7 GHz and a phase noise of -99 dBc/Hz at 1-MHz offset from the carrier. The core circuit consumed a 3.6 mW of DC power from a 1.2-V power supply.

Wide tuning range was achieved by using MOS, accumulation-mode varactors instead of the conventional reverse-biased p/n junction and MOS, depletion/inversion varactors.

In [20], a 10-GHz, CMOS, distributed, voltage-controlled oscillator (DVCO) was designed in a 0.35-micron, BiCMOS process. It achieved a tuning range of 1.2 GHz

and a phase noise of -103 dBc/Hz at 600 kHz offset from the carrier. The circuit drew 14 mA of DC current from a 2.5-V power supply.

Two techniques to tune the output frequency were described. The first was to introduce explicit varactors on the transmission lines. This technique suffered from a severe reduction in the output frequency due to the constant, zero-bias capacitance added to the transmission lines. Thus, canceling the advantage obtained by using a distributed topology, namely, higher operation frequency. Also, the quality factor of the varactors significantly degraded at higher frequencies which made them more undesirable.

The second technique was to change the round-trip time-delay by changing the length of the transmission lines. Although the physical length cannot be changed, the effective length can be varied. This effect was achieved via current steering technique.

From these examples, a strategy for designing VCO's in the 10-GHz frequency region (and above) can be obtained.

- In the 10-GHz frequency region and above, two main topologies were used to implement a VCO: LC-tank-based topology [18, 19] and distributed topology [20].
- Different processes were used to design the VCO, e.g., 0.25-micron, CMOS process in [18]; 0.13-micron, standard-digital, CMOS process in [19]; and 0.35-micron, BiCMOS process in [20].
- Supply voltage ranged from 1.2 V to 2.5 V.
- Phase noise was improved compared to the target-application requirements [19], namely, -90 dBc/Hz at 1-MHz offset from a 10-GHz carrier. For example, the phase noise at 400-kHz offset from the carrier ranged from -101 dBc/Hz at the low end to -87 dBc/Hz at the high end of the tuning range in [18]; a phase noise of -99 dBc/Hz was measured at 1-MHz offset from a carrier in [19]; and a phase noise of -103 dBc/Hz was measured at 600-kHz offset from the carrier in [20]. It should be noted that this improvement was achieved at the cost of increased power dissipation.

- The inadequacy of the conventional technique, namely, using reverse-biased p/n junctions, to achieve wide tuning range was reported [19, 20]. To achieve wide tuning range, an improved variant of it [19] or a new approach [20] was used.

- As a measure of power dissipation, the DC current drawn by the circuit ranged from 2.4 mA [18] to 14 mA [20].

In this thesis a 10-GHz VCO is designed in 0.18-micron, mixed-signal, 6-metal-2-poly, CMOS process. The designed VCO uses an LC topology to achieve superior phase-noise performance. The phase noise is -95 dBc/Hz at 1-MHz offset from the carrier. A novel tuning technique is used to increase its tuning range to 600 MHz compared to the achieved 200-MHz value when the conventional tuning technique is used. It draws 10 mA of DC current form a 1.8-V power supply. A comparison among the above techniques and the proposed one in this thesis is presented in Table 3.1.

Source	Supply Voltage	Phase Noise	Tuning Range	DC-Current Consumption
[18]	2 V	-101 dBc/Hz @ 400-kHz	700 MHz	2.4 mA
[19]	1.2 V	-99 dBc/Hz @ 1-MHz	3.7 GHz	3 mA
[20]	2.5 V	-103 dBc/Hz @ 600-MHz	1.2 GHz	14 mA
Proposed Technique	1.8 V	-95 dBc/Hz @ 1-MHz	600 MHz	10 mA

Table 3.1: Performance metrics of different techniques to implement a 10-GHz, LC oscillator.

Chapter 4

The Proposed Circuit Design

In this chapter, the detailed design of the proposed VCO is presented as well as one of its application examples.[1]

4.1 The Voltage-Controlled Oscillator Circuit

Integrating ring oscillators on a monolithic IC is easy, results in a compact design, and several order of magnitude tuning range is achievable [21]. Their main limitation is the poor spectral purity of the output specifically in the high-frequency region [7]. On the other hand, integrating LC oscillators is hard due to the lack of high-quality, passive inductors in standard IC technologies and their large size. Moreover, tuning range is limited by the non-controllable parasitics of the circuit and the supply voltage which continues to decrease as new IC technologies emerge. However, they exhibit a much higher frequency stability and spectral purity as they employ passive resonators.

As it was reported in [22], ring oscillators with active resistive loads designed and fabricated in 0.18-micorn, mixed-signal, 6-metal-2-poly, CMOS process did not operate in the 10-GHz frequency region. Satisfactory results were obtained by replacing the ring oscillator with an LC one [23]. Moreover, ring oscillators with active inductive loads [32], when designed in the same technology, failed to operate in the same frequency region.

Due to the increase of the data rates in the applications where oscillators represent an important building block, e.g., optical receivers, and the availability of high-quality,

[1]The circuits described in this chapter were simulated using 0.18-micron technology in Cadence®.

passive inductors in the IC process used in this work, it was decided to use an LC-oscillator topology. To overcome its main limitation, namely, narrow tuning range, a novel tuning approach was employed.

Typically, a controlled oscillator consists of a bias, a core circuit (or oscillator), and a buffer building blocks as shown in Figure 4.1. In the following sections, the transistor-level design and simulation results of each of these building blocks are presented.

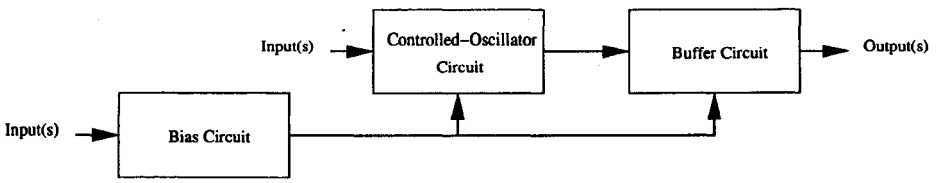


Figure 4.1: Block diagram of a controlled oscillator.

4.2 The Core Circuit

As shown in Figure 4.2(a), two reverse-biased diodes, D_1 and D_2, are used as varactors to tune the output frequency of a differential tuned stage. To avoid forward-biasing the diodes significantly, V_{ctrl} must not exceed V_{out} or $V_{out\_}$ by more than $V_{cut-off}$[2]. Thus, if the amplitude of V_{out} or $V_{out\_}$ is A, $0 < V_{ctrl} < V_{dd} - A + V_{cut-off}$, which indicates a trade-off between the output swing and the tuning range of this circuit.

Standard CMOS process offers two implementations of a diode. In the first, referred to as n^+/p diode, the p-substrate is used as the diode's anode and an n^+ region as its cathode. In the second, referred to as p^+/n diode, a p^+ region is used as the diode's anode and an n-well region as its cathode. Since the substrate is usually connected to ground, the first implementation cannot serve as a varactor. Using an n-well region in the second implementation pauses two problems. Its high resistivity creates a resistance in series with the reverse-biased diode which lowers the quality

[2]It is assumed that the diode conducts a negligible current when it is forward-biased by $V_{cut-off}$ [V].

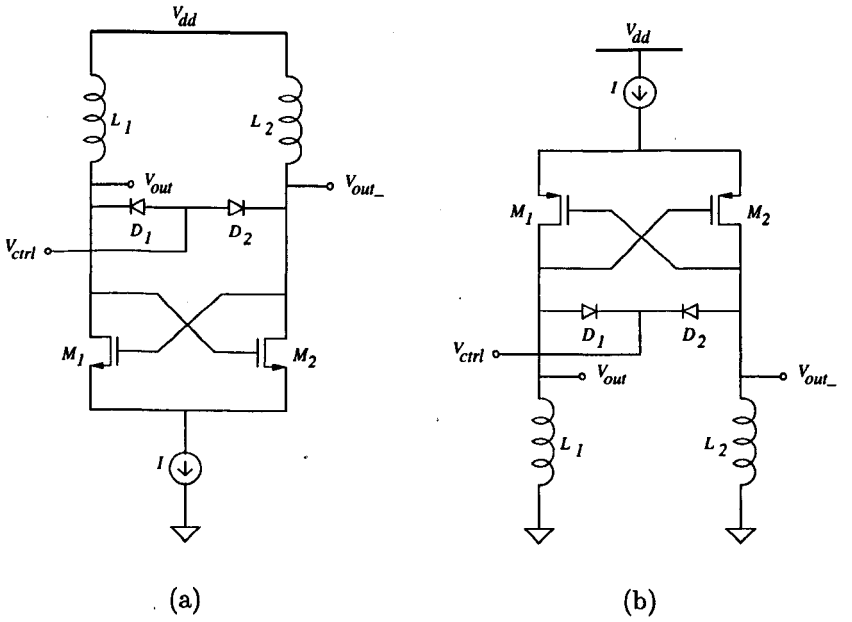


Figure 4.2: (a) Using varactor diodes to tune the output frequency of a differential tuned stage; (b) a variant of the circuit in (a).

factor of its capacitance. Moreover, the n-well region exhibits a substantial parasitic capacitance to the substrate which increases the constant capacitance of the LC tank and limits its tuning range.

Surrounding the p^+ region by an n^+ ring decreases the series resistance of the diode as it reduces the resistance seen by the displacement current through the junction capacitance [27]. On the other hand, it increases the size of the n-well region which increases its parasitic capacitance to the substrate. This drawback can be eliminated by using the variant of the differential tuned stage shown in Figure 4.2(b). However, to obtain the same transconductance, the PMOS devices in this variant must be wider than their NMOS counter parts to account for their lower mobility. This degrades the constant capacitance of the LC tank.

Despite these optimizations, the tuning range of the differential tuned stage remains limited by the supply voltage [27] which continues to decrease as new IC technologies emerge. This limitation can be minimized if a technique, that does not rely on varactors, to tuning the output frequency can be found. Figure 4.3 shows such a

technique[3].

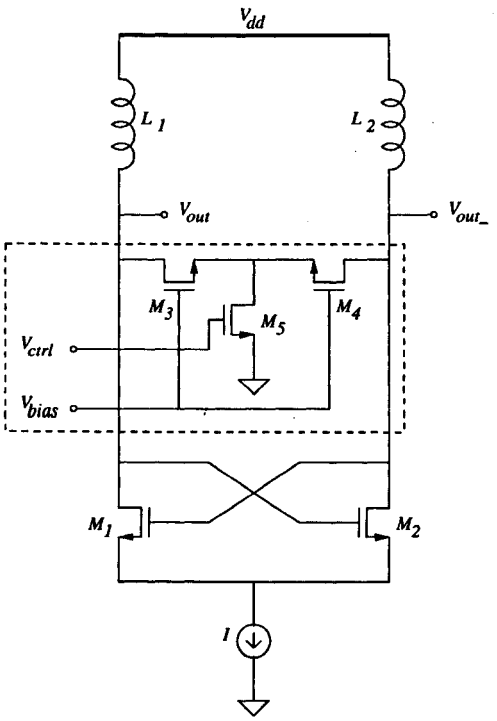


Figure 4.3: The proposed technique (enclosed in the dashed box) to tune the output frequency of a differential tuned stage.

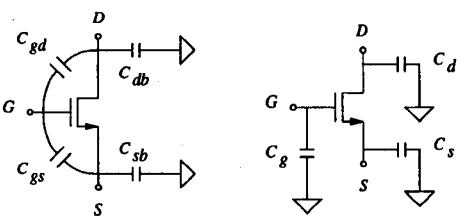
M_1 and M_2 are cross coupled to provide a small-signal resistance of $-2/g_{m1,2}$[4] where $g_{m1,2}$ is the small-signal transconductance of any of them. M_3, M_4, and M_5 control the current flowing in differential tuned stage. Varying V_{ctrl} varies the current through M_5, hence the current drawn form nodes V_{out} and $V_{out\_}$ by M_3 and M_4.

The LC tanks are formed by L_1 and L_2 and the parasitic capacitance at nodes V_{out} and $V_{out\_}$. For the tank formed by L_1 and the parasitic capacitance at node V_{out}, each of its components contribute to its capacitance. While the contribution of L_1 is constant, that of M_1, M_2 and M_3 is controllable. Figure 4.4(a) shows the parasitic capacitances of a MOSFET. These capacitances can be represented by three lumbed capacitances at the drain, gate, and source terminals of the MOSFET as shown in Figure 4.4(b). Including the parasitic capacitances of each transistor in Figure 4.3,

[3]

[4]The derivation of this expression is provided in Appendix C.

the controllable parasitic capacitance at node V_{out} composed of $C_{d;M_1}$, $C_{g;M_2}$, and $C_{d;M_3}$.



(a) (b)

Figure 4.4: (a) Parasitic capacitances of a MOSFET; (b) represinting the capacitances in (a) with lumbed capacitances at the MOSFET terminals.

Varying the current of the differential tuned stage varies the parasitic capacitance of M_1, M_2 and M_3, and its output frequency consequently. Assuming that oscillation conditions are fulfilled, the upper bound of the tuning range is set by the supply voltage whereas its lower bound is set by the region of operation of M_5.

In-phase and quadrature, differential outputs can be obtained by connecting two differential tuned stages as shown in Figure 4.5. The transient and steady-state outputs of this configuration are shown in Figure 4.6. The steady-state output shows that the oscillator generates in-phase and quadrature, differential outputs.

The frequency content of the core circuit's output is shown in Figure 4.7. It shows that it generates a near-sinusoidal output with a dominant harmonic at 10 GHz.

A practical LC tank resonates at a frequency given by [16]

$$\omega_c = \sqrt{\frac{1}{LC} - \left(\frac{R}{L}\right)^2}. \tag{4.1}$$

The magnitude of the impedance of the tank peaks at a frequency ω_p higher than its resonance frequency ω_c. That is, if the tank used to load a tuned stage in an LC oscillator, the output frequency of the oscillator can be tuned from ω_c to ω_p.

Typically, the tuning range of an LC oscillator is 1% to 2% of its center frequency [2]. The characteristic of the proposed LC oscillator is shown in Figure 4.8.

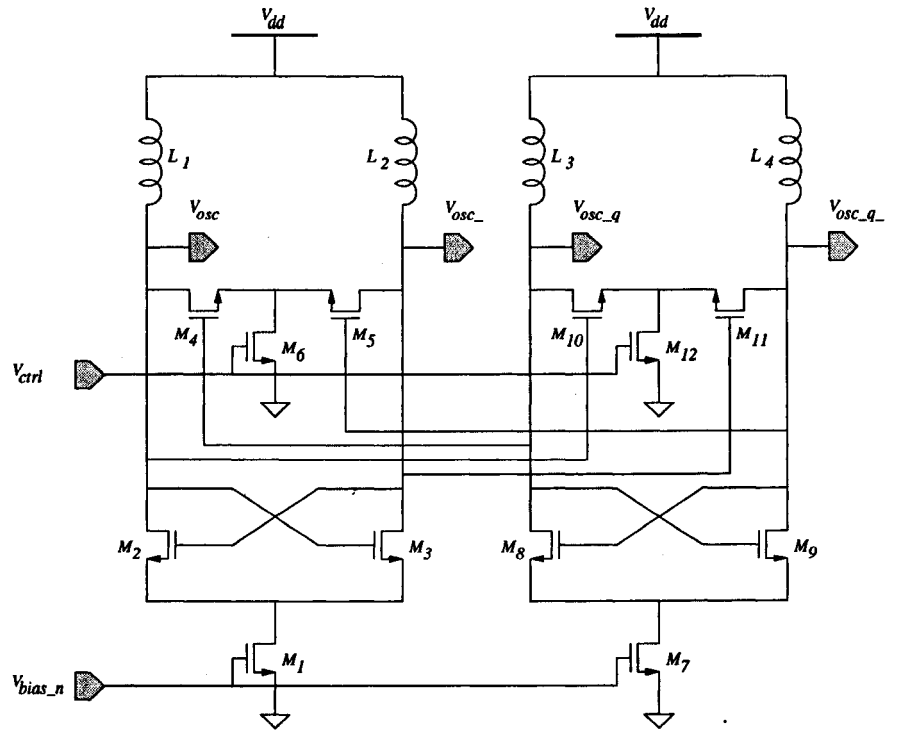


Figure 4.5: Connecting two differential tuned stages to obtain in-phase and quadrature, differential outputs.

It shows that the new tuning technique increased the tuning range of the oscillator to 6% of its center frequency . Also, it shows that the characteristic exhibits good linearity throughout the tuning range.

4.2.1 Waveform Analysis

Referring to Figures 4.6 to 4.8, the following observations can be made:

- The waveforms in Figure 4.6 were magnified at two time instants: during the transient and steady state of the output. The magnified view during the steady state of the outpu t shows that the core circuit generates in-phase and quadrature, differential outputs.
- The waveform in Figure 4.7 was magnified to show that the core circuit generates a near-sinusoidal output with a dominant harmonic at 10 GHz.
- The waveform in Figure 4.8 shows that the output frequency can be tuned from

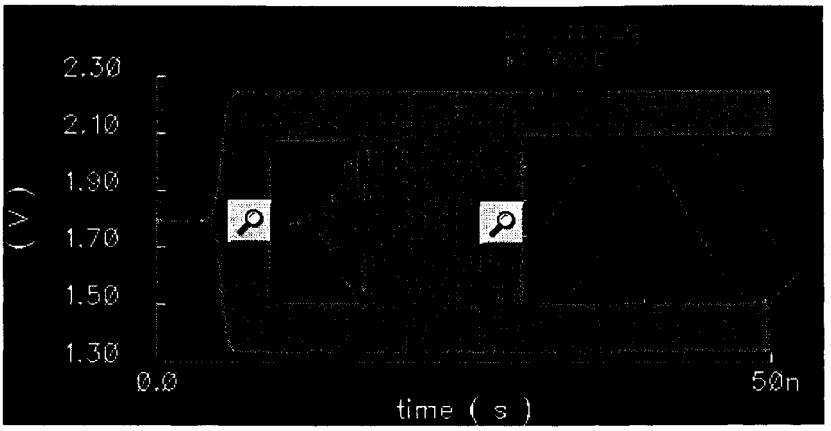


Figure 4.6: The transient and steady-state outputs of the core circuit. The horizontal axis represents the time in [s] and the vertical axis represents the output in [V].

Figure 4.7: The frequency content of the output of the core circuit. The horizontal axis represents the harmonic frequency in [Hz] and the vertical axis displays the harmonic amplitude.

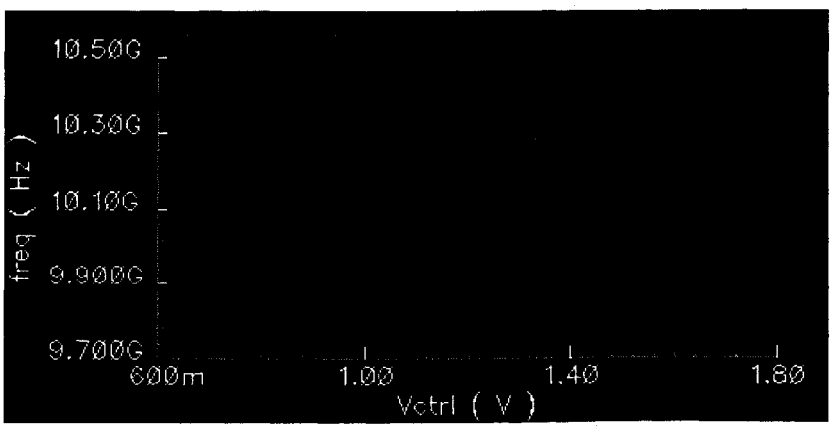


Figure 4.8: The characteristic of the core circuit. The horizontal axis represents V_{ctrl} in [V] and the vertical axis represents the output frequency in [Hz].

9.7 GHz to 10.3 GHz by varying V_{ctrl} from 0.6 V to 1.7 V. Also, it shows that the characteristic exhibits good linearity throughout the tuning range.

4.3 Monolithic Inductors: Design Guidelines

The efficiency of an inductor is measured by its Q, which is limited by the parasitics [24]. The energy storage and loss mechanisms in an inductor can be described by the equivalent energy model shown in Figure 4.9, where L_s, R_s, R_p, and $C_o = C_s + C_p$ represent the overall inductance, conductor loss, substrate loss, and capacitance, respectively.

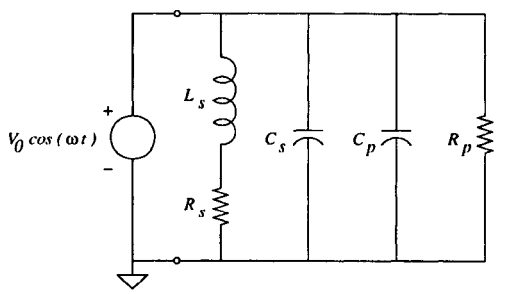


Figure 4.9: Equivalent energy model representing energy-storage and energy-loss mechanisms in a monolithic inductor.

From this model, peak electric and magnetic energies and energy loss in one oscillation cycle are given by

$$E_{E;peak} = \frac{V_0^2 C_o}{2}, \tag{4.2}$$

$$E_{M;peak} = \frac{V_0^2 L_s}{2\left[(\omega L_s)^2 + R_s^2\right]}, \text{ and} \tag{4.3}$$

$$E_{loss} = \frac{2\pi}{\omega}\frac{V_0^2}{2}\left[\frac{1}{R_p} + \frac{R_s}{(\omega L_s)^2 + R_s^2}\right], \tag{4.4}$$

respectively.

Only the energy stored in the inductor magnetic field is of interest. Any energy stored in its electric field, because of some inevitable parasitic capacitances, is a loss. Thus, Q is proportional to the net magnetic energy stored, which is equal to the difference between the peak magnetic and electric energies. An inductor is at

self-resonance when the peak magnetic and electric energies are equal. Therefore, Q vanishes to zero at the self-resonance frequency. Above the self-resonance frequency, no net magnetic energy is available from an inductor to any external circuit.

Using Equations (4.2), (4.3), and (4.4),

$$\begin{aligned} Q &= 2\pi \frac{E_{M;peak} - E_{E;peak}}{E_{loss}} \\ &= \frac{\omega L_s}{R_s} \frac{R_p}{R_s + \frac{(\omega L_s)^2}{R_s} + R_p} \left(1 - \frac{R_s^2 C_o}{L_s} - \omega^2 L_s C_o\right), \end{aligned} \tag{4.5}$$

where the first term accounts for the magnetic energy stored and the ohmic loss in the inductor's conductor. The second term is the substrate loss factor representing the energy dissipated in the substrate. The last term is the self-resonance factor describing the reduction in Q due to the increase in the peak electric energy with frequency and the vanishing of Q at the self-resonant frequency.

An important effect that degrades Q is the current crowding effect. Typically, current crowding is a strong function of frequency and the resistance and increases at higher than linear rate. This causes Q to go down in a concave. A constraint on minimum quality factor, Q_{min}, can be derived from Equation 4.5

$$Q_{min} \frac{R_s}{\omega L_s R_p} \left[R_s + \frac{(\omega L_s)^2}{R_s} + R_p\right] + \frac{R_s^2 C_o}{L_s} + \omega^2 L_s C_o \leq 1. \tag{4.6}$$

Thus, a minimum required quality factor can be specified or the quality factor can be maximized subject to constraint (4.6).

A constraint on minimum self-resonance frequency, $\omega_{sr;min}$, can be derived from Equations (4.2) and (4.3)

$$\omega_{sr;min}^2 L_s C_o + \frac{R_s C_o}{L_s} \leq 1. \tag{4.7}$$

Thus, a minimum required self-resonance frequency can be specified or the self-resonance frequency can be maximized subject to constraint (4.7).

A common problem faced when designing an inductor is to maximize its Q for a given inductance value and for a minimum ω_{sr}. A solution to this problem may be sought using the following guidelines.

- The width of the inductor's strip, W, and the spacing between its traces, S, must satisfy the inequalities $W > W_{min}$ and $S > S_{min}$ to account for the processing constraints that limit the minimum feature size.

- Increasing the width of the inductor's strip decreases its series resistance while its inductance remains the same. The inductor's strip should be as wide as possible until the skin effect becomes significant.

- Increasing the spacing among the inductor's traces decreases the mutual inductance among them, hence its total inductance. Moreover, the inductor's series resistance and total area increase. The spacing between the inductor's traces should be as small as possible.

- The inductor's radius is a very complex parameter to select. For small radii, increasing the inductor's radius increases its Q. On the contrary, for large radii, increasing the inductor's radius increases the losses induced by eddy currents and degrades its Q. Moreover, increasing the inductor's radius increases the shared area between the inductor and the substrate, hence the parasitic capacitance between them, which reduces its resonance frequency. Therefore, the radius should be selected so that the frequency of operation of the inductor is not close to its resonance frequency.

In summary, narrow-strip inductors have higher inductance and lower shunt capacitance per trace compared to a wide-strip inductor. Unlike narrow-strip inductors, wide-strip, narrow-spacing, multi-turn inductors suffer from eddy current and proximity effects especially in the loops closest to the center of the inductor. However, the wide strips and the associated metal thickness reduce its DC resistance significantly. If a narrow-strip and wide-strip inductors were designed with the same trace-to-trace spacing and in the same two-dimensional area, the narrow-strip inductor would have a much higher inductance, similar capacitance, lower self-resonance frequency, and similar resistance (AC+DC) as compared to the wide-strip one.

The inductor used in this work exhibits Q_{max} of 6.41 at 6.51 GHz. Its Q at 10 GHz is 3.85 and its self-resonance frequency is 12.33 GHz.

4.4 The Buffer Circuit

The schematic diagram of the buffer circuit is shown in Figure 4.10. M_5 to M_8 form two differential pairs whose respective drain terminals are tied together and loaded with M_9 and M_{10}. The inputs of the differential pairs are the in-phase and quadrature, differential outputs of the core circuit. The DC level of their outputs is level shifted by applying them to the source followers M_{11} and M_{12}. M_1 to M_4 are used to bias the differential pairs and the source followers.

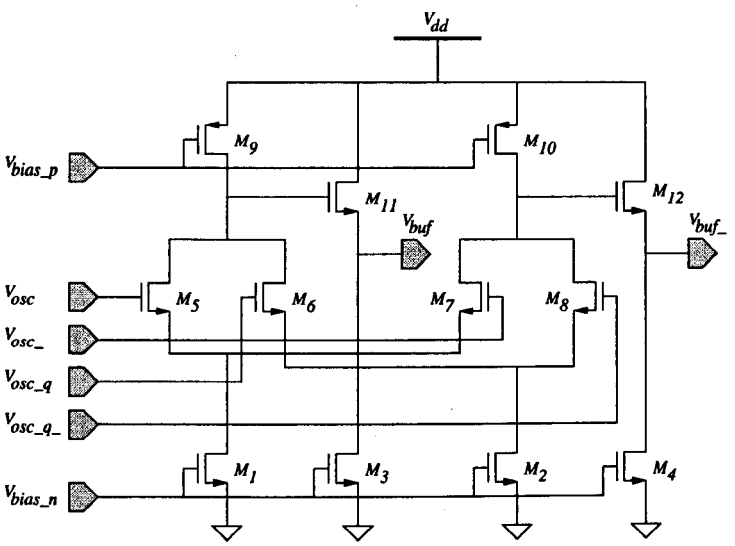


Figure 4.10: Schematic diagram of the buffer circuit.

The transient and steady-state outputs of the buffer circuit are shown in Figure 4.11. It shows that the buffer circuit generates differential output in the steady state. The suppression of the first six harmonics of the output is shown in Table 4.1.

The phase noise, simulated relative to the fundamental harmonic of the buffer circuit's output for different values of V_{ctrl}, is shown in Figure 4.12. This figure shows that the phase noise does not vary considerably throughout the tuning range of V_{ctrl} and approximately equals -95 dBc/Hz at 1-MHz offset from the fundamental harmonic of the buffer circuit's output.

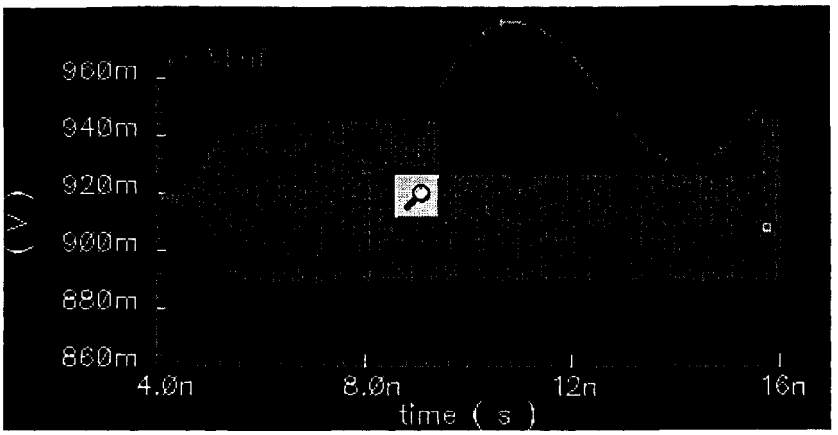


Figure 4.11: The transient and steady-state outputs of the buffer circuit. The horizontal axis represents the time in [s] and the vertical axis represents the output in [V].

Harmonic	Suppression [dBc]
1	0
2	32
3	35.24
4	41.29
5	50.56
6	76.71

Table 4.1: Suppression of the first six harmonics of the oscillator's output.

The output noise, simulated relative to the fundamental harmonic of the buffer circuit's output for different values of V_{ctrl}, is shown in Figure 4.13. This figure shows that the output noise does not vary considerably throughout the tuning range of V_{ctrl} and approximately equals -130 dBc at 1-MHz offset from the fundamental harmonic of the buffer circuit's output.

4.4.1 Waveform Analysis

Referring to Figures 4.11 to 4.13, the following observations can be made:

- The waveforms in Figure 4.11 were magnified during the steady state of the output. The magnified view shows that the buffer circuit generates differential outputs.

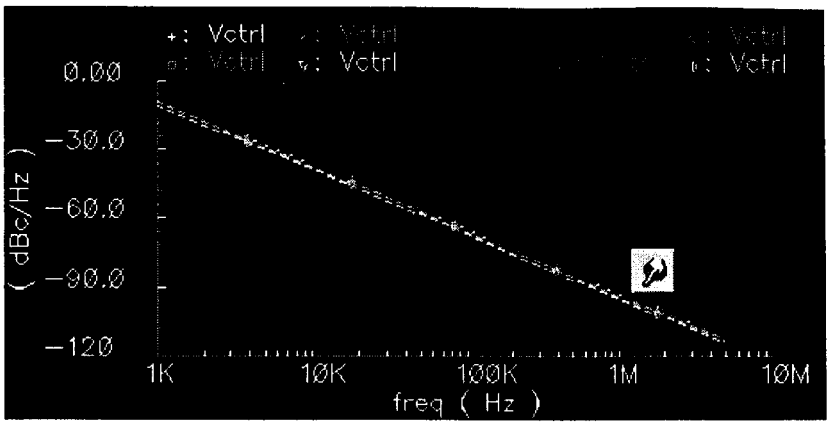


Figure 4.12: Simulated phase noise relative to the fundamental harmonic of the buffer circuit's output for different values of V_{ctrl}. The horizontal axis represents the frequency offset from the fundamental harmonic of the buffer circuit's output in [Hz] and the vertical axis represents the phase noise in [dBc/Hz].

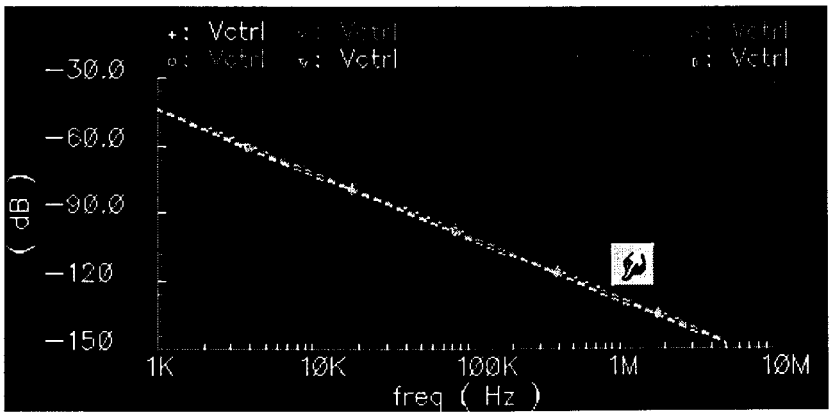


Figure 4.13: Simulated output noise relative to the fundamental harmonic of the buffer circuit's output for different values of V_{ctrl}. The horizontal axis represents the frequency offset from the fundamental harmonic of the buffer circuit's output in [Hz] and the vertical axis represents the output noise in [dB].

- The waveforms in Figure 4.12 show that the phase noise does not vary considerably throughout the tuning range of V_{ctrl} and approximately equals -95 dBc/Hz at 1 MHz.

- The waveforms in Figure 4.13 show that the output noise does not vary considerably throughout the tuning range of V_{ctrl} and approximately equals -130 dB at 1 MHz.

4.5 The Bias Circuit

The schematic diagram of the bias circuit is shown in Figure 4.14. M_1 is a diode-connected device loaded with M_2. The non-inverting input of the opamp is connected to an external reference voltage V_{ref} whereas the inverting one to node X. If the voltage of node X increases, the output of the opamp decreases which increases V_{SG2}. Consequently, V_{SD2} increases which decreases the voltage of node X. Thus, the opamp and M_2 provide negative feedback to the bias circuit.

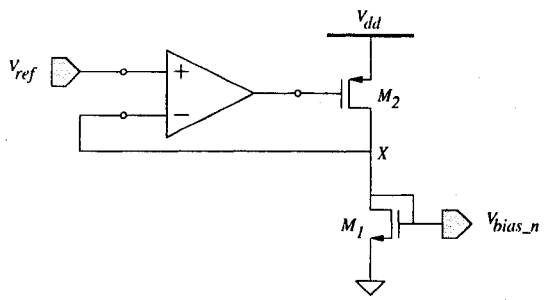


Figure 4.14: Schematic diagram of the bias circuit.

The schematic diagram of the opamp is shown in Figure 4.15. It is implemented as a simple, three-stage opamp. The first stage is a differential pair formed by M_5 and M_6 and loaded with the current mirror M_7 and M_8. The second stage is a gain stage formed by the common source device M_9. The third stage is an output stage formed by the source follower device M_{10}. The resistor R and M_1 to M_4 are needed to bias different stages of the opamp. The capacitor C is needed to ensure stable operation of the opamp in closed loop.

The transient and steady-state outputs of the bias circuit is shown in Figure 4.16.

4.6 Application Example: Phase-Locked Loop

As it is used to demonstrate the importance of the contribution of this thesis, namely, improving the tuning range of the conventional LC-oscillator topology, the theory

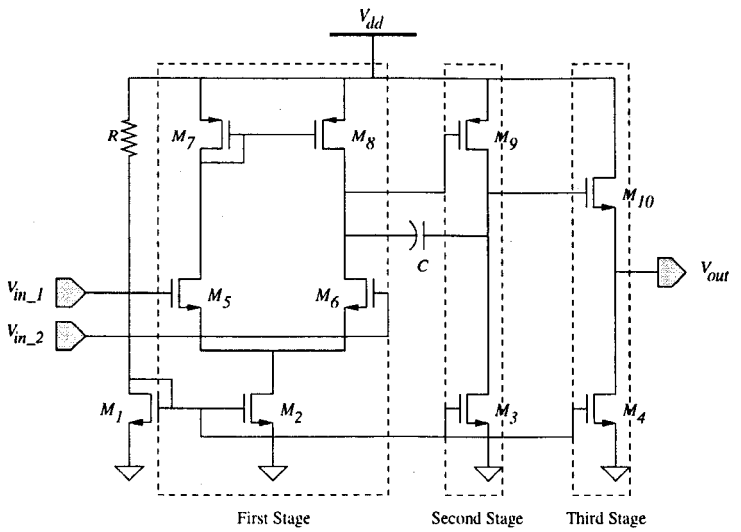


Figure 4.15: Schematic diagram of the opamp.

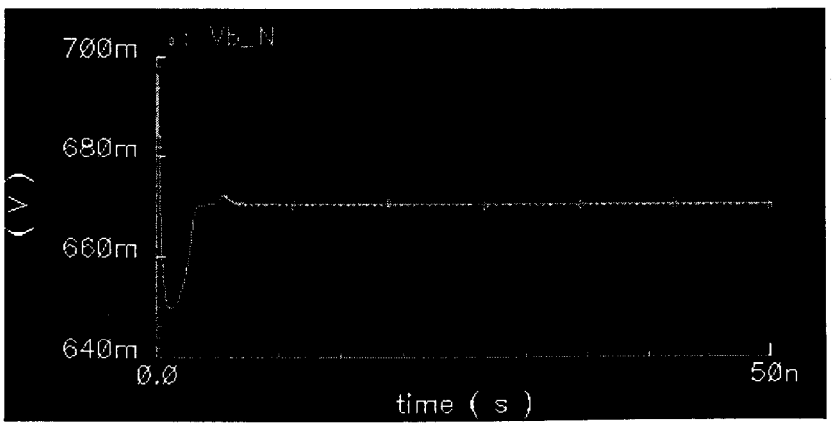


Figure 4.16: The transient and stead-state outputs of the bias circuit. The horizontal axis represents the time in [s] and the vertical axis represents the output in [V].

behind PLL's is reviewed in Appendix D. It should be noted that this theory is extensively covered in many text books [26, 27, 28, 29, 30].

Using Table D.1, a charge-pump PLL was designed. Its parameter values are summarized in Table 4.2.

Substituting these values in the closed-loop transfer function of the third-order, charge-pump PLL in [31], its characteristic equation is given by

$$D(s) = 2.622 \times 10^{-20}\, s^3 + 2.727 \times 10^{-11}\, s^2 + 0.006556\, s + 2.622 \times 10^5. \qquad (4.8)$$

Figures 4.17 and 4.18 show the root locus and step response of such a system, respec-

Parameter	Value
K_{PD}	79.577×10^{-6} [V/rad]
I_{CP}	0.5 [mA]
C_1	27.271 [pF]
R_1	916.725 [Ω]
C_2	1.091 [pF]
K_{VCO}	3.427×10^{9} [rad/s/V]

Table 4.2: Parameter values of the charge-pump PLL.

tively.

The PFD signals for locked inputs, i.e., no frequency- or phase-difference between them, are shown in Figure 4.19. Its signals when the reference frequency is faster than that of the VCO output (or when the reference leads the VCO output) are shown in Figure 4.20. Also, its signals for the reverse situation are shown in Figure 4.21.

To demonstrate the effect of increasing the VCO tuning range on the locking performance of the charge-pump PLL, two VCO's with tuning ranges of 200 and 600 MHz around the center frequency were used. The characteristics of these VCO's are shown in Figure 4.22.

The locking performance of the charge-pump PLL is shown in Figure 4.23. This figure indicates that increasing the VCO tuning range increases the acquisition and tracking ranges of the charge-pump PLL. In other words, its acquisition range increased from 100 to 300 MHz around the VCO center frequency and as a measure of its tracking range, the maximum frequency slew rate of its input was improved by 40%.

4.6.1 Waveform Analysis

Referring to Figures 4.17 to 4.23, the following observations can be made:

- Figure 4.17 shows that the system has one real pole and two complex-conjugate poles in the left half of the s plane which confirms its stability.

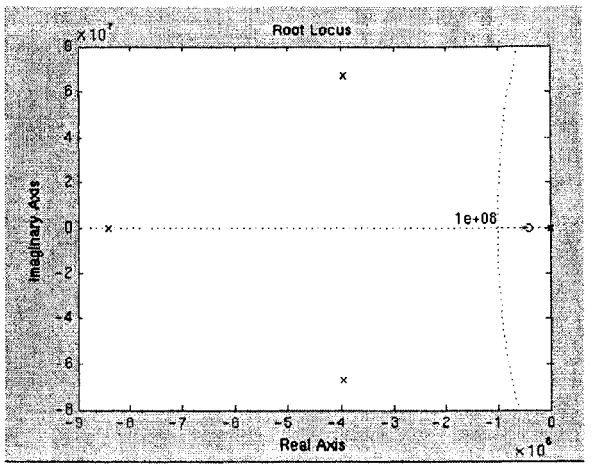


Figure 4.17: The root locus of a third-order, charge-pump PLL. The horizontal axis represents the real component of the pole's location and the vertical axis represents the imaginary component of the pole's location.

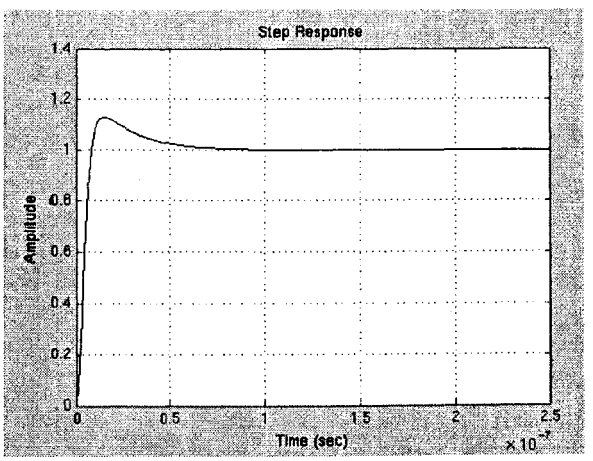


Figure 4.18: The step response of a third-order, charge-pump PLL. The horizontal axis represents the time in [s] and the vertical axis represents the output level.

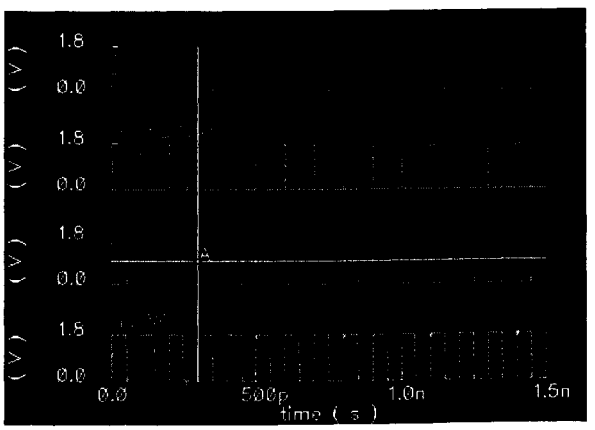


Figure 4.19: The PFD signals for locked inputs. The horizontal axis represents the time in [s] and the vertical axes represent the corresponding signal level in [V].

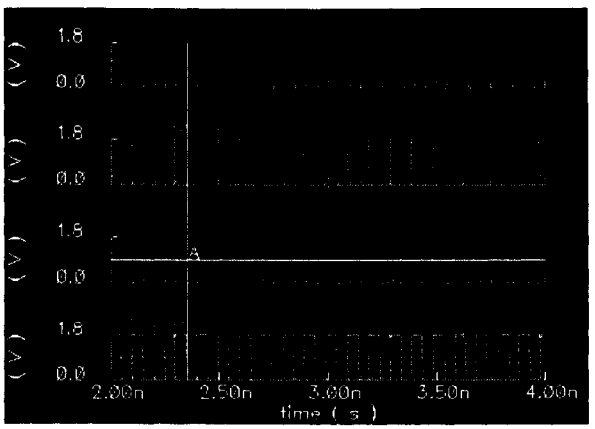


Figure 4.20: The PFD signals when the reference leads the VCO output. The horizontal axis represents the time in [s] and the vertical axes represent the corresponding signal level in [V].

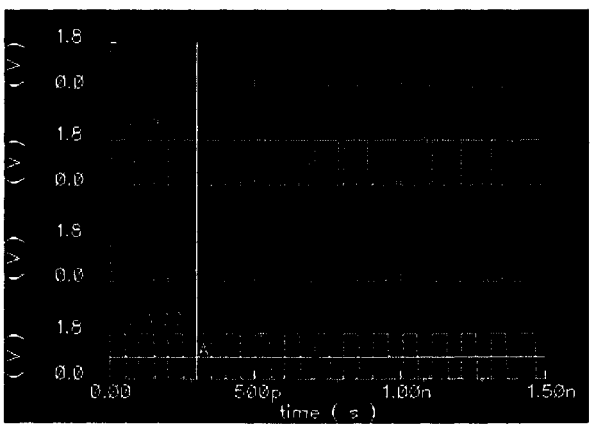
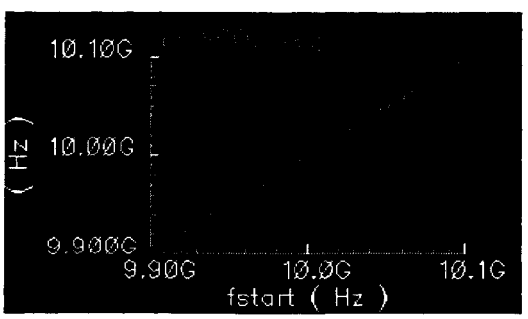
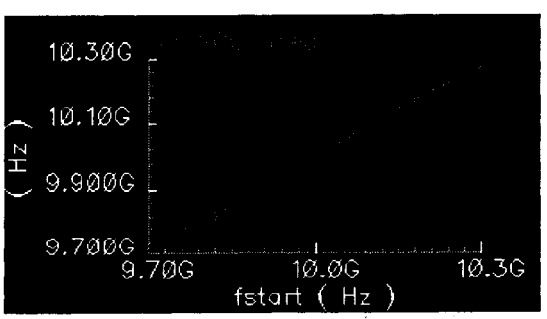


Figure 4.21: The PFD signals when the reference lags the VCO output. The horizontal axis represents the time in [s] and the vertical axes represent the corresponding signal level in [V].



(a)



(b)

Figure 4.22: The characteristic of a (a) 200-MHz, and (b) 600-MHz, tuning-range VCO. The horizontal axes represents the input frequency in [Hz] and the vertical axes represents the output frequency of the VCO in [Hz].

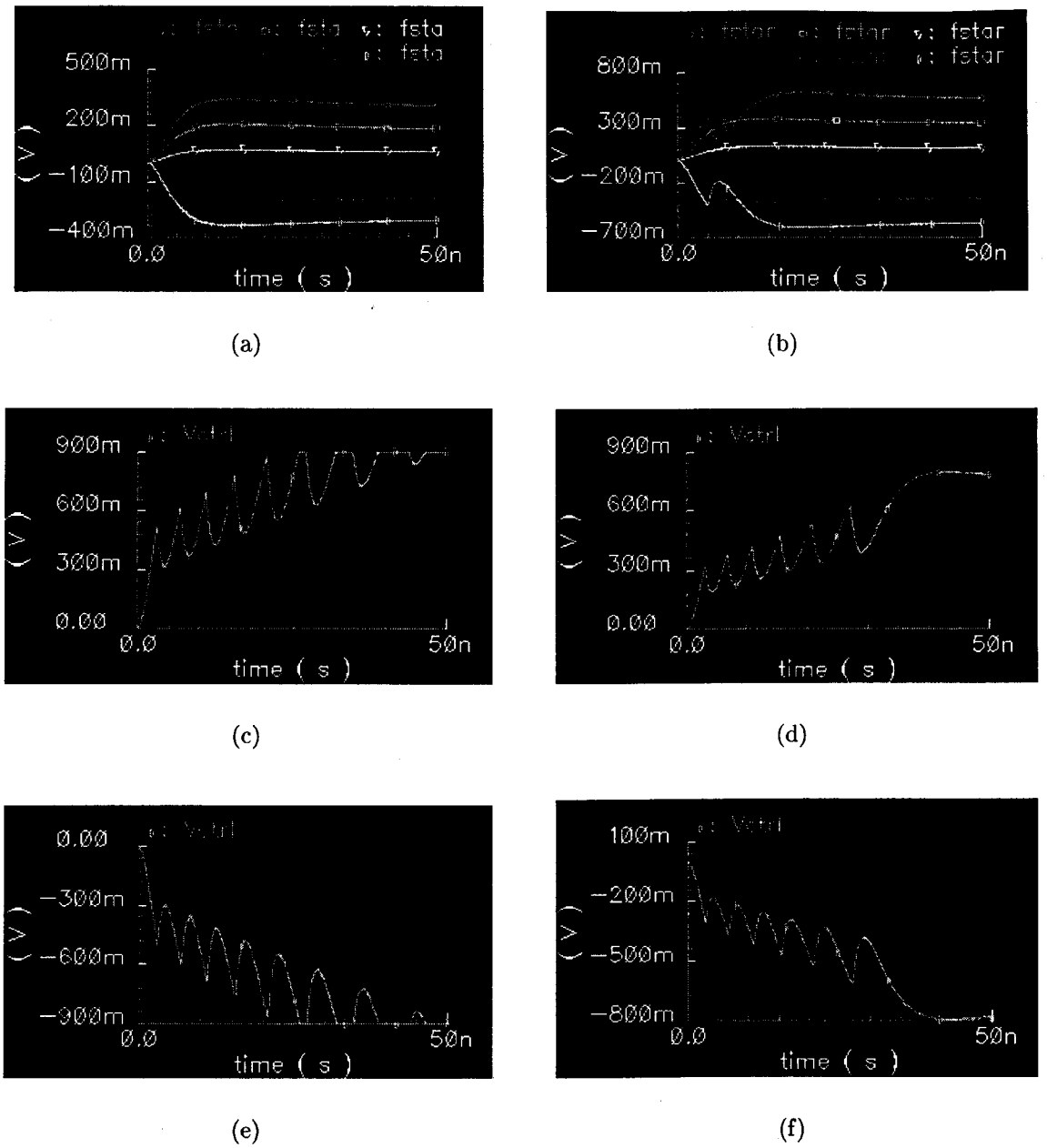


Figure 4.23: The locking performance of a charge-pump PLL employing a 200-MHz, and 600-MHz, tuning-range VCO's: (a) and (b) within its acquisition range; (c), (d), (e) and (f) outside its acquisition range. The horizontal axes represent the time in [s] and the vertical axes represent V_{ctrl} in [V].

- Figure 4.18 shows that the system exhibits approximately 10% overshoot and 0.1 μs settling time.

- Figure 4.19 shows that the PFD inputs are the Ref and VCO signals and its outputs are the P_up and P_down signals. Since there is no phase or frequency deviation between the inputs as confirmed by marker A, no pulses appear on the P_up or P_down line (except for the reset pulses).

- Figure 4.20 shows that the PFD inputs are the Ref and VCO signals and its outputs are the P_up and P_down signals. Since Ref leads VCO as confirmed by marker A, error pulses appear on the P_up line while the P_down line stays calm (except for the reset pulses).

- Figure 4.21 shows that the PFD inputs are the Ref and VCO signals and its outputs are the P_up and P_down signals. Since Ref lags VCO as confirmed by marker A, error pulses appear on the P_down line while the P_up line stays calm (except for the reset pulses).

- Figure 4.22(a) shows that the VCO output frequency can be varied from 9.9 GHz to 10.1 GHz, while in Figure 4.22(b) it can be varied from 9.7 GHz to 10.3 GHz.

- Figure 4.23 shows that throughout the VCO tuning range, 9.9 GHz to 10.1 GHz in (a) and 9.7 GHz to 10.3 GHz in (b), the charge-pump PLL acquires the input frequency and locks to its phase. Above the upper bound of the VCO tuning range, 10.1 GHz in (c) and 10.3 GHz in (d), the charge-pump PLL fails to acquire the input frequency or to lock to its phase. Also, below the lower bound of the VCO tuning range, 9.9 GHz in (e) and 9.7 GHz in (f), the charge-pump PLL fails to acquire the input frequency or to lock to its phase.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In conclusion A 10-GHz, wide-tuning-range, linear, CMOS, voltage-controlled oscillator was designed in 0.18-micron, mixed-signal, CMOS process. The main contribution of this work is increasing the oscillator's tuning range to 6% of its center frequency. It was reported in literature that oscillators utilizing the same topology as the one described in this work and varactors to tune the output frequency exhibit a tuning range of 1% to 2% of the center frequency. Also, the VCO exhibited a good linearity throughout its tuning range; drew 10 mA of DC current from a single, 1.8-V supply; provided quadrature and differential outputs; and exhibited a phase noise of -95 dBc/Hz at a 1-MHz offset from the fundamental harmonic of its output.

The effect of optimizing the tuning range of the VCO on the locking performance of a charge-pump PLL was studied. Simulation results showed that the PLL acquisition range increased to 300 MHz and the maximum frequency slew rate of its input by 40%.

5.2 Future Work

The common trend in communication is toward battery-powered applications. This trend creates a necessity for low-voltage/low-power building blocks. Although the VCO presented in this thesis can operate from a supply voltage as low as 1.5 V, it would be beneficial to reduce its supply voltage and the power it consumes further.

It was mentioned in Chapter 3 that two different topologies are commonly used to implement a VCO in the 10-GHz frequency region, namely, LC topology and distributed topology. It would be informing to design a DVCO in the same process used in this thesis and compare the performance of the two implementations.

It was mentioned that optimizing the tuning range of the VCO was targeted to allow the charge-pump PLL to cope with larger drifts in the frequency and phase of its input and, ultimately, to relax design trade-offs in the target application, namely, fiber-optic receiver. To demonstrate the effectiveness of the proposed solution in this thesis, it would be more convincing to design the whole system in the same process used in this thesis and compare its performance to the conventional system.

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Appendix A

The Quality factor of a Resonant Circuit

The phase noise of an LC oscillator depends on its Q. The higher its Q the sharper its resonance and the lower its phase noise. It is instructive to examine three definitions of Q.

Basic physics defines Q as $2\pi\times$ (energy stored / energy dissipated per one cycle). For an LC tank, it is an indication of the lost energy as it reciprocates between its capacitor and inductor.

Typically, a resonant circuit exhibits a bandpass transfer function. Another definition of Q is the "sharpness" of the magnitude of a resonant circuit's transfer function. More specifically, as shown in Figure A.1, Q is defined as the resonance frequency, ω_r, divided by the two-sided, -3 dB bandwidth, $\Delta\omega$. This definition is an indication of the resonant circuit's selectivity and it yields the same value as the previous one for a simple LC tank.

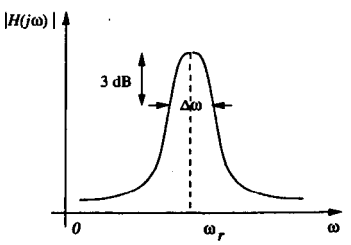

Figure A.1: The magnitude of a resonant circuit's transfer function.

Another definition of Q that proves especially useful in oscillator design is illustrated in Figure A.2. The circuit is considered as a feedback system and the phase of the open-loop transfer function, $\phi(\omega)$, is examined at resonance. The Q is then defined as

$$Q = \frac{\omega_r}{2} \left| \frac{d\,\phi(\omega)}{d\,\omega} \right|. \tag{A.1}$$

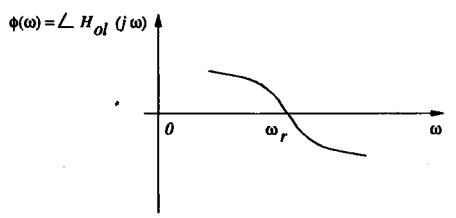

Figure A.2: The phase of an oscillator's open-loop transfer function.

Referred to as "open-loop Q", this definition has an interesting interpretation.To generate steady oscillation, the total phase shift around the oscillator's loop must be zero. If the oscillator's frequency deviates from ω_r and the phase of its open-loop transfer function exhibits large slope at ω_r, a significant change in the total phase shift around the oscillator's loop arises, thus violating the condition of steady oscillation and forcing the frequency to return to ω_r. In other words, the open-loop Q is a measure of the opposition of the closed-loop system to variations in the frequency of oscillation.

Appendix B

Narrowband Frequency Modulation

A carrier defined by $A_c \cos(2\pi f_c t)$ is frequency modulated by a message signal defined by $m(t) = A_m \cos(2\pi f_m t)$ as shown in Figure B.1.

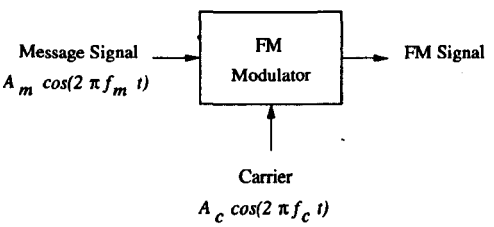

Figure B.1: Frequency modulating a carrier by a message signal.

The instantaneous frequency of the resulting FM signal is given by

$$f_i(t) = f_c + k_f A_m \cos(2\pi f_m t) \quad \text{(B.1)}$$

$$= f_c + \Delta f \cos(2\pi f_m t), \quad \text{(B.2)}$$

where k_f is the frequency sensitivity of the FM modulator in [Hz/V] assuming that $m(t)$ is a voltage signal. The quantity Δf is the frequency deviation, representing the maximum departure of the instantaneous frequency of the FM signal from the carrier frequency f_c. A fundamental characteristic of an FM signal is that the frequency deviation is proportional to the amplitude of the modulating signal and is independent of the modulating frequency.

The instantaneous angle of the FM signal is given by

$$\theta_i(t) = 2\pi \int_0^t f_i(t)\, dt \tag{B.3}$$

$$= 2\pi f_c t + \frac{\Delta f}{f_m} \sin(2\pi f_m t). \tag{B.4}$$

The ratio of the frequency deviation to the modulation frequency is the modulation index of the FM signal and is denoted by β, hence

$$\theta_i(t) = 2\pi f_c t + \beta \sin(2\pi f_m t). \tag{B.5}$$

From Equation (B.5) we see that, in physical sense, the parameter β represents the phase deviation of the FM signal, that is, the maximum departure of the angle $\theta_i(t)$ from the angle $2\pi f_c t$ of the demodulated carrier; hence, β is measured in radians.

The FM signal itself is given by

$$s(t) = A_c \cos[2\pi f_c t + \beta \sin(2\pi f_m t)]. \tag{B.6}$$

Depending on the value of the modulation index β, we may distinguish two cases of frequency modulation: narrowband FM, for which β is small compared to one radian, and wideband FM, for which β is large compared to one radian.

Expanding Equation (B.6) results in

$$s(t) = A_c \cos(2\pi f_c t) \cos[\beta \sin(2\pi f_m t)] - A_c \sin(2\pi f_c t) \sin[\beta \sin(2\pi f_m t)]. \tag{B.7}$$

Assuming that the modulation index β is small compared to one radian, the following approximations may be used

$$\cos[\beta \sin(2\pi f_m t)] = 1, \tag{B.8}$$

and

$$\sin[\beta \sin(2\pi f_m t)] \approx \beta \sin(2\pi f_m t). \tag{B.9}$$

Hence, Equation (B.7) simplifies to

$$s(t) \approx A_c \cos(2\pi f_c t) - \beta A_c \sin(2\pi f_c t) \sin(2\pi f_m t). \tag{B.10}$$

Equation (B.10) defines the approximate form of a narrowband FM signal generated by a sinusoidal modulating signal $A_m \cos(2\pi f_m t)$.

Appendix C

Generation of a Small-Signal, Negative Resistance

One way of realizing an oscillator, e.g., LC oscillator, is by connecting a one-port, negative-resistance network and a one-port, frequency-determining network. Consequently, a one-port network which exhibits a small-signal, negative resistance is required. A common implementation of such network is by cross coupling two MOSFETs as shown in Figure C.1(a).

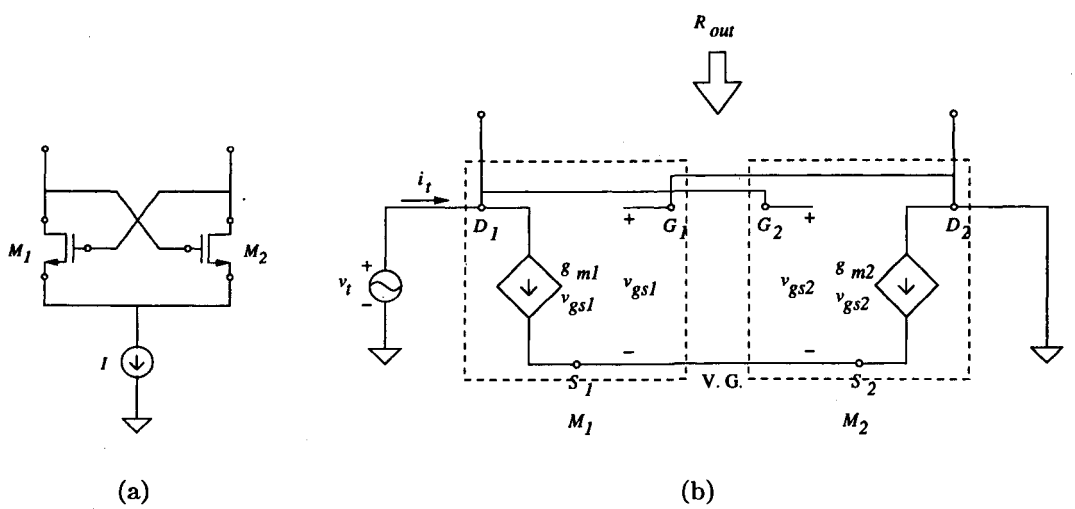

Figure C.1: (a) Implementing a one-port, negative-resistance network by a cross-coupled pair of MOSFET's; (b) the small-signal equivalent of the circuit in (a).

The small-signal equivalent [25] of this circuit is shown in Figure C.1(b). To simplify the analysis of this circuit, the dependence of the signal quantities on time

will be dropped.

From Figure C.1(b)

$$v_t = v_{gs2} - v_{gs1}, \tag{C.1}$$

and

$$i_t = g_{m1}\, v_{gs1} = -g_{m2}\, v_{gs2}, \tag{C.2}$$

thus,

$$R_{out} = \frac{v_t}{i_t} = \frac{-1}{g_{m1}} - \frac{1}{g_{m2}}. \tag{C.3}$$

If M_1 and M_2 are matched devices, i.e., $g_{m1} = g_{m2}$, then

$$R_{out} = \frac{-2}{g_m}. \tag{C.4}$$

Appendix D

Phase-Locked Loop: A Background

The basic architecture of the PLL is described in Section 1.5 and shown in Figure 1.3. According to the implementation of its building blocks, a PLL can be categorized into three main categories: analog, analog-digital (hybrid), or all digital PLL [28].

D.1 Modeling the Building Blocks of the PLL

Although the PLL is a nonlinear, time-varying system, a linear, time-invariant approximation may be utilized to gain insight in its design trade-offs. To arrive at this approximation, each of its building blocks needs to be characterized and modeled.

The ideal PD generates an output whose average is proportional to the phase difference between its inputs, hence, it can be characterized by

$$\overline{v_{PD}(t)} = K_{PD}\,\Delta\phi(t), \tag{D.1}$$

where K_{PD} is the gain of the PD in [V/rad] and $\Delta\phi(t)$ is the phase difference between its inputs. Thus, it can be modeled by a subtractor and a gain block followed by a LPF as shown in Figure D.1.

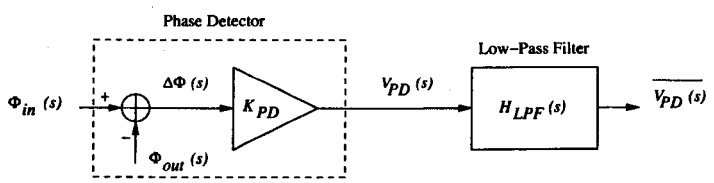

Figure D.1: Block diagram of the PD.

Due to its sufficient performance, the LPF is often implemented as a first- or second-order, passive, RC filter. The most common implementations are shown in Figure D.2.

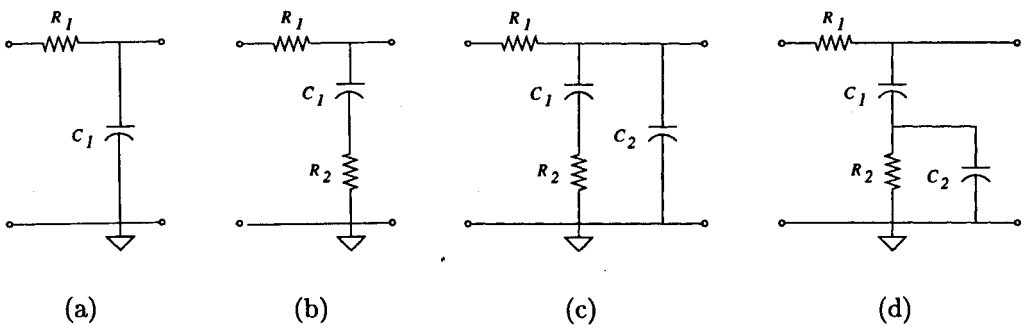

Figure D.2: Common implementations of the LPF.

Filters D.2(a) and D.2(b) exhibit first-order characteristic. Thus, their transfer functions do not contain an ideal integrator which limits the acquisition and tracking ranges of the PLL. Moreover, filter D.2(a) introduces trade-offs among the parameters controlling the dynamic behavior of the PLL [2]. To eliminate these trade-offs, it is usually replaced by filter D.2(b).

On the other hand, filters D.2(c) and D.2(d) exhibit second-order characteristic. C_2 is needed to suppress the glitches across R_2 due to the sudden changes in the input of the filter. Introducing C_2 results in a third-order PLL. Since less understanding is attained for third-order systems than second-order ones, C_2 is usually chosen to be 10 times smaller than C_1, hence, the PLL can be approximated by a second-order system.

In a charge-pump PLL [31], the input to the LPF is a current signal. To adapt filters D.2(c) and D.2(d) to this change, R_1 is usually removed[1].

The ideal VCO generates a periodic output whose frequency is proportional to its control voltage, hence, it can be characterized by

$$\omega_{VCO}(t) = \omega_{FR} + K_{VCO}\, v_{ctrl}(t), \tag{D.2}$$

[1] An alternative approach is to introduce a V-to-I building block between the charge pump and the LPF [32].

where ω_{FR} is the free-running frequency, K_{VCO} is the gain in [rad/s/V], and $v_{ctrl}(t)$ is the control voltage of the VCO. Since the PD compares the phases of its inputs, the VCO is usually modeled as a linear, time-invariant system whose input is the control voltage and the output is the excess phase generated by this control voltage as shown in Figure D.3,

$$\phi_{VCO}(t) = K_{VCO} \int v_{ctrl}(t)\, dt, \tag{D.3}$$

hence, its transfer function is given by

$$\frac{\Phi_{VCO}(s)}{V_{ctrl}(s)} = \frac{K_{VCO}}{s}. \tag{D.4}$$

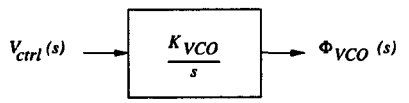

Figure D.3: Block diagram of the VCO.

D.2 The Linearized Model of the PLL

Since it contains a wide range of time constants, simulating a PLL at transistor level is very difficult. A very large time constant, on the same order as that of the PLL, is introduced by the LPF, while a much smaller time constant, often less than one ten-thousandth of that of the PLL, is introduced by the VCO. Thus, the PLL must be simulated using a very small time step to obtain accurate results, and for a very long time period to observe the behavior of the overall system. This places unreasonable requirements on computer resources, unless extremely simple circuitry is used [2].

The linearized model of the PLL is shown in Figure D.4.

This model approximates the dynamics of the PLL under the following conditions

- The PLL is locked.
- The attribute of interest, phase or frequency, of the input and the output of the PLL changes slowly and by small amounts around its operating point. In other words, this model relates the *changes* in the input and the output of the PLL.

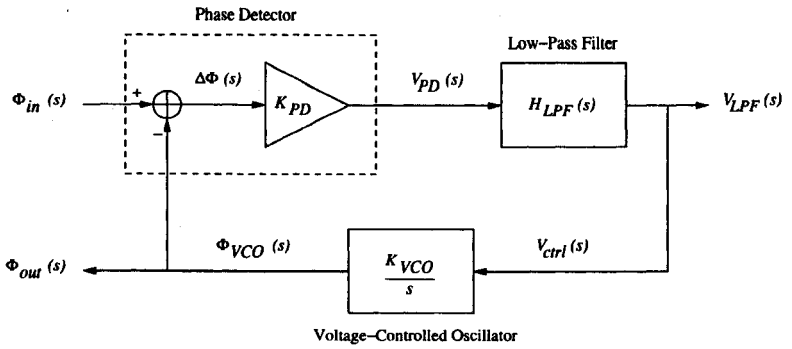

Figure D.4: The linearized model of the PLL.

Most PLL's differ in the the realization of their building blocks. Despite this difference, the analysis of the dynamics of any PLL is usually carried out using its closed-loop transfer function. Referring to Figure D.4, several closed-loop transfer functions (which relate different variables) can be defined.

In general, the closed-loop transfer function that relates $V_{ctrl}(s)$ to $\Phi_{in}(s)$ applies to most PLL's. It is given by

$$H_{cl}(s) = \frac{V_{ctrl}(s)}{\Phi_{in}(s)} = \frac{s\,K_{PD}\,H_{LPF}(s)}{s + K_{PD}\,H_{LPF}(s)\,K_{VCO}}, \tag{D.5}$$

where $H_{LPF}(s)$ is the transfer function of the LPF. For most PLL's, the transfer function of the LPF can be approximated by

$$H_{LPF}(s) = \frac{1 + s\,\tau_z}{1 + s\,\tau_p}, \tag{D.6}$$

where $\tau_z \ll \tau_p$.

The denominator of Equation (D.5) indicates that the characteristic equation of the PLL is of the second order. Its standard form is given by

$$D(s) = 1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}, \tag{D.7}$$

where ω_0 is the pole frequency and Q is the pole Q factor [2]. A geometric interpretation for ω_0 and Q of a pair of complex-conjugate poles is shown in Figure D.5.

The value of Q is chosen such that the PLL may acquire a specific dynamic behavior. Assuming a step change in the attribute of interest, phase or frequency, of the input of the PLL, one of the following choices may be made [26]:

[2] In terms of the damping factor ζ, $Q = 1/2\zeta$.

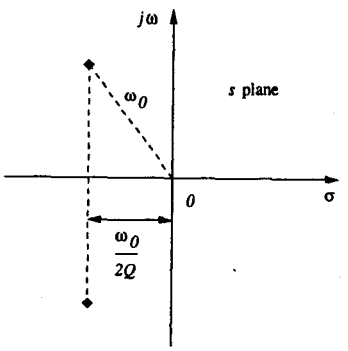

Figure D.5: Definition of ω_0 and Q of a pair of complex-conjugate poles.

- $Q = 1/2$ to achieve good settling behavior.
- $Q = 1/\sqrt{2}$ to achieve maximally-flat amplitude response.
- $Q = 1/\sqrt{3}$ to achieve maximally-flat group delay.

For most PLL's the first choice is recommended. In this case the transient time constant of the PLL is given by

$$\tau_{PLL} \approx \frac{1}{\omega_0}. \tag{D.8}$$

In most cases, e.g., high-frequency region, ω_0 is much less than the free-running frequency of the VCO. Using Equations (D.5), (D.6), and (D.7), ω_0 and Q are given by

$$\omega_0 = \frac{K_{PLL}}{\sqrt{\tau_p}}, \tag{D.9}$$

where $K_{PLL} = \sqrt{K_{PD}\, K_{VCO}}$ assuming unity gain in the passband of the LPF, and

$$\begin{aligned} Q &= \frac{\sqrt{\tau_p}}{\frac{1}{K_{PLL}} + \tau_z K_{PLL}} \\ &\approx \frac{\sqrt{\tau_p}}{\tau_z K_{PLL}}. \end{aligned} \tag{D.10}$$

Inspection of Equations (D.9) and (D.10) indicates that the independent selection of ω_0 and Q is possible. On the contrary, when $\tau_z = 0$, Q and ω_0 are given by

$$Q = K_{PLL}\sqrt{\tau_p} \tag{D.11}$$

and

$$\omega_0 = \frac{K_{PLL}^2}{Q} \tag{D.12}$$

and such selection is not possible.

D.3 Lock Metrics

The locking performance of the PLL is described by two main metrics, namely, acquisition and tracking ranges.

D.3.1 Acquisition Range

The maximum difference between the input frequency and the free-running frequency of the VCO where the PLL can acquire lock.

D.3.2 Tracking Range

Assuming the PLL is locked to a signal whose frequency is equal to the free-running frequency of the VCO, the maximum drift in the input frequency from the free-running frequency of the VCO where the PLL can maintain lock is referred to as tracking range.

D.4 Charge-Pump PLL

Enhancing the acquisition and tracking ranges of the PLL relaxes many of the system's design trade-offs where it is intended to be used. This can be achieved by maximizing the pole frequency of its LPF or using some frequency acquisition means. Since the first alternative trades with other parameters which affect the quality of output of the PLL and its stability, the second alternative is usually favored.

Typically, the acquisition and Tracking ranges of a PLL (e.g., analog PLL and analog-digital PLL with a flip-flop PD) are mainly limited by the characteristic of its PD. As its input frequency deviates substantially from the free-running frequency of its VCO, the PD saturates and fails to generate the required error signal(s) to acquire the lock.

On the contrary, the characteristic of the charge-pump PFD [33, 34, 35, 36, 37], shown in Figure D.6, does not exhibit this limitation, hence, the acquisition and

tracking ranges of the charge-pump PLL are mainly limited by the characteristic of its VCO. Moreover, charge-pump PLL acquires lock quickly with zero phase error between its input signal and the output signal of the VCO and does not exhibit false lock.

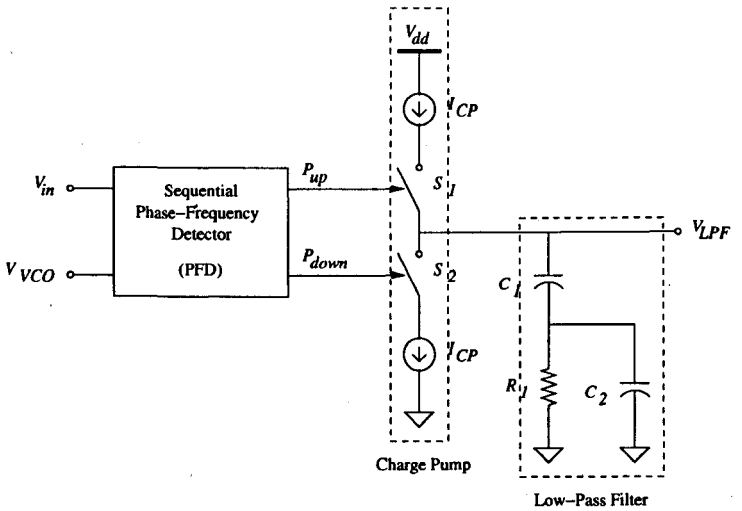

Figure D.6: Block diagram of the charge-pump PFD.

If the input and output of the charge-pump PLL are of the same frequency but out of phase, I_{CP} flows into its LPF for a duration equivalent to the phase difference between its input and output whereas no current flows for the rest of the period. This illustrates the time-variant nature of the unlocked charge-pump PLL. To simplify its analysis, a time-invariant system that has the same *average* current flowing into the LPF is used.

The average current flowing into the LPF in Figure D.6 is given by

$$i_{avg}(t) = \frac{\Delta\phi(t)}{2\pi} I_{CP}. \tag{D.13}$$

The charge pump and the PFD can be characterized by

$$i_{avg}(t) = K_{PD}\,[\phi_{in}(t) - \phi_{out}(t)] = K_{PD}\,\Delta\phi(t), \tag{D.14}$$

thus,

$$K_{PD} = \frac{I_{CP}}{2\pi}. \tag{D.15}$$

Quantity	Formula
PLL Transfer Function	$H_{cl}(s) = \frac{1}{K_{VCO}} \frac{s(1+s R_1 C_1)}{1+s R_1 C_1 + \frac{s^2 C_1}{K_{PD} K_{VCO}}}$
PD Gain	$K_{PD} = \frac{I_{CP}}{2\pi}$
LPF Transfer Function	$H_{LPF}(s) \approx \frac{1+s R_1 C_1}{s C_1}$
PLL Pole Frequency	$\omega_0 = \sqrt{\frac{K_{PD} K_{VCO}}{C_1}}$
PLL Time Constant	$\tau_{PLL} \approx \frac{1}{\omega_0}$
PLL Quality Factor	$Q = \frac{1}{R_1 C_1 \omega_0}$
PLL Acquisition Range	Limited by the VCO tuning range.
PLL Tracking Range	Limited by the VCO tuning range.

Table D.1: Design formulas of a second-order, charge-pump PLL.

Neglecting C_2, the transfer function of the LPF is given by

$$H_{LPF}(s) = \frac{V_{LPF}(s)}{I_{avg}(s)} = \frac{1 + s R_1 C_1}{s C_1}. \tag{D.16}$$

Substituting Equations (D.14) and (D.16) into Equation (D.5) and comparing the denominator of the result to Equation (D.7), the following results are obtained

$$H_{cl}(s) = \frac{1}{K_{VCO}} \frac{s(1 + s R_1 C_1)}{1 + s R_1 C_1 + \frac{s^2 C_1}{K_{PD} K_{VCO}}}, \tag{D.17}$$

$$\omega_0 = \sqrt{\frac{K_{PD} K_{VCO}}{C_1}}, \tag{D.18}$$

$$Q = \frac{1}{R_1 C_1 \omega_0} = \frac{1}{R_1 \sqrt{C_1 K_{PD} K_{VCO}}} = \frac{1}{R_1} \sqrt{\frac{2\pi}{C_1 I_{CP} K_{VCO}}}. \tag{D.19}$$

The design formulas of a charge-pump PLL, based on its linearized, second-order model, are summarized in Table D.1.