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Radio-Frequency Power Harvest And Remote Clock Frequency Calibration Of Passive Wireless Microsystems

Nima Soltani
Ryerson University

Radio-Frequency Power Harvest and Remote Clock Frequency Calibration of Passive Wireless Microsystems

by

Nima Soltani

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Abstract

Radio-Frequency Power Harvest and Remote Clock Frequency Calibration of Passive Wireless Microsystems

Nima Soltani

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This thesis deals with radio frequency power harvest and remote calibration of system clock of passive wireless microsystems. The proposed method of RF power harvesting utilizes a step-up transformer inserted between the antenna and voltage multiplier of passive wireless microsystems to perform both impedance transformation for power matching and voltage amplification prior to rectification. The series resistance of the primary winding is minimized while in the secondary winding, the shunt capacitive losses are minimized. The detailed analysis of the proposed method and simulation results from Spectre of Cadence Design Systems are presented. The proposed power-matching and gain-boosting network, together with voltage multipliers, has been implemented in TSMC-0.18..m 1.8V 6-metal CMOS technology with thick metal options. For the purpose of comparison, a LC power-matching and gain-boosting network with the identical voltage multiplier has also been implemented on the same chip. Measurement results demonstrate that the proposed transformer power-matching and gain-boosting technique greatly improves the power sensitivity and efficiency as compared with widely used LC matching approaches.

The proposed calibration method adjusts the frequency of the local oscillator of passive UHF wireless transponders to the desired values using an injection-locked phase-locked loop (IL-PLL). A new relaxation oscillator whose oscillation frequency is less sensitive to supply voltage fluctuation is also proposed. The power consumption of the

proposed IL-PLL is minimized by operating it the sub-threshold. A detailed analysis of non-harmonic injection locking of relaxation oscillators including locking and pulling dynamics is presented. A new integrating feedback is proposed to increase the lock range and hold the locked frequency in the absence of the injection signal. The proposed IL-PLL has been fabricated in TSMC-0.18μm 1.8V 6-metal 1-poly CMOS technology. The performance of the IL-PLL is validated using both simulation and measurement results. The measured power consumption of the IL-PLL with a 10 mV (640 pW) 1 MHz injection signal is 960 nW. The lock range of the IL-PLL is 30 KHz without integrating feedback and 400 KHz with integrating feedback. The frequency of the locked oscillator drifts over time at a rate of 5 Hz/ms when the external injection signal is removed.

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List of Symbols

ADC Analog-to-Digital Converter

ADS Advanced Design Systems

AM Amplitude Modulation

ASK Amplitude-Shift Keying

BER Bit Error Rate

CAD Computer-Aided Design

CMOS Complementary Metal-Oxide Semiconductor

dBm Decibel power with respect to 1 Milliwatt

EEPROM Electronically Erasable Programmable Read-Only Memory

EM Electromagnetic

EPC Gen2 Electronic Product Code Generation 2

FF (nMOS)Fast-(pMOS)Fast

FM Frequency Modulation

FS (nMOS)Fast-(pMOS)Slow

FSK Frequency-Shift Keying

HP Hewlett-Packard

IL-PLL Injection-Locked Phase-Locked Loop

ILO Injection-Locked Oscillator

ISM Industrial Scientific Medical (radio bands)

ISO International Organization for Standardization

LC Inductor-Capacitor

LO Local Oscillator

MH Manual Handeling

MIM(-cap) Metal-Insulator-Metal (Capacitor)

nMOS n-channel Metal-Oxide Semiconductor

PLL Phase-Locked Loop

PM Phase Modulation

pMOS p-channel Metal-Oxide Semiconductor

POR Power-ON Reset

PSK Phase-Shift Keying

PVT Process (supply-)Voltage Temperature

reltol relative tolerance

RF Radio Frequency

RFID Radio Frequency Identification system

RLC Resistor-Inductor-Capacitor

SF (nMOS)Slow-(pMOS)Fast

SS (nMOS)Slow-(pMOS)Slow

TSMC Taiwan Semiconductor Manufacturing Company

TT (nMOS)Typical-(pMOS)Typical

UHF Ultra High Frequency

VCO Voltage-Controlled Oscillator

Chapter 1

Introduction

RF powered microsystems, also known as passive transponders, are critically needed in many applications such as automated payment systems, irretrievable pressure sensors in cement structures, and remote tracking devices. They have also found emerging applications in implantable electronics [61, 62, 63, 64], retinal prosthetic device [65], neuromuscular stimulation [66], wireless environme ntal monitoring [67], RFID [68], wireless medical endoscopy [9, 10], to name a few. The great advantage of a passive transponder is not having a power supply on-board. This enables it to operate indefinitely without requiring a battery exchange or recharge. Moreover, not having a power source attached to them, the transponders can be manufactured in very small sizes, making them attractive for producing implantable discrete wireless sensors.

1.1 Background

An RF powered transponder is a small wireless system that communicates with a nearby station called the *reader*. The reader provides the transponder with power and initial information through a wireless channel. The reader-transponder communication protocol always starts with a relatively long power-up period during which the storage capacitor of the transponder is charged to an operational level [18]. At this point, the reader may send a data request which will be acknowledged by the transponder should the requested data be available. The transponder data are usually sensor readings or identification codes. These data are processed by the reader to gain the knowledge of the transponder's

environment or identify subjects carrying the device.

1.1.1 Architecture

The architecture of an RF powered transponder has two majors layers: (1) an RF front and (2) baseband data units. The baseband circuits provide processing, generation and/or storage of baseband data– or any combination of the three. These units may include EEPROM's for the storage of long ID codes, ADC's for quantizing sensor readings or even microprocessors that provide basic data/signal processing at the transponder. Fig.1.1 is the block diagram of a generic transponder architecture. All these blocks will have very stringent power constraints in an RF powered microsystem. Design for lower power consumption remains the top challenge. The study of baseband circuits, however, is beyond the scope of this thesis and will not be discussed here.

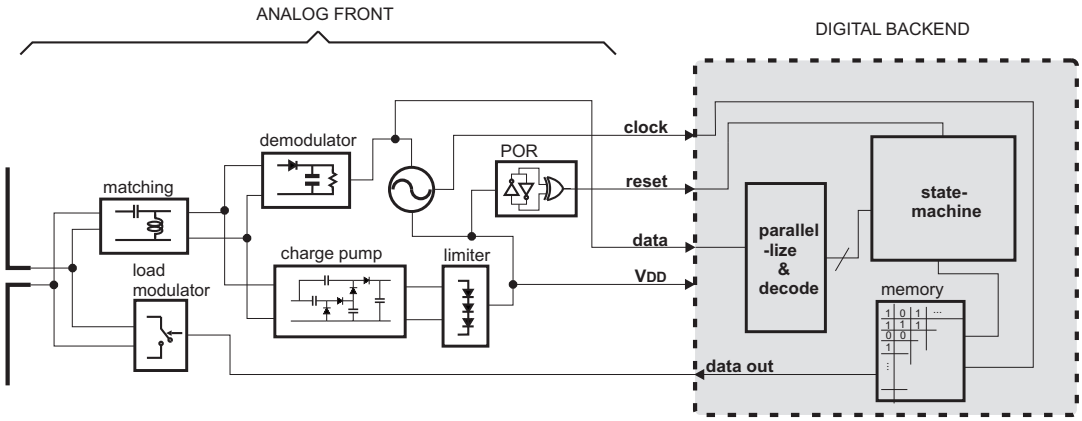

Figure 1.1: Architecture of a typical passive transponder device.

The RF front is responsible for supply of power to the chip, and the wireless data interface with the reader. Major RF front components are antenna, antenna matching network, RF-to-DC converter, modulator and demodulator. The matching network and RF-DC conversion block are some times together referred to as *RF power harvester*. Each block will be briefly described here, and more detailed presentation will be given in the next two chapters.

1.1.2 Antenna

The antenna supplies the chip with power by gathering the electromagnetic wave coming from the reader. It also receives the envelope of data modulated by the reader on the same carrier that provides the power. The shape and dimensions of the antenna are determined by the carrier wavelength, channel bandwidth and polarization of the EM field. For example, lower frequency (near-field) transponders often use magnetic coils whereas dipole, folded-dipole and meander-line antennas are the popular configurations in UHF and microwave transponders. Small loop antenna is also popular geometry especially when the size of the antenna is required to be significantly smaller than the wavelength. Another advantage of the small loop antenna is its large inductive reactance which could be used to create passive voltage gain in the received signal for power harvesting purposes. Fig.1.2 shows different antennas used in RFID's (radio-frequency-identification) and passive transponders.

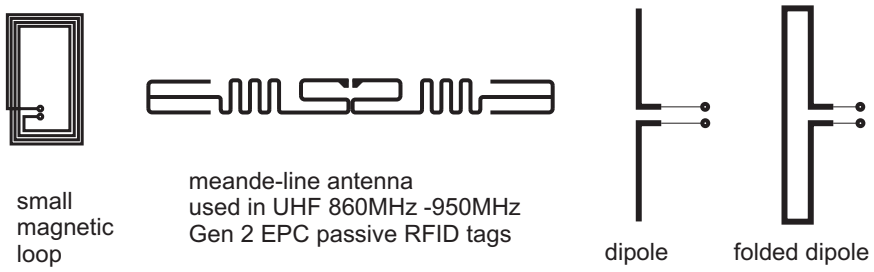

Figure 1.2: Popular antenna geometries for RFID's and passive transponders.

1.1.3 Matching Network

Regardless of the configuration, the impedance of the antenna has to be matched to that of the chip to ensure maximum transfer of power. This is accomplished by using a power matching block, which is a network of inductors and capacitors. Since these elements have purely imaginary impedances, ideally the power matching network does not dissipate power. However due to the conductive loss of the inductor traces, the efficiency of the matching network becomes a pressing issue especially in on-chip matching where, in addition to the conductive loss, a significant portion of the available power is consumed in the substrate. Loss of energy in the substrate is mainly due to the

radial and circular currents caused by coupling of electric and magnetic fields into the substrate. Another power-matching issue is the varying of the chip impedance under different loading conditions and proximities of the reader. These issues, however, are not as problematic. One solution to design the matching network for the worst case condition where the load consumption is the largest. Power matching will be further discussed in 3. Fig.[1.3] shows the diagram of a typical matching network placed between the antenna and the rectification block.

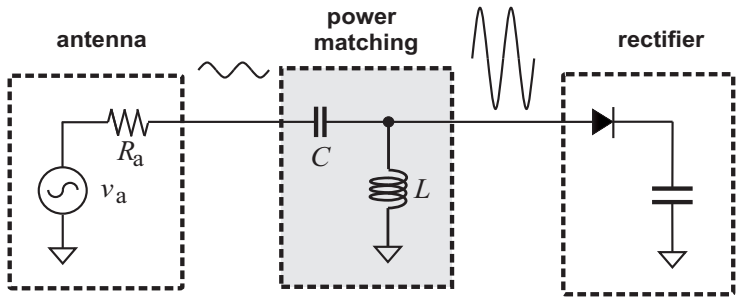

Figure 1.3: A typical matching network used to matching the input impedance of the rectifier to the radiation impedance of the antenna.

1.1.4 Rectification

RF-to-DC conversion is implemented using rectifiers or voltage multipliers. In the higher frequencies however, due to smaller antenna aperture, the signal at the transponder is more attenuated. Most transponders operating at these frequencies use special rectifying charge-pump circuits that also boost the voltage of the signal. Such architectures are called voltage multipliers. The DC output of a voltage multiplier is normally higher than the peak AC voltage applied to it. The main challenge in the design of voltage multipliers is their conversion efficiency which is typically limited to less than 30% in most reported designs. In fact, efficiencies higher than 15% can only be achieved by use of non-standard features such as shottky diodes or silicon on insulator technologies [15, 12, 16].

1.1.5 Modulation Backscatter/Load Modulation

In passive designs, the absence of power source makes the transmission of signals from the transponder very challenging. Most designs do not allocate any DC power for RF transmission. Instead, they take advantage of a phenomenon called *backscattering* or *backscatter modulation*. Backscatter in antennas is similar to the reflection phenomenon in radars. Here, a portion of the received signal is reflected from the antenna back to the reader. The amount of power reflected and the delay of the reflected wave are determined by the input impedance seen between the two terminals of the receiver antenna. Therefore, by modulating the termination impedance (or load) of the antenna, the reflected wave is modulated. Load modulation eases the power constraints of the design to a great extent. In fact, by using this method along with other low-power design techniques, some of the recent UHF and microwave transponders have been able to lower the overall power consumption to a few microwatt, whereby increasing the operational range to up to over 12 meters, while keeping the reader's transmission powers within the ISM bands regulations[12, 16]. Fig.1.4 shows the principle of backscattering in passive transponders.

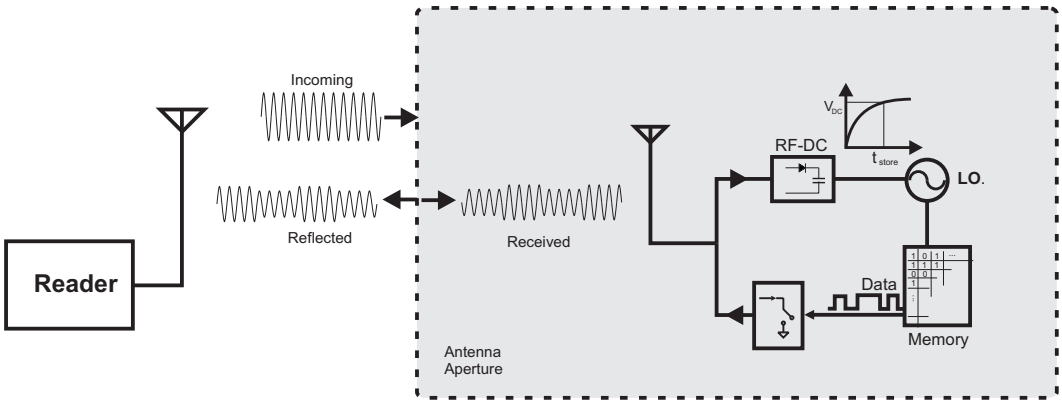

Figure 1.4: Different matching network topologies for RF power harvesting. Transformer power matching circuit is proposed in this thesis.

1.1.6 Demodulation

As shown in Fig.1.1, the demodulator is located in parallel with the RF-DC conversion block, and draws a small fraction of the total RF current flowing into the chip. Due to power limitations, demodulation is usually done incoherently using an envelope detector followed by gain and signal quantizing circuits. Since the received signal must be large enough to power the device, envelope detection is well feasible in most cases.

1.1.7 Wireless Link

Based on the wireless link characteristics with readers, transponders are typically categorized into *inductively-coupled*, *electromagnetically-coupled* and *close-coupled*. In inductive coupling, the transponder is physically located in the near field of the reader. By approximation, the near field corresponds to a distance of $\frac{\lambda}{2\pi}$ or 0.16λ from the reader's transmission antenna [18], where λ is the wavelength of the carrier signal. This type of coupling is only viable for frequency bands up to tens of Mega Hertz where the wavelengths are in the meter range. An example is the ISM bands 6.7 MHz and 13.6 MHz. Electromagnetic coupling is a full-fledged wireless link between a reader and a transponder and is used in higher frequency bands, such as UHF and microwave.

System modeling and classification of RF powered microsystems have been extensively studied in the past [18]. The objective of this thesis is to design power-efficient circuits in standard CMOS technologies for use in the RF front of passive transponders and microsensors. The particular frequencies of the circuits proposed in this thesis are the ISM UHF band (900 MHz) and Microwave band (2.45 GHz) which correspond to ISO 18000-6 and ISO 18000-4 RFID standards respectively.

1.2 Motivations

The major motivation of this thesis has been to work toward overcoming the following major challenges in the design of passive wireless transponders:

1.2.1 Challenges in Wireless Transfer of Power

In wireless communication systems, a mobile system must be able to receive data from its base station as well as to transmit packets of data back to the base station over a wireless channel. In active mobile systems, such as cellular phones, large energy storage devices, i.e. batteries, allow for the filtering and amplification of incoming signals as small as a few microvolts of amplitude, and peak transmission output power as large as a few watts. In passive mobile stations, such as RFID tags, however, the only source of energy available to the systems is the power of the radio-frequency waves coming from the base station. Due to the unavailability of large storage capacitors in these passive systems and the fast response requirement of these systems, it is often impractical to store energy for later usage [19]. Therefore, power constraints on design of practical passive mobile wireless systems are:

1. A total change of energy over each transaction is zero or negative (no source).

2. all the power entering the system should exit *shortly* after (no storage).

The immediate consequence of these constraints is that the power of the output signal from the transponder is directly sourced from the power of the input signal. In other words, the total power available to the transponder at every instance is the power that enters the system through the antenna within a very short time span prior that instance. The instantaneous power flow is due to the lack of large storage devices in these microsystems (the second constraint). The total amount of available power is determined by the following:

1. Operating frequency: determines the effective aperture of the antenna. Antenna aperture and available power are larger at low operating frequencies.

2. Gain of the antenna: determined by antenna efficiency and directivity.

3. Efficiency of RF power harvesting circuit: determined by matching and rectification efficiencies.

4. Operating distance: less power is available at a farther distance from the reader.

Here, we will go through each of these factors by discussing their effect of wireless power transfer as well as their limitations in improving the power transfer efficiency:

In most designs, a large operating distance desirable. Usually, all other factors are optimized so as to maximize the operation distance. In cases where a far-reaching operation range is not very critical, optimizing the first three factors leads to more available power. This in turn facilitates the design of a faster, more accurate and/or more complex back-end circuitry.Even though the use of lower operating frequencies leads to higher power availability at a given distance, antennas are much larger in size at lower frequencies. This makes them impractical for many applications such as object tracking and implantable devices.

Increasing the gain of transponder antenna requires larger and more cumbersome geometries. Increasing the directive gain also requires the transponder antenna to be in a particular physical alignment with the reader during operation; a condition that would make the device less attractive for many applications.

The efficiency of RF power harvesters is usually limited to less than 10% using standard CMOS technologies [15] and to around 30% when using off-chip matching circuit and/or more expensive non-standard features such as shottky diodes or silicon-on-insulator technology, such as the ones reported in [17, 12, 13, 16]. In addition to power efficiency, the sensitivity of the power harvester is also limited by the threshold voltage of the rectifying diodes of diode-connected devices. In other words, even when power loss of the RF-DC conversion circuit is small, the rectifier cannot operate when the voltage swing at its input is less than the voltage drop of the diodes.

The operating distance in many applications is desired to be as large so that the transponder can be operational even at farther distances from the reader. Larger operating distance, however, imposes stringent limitation on the amount of available power to the transponder as well as the efficiency of RF power harvesting. As the transponder moves farther away from the reader, the electric and magnetic field components attenuate by a factor of square of distance which means the signal received by the antenna will be much smaller resulting in smaller available power and RF-DC conversion efficiency.

1.2.2 Challenges in Data Communication

In a passive transponder system, the available power is equal to the instantaneous incoming RF power. The power of the signal transmitted by the transponder is indeed less than the available power. Upon arriving at the reader, the signal from the transponder will be extremely attenuated, making the task of receiver design particularly difficult in the reader. If the exact center frequency and bandwidth of the transponder signal is not known to the receiver, the filter has to be designed to have wider passband than the actual bandwidth of the signal so as to cover all possible center frequencies and bandwidths of the transponder signal. Wider passband will result in more noise being filtered through, significantly increasing the BER of the downlink[20]. This point is illustrated graphically in Fig.1.5(b).

Fig.1.5(c) shows a special case were transponder data are modulated by a carrier prior to being backscattered. This method is called backscattering with subcarriers and provides separation between the carrier and the backscattered signal so that the reader can pick up the backscattered signal more easily. The bandwidth and the center frequency of the backscattered signal are set by the local oscillator of the transponder.

The center frequency and bandwidth of transponder signal are set by the frequency of the local oscillator of the transponder. Generating a precise frequency requires quality reference components such as high-precision resistors and capacitors. Due to the low frequency of baseband oscillators, use of the on-chip inductors is usually not practical. High precision components are either not available in standard CMOS processes or they come at an additional cost. An alternative to using high-precision components is to calibrate the frequency of the local oscillator prior to each downlink transaction by having the reader send a calibrating signal of a known duration (pulse width) or frequency. This method is a widely accepted solution to the problem of uncertain LO frequency in low-cost transponder design [20].

In designing frequency calibration for passive transponders and RFIDs, there is an inevitable trade-off between calibration speed and the power consumption of the calibration circuit. This is due to the fact that to transmit the symbol zero, the RF wave must be severely attenuated. This attenuation of the carrier signal lead to less power being available to the transponder. The duration of the attenuation is dictated by the data rate of the wireless link [12]. The amount of attenuation is dictated by the input SNR

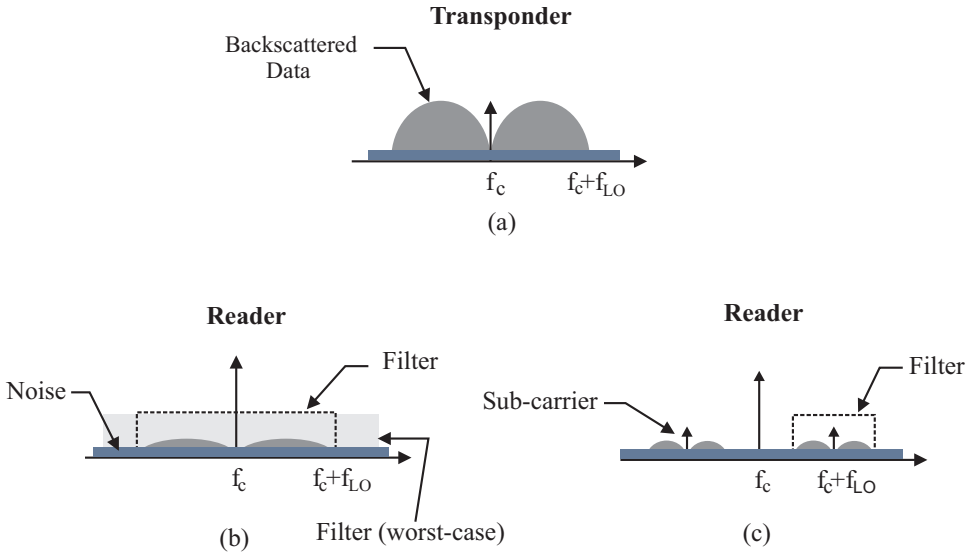

Figure 1.5: Power spectrum of signals (a) at the transponder, (b) at the reader without subcarrier, and (c) at the reader with subcarrier.

requirement of the transponder detection circuit which is typically very high due to the small amount of power available. In the ISO-18000-C (EPC Gen2) standard–the most recent standard for UHF RFIDs– to communicate a zero, the RF signal must be attenuated by at lest 90% for at lest 50% of the symbol duration. Performing fast calibration requires sending a high-frequency reference signal to the transponder. This will lead to a sudden drop in the supply voltage.

1.3 Objectives

The objectives of this thesis are the following:

1. to design a highly-efficient power harvesting circuit developed entirely on-chip and using only standard CMOS technology components. Such system is critically needed for increasing the power available to the transponder, thereby increasing the operating range and/or functionalities of the system.

2. to design an ultra-low power frequency calibration system with fast operation. Such system is critically needed for establishing a reliable wireless data link without compromising the transponder response time.

1.3.1 Efficient Power Harvesting

In this thesis, the objective is to increase power harvest efficiency and sensitivity by targeting the performance of the matching network. In transpodners, matching network is the passive circuit placed between the antenna and the rectifier/voltage-multiplier to match the impedance of the two blocks. Doing that, the matching network will provide passive voltage gain to the signal coming from the antenna. The increased voltage swing of the RF signal will increase both the efficieny and the sensitivity of the power harvesting circuit.

1.3.2 Low-Power Fast Frequency Calibration

The main focus in design of frequency calibration system in this thesis is to improve the calibration time while maintaining the same low power consumption reported for digital calibration techniques used in [20, 62]. As discussed in Section 1.2.2, the major limitation of digital calibration techniques is the theoretical limit on the speed of the total operation. In this thesis, our effort has been to design an analog calibration techniques using the phenomenon injection locking that can speed up the process of frequency calibration while having a total power consumption in the same range as the ones reported for the digital calibration techniques.

1.4 Contributions

This thesis contains the following original contributions:

- A technique to increase the available power to a passive transponder as outlined in Section 1.3 objective (1). The proposed method provides impedance matching using on-chip an transformer that provides a larger voltage gain than the conventional LC matching network, thereby providing a significantly higher conversion efficiency.

- A low-power frequency calibration technique using injection locking as outlined in Section 1.3 objective (2). This technique injects a small calibrating signal into the local oscillator of the transponder to adjust its oscillation frequency. To make the frequency adjustments permanent, an integrating feedback is simultaneously applied to correct the control voltage of the VCO. This way, the VCO frequency remains at the calibrated value when the injection signal is removed. The external feedback also increases the locking range of the VCO, reducing the minimum required amplitude of the calibrating signal.

- A comprehensive theory of injection locking and pulling in non-harmonic oscillator. The proposed time-domain analysis delivers results analogous to the frequency-domain model provided in [21, 22] for harmonic oscillators. The frequency-domain model, however, is not applicable to digital and other non-harmonic oscillators where the open-loop transfer function is non-linear. This thesis uses discrete time-domain analysis to capture the behavior of non-harmonic oscillators under injection.

- An ultra-low power low-V_{DD}-sensitivity relaxation oscillator to operate under low-supply condition has been proposed. The design reduces the sensitivity of the oscillation frequency to supply voltage by increasing the hysteresis width of the open-loop circuit while using only one timing capacitor. The significance of the single-capacitor design is that the oscillator has a single injection point whereas in the dual-capacitor design ([23, 24]) the injection signal has to be steered between the two capacitors over every charge and discharge interval.

  The results of the research presented in this thesis has been published at different stages of their development in the following book chapter, journals and conference proceedings:

  1. N. Soltani and F. Yuan, "Remote frequency calibration of passive wireless microsystems" in *Integrated Bio-Microsystems : Where Electronics Meets Biology*, Ed. Kris Iniewski. Accepted, 2010.

  2. N. Soltani and F. Yuan, "A High-Gain Power-Matching Technique for Efficient Radio-Frequency Power Harvest of Passive Wireless Microsystems," *IEEE Trans. Cir. & Sys. I: Regular Papers*, May 2010, In Press.

3. N. Soltani, F. Yuan "Nonharmonic Injection-Locked Phase-Locked Loops With Applications in Remote Frequency Calibration of Passive Wireless Transponders," *IEEE Trans. Cir. & Sys. I: Regular Papers*, May 2010, In Press.
4. N. Soltani and F. Yuan, "A step-up transformer impedance transformation technique for efficient power harvesting of passive transponders," *Microelectronics Journal*, Vol.41, pp.75-84, 2010.
5. N. Soltani, F. Yuan "Low-voltage low V_{DD} sensitivity relaxation oscillator for passive wireless microsystems," *Electronics Letters*, Vol. 45 , No. 21, pp. 1057 - 1058, Oct. 2009.
6. N. Soltani and F. Yuan, "Remote frequency calibration of passive wireless microsensors and transponders using injection-locked phase-locked loop," *Proc. IEEE Int'l Symp. Circuits Syst.*, pp.541-544, Taipei, May 2009.
7. N. Soltani and F. Yuan, "A high-gain impedance matching technique for efficient power harvesting of passive wireless microsystems," *Proc. IEEE Int'l Symp. Circuits Syst.*, accepted in Jan. 2010.
8. N. Soltani and F. Yuan "Remote frequency calibration of passive wireless transponders using injection-locked PLL," *Microsystems and Nanoelectronics Research Conference*, 2009, pp. 1 - 4, Oct. 2009.
9. N. Soltani and F. Yuan, "An autotransformer impedance transformation techniquefor efficient powe harvesting of passive transponders and wireless microsensors," Proc. IEEE Mid-West Symp. Cir. Syst., pp. 898-901, Knoxville, TN., Aug. 2008.
10. F. Yuan and N. Soltani, "Design techniques for power harvesting of passive wireless microsensors," *Proc. IEEE Mid-West Symp. Circuits Syst.*, pp.289-293, Knoxville, TN. Aug. 2008.

1.5 Thesis Organization

This thesis is organized as follows:

Chapter 1 provides a conceptual overview of passive wireless microsystems. Configuration of the Analog Front of passive transponders is introduced and the functionality of each block is discussed in brief. This chapter also provides some of

the main challenges currently faced in the design of passive communication systems. The objectives of the thesis is defined based on these challenges. Finally, the contributions that the research has made toward achieving those objectives is stipulated.

Chapter 2 provides the state-of-the-art reviews of the two major building blocks of interest in this thesis, namely power harvester and clock frequency calibration systems. This chapter reviews the current trends in the two areas based on the conducted literature reviews, and compares the designs based on their cost and performance.

Chapter 3 describes the proposed technique for radio frequency power harvesting using monolithic transformers. The technique is compared with RF power harvesters using LC resonators. The proposed power harvester improved RF sensitivity and power efficiency. The design is also compared with recently published designs.

Chapter 4 describes the proposed method for remote frequency calibration in passive transponders. A new theory on injection locking and pulling of non-harmonic oscillator is introduced in this chapter. The behavior of relaxation oscillators under injection is studied. The effect of adding an external integrating feedback is also studied.

Chapter 5 summarizes the thesis. The directions of future work are also outlined.

1.6 Chapter Summary

In this chapter we presented an overview of passive wireless communication systems. We presented a brief introduction to passive transponder architecture and the wireless protocols for communication with the reader. Fundamental building blocks of the analog front of the passive transponders were enumerated and briefly discussed in terms of their functionality, implementation and design challenges. It was argued that one the most important areas of improvements in passive transponder systems is the RF power harvesting circuit. The power efficiency of this block is currently imposing significant limitations on the overall efficiency of the transponder systems especially in the ones developed in low-cost CMOS technologies. It was

also pointed out that a critical element is data communication between the reader and the transponder is the local oscillator which is required to provide stable oscillation frequency. Creation of such oscillation requires a frequency calibration system to be implemented on the transponder. The design of frequency calibration system is also a subject of study in this thesis.

Chapter 2

A State-of-the-Art Review in Design of Power Harvesting and Clock Calibration Circuits for Passive Transponders

2.1 Power Harvester Design

Radio-frequency power harvesting efficiency is determined by the efficiency of the antenna of the transponder, the quality of power matching between the antenna and the voltage multiplier for the maximum power transmission, and the power efficiency of the voltage multiplier that converts the received RF signal into a dc voltage from which microsystems are powered. The power efficiency of voltage multipliers has been frequently studied [25, 17, 15] and an in-depth review of the design techniques for voltage multipliers was provided in [28]. Although increasing the gain of the voltage multiplier improves the amount of the power of passive wireless microsystems, voltage multipliers implemented in standard CMOS technologies suffer from a low efficiency, typically less than 14%.

Fig.2.2 shows two of the charge-pump topologies that are widely used in passive transpodners. A major limiting factor on the efficiency of multipliers is the small

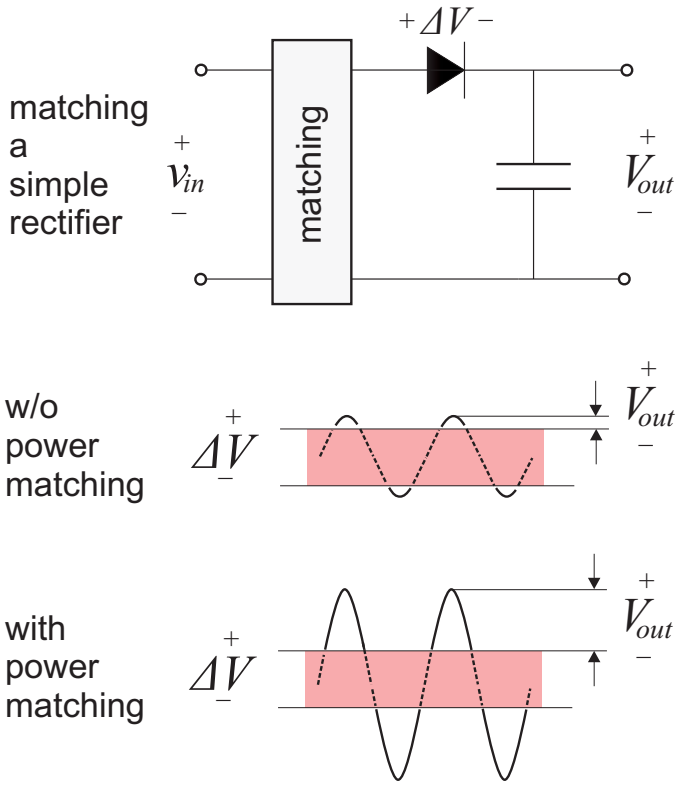

Figure 2.1: Impedance transformation network ensures maximum transfer of power by creating passive voltage gain.

voltage across the antenna. It was shown in [31] that to boost the power efficiency of the voltage multiplier, the amplitude of the voltage from antenna must be maximized. The dimension and type of the antenna of passive wireless microsystems determine the radiation resistance and the induced voltage of the antenna. The finite antenna dimension of passive wireless microsystems limits the voltage provided by the antenna. To improve the efficiency of power harvester a matching or impedance transformation network is inserted between the antenna and the rectifier/voltage multiplier, as shown in Fig.[2.1].

An impedance transformation network converts the input impedance of the voltage multiplier to the matching impedance of the antenna to ensure maximum power transfer to the voltage multiplier. In [68], a shunt inductor power-matching network between the antenna and voltage multiplier was employed, as shown in Fig.[2.3](a),

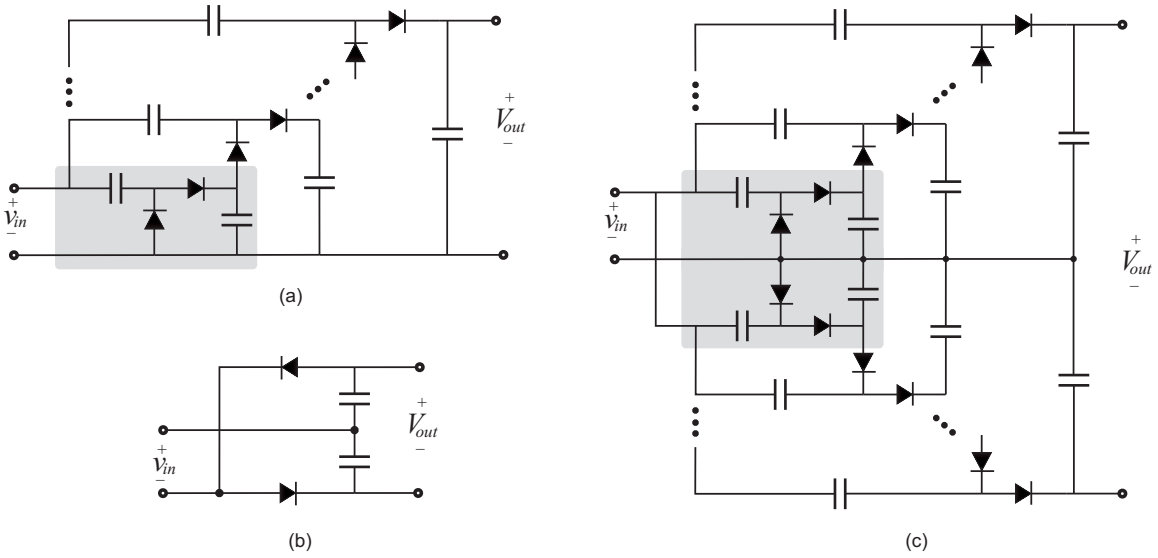

Figure 2.2: Dickson charge-pump [16] and Nakamoto's dual half-wave rectifier [17] widely used for RF signal rectification and voltage boost in transponders

to resonate out the capacitive part of the input impedance of the voltage multiplier. No attempt, however, was made to match the real part of the input impedance of the multiplier to the radiation resistance of the antenna, leaving the task of power-matching entirely to the voltage multiplier. De Vita and Iannaccone proposed a LC power-matching network, shown in Fig.[2.3](b), that consists of one floating inductor, a shunt capacitor, and a grounded inductor [19]. The grounded inductor is used to resonate out the input capacitance of the downstream voltage multiplier while the LC network provides the matching impedance and voltage gain. The LC power-matching network used by Shameli *et al.* consists of a grounded inductor and a floating capacitor [13]. When used with a 2-stage voltage multiplier made of low-threshold native devices, a 1 V dc output voltage was achieved at design frequency 920 MHz with -14.1 dBm input power and 500 KΩ output load. Fig.2.3 shows some of the popular topology matching networks. Fig.[2.3](a), (b) and (c) are widely used in transponders while Fig.[2.3](d) is proposed in this paper for on-chip RF power matching in transponders.

This thesis proposes an RF power harvesting circuit which uses on-chip transformers for power matching. The transformer is shown to provide significantly more voltage

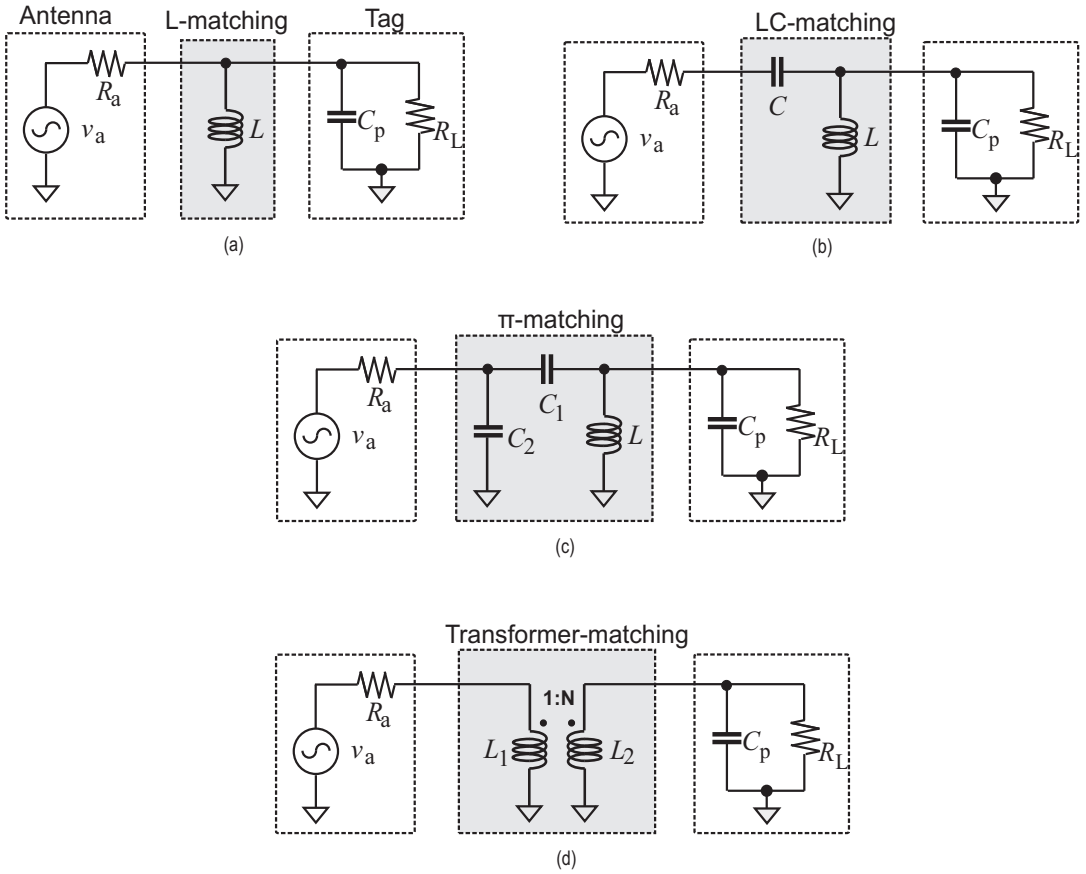

Figure 2.3: (a), (b) and (c): Matching network topologies for RF power harvesting used in [12, 13] and [14] respectively. (d) Transformer power matching circuit proposed in this thesis.

gain and RF sensitivity than an LC matching circuit similar to the used in [13]. The proposed power harvester is shown, in 3, to have similar performance to the design developed using non-standard features such as Silicon-on-insulator or low-V_T devices. Fig.[2.4](a) is the 3D illustration of the matching network used in [13], and Fig.[2.4](b) is the matching network proposed in this thesis.

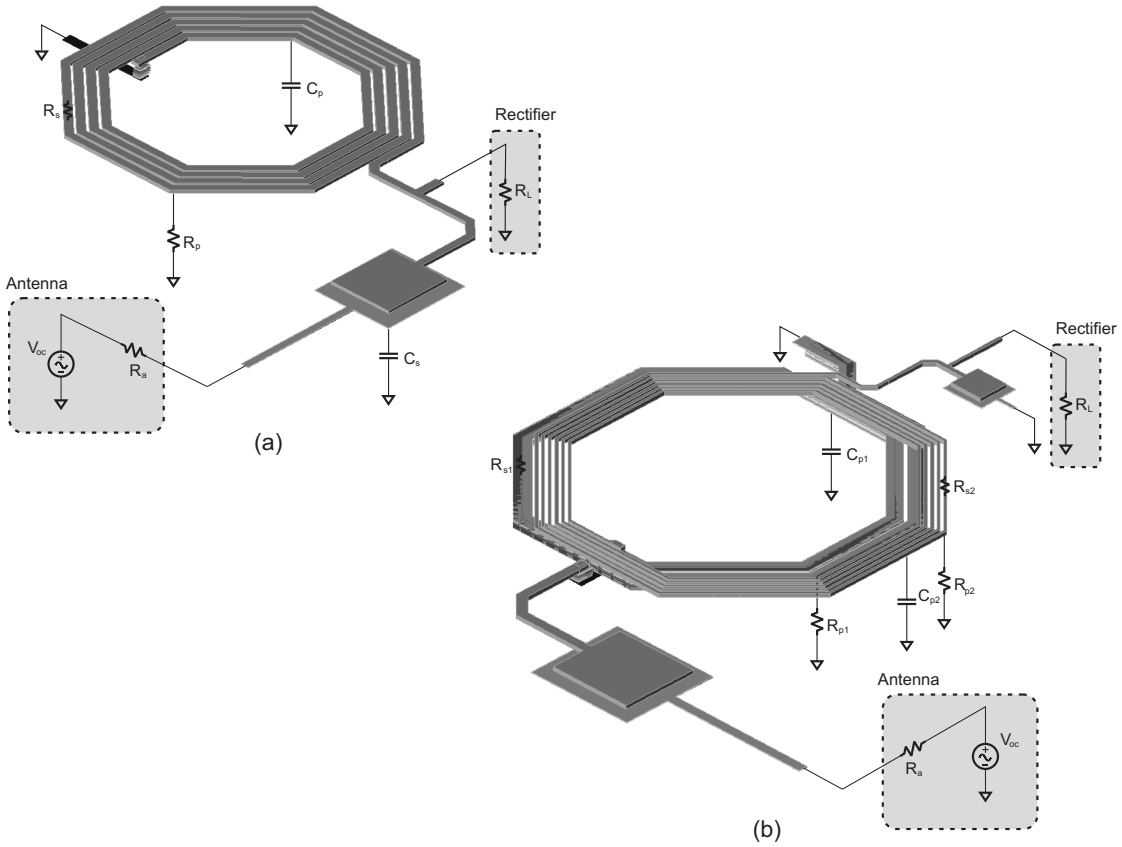

Figure 2.4: (a) RF power harvester proposed by [12, 13]. (b) Transformer power matching circuit proposed in this thesis.

2.2 Current Trends in Frequency Calibration

The local oscillator of a passive wireless transponder provides the clock signal for its baseband units and determines the data rate of the backscattered signals sent by the transponder to its base station [16, 12]. In addition, it creates sub-carriers for backscatter modulation, lowering the interference of the carrier at the base station [18]. Arising from process variation, supply voltage fluctuation, and temperature drift (PVT), the local oscillator of the transponder exhibits a high level of uncertainty in its oscillation frequency [20]. Although the effect of supply voltage fluctuation and temperature variation can be compensated using compensation circuitry [36, 37], their effectiveness is largely hindered by the limited power resources

of passive wireless transponders. An alternative solution is to use an external calibrating signal sent by the base station to the transponder to adjust the oscillation frequency of the local oscillator of the transponder. Frequency calibration must be carried out frequently such that the drift of the frequency of the local oscillator is within the required tolerance. One approach to remotely calibrate the oscillation frequency of the local oscillator of transponders is to estimate the oscillator frequency of the local oscillator using a timing signal provided by the base station and adjust the frequency of the local oscillator using a digital timing feedback loop as shown in Fig.[2.5]. This approach was used by Tran and Lee in [70] where a 9-bit counter was used to estimate the period of the local oscillator. The estimate is then used to adjust the content of an 8-bit successive approximation register whose binary value scales the oscillation frequency. It was demonstrated that this technique can reduce the center frequency error to 0.4% after 8 calibration cycles. This approach, however, requires a long calibration time and complex logic circuitry.

Another method of calibration the frequency of the local oscillator is injection-locking the oscillator using a signal received from the reader. This method was employed in the transponder developed in [57] where the 900MHz carrier of the reader was used to injection lock the on-chip LC oscillator of the transponder operating at 450MHz. An in-depth study of injection-locking as a way of remotely calibrating the frequency of the oscillator of passive wireless transponders is presented in this thesis. Injection locking of harmonic oscillators has been studied extensively using both linear models [21, 22] and nonlinear models [42, 43, 44, 45, 46]. Chang *et al.* further showed that the injection of a low-frequency feedback signal obtained from the output of a harmonic VCO under injection to the control signal of the VCO increases the lock range and lowers the phase noise of the VCO [47, 48, 49, 50]. The analysis of the injection locking of harmonic oscillators is greatly simplified considering the bandpass characteristics of the LC tank of these oscillators. The injection locking of non-harmonic oscillators (ring oscillators and relaxation oscillators) is more complex due to the existence of multiple frequencies and has received less attention. Betancourt-Zamora *et al.* investigated injection-locked ring oscillator prescalers [51] by assuming that the low-pass filtering formed by the output resistance of each stage and the input capacitance of the following stage sufficiently

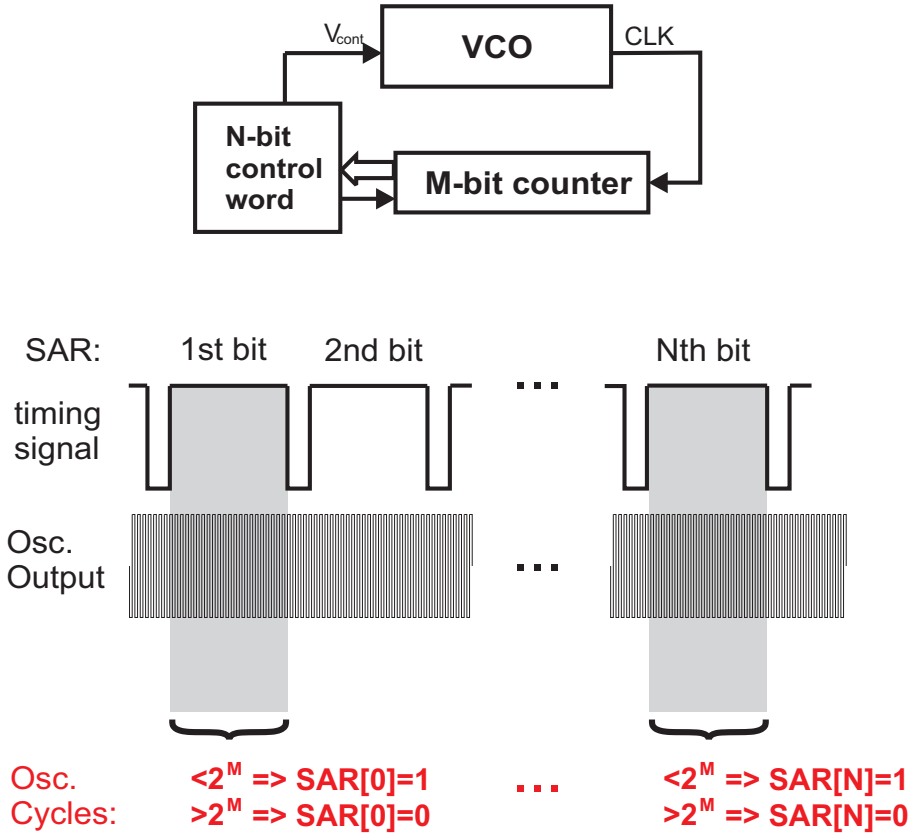

Figure 2.5: The "Digital Timing Feedback Loop" frequency calibration system used in [70]

suppress the frequency components higher than the frequency of the oscillator. Kinget *et al.* proposed precision quadrature generation using an injection-locked ring oscillator [52]. In [53], a differential-mode tail injection scheme with shunt inductance resonance was proposed for ring oscillators to achieve a wide frequency range. A phasor-domain treatment of the injection locking of ring oscillators was given in [54]. The time-domain analysis of the injection locking of ring oscillators was also conducted by Gangisani and Kinget [55, 56].

To extend the capabilities of injection-locking in calibrating the frequency of local oscillator, this thesis proposes the use of an external integrating feedback. This block, as shown in Fig.[2.6](b) accumulates the frequency variations caused by the

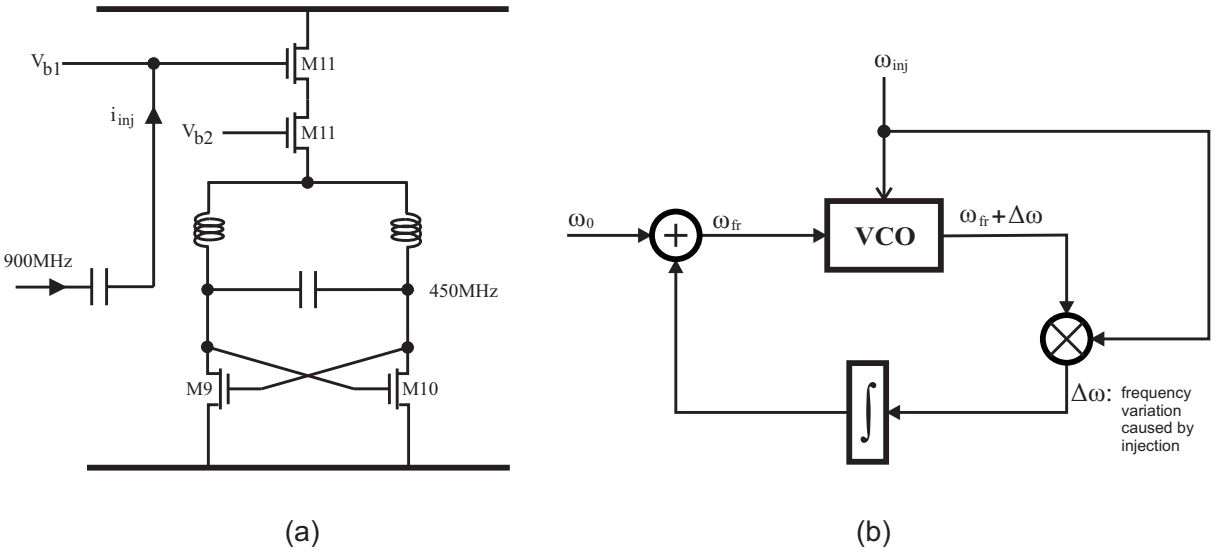

Figure 2.6: The "Digital Timing Feedback Loop" frequency calibration system used in [70]

injection of the reference signal. This value is then used to adjust the intrinsic frequency of the local oscillator. The steady state output frequency of the system shown in Fig.[2.6](a) is equal to the frequency of the injected signal. Also, the intrinsic (free-running) frequency of the oscillator is also equal to the injected frequency which means that the frequency of the calibrated oscillator stays at the desired value even if the injection source in removed.

2.3 Chapter Summary

A state-of-the-art review of RF power harvester and remote clock frequency calibration in passive transponders was presented. In power harvesting, while most of the current designs use the Dickson charge-pump for rectification and voltage boosting, depending on the characteristics of the antenna, they use different matching networks configuration to resonate out the capacitive component of the multiplier impedance, create voltage gain, or both. In frequency calibration systems, the dig-

ital timing feedback loop was noted as the most widely used method of frequency calibration. Injection locking is another method of frequency calibration which will be studied in thesis.

Chapter 3

Radio Frequency Power Harvesting in Passive Wireless Microsensors[1]

3.1 Introduction

Passive wireless microsystems harvest their power from radio-frequency waves emitted from base stations located in the proximity. The efficiency of power harvest determines the maximum distance over which reliable links between base stations and microsystems can be established and the complexity subsequently the functionalities of the microsystems. Power harvesting efficiency is determined by the efficiency of the matching network as well as that of the voltage multiplier. The efficiency of the voltage multiplier, to a great extent, depend on the peak amplitude of the RF signal at the input such that the conversion efficieny becomes very small if the input swing is close to the voltage drop of the diodes. Therefore, a very effective method of increasing RF-DC conversion efficiency is increasing the amplitude of the RF Signal by increasing the voltage gain of the matching network.

[1]The preliminary results of the research regarding radio frequency power harvesting has been published in IEEE conference proceedings [26, 27, 28] and the Elsvier Microelectronics journal [29]. More comprehensive research results on this subject was published in the IEEE Transactions on Circuits and Systems I - Fundamental Theory and Applications [30].

The voltage gain of LC-based power-matching approaches is limited by the low quality of spiral inductors in standard CMOS technologies. In this chapter, we propose a step-up transformer power-matching and gain-boosting technique to provide a matching impedance to the antenna and at the same time a large voltage gain such that both the power transfer from the antenna to the voltage multiplier and the power efficiency of the downstream voltage multiplier are maximized. Utilizing the unique characteristics of the low voltage and large current of the primary winding and the high voltage and low current of the secondary winding of step-up transformers, both the series and shunt losses of the transformer power-matching network are minimized simultaneously by using multiple metal layers connected using vias for the primary winding and by reducing the width of the spiral of the secondary winding. The reduction of the spiral width of the secondary winding accommodates more turns of the secondary winding in the area specified by the primary winding such that the turn ratio of the transformer subsequently the voltage of the secondary winding can be maximized. The paper is organized as the follows : Section 3.2 investigates power-matching and gain-boosting using LC networks. Design principles and constraints are developed. Section 3.3 presents the proposed step-up transformer power-matching and gain-boosting technique. A detailed analysis of the proposed approach is provided. Frequency tuning mechanisms are investigated in Section 3.4. Section 4.6 presents the measurement results of the proposed power-matching network, together with the measurement results of a LC power-matching network for comparison. Both were implemented in TSMC-0.18μm 1.8V 6-metal CMOS technology with thick metal options. The chapter is summarized in Section 3.6.

3.2 LC Matching Network

Power-matching and gain-boosting can be achieved simultaneously by inserting a passive impedance transformation network consisting of a spiral inductor and a metal-insulator-metal (MIM) capacitor between the antenna and the multiplier, as shown in Fig.3.1 [13]. The functionality of the impedance transformation network is two-fold : to provide a matching impedance to the antenna in order to max-

imize the power transmission from the antenna to the voltage multiplier at the carrier frequency, and to resonate at the carrier frequency such that the voltage at the output of the impedance transformation network is maximized. Because spiral inductors suffer from both resistive and capacitive losses, power matching, power efficiency, and voltage gain of the impedance transformation network must be considered equally.

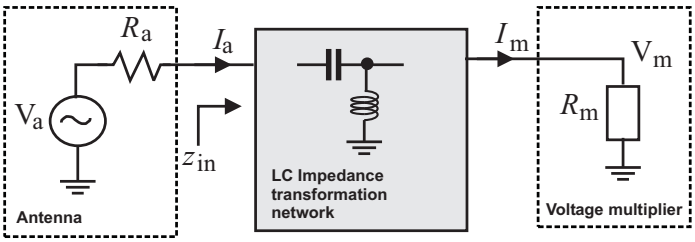

Figure 3.1: Impedance transformation network for power matching and gain boosting.

3.2.1 Power Matching

To maximize the power transfer from the antenna to the multiplier, the impedance transformation network in Fig.3.1 must be designed in such a way that $z_{in} = R_a$. Fig.3.2 shows a simplified schematic of a power-matching gain-boosting network using a shunt spiral inductor and a series MIM capacitor. To simplify analysis, the MIM capacitor is assumed to be ideal and is represented by an ideal capacitor C. The spiral inductor is modeled using the RLC network with R_s and R_p the series and shunt parasitic resistances and C_p the parasitic shunt capacitance. The multiplier is modeled used resistor R_m in parallel with capacitor C_m.

To facilitate analysis, the series $R_s \sim L$ network of the inductor is replaced with the equivalent parallel $R'_s \sim L'$ network shown in Fig.3.2 with

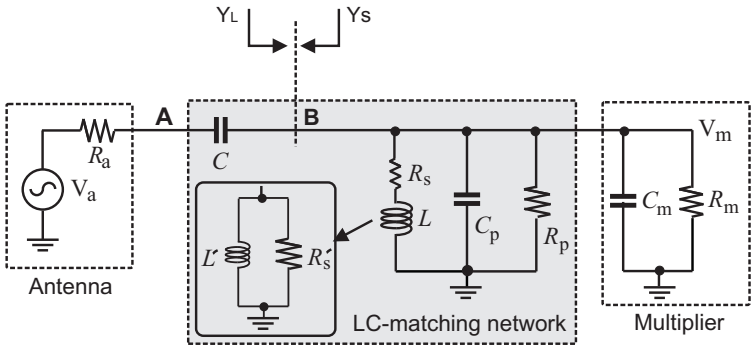

Figure 3.2: Power-matching and gain-boosting network using a shunt spiral inductor and a series MIM capacitor.

$$L' = L\left[1 + \left(\frac{R_s}{\omega L}\right)^2\right],$$
$$R'_s = R_s\left[1 + \left(\frac{\omega L}{R_s}\right)^2\right] \tag{3.1}$$

For practical spiral inductors, $\omega L \gg R_s$ holds. As a result, $L' \approx L$. It can be shown that the matching condition for the maximum power transfer at node A can be shifted to node B. Moving the impedance matching from node A to node B greatly simplifies analysis. Because

$$Y_L = \frac{1}{R_L} + \frac{1}{R_p} + \frac{1}{R'_s} + j\left[\omega\left(C_P + C_L\right) - \frac{1}{\omega L}\right],$$
$$Y_s = \frac{1}{R_a + \frac{1}{j\omega C}} = \frac{\omega^2 C^2 R_a + j\omega C[1 + \omega^2 R_a^2 C]}{1 + \omega^2 R_a^2 C^2}, \tag{3.2}$$

from matching condition $Y_L = Y_s^*$, we have

$$Q = \sqrt{\frac{R_e}{R_a} - 1}, \tag{3.3}$$

and

$$\omega_o \approx \frac{\omega_n}{\sqrt{1+\frac{C'_p}{C}}}, \tag{3.4}$$

where

$$R_e = R'_s||R_p||R_m \tag{3.5}$$

is the *effective load*, $C'_p = C_m + C_p$ is the total shunt capacitance,

$$Q = \frac{1}{\omega R_a C} \tag{3.6}$$

is the quality factor of $R_a \sim C$ network, and

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{3.7}$$

is the resonance frequency of the impedance transformation network when its parasitics are not accounted for. Note that $Q^2 \gg 1$ was utilized in derivation of (3.4). Fig.3.3 shows the simplified schematic of the LC power-matching and gain-boosting network.

3.2.2 Power Efficiency

The impedance transformation network is lossy due to the power dissipation of R'_s and R_p. To maximize the amount of power transferred from the antenna to the multiplier, the power loss of the impedance transformation network should be

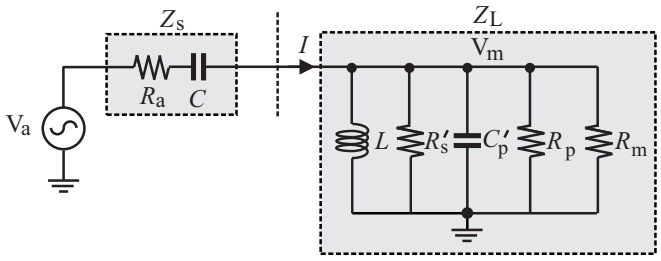

Figure 3.3: Simplified schematic of LC-based power-matching and gain-boosting network.

minimized. The power efficiency of the impedance transformation network defined as the ratio of the power delivered to the multiplier, denoted by P_m, to the power available at the input of the impedance transformation network, denoted by P_{in}, i.e

$$\eta = \left.\frac{P_m}{P_{in}}\right|_{z_{in}=R_a} \tag{3.8}$$

must therefore be maximized [19]. Since $\omega L \gg R_s$ holds for spiral inductors, we have from (3.1) $R_s' \approx \frac{(\omega L)^2}{R_s}$. Further from (3.4) and (3.7), we have $(\omega L)^2 = \frac{1}{\omega^2 (C + C_p')^2}$. As a result,

$$R_s' = \frac{1}{R_s \omega^2 (C + C_p')^2}. \tag{3.9}$$

Utilizing (3.3), (3.6), and noting $Q \gg 1$, we have

$$\frac{1}{\omega R_a C} \approx \sqrt{\frac{R_e}{R_a}}. \tag{3.10}$$

Making use of (3.10), we can write (3.9) as

$$R'_s = \left[\frac{R_a}{R_s}\left(\frac{C}{C+C'_p}\right) - 1\right](R_m||R_p). \tag{3.11}$$

It is seen from (3.11) that C'_p lowers R'_s. This is echoed with an increase in the ohmic loss of the inductor. The power efficiency of the impedance transformation network is obtained by

$$\eta = \frac{P_m}{P_{in}} = \frac{\frac{V_m^2}{R_m}}{\frac{V_m^2}{R_e}} = \frac{R_e}{R_m}. \tag{3.12}$$

Since

$$\frac{1}{R_e} = \frac{1}{R'_s} + \frac{1}{R_p} + \frac{1}{R_m}, \tag{3.13}$$

making use of (3.11), we can write (3.13) as

$$\frac{1}{R_e} = \left(\frac{1}{R_p} + \frac{1}{R_m}\right)\frac{\frac{R_a}{R_s}\left(\frac{C}{C+C'_p}\right)^2}{\frac{R_a}{R_s}\left(\frac{C}{C+C'_p}\right)^2 - 1}. \tag{3.14}$$

Substituting (3.14) into (3.12) yields

$$\eta = \frac{1 - \frac{R_s}{R_a}\left(1 + \frac{C'_p}{C}\right)}{1 + \frac{R_m}{R_p}}. \tag{3.15}$$

Since $\frac{R_m}{R_p} \ll 1$ typically holds, making use of $\frac{1}{1+x} \approx 1-x$ when $|x| \ll 1$, we can write (3.15) as

$$\eta \approx 1 - \frac{R_s}{R_a}\left(1 + \frac{C_p'}{C}\right) - \frac{R_m}{R_p}. \tag{3.16}$$

It is evident from (3.16) that the power efficiency of the impedance transformation network is less than 100% due to the non-zero parasitic series resistance R_s, the finite parasitic shunt resistance R_p, and the shunt capacitance C_p'. To improve η, R_s and C_p' should be minimized while R_p should be maximized. In other words, the shunt-peaking spiral inductor should be as ideal as possible.

3.2.3 Voltage Gain

As pointed out earlier, the overall power efficiency of the power harvester can be improved if a large voltage gain can be provided by the impedance transformation network. Consider Fig.3.3. The power delivered to the multiplier is computed from

$$P_m = \frac{V_m^2}{R_e} = \frac{A_v^2 V_a^2}{R_e}, \tag{3.17}$$

where $A_v = \frac{V_m}{V_a}$ is the voltage gain of the impedance transformation network. The maximum power delivered to the multiplier is given by

$$P_{m,max} = \frac{V_a^2}{4R_a}. \tag{3.18}$$

Equating (3.17) and (3.18) yields the optimal voltage gain of the impedance transformation network at which the maximum power transfer takes place

$$A_v = \frac{1}{2}\sqrt{\frac{R_e}{R_a}}. \tag{3.19}$$

Substituting (3.5) and (3.11) into (3.19), we arrive at

$$A_v = \frac{1}{2}\sqrt{\frac{R_p||R_m}{R_a}\left[1 - \frac{R_s}{R_a}\left(1 + \frac{C'_p}{C}\right)\right]}. \tag{3.20}$$

We comment on the preceding development : (i) If $R_m > R_p$, $R_p||R_m$ will be dominated by R_p. Boosting R_m beyond R_p will no longer improve $R_p||R_m$ subsequently the voltage gain. (ii) To improve the voltage gain, R_s must be made much smaller than R_a. (iii) Parasitic shunt capacitances of the spiral inductor C'_p increases the effect of conductive loss by a factor of $\left(1 + \frac{C'_p}{C}\right)$. To minimize its effect, $C'_p \ll C$ is desirable.

3.2.4 Numerical Results

The shunt peaking inductor is implemented using M6 of TSMC-0.18μm 6-metal CMOS technology with thick metal options. The physical dimensions of the transformer, such as the thickness of the spiral, the dielectric constant of the substrate, and the distance between the spiral and substrate, are provided by TSMC. The spiral inductor is characterized using Advanced Design Systems from HP. A netlist corresponding to the geometry and operation frequency of the transformer is generated. It is then imported to Spectre from Cadence Design Systems to complete simulation with other IC components included. Fig.3.4 shows the dependence of the series and shunt resistive losses of a 5-turn inductor on the width of the spiral at different frequencies. It is seen that increasing the spiral width reduces the series resistance. This effect is more prominent at low frequencies where skin effect can be neglected. Resistance reduction diminishes at high frequencies where skin effect becomes dominant and the effective series resistance is determined by the skin depth rather than the physical dimensions of the cross section of the spiral.

Increasing the spiral width increases the parallel resistance directly. R_p, however, is much smaller as compared with R_s. The effect of the spiral width on the inductance of the inductor is shown in Fig.3.5. As observed narrow spirals exhibit a large inductance. This observation reveals that the self-inductance of the secondary winding of a step-up transformer can be effectively increased by reducing the width of the spirals of the secondary winding. This also allows us to accommodate more turns for a given silicon space. More importantly, the reduction of the width of the spirals of the secondary winding has a minor impact on the series resistance of the spiral at high frequencies, as observed a moment ago. We will further explore this and their applications in details in Section 3.3. Fig.3.6 shows the dependence of the parasitic capacitances of spirals on the width of the spiral. It is seen that the parasitic capacitances are less sensitive to the width of the spirals.

3.3 Transformer Matching Network

It is well understood that the magnetic energy stored in the core of an inductor is related to the amount of current multiplied by the number of turns. An inductor with a higher number of turns can extract core energy with less current. Step-up transformers are characterized by a small voltage and a large current in the primary winding and a large voltage and a small current in the secondary winding. The current and voltage of the primary winding and those of the secondary winding of a lossless step-up transformer relate to each other

$$\frac{I_1}{I_2} = \frac{n_2}{n_1}, \qquad \frac{V_1}{V_2} = \frac{n_1}{n_2}, \tag{3.21}$$

I_1, I_2 and V_1, V_2 are the current and voltage of the primary winding and secondary winding, respectively, n_1 and n_2 are the turns of the primary winding and that of the secondary winding, respectively. With $n_2 > n_1$, we have $I_2 < I_1$ and $V_2 > V_1$. By employing a step-up transformer, the same power can be delivered from the primary winding to the secondary winding with a higher voltage at the secondary winding.

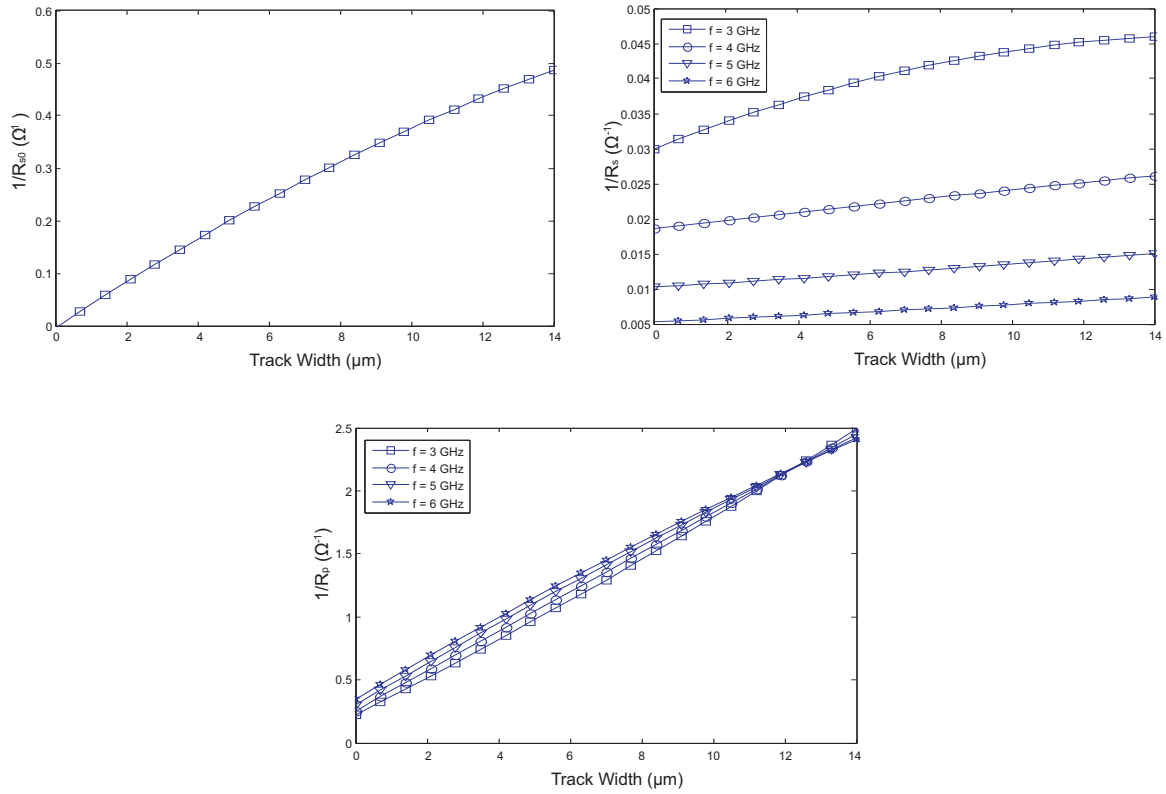

Figure 3.4: Simulated dependence of the series and shunt resistive losses of a 5-turn octagonal inductor implemented in M6 of TSMC-0.18μm CMOS technology. The average imension of the inductor, i.e. $(d_{in} + d_{out})/2$, where d_{in} and d_{out} are the inner and outer diameters of the inductor, respectively, is 200 μm. (a) Series conductance at low frequencies. (b) Series conductance at high frequencies, and (c) Parallel conductance at high frequencies.

Fig.3.7 shows the configuration of power-matching and gain-boosting using a step-up transformer. The secondary winding is implemented using M6, the top thick metal layer offered by TSMC-0.18μm 6-metal CMOS technology. The primary winding is implemented using three metal layers M3-M5 connected using vias to minimize its series resistance. Fig.3.8 shows the equivalent circuit of power harvest using a step-up transformer. The transformer is represented using its narrow-band model [32, 33]. Capacitors C_1 and C_2 are used to resonate out the self-inductance of the primary winding and that of the secondary winding.

Because the voltage of the primary winding is small, the resonance of the primary

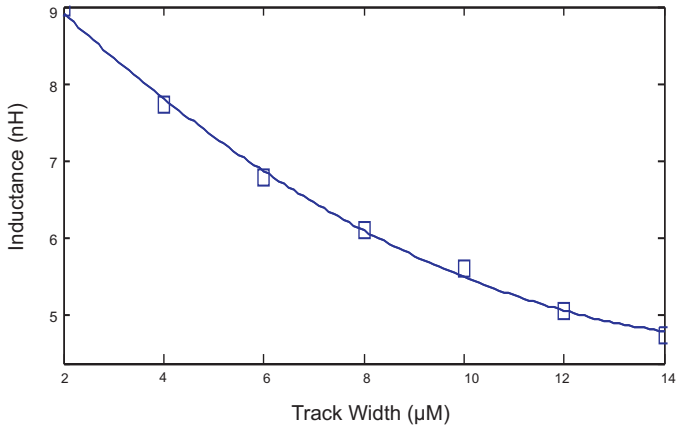

Figure 3.5: Simulated effect of spiral width on the inductance of a 5-turn octagonal inductor implemented in M6 of TSMC-0.18μm CMOS technology.

winding only creates a small voltage gain. The large current of the primary winding demands that the cross-section of the spiral of the primary winding be large. This is achieved by using multiple metal layers connected using vias for the primary winding. Further, since the primary winding has a fewer turns, its spiral is implemented using lower metal layers without encountering a significant substrate loss. The resonance at the secondary winding, on the other hand, is significant due to its large self-inductance needed to produce a large voltage gain. To analyze the voltage gain obtained from the resonance of the secondary winding, we follow the approach used for analysis of power harvest using LC matching networks in Section 3.2, specifically L_2 is separated from the rest of the transformer, as shown in Fig.3.9. A Thevenin equivalent circuit is used to represent the overall effect of the matching network excluding L_2 and C_2. To further simplify analysis, we use $C_2' = C_2 + C_{p2} + C_m$ and $R_2' = R_{p2}||R_m$ to account for all shunt capacitances and shunt resistances, respectively. Note that the simplified circuit has the same topology as that of Fig.3.3. The approach used for analysis of Fig.3.3 can thus be followed to analyze Fig.3.9.

Thevenin voltage V_T is obtained by open-circuiting the secondary winding and deriving the voltage across the series resistance R_{s2} and mutual inductance M due to V_a with L_1 and C_1 resonated out, i.e. $j\omega L_1 + \dfrac{1}{j\omega C} = 0$

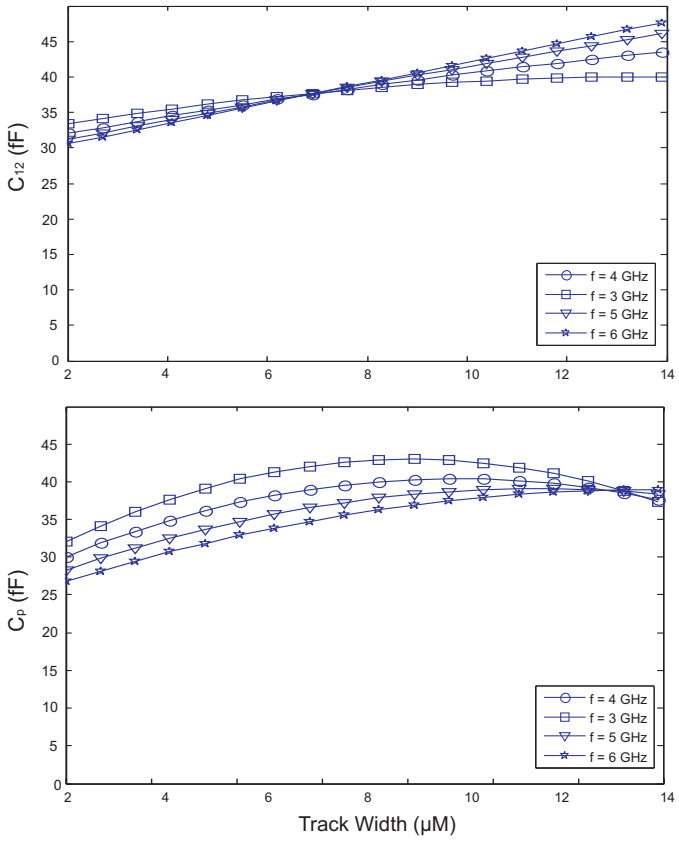

Figure 3.6: Simulated dependence of the capacitive losses of a 5-turn octagonal inductor implemented in M6 of TSMC-0.18μm CMOS technology. The average dimension of the inductor, i.e. $(d_{in} + d_{out})/2$, where d_{in} and d_{out} are the inner and outer diameters of the inductor, respectively, is 200 μm. (a) Overlapping capacitance between spirals. (b) Spiral-to-substrate capacitance.

$$V_T = \frac{j\omega M}{R_a + R_{s1}} V_a, \tag{3.22}$$

where $M = K\sqrt{L_1 L_2}$ is the mutual inductance and K the coupling coefficient. Thevenin impedance is obtained by short-circuiting V_a and applying a test voltage source over R_{s2} and M with L_1 and C_1 resonated out

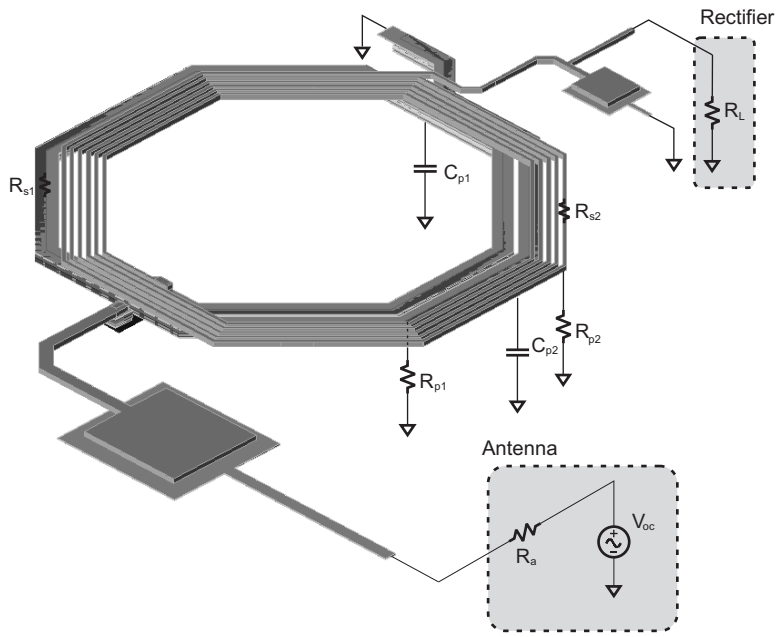

Figure 3.7: Configuration of step-up transformer power-matching and gain-boosting network.

$$Z_T = R_{s2} + \frac{(\omega M)^2}{R_a + R_{s1}}. \tag{3.23}$$

It is seen from (3.23) that Thevenin impedance is purely resistive. Also, it has two components: the series resistance of the secondary winding and the resistance of the primary winding referred to the secondary winding.

To find out the voltage gain from V_T to V_m, we notice that for the maximum power transfer, $Z'_L = (Z'_s)^*$ is required where $Z'_L = R'_2 || \frac{1}{j\omega C'_2}$ and $Z'_s = Z_T + j\omega L_2$. The voltage gain is obtained from

$$\left|\frac{V_m}{V_T}\right| = \left|\frac{Z'_L}{Z'_L + Z'_s}\right| = \frac{1}{2}\sqrt{1 + \left(\frac{\omega L_2}{Z_T}\right)^2}. \tag{3.24}$$

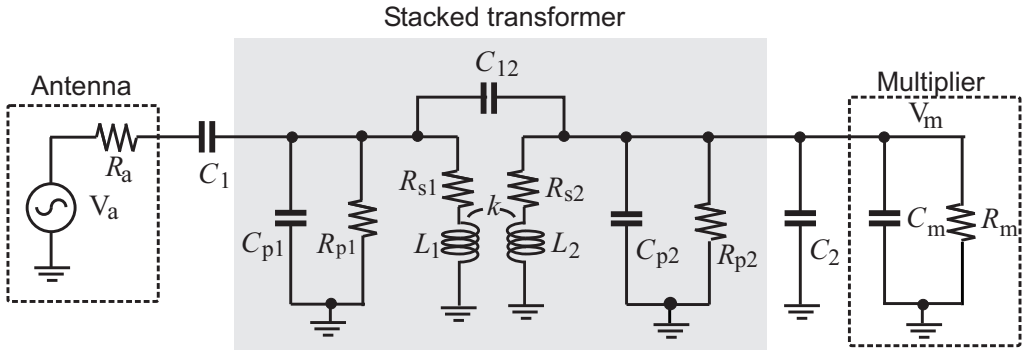

Figure 3.8: Equivalent circuit of step-up transformer power-matching and gain-boosting.

Substituting (3.23) into (3.24) yields

$$\left|\frac{V_m}{V_T}\right| = \frac{1}{2}\sqrt{1+\left[\frac{R_{s2}}{\omega L_2}+\frac{\omega^2 M^2}{\omega L_2(R_a+R_{s1})}\right]^{-2}}. \tag{3.25}$$

The self quality factor of the secondary winding $Q_2 = \dfrac{\omega L_2}{R_{s2}} \gg 1$ and $Q_1 = \dfrac{\omega L_1}{R_a + R_{s1}}$ is the equivalent self quality factor of the primary winding [34]. Eq.(3.25) becomes

$$\left|\frac{V_m}{V_T}\right| = \frac{1}{2}\sqrt{1+\left(\frac{Q_2}{k^2 Q_1 Q_2 + 1}\right)^2}, \tag{3.26}$$

It is seen from (3.26) that a large voltage gain of the step-up transformer matching network can be obtained by (i) boosting the mutual inductance M, (ii) lowering the series resistance of the primary winding, (iii) lowering the series resistance of the secondary winding, and (iv) increasing the self inductance of the secondary winding. There are two ways to increase M : increase the coupling coefficient or increase the turn ratio. The former can only be achieved by using stacked configuration while the latter requires more turns of the secondary winding. The series resistance of the primary winding can be lowered effectively by increasing the spiral width of the primary winding and by using multiple metal layers connected together using vias for the primary winding. The self-inductance of the secondary winding and

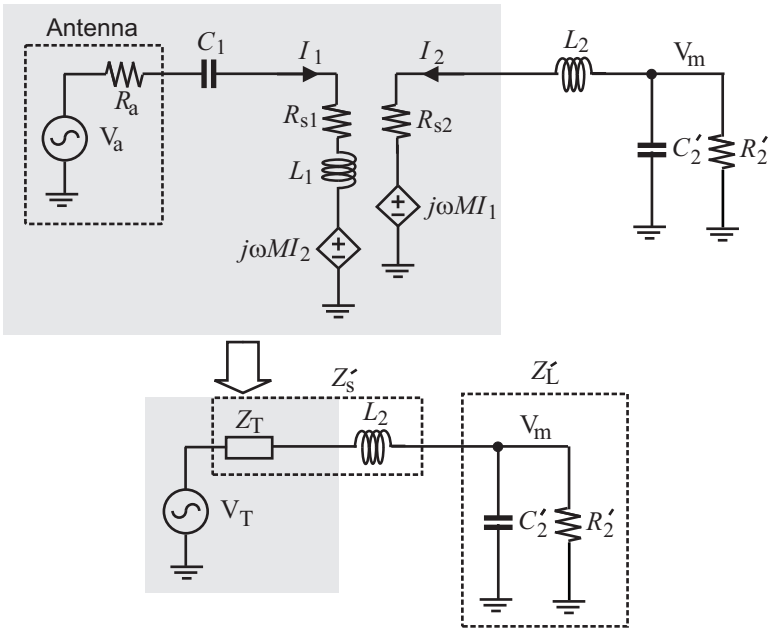

Figure 3.9: Thevenin equivalent circuit of step-up transformer power-matching and gain-boosting.

the coupling coefficient can be increased simultaneously by reducing the width of the spiral of the secondary winding. This, however, is at the cost of the increased series resistance of the secondary winding. Fortunately, the current of the secondary winding of the step-up transformer is small as compared with that of the primary winding, its winding loss is insignificant.

To find out the overall voltage gain, we make use of the Thevenin model of the secondary in Fig.[3.9]. Since this circuit to itself is an LC transformation network, we can use (3.19) to write the voltage gain from Z_T to Z_L

$$A_v = \frac{1}{2}\sqrt{\frac{R_2'}{Z_T}}. \tag{3.27}$$

Note that Z_T is purely resistive. Substituting R_2' and Z_T with their values, the overall voltage gain of the transformer matching network is obtained as

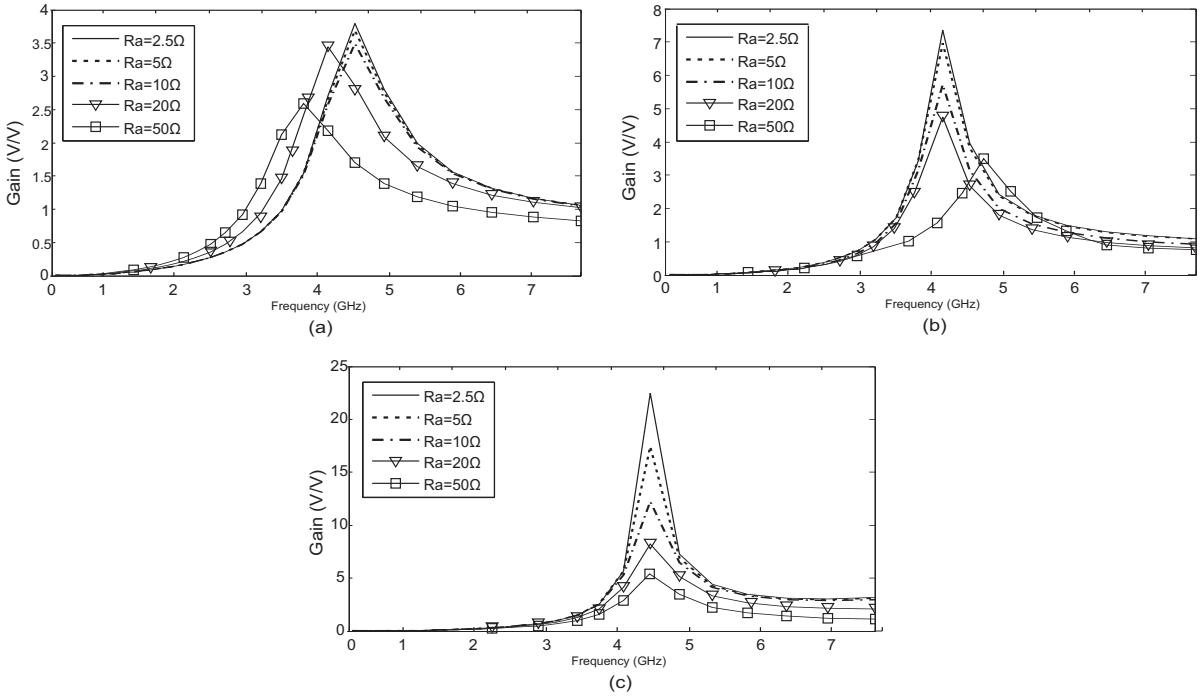

Figure 3.10: Simulated passive gain for different values of radiation resistance. (a) LC matching network (spiral width =5μm). (b) LC matching network reduced spiral width (spiral width =1.5μm). (c) Step-up transformer matching network (spiral width in primary winding : 5μm, spiral width in secondary winding : 1.5μm. The load resistance is fixed at $R_L = 40k\Omega$.

$$\begin{aligned} A_v &= \frac{1}{2}\left(\frac{\omega M}{R_a + R_{s1}}\right)\sqrt{\frac{R_2'}{Z_T}} \\ &= \frac{1}{2}\sqrt{\frac{R_m||R_{p2}}{\frac{R_{s2}}{A_{ind}^2} + R_a + R_{s1}}}. \end{aligned} \tag{3.28}$$

where

$$A_{ind} = \frac{\omega M I_1}{V_a} = \frac{\omega M}{R_a + R_{s1}} \tag{3.29}$$

is termed inductive gain which is the voltage gain from V_a to V_T. We comment on the preceding development : (i) The effect of the series resistance of the secondary winding is scaled down by A_{ind}^2. This finding is significant as it allows us to use more turns with reduced spiral width in the secondary winding to boost the voltage gain without encountering a large shunt loss. To increase A_{ind}, the mutual inductance of the transformer M must be increased and R_{s1} must be decreased. There are two ways to increase M: increase the coupling coefficient or increase the turn ratio. The former can be achieved by using stacked configurations while the latter requires more turns of the secondary winding. (ii) The series resistance of the primary winding R_{s1} is low due to the small number of turns and the use of multi-layer spirals connected using vias, the effect of series loss of the primary winding on the overall is negligible. (iii) Step-up transformer matching technique is particularly attractive for antennas with a low R_a. Since in (3.28) all terms except R_a are small, reducing R_a significantly increases A_v. Reducing the source impedance below $R_{s1} + \dfrac{R_{s2}}{A_{ind}^2}$ does not contribute further to the optimal voltage gain. (iv) When R_a is large, from (3.29) we know that A_{ind} will be small. In this case, a large voltage gain can be achieved by reducing the track width of the secondary. This is because reducing the track width will reduce the winding area and the shunt loss of the secondary winding [66]. The series loss of the secondary winding, however, is also increased, which will in turn lowers the overall voltage gain. It is seen from (3.28) that when R_a is significantly larger than $R_{s1}+\frac{R_{s2}}{A_{ind}^2}$, it will dominate the denominator of (3.28) such that an increase in R_{s2} will have a less impact on the overall voltage gain. Decreasing the track width of the secondary winding is beneficial to the overall gain when the radiation resistance is large. It should be noted that an additional gain obtained is due to the resonance of the secondary winding with C'_{p2} as quantified by (3.26).

Fig.3.10 demonstrates the capability of the transformer matching network in comparison with LC matching networks in matching antennas with radiation resistances between 2.5Ω and 50 Ω to a 40 KΩ load. As evident from the results, the proposed design offers a higher gain especially when the source impedance is small.

3.4 Frequency Tuning

Although the impedance transformation network should be designed in such a way that it resonates preciously at the carrier frequency, due to parameter spreading caused by process variations, the resonant frequency of fabricated impedance transformation networks deviates from the desired value. It is therefore highly desirable that the resonant frequency of impedance transformation networks be tunable. As shown in Fig.3.11(a), the resonant frequency of the LC impedance transformation network studied in Section 3.2 can be made tunable by placing a variable capacitor C_v in parallel with the voltage multiplier. Similarly, the resonant frequency of the transformer impedance transformation network can also be made tunable by replacing C_1 and C_2 in Fig.3.8 with variable capacitors C_{v1} and C_{v2}, as shown in Fig.3.11(b). Even though load can be matched at any tuned frequency, the quality of matching will deteriorate if the resonant frequency deviates far away from the desirable value.

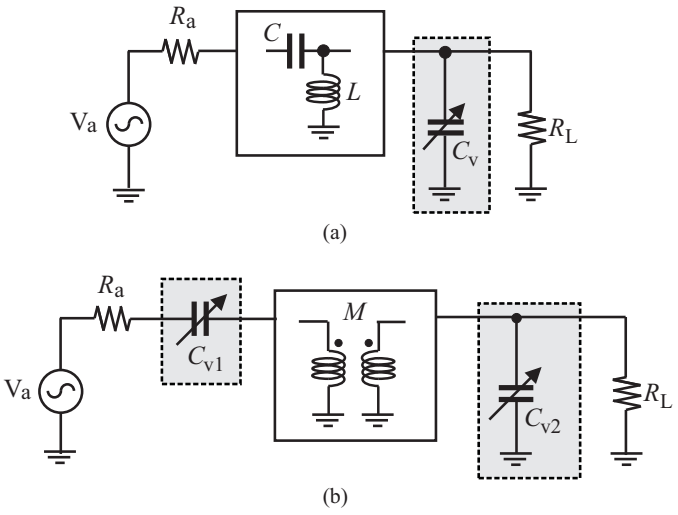

Figure 3.11: Frequency tuning in (a) LC impedance transformation network and (b) step-up transformer impedance transformation network.

3.4.1 Frequency Tuning of LC Impedance Transformation Network

Rewriting (3.4)

$$\omega_o \approx \frac{1}{\sqrt{L(C + C'_p)}}, \tag{3.30}$$

we observe that both C and C'_p can be used to tune the resonant frequency of the LC impedance transformation network. Since the quality factor of the matching network Q is inversely proportional to C. When $Q^2 \gg 1$, the voltage gain of the network can be written as $A_v \approx \frac{Q}{2}$ [35]. Thus, varying C will affect the voltage gain of the impedance transformation network. This is clearly undesirable. On the other hand, it is observed from (3.20) that the dependence of the voltage gain on the shunt capacitance C'_p in Fig.3.3 is governed by a much weaker function. This observation reveals that the variable capacitor to tune the resonant frequency of the LC impedance transformation network should be placed in parallel with C'_p, as shown in Fig.3.11(a).

3.4.2 Frequency Tuning of Transformer Impedance Transformation Network

To tune the resonant frequency of the transformer impedance transformation network of Fig.3.11(b), both capacitors C_{v1} and C_{v2} have to be adjusted. Lowering the resonant frequency using capacitors will result in a gain roll-off. As pointed out in Section 3.3, a key advantage of using a transformer instead of an inductor for matching is the reduction of the effect of the series resistive loss of the secondary winding, as described by (3.28). By reducing the resonant frequency using capacitors, the mutual inductance M will remain unchanged while the circuit operates at a lower frequency. This will result in a reduction in A_{ind}, as expected from (3.29). In other words, by tuning down the frequency using additional capacitors, the transformer matching network will perform more like an LC matching network.

Fig.3.12(a) shows the gain roll-off caused by tuning down the resonant frequency of the step-up transformer. Fig.3.12(b) shows the dependence of the resonant frequency and voltage gain on C_{v2}. As can be seen that the voltage gain drops from 5.0 at 3.7 GHz to 4.35 at 2 GHz.

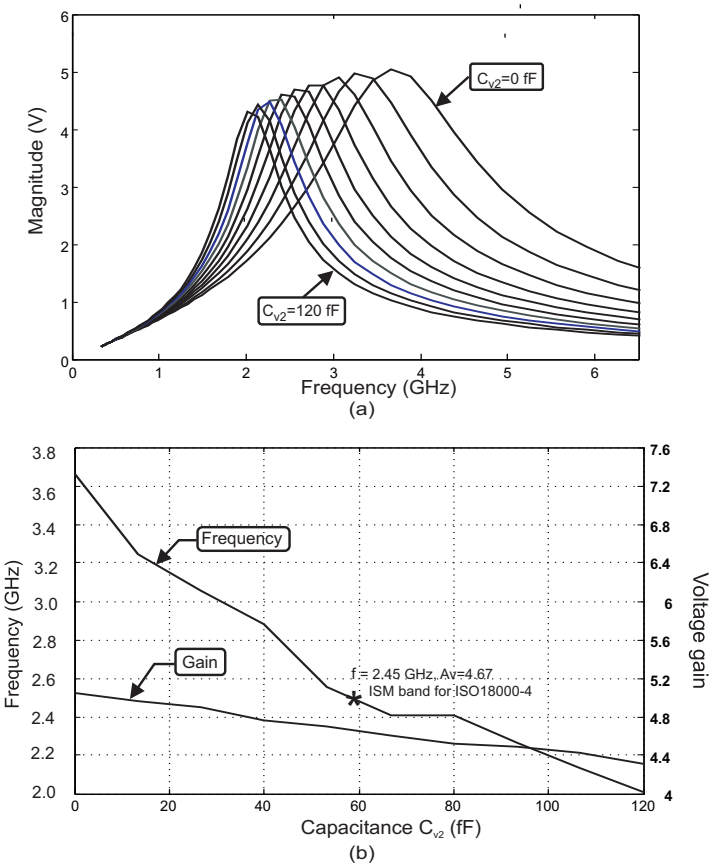

Figure 3.12: (a) Simulated dependence of the voltage gain of transformer impedance transformation network on C_{v2} and C_{v1}. (b) Simulated dependence of resonant frequency and voltage gain of transformer impedance transformation network on C_{v2}. note that C_{v1} is also varied with C_{v2} to maintain that the resonant condition is on the primary side.

3.5 Measurement Results

The proposed step-up transformer impedance matching and gain boosting network has been designed in TSMC-0.18μm 1.8V 6-metal CMOS technology with thick

metal options. The primary winding has 1.5 turns and is implemented using metal layers 3 to 5 with identical thickness of 1 μm connected using vias to minimize the winding resistance. The secondary winding has 5.5 turns and is implemented using the top metal layer (M6, thick metal layer with thickness 2.3 μm). The width of the spiral in the primary winding is 8 μm and that in the secondary winding is 1.5 μm. For the purpose of comparison, a LC matching network with the same loading condition has also been implemented on the same chip. The inductor of the LC matching network has 4.5 turns spiral implemented using M6 of width 5 μm. Fig.3.13 is the micro-photo of the fabricated chip. On-wafer probing is conducted using a Cascade Microtech RF-1 probe station with four MH5 positioners, RF and DC probes.

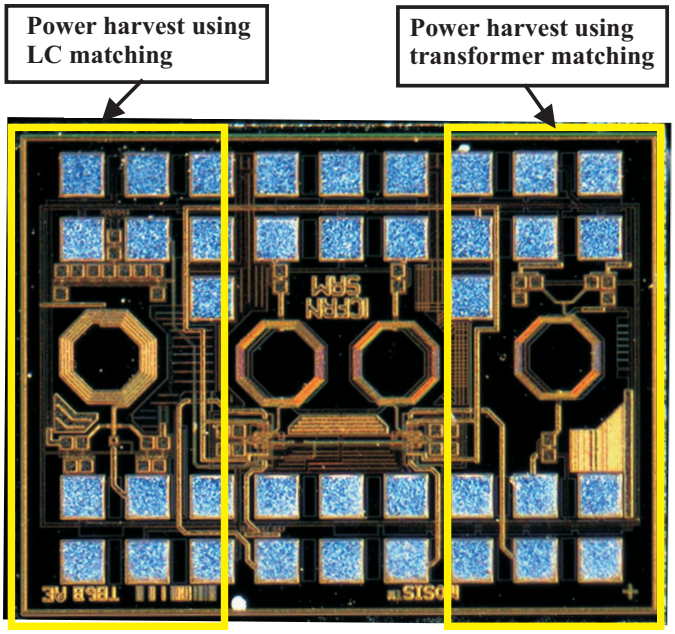

Figure 3.13: Microphoto of fabricated chip. Bonding pads are arranged in accordance with the configuration of available probes available.

Since the design is to be tested using off-chip RF source, the choice of source impedance is set to 50Ω. To measure the output voltage, the power-matching circuits are connected to dual-half-wave rectifiers, each consisting of two diode-connected standard PMOS devices, one rectifying the positive and the other rectifying the negative half of the signal coming from the output of the matching

network. Fig.3.14 is the block diagram of the chip containing the two RF-DC power converters. The rectifiers are loaded externally using discrete resistors.

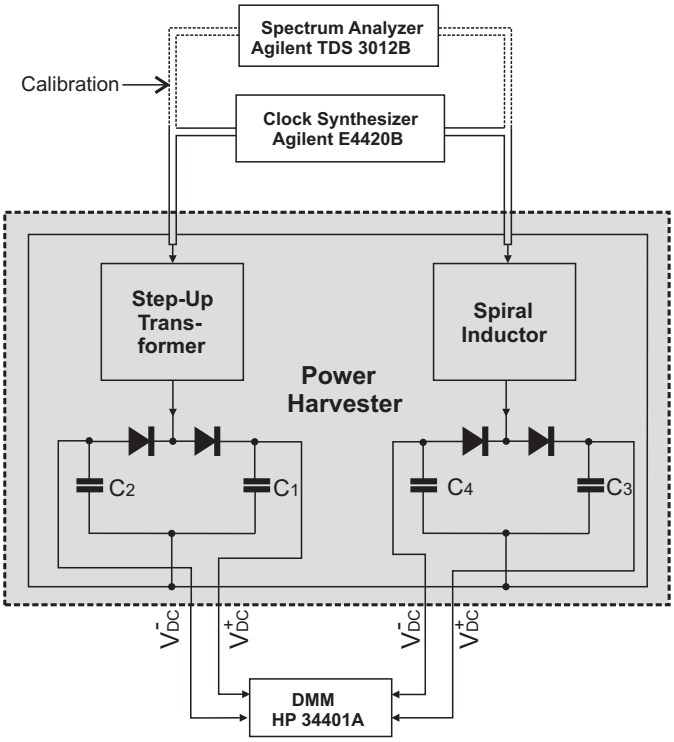

Figure 3.14: Measurement setup.

The sensitivity measurement of the power harvesting circuit with the proposed power-matching and gain-boosting network and that with LC power-matching and gain-boosting network is performed by measuring the dc output voltage for different levels of input signal power. The results are shown in Fig.3.15. It is observed that the larger the load resistance, the higher the output voltage. This agrees with the theoretical results derived earlier. It is also observed that the sensitivity of the power harvesting circuit with the proposed transformer matching network is more than twice that with the LC matching network.

Fig.3.16 plots the output DC voltage of both designs over frequencies ranging from 1 GHz to 7 GHz. The output voltage of the power harvester with the LC matching network peaks at 3.5 GHz whereas that with the transformer matching network peaks at 3.8 GHz. Although the the impedance matching networks are designed

to peak at 2.45 GHz, parameter spreading caused by process variations gives rise to a large deviation of the resonant frequency of the fabricated circuit from the value predicted by the EM simulator (ADS from HP) in design. The transformer used in the design is not standard not only because the spiral width of the primary winding and that of the secondary winding are sized differently, the stacking of the primary and secondary windings also has an offset in order to minimize the mutual capacitance between the windings. As a result, these passive components are not available from the design libraries. They are designed and analyzed using the EM solver. The corresponding netlist produced by the EM solver is fed to Spectre of Cadence Design Systems so that complete power harvesters can be simulated. The corner analysis models provided by TSMC do not account for the effect of process variation on these passive components. The power harvesters proposed in this paper were designed with no frequency-tuning capability. As a result, we can not tune the resonant frequency of the fabricated power harvesters to the desired 2.45 GHz unless an external capacitor is used. The use of an external capacitor, however, will reduce the gain of the harvesters. This experience highlights the criticalness of the tunability of the resonant frequency of matching networks in design of power harvesters. Table 4.1 compares the performance of recently reported power harvesters and the two power harvesters of this study.

3.6 Chapter Summary

In this chapter, the critical role of a matching network in an RF power harvesting system was discussed. Some of the design challenges in the on-chip implementation of these passive networks were also studied. Analytical expression of gain and efficieny of LC and transformer matching networks were developed. It was shown through theory and CAD simulations that the proposed transformer matching network provides higher voltage gain than the conventional LC resonator. Based on expressions of the gain of the two networks, it was argued that the advantage of the transformer matching technique is due to the reduced effect of the series resistance of the secondary inductor of the tranformer.

To test the proposed technique, the two RF power harvesters (LC and transformer)

Table 3.1: Performance comparison of power harvesters.

Ref.	Sensitivity	Power	Matching Network	Rectifier
[13]	-14.1 dBm	2.0 μW	on-chip LC	2-stage multiplier with native devices
[68]	-12.6 dBm	1.0 μW	off-chip LC	3-stage full-wave multiplier
This work	-5.0 dBm	2.0 μW	on-chip LC	dual half-wave rectifier
This work	-12.0 dBm	2.0 μW	on-chip stacked transformer	dual half-wave rectifier

Ref.	Technology	Freq.	Source Imp.	Spiral Size (μm$\times\mu$m)
[13]	0.18μm CMOS with native devices	900 MHz	50 Ω	455×455
[68]	5μm silicon-on-sapphire	2.45 GHz	73 Ω	N/A
This work	0.18μm CMOS	3.53 GHz	50 Ω	230×230
This work	0.18μm CMOS	3.85 GHz	50 Ω	200×200

were developed. From the measurement results presented in this chapter, it is evident that the power harvester developed using the transformer offers 8 dB more sensitivity.

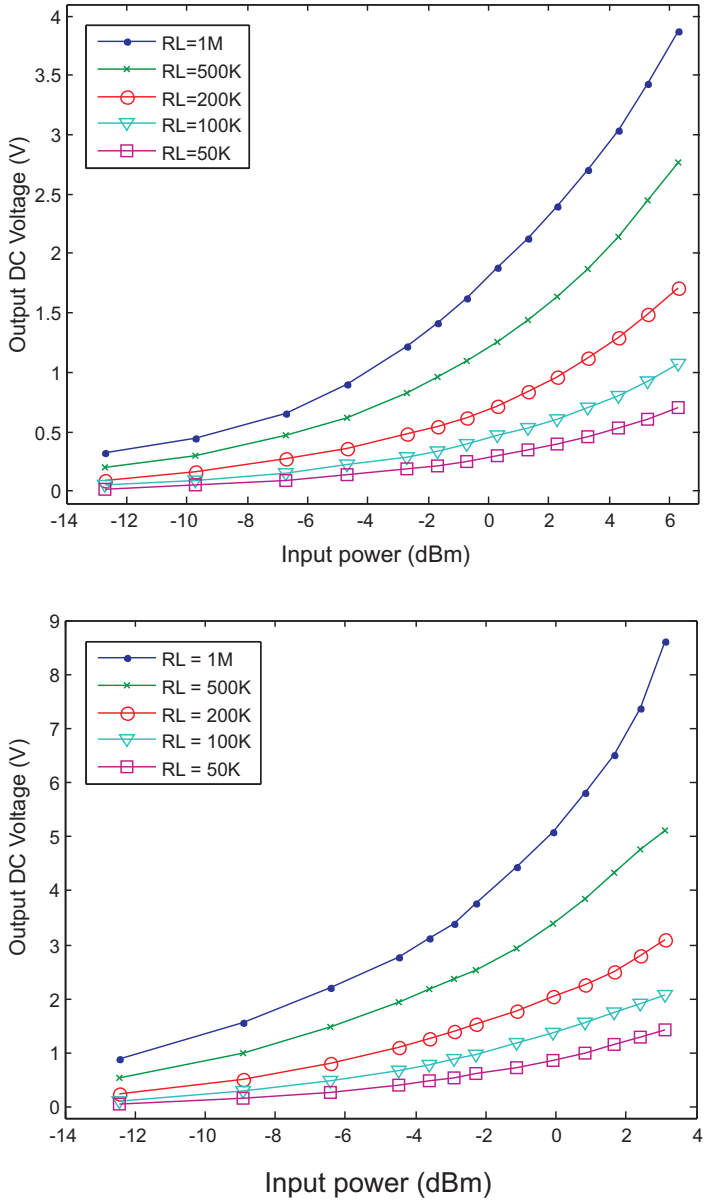

Figure 3.15: Measured sensitivity of the fabricated power harvesters for different values of output load. (a) Power harvester with LC matching network. (b) Power harvester with step-up transformer matching network.

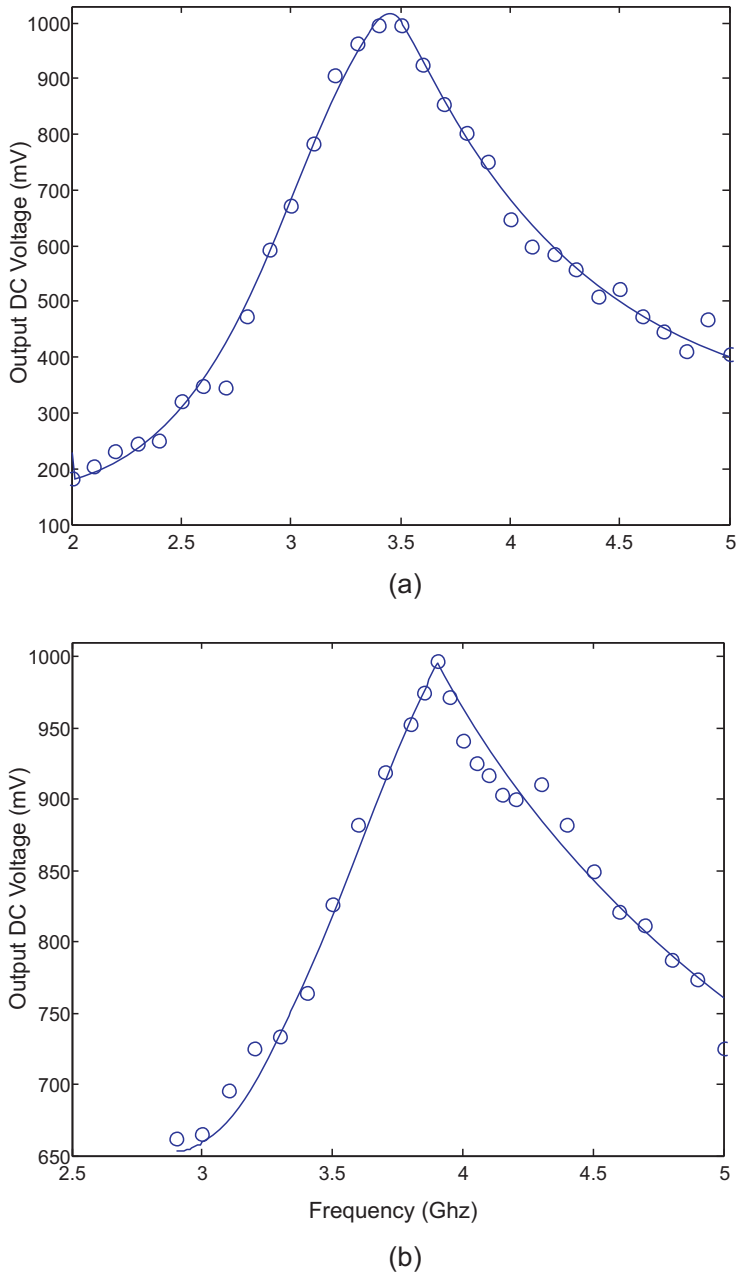

Figure 3.16: Measured DC output voltage of the fabricated power harvesters for different input frequencies. (a) Power harvester with LC matching network. Input power -4 dBm. (b) Power harvester with step-up transformer matching network. Input power -11.9 dBm.

Chapter 4

Remote Clock Frequency Calibration of Passive Wireless Microsystems[1]

4.1 Introduction

The reliability of data communications between passive wireless transponders and their base stations is heavily affected by the change in the condition of the environment in which these passive transponders reside. Change in electric field strength, temperature and pressure can cause the frequency of the local oscillator of the transpoder to deviate from its desired value. The LO frequency can be kept at a pre-determined value by periodically calibrating the oscillator to a known reference value.

In this chapter, we propose a remote frequency calibration method that allows a passive wireless transponder to adjust the frequency of its local relaxation oscillator to a desired frequency using an injection-locked phase-locked loop (IL-PLL) [39]. Integrating feedback to increase the injection lock range and hold the frequency

[1]The preliminary results of the research regarding remote clock frequency calibration has been published in the book chapter [38] and IEEE conference proceedings [40, 39]. More comprehensive research results on this subject was published in the IEEE Transactions on Circuits and Systems I - Fundamental Theory and Applications [41].

of the locked local relaxation oscillator once the injection signal is removed is proposed. In addition, a new relaxation oscillator with a current pulse generator is proposed. The proposed IL-PLL is an analog system that consumes significantly less power as compared with its digital counterparts. The paper is organized as follows : Section 4.2 presents the time-domain analysis of relaxation oscillators under injection. Section 4.3 studies the injection locking of relaxation oscillators with integrating feedback. The dynamics of the relaxation oscillator and those of injection-locked PLLs are investigated in this section. Section 4.4 details the design of the proposed injection-locked phase-locked loop. Section 4.5 presents the simulation results of the injection-locked phase-locked loop. The measurement results of the fabricated system is presented in Section 4.6. The chapter is summarized in Section 4.7.

4.2 Injection Locking

4.2.1 Free-Running Relaxation Oscillators

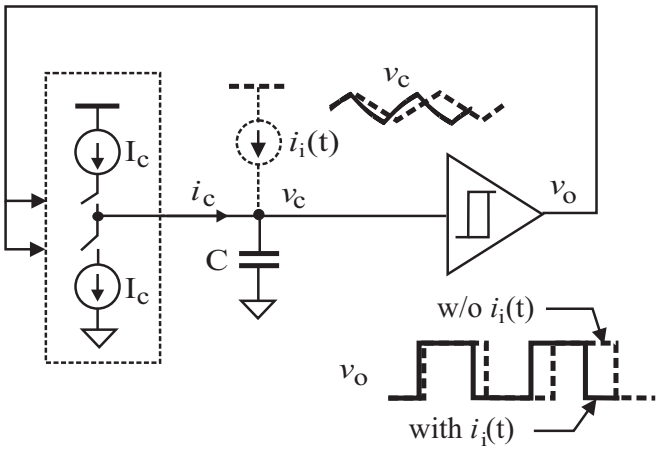

Figure 4.1: Configuration of relaxation oscillators.

Consider a relaxation oscillator in its free running state, as shown in Fig.4.1 (without $i_i(t)$). Assume that the charge pump current I_c is constant. The voltage of the

timing capacitor C is given by $v_c(t) = V_L + \frac{I_c}{C}t$ (charging) and $v_c(t) = V_H - \frac{I_c}{C}t$ (discharging). The output voltage of the oscillator has a 50% duty cycle with period T_n given by $T_n = 2\left(\frac{C\Delta V}{I_c}\right)$.

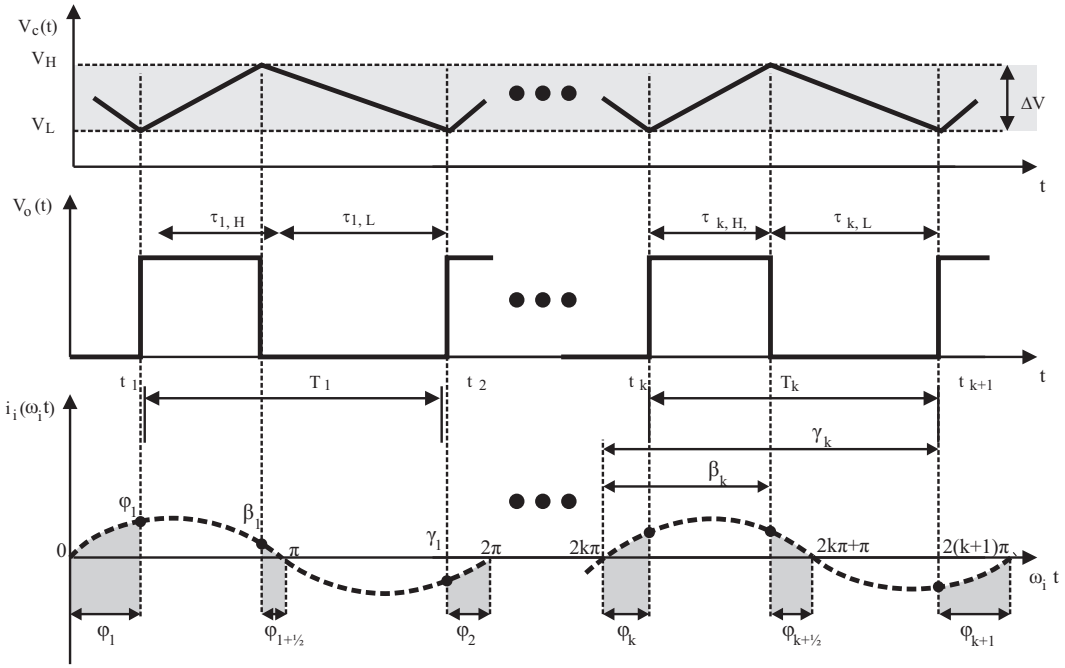

Figure 4.2: Waveforms of relaxation oscillators under injection with definitions of phase angles and time intervals (Duty-cycle variations have been exaggerated.)

4.2.2 Relaxation Oscillators Under Injection

Consider the small current signal of $i_i(t) = I_i\cos(\omega_i t)$ being injected into the timing capacitor C, as shown in Fig.4.1. $i_i(t)$ will alter the charge of the timing capacitor and modulate both the period and duty cycle of the output voltage v_o, as illustrated graphically in Fig.4.2. Consider the first oscillation cycle under injection. It can be shown that

$$C\frac{dv_c}{dt} = I_c + I_i\cos(\omega_i t + \phi_1), v_c(0^-) = V_L, \tag{4.1}$$

where ϕ_1 is the phase angle of $i_i(t)$ at $t = t_1$ with reference to the origin, as shown in Fig.4.2. Since our objective is to align $i_i(t)$ and $v_o(t)$, the phase angle of $i_i(t)$ measured at the rising edge of $v_o(t)$ quantifies the amount of mis-alignment between $i_i(t)$ and $v_o(t)$. When both the waveforms are perfectly lined up, the phase angle becomes zero. Note that because the rising edge of $v_o(t)$ varies with time during the locking process, the phase angle also varies with time. The use of the phase angle to quantify the amount of mis-alignment between $i_i(t)$ and $v_o(t)$ will greatly simplify the analysis, as to be seen shortly. The solution of (4.1) at $t = \tau_{1,H}$ is given by

$$V_H = V_L + \frac{I_c \tau_{1,H}}{C} + \frac{I_i}{C\omega_i}\Big[\sin\left(\omega_i \tau_{1,H} + \phi_1\right) - \sin\phi_1\Big]. \tag{4.2}$$

Solving for $\tau_{1,H}$ from (4.2) yields

$$\tau_{1,H} = \frac{T_n}{2} - \frac{m}{\omega_i}\Big[\sin\left(\omega_i \tau_{1,H} + \phi_1\right) - \sin\phi_1\Big], \tag{4.3}$$

where $m = \frac{I_i}{I_c}$ is the injection index. Similarly, one can show that the time duration of k^{th} period where the output of the oscillator is at logic 1 is given by

$$\tau_{k,H} = \frac{T_n}{2} - \frac{m}{\omega_i}\left[\sin\left(\omega_i \tau_{k,H} + \phi_k\right) - \sin\phi_k\right], \tag{4.4}$$

where ϕ_k denotes the phase angle of $i_i(t)$ at $t = t_k$ with reference to the $(2k)^{th}$ zero-crossing of $i_i(t)$, as shown in Fig.4.2. In a similar manner, the time duration of k^{th} oscillation period where the output of the oscillator is at logic 0 is given by

$$\tau_{k,L} = \frac{T_n}{2} + \frac{m}{\omega_i}\left[\sin\left(\omega_i T_k + \phi_k\right) - \sin\left(\omega_i \tau_{k,H} + \phi_k\right)\right]. \tag{4.5}$$

Let β_k and γ_k denote the phase angle of $i_i(t)$ at $t = t_k + \tau_{k,H}$ and $t = t_{k+1}$ with

reference to the $(2k)^{th}$ zero crossing of $i_i(t)$ respectively, as shown in Fig.4.2. It follows that $\beta_k = \phi_k + \omega_i \tau_{k,H}$ and $\gamma_k = \phi_k + \omega_i T_k$. Making use of (4.4), we obtain

$$\beta_k = \phi_k + \frac{a_0}{2} - m\Big[\sin\beta_k - \sin\phi_k\Big], \tag{4.6}$$

where $a_0 = \omega_i T_n$. Substitute β_k into $\sin\beta_k$ in (4.6) and

$$\begin{aligned} \beta_k &= \phi_k + \frac{a_0}{2} - m\Big\{\sin\beta_k \\ &- \sin\left[\beta_k - \frac{a_0}{2} + m(\sin\beta_k - \sin\phi_k)\right]\Big\}. \end{aligned} \tag{4.7}$$

If the injection index m is small, i.e., the amplitude of the injection signal is much smaller as compared with the current of the charge pump, we can expand $\sin\left[\phi_k + \frac{a_0}{2} - m\left(\sin\beta_k - \sin\phi_k\right)\right]$ at $\phi_k + \frac{a_0}{2}$ in its Taylor series to the first order and neglect the high-order terms, i.e. the terms associated with m^2, m^3, ...

$$\beta_k \approx \phi_k + \frac{a_0}{2} - m\left[\sin\left(\phi_k + \frac{a_0}{2}\right) - \sin\phi_k\right]. \tag{4.8}$$

Note that the first-order approximation performed here is valid if the amplitude of the injected signal is much smaller than the current of the charge pump of the relaxation oscillator. If the amplitude of the injected current is comparable to the charge pump current, higher-order terms will be required. This will significantly complicate the analysis. Fortunately, for the applications targeted in this paper, the assumption that the injection signal is weak holds.

Similarly, substituting (4.5) into $\gamma_k = \beta_k + \omega_i \tau_{k,L}$ yields

$$\gamma_k = \beta_k + \frac{a_0}{2} + m\left[\sin\beta_k - \sin\gamma_k\right]. \tag{4.9}$$

Substituting γ_k into $\sin\gamma_k$ and expanding $\sin\left[\beta_k + \frac{a_0}{2} + m(\sin\beta_k - \sin\gamma_k)\right]$ at $\beta_k + \frac{a_o}{2}$ to the first order yield

$$\gamma_k \approx \beta_k + \frac{a_0}{2} + m\left[\sin\beta_k - \sin\left(\beta_k + \frac{a_0}{2}\right)\right]. \tag{4.10}$$

Using (4.6) we can write

$$\gamma_k = \phi_k + a_0 - 4m\sin^2\left(\frac{a_0}{4}\right)\sin\beta_k. \tag{4.11}$$

As shown in Fig.4.2, $\phi_{k+\frac{1}{2}}$ and ϕ_{k+1} are essentially β_k and γ_k but measured from reference points displaced by π and 2π respectively. Therefore, $\beta_k = \pi + \phi_{k+\frac{1}{2}}$ and $\gamma_k = 2\pi + \phi_{k+1}$. Define $a_1 = a_o - 2\pi = 2\pi\left(\frac{T_n - T_i}{T_i}\right) = (\omega_i - \omega_n)T_n$. Eq.(4.11) becomes

$$\Delta\phi_k = a_1 + a\sin\phi_{k+\frac{1}{2}}, \tag{4.12}$$

where $a = 4m\cos^2\left(\frac{a_1}{4}\right)$ and $\Delta\phi_k = \phi_{k+1} - \phi_k$. The first term in (4.12) is the initial phase angle of $i_i(t)$ and the second term quantifies the effect of the injection signal.

4.2.3 Locking Dynamics

Let ϕ_x be a continuous function of x with $\phi_x|_{x=k} = \phi_k$. Over each cycle of the oscillator, the value of x is continuously incremented by 1, as shown graphically in Fig.4.3. From (4.12), the change in ϕ_x from $x = k$ to $x = k + 1$ will equal to $a_1 + a\sin\phi_x$ at $x = k + \frac{1}{2}$, as shown in Fig.4.4. If we assume that the average value of $\frac{d\phi_x}{dx}$ over the interval $[k, k+1]$ is approximately equal to its value at the midpoint of the interval, we can write

$$\frac{d\phi_x}{dx} = a_1 + a\sin\phi_x. \tag{4.13}$$

Note that the preceding approximation is valid for each [k,k+1] interval. Eq.(4.13) can be solved from

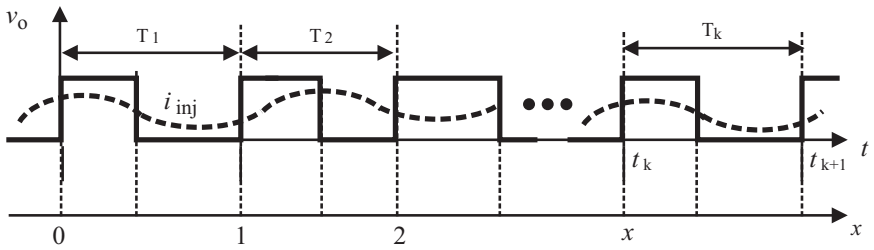

Figure 4.3: Waveforms of v_o and $i_i(t)$. For each cycle of $v_o(t)$, x is incremented by one.

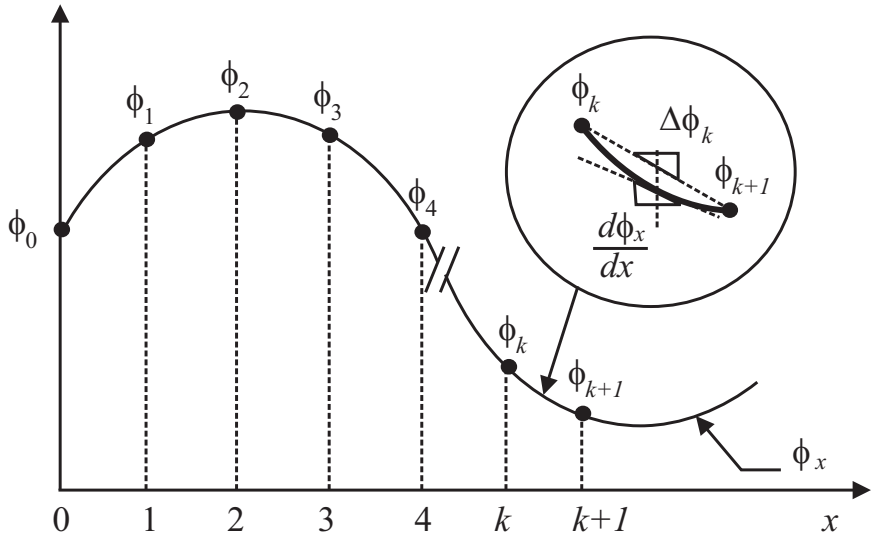

Figure 4.4: Phase angle sequence.

$$\int_{\phi_o}^{\phi_x} \frac{du}{a_1 - a\sin u} = \int_0^x dx. \tag{4.14}$$

The result is given by

$$\tan\left(\frac{\phi_x}{2}\right) = \frac{a}{a_1} - \frac{a_2}{a_1}\tan\left(\frac{a_2 x}{2}\right), \tag{4.15}$$

where $a_2^2 = a^2 - a_1^2$ is assumed for simplification. We comment on the preceding development:

- If a_2 is real, i.e. $a > |a_1|$, $\tan\left(\frac{a_2 x}{2}\right)$ will be a periodic function of x with period

$$X_P = \frac{\pi}{\left(\frac{a_2}{2}\right)} = \frac{2\pi}{\sqrt{a^2 - a_1^2}}. \tag{4.16}$$

  $tan(\frac{\phi_x}{2})$ will have discontinuities at $x = \frac{X_P}{2} + X_p$, ..., $\frac{X_P}{2} + nX_P$ where $\phi_x = \pi$, $\pi + 2\pi$, ..., $\pi + n\pi$.
- If a_2 is imaginary, i.e. $a < |a_1|$, $\tan\left(\frac{a_2 x}{2}\right)$ converges to j as x increases. In this case, the right hand side of (4.15) will no longer be periodic. For each value of a_1, ϕ_x will converge to a finite value with the increase of x, i.e. the oscillator will lock to the injection signal $i_i(t)$.
- If $a_2 = 0$, we have $a_1 = |a|$ and $\phi_x = \frac{\pi}{2}$ follows. The phase angle of $i_i(t)$ is approximately $\frac{\pi}{2}$. This agrees with the results given in [22]. This condition is called "quasi-lock" which occurs when the oscillator is exactly at either ends of the locking range.

The preceding analysis shows that the locking range of the oscillator can be determined from the constraint that the value of a_2 must be imaginary. Making use of this observation and noting $a > 0$, we have $a \geq |a_1|$. It follows that $4m\cos^2\left(\frac{a_1}{4}\right) \geq |a_1|$. When ω_i is within the lock range, a_1 is small such that $\cos^2\left(\frac{a_1}{4}\right) \approx 1$. The upper bound of a_1 below which the oscillator will lock to the injection signal is therefore given by

$$|a_1| \leq 4m. \tag{4.17}$$

Making use of $\omega_n = \frac{2\pi}{T_n}$ and $\omega_i = \frac{2\pi}{T_i}$, we arrive at

$$|\Delta\omega_L| = \left(\frac{2}{\pi}\omega_n\right) m, \tag{4.18}$$

where $\Delta\omega_L = \omega_i - \omega_n$ is the locking range of the oscillator which is centered at ω_n, i.e. $\omega_{i,max} = \omega_n + |\Delta\omega_L|$. It is evident from (4.18) that the locking range is proportional to both the amplitude of the injection signal and the free-running frequency of the oscillator. The scaling of locking range with ω_n is verified by noting that for a given charge pump current amplitude, higher ω_n means smaller timing capacitance. As a result, the same injected current will give rise to a larger change in the voltage of the timing capacitor, causing a larger change in the oscillation frequency.

4.2.4 Injection Pulling

The phase of the injection signal $i_i(t)$ is quantified by $\omega_i t$ while that of the output of the oscillator $v_o(t)$ at x is given by $2\pi x$, as seen from Fig.4.3. The phase angle of $i_i(t)$ at x is given by $\phi_x = \omega_i t - 2\pi x$ from which we arrive at $t = xT_i + \frac{\phi_x}{\omega_i}$. When the oscillator is locked to the injection signal, ϕ_x will be a constant. In this case, t and x will have a linear relation, and $dt = T_i dx$ holds. In the pulling state, however, since ϕ_x varies with x, no linear relation between x and t exists.

Since the period of the oscillator varies with time in the pulling process, we use the average period of the oscillator to quantify this change. The average value of the period of the oscillator in x-domain, denoted by T_x, over X_P is given by

$$\overline{T_x} = \frac{1}{X_P}\int_x^{x+X_P} T_x dx. \tag{4.19}$$

Without the loss of generality, we assume $T_n > T_i$. Note $\phi_x = \omega_i t - 2\pi x$ and $\phi_{x+X_P} = \omega_i(t+T_P) - 2\pi(x+X_P)$, where T_P is the time duration from x to $x+X_P$

and is obtained from $T_P = \int_x^{x+X_P} T_x dx$. It follows that $T_P = \overline{T_x} X_P$. Utilizing this property we obtain

$$\phi_{x+X_P} - \phi_x = \omega_i X_P \overline{T_x} - 2\pi X_P. \tag{4.20}$$

As pointed out earlier, when x varies from x to $x + X_P$, ϕ_x will vary from ϕ_x to $\phi_x + 2\pi$, i.e., $\phi_{x+X_P} = \phi_x + 2\pi$. Eq.(4.20) becomes

$$\overline{T_x} = T_i \left(1 + \frac{1}{X_P}\right). \tag{4.21}$$

Substitute (4.16) into (4.21)

$$a_2 = 2\pi \left(\frac{\overline{T_x} - T_i}{T_i}\right). \tag{4.22}$$

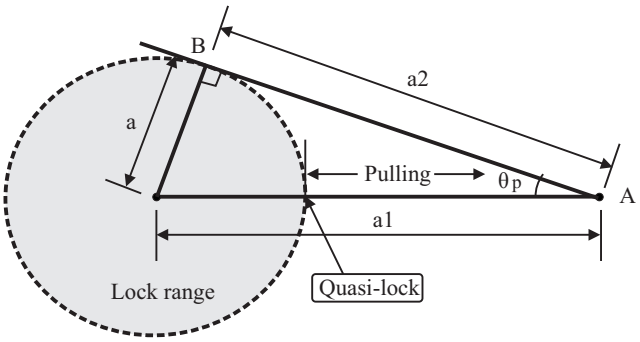

Figure 4.5: Graphical representation of the pulling of oscillators under injection.

Fig.4.5 provides the graphical representation of the injection pulling of the oscillator. The right triangle is constructed from $a_2^2 = a_1^2 - a^2$ derived earlier. Because $\sin\theta_p = \frac{a}{a_1}$ and $\cos\theta_p = \frac{a_2}{a_1}$, we have

$$\tan\left(\frac{\theta_p}{2}\right) = \frac{1-\cos\theta_p}{\sin\theta_p} = \frac{a_1 - a_2}{a}. \tag{4.23}$$

If we define $a_3 = 2\pi\left(\frac{\overline{T_x}-T_n}{T_i}\right)$, it follows that $a_3 = a_2 - a_1$. Utilizing this result in (4.23) yields

$$a_3 = -a\tan\left(\frac{\theta_p}{2}\right). \tag{4.24}$$

θ_p is termed the injection pulling angle. The larger the angle, the stronger the effect of injection pulling. The maximum pulling angle is 90^o, occurring in the quasi-lock state where $a_2 = 0$ or equivalently $|a_1| = a$. When the injection signal is far outside the lock range ($|a_1| \gg a$), injection has a little effect on the oscillator ($\theta_p \approx 0$). The negative sign in (4.24) indicates that injection pulling is toward the lock range.

4.3 Integrating Feedback

In Section 4.2.4 we showed that, when the injection signal fails to lock the oscillator, the average period variation caused by the injection is still toward the locking range. In this section, we show how the accumulated period variations (difference between the period of the oscillator under injection and its free-running period) can be used as a feedback signal to adjust the intrinsic frequency of oscillator.

4.3.1 Constructing an Integrating Feedback

The periodic condition of the relaxation oscillator requires the net variation of the voltage of the timing capacitor C over one period be zero in the steady state, i.e.

$$\int_t^{t+T_n} X i_c(t)dt = 0, \tag{4.25}$$

where X is a Boolean variable depicting the logic state of the output of the comparator. $X = 1$ when the output voltage of the comparator is at logic-1 and $X = -1$ otherwise. When the injection current $i_i(t)$ is present, Eq.(4.25) becomes

$$\int_t^{t+T} X\Big[i_c(t) + i_i(t)\Big]dt = 0, \tag{4.26}$$

where T is the period of the oscillator under injection. Let $T = T_n + \Delta T$ with $\Delta T \ll T$ quantifying the variation of the period of the oscillator caused by $i_i(t)$, Eq.(4.26) becomes

$$\begin{aligned} &\int_t^{t+T_n} X i_c(t)dt + \int_{t+T_n}^{t+T_n+\Delta T} X i_c(t)dt \\ + &\int_t^{t+T} X i_i(t)dt = 0. \end{aligned} \tag{4.27}$$

The first integral in (4.27) vanishes. Also, because $X = -1$ when $t + T_n \leq t < t + T_n + \Delta T$, Eq.(4.27) becomes

$$\Delta T = \frac{1}{I_c}\int_t^{t+T} X i_i(t)dt. \tag{4.28}$$

Write (4.28) over all the oscillation periods within the interval $0 \leq t \leq t_k$

$$\int_0^{t_k} X i_i(t)dt = \sum_{j=0}^{k-1}\int_{t_j}^{t_{j+1}} X i_i(t)dt = I_c \sum_{j=1}^{k} \Delta T_j. \tag{4.29}$$

Eq.(4.29) reveals that the accumulated period variation of the oscillator can be obtained by integrating the injection current modulated by the output of the comparator.

4.3.2 Dynamics of Injection-Locked Relaxation Oscillator Without Integrating Feedback

In this section, we investigate the dynamics of injection-locked relaxation oscillators in the vicinity of the lock state without integrating feedback. To avoid ambiguity, we use T to denote the period of the oscillator when both the external injection and internal integrating feedback are present. Also, a_1 becomes $a_1(t) = 2\pi\left(\frac{T-T_i}{T_i}\right) = (\omega_i - \omega)T$. It was shown earlier that in the lock state $dt = T_i dx$. Substituting this result into (4.13) yields

$$\begin{aligned} T_i\frac{d\phi(t)}{dt} &= a_1(t) + a\sin\phi(t) \\ &\approx -a\phi(t) + a_1(t), \end{aligned} \tag{4.30}$$

where $\phi(t)$ is the phase angle of $i_i(t)$. Note that we have utilized $\sin\left[\phi + \frac{a_1(t)}{2}\right] \approx \phi + \frac{a_1(t)}{2}$ in simplifying (4.30). Assume $\phi(0^-) = 0$. Laplace transform of (4.30) gives

$$\Phi(s) \approx \frac{1}{sT_i + a} A_1(s), \tag{4.31}$$

where $\Phi(s)$ and $A_1(s)$ are the Laplace transform of $\phi(t)$ and $a_1(t)$, respectively. If $a_1 = A_m u(t)$, one can show that

$$\phi(t) = \frac{A_m T_i}{a}\left(1 - e^{-\frac{a}{T_i}t}\right). \tag{4.32}$$

It is evident that $\phi(\infty) = \frac{A_m T_i}{a}$ is the steady-state phase error. Since $a \approx 4m$ in the lock state, the stronger the injection signal, the faster the phase angle will reach its final value, and the smaller the steady-state phase error. Also observed is that the larger the initial phase angle, the larger the final phase error.

4.3.3 Dynamics of Injection-Locked Relaxation Oscillator With Integrating Feedback

Let us now consider the relaxation oscillator with both external injection and internal integral feedback. The output of the integrating feedback block, denoted by v_f, is given by

$$v_f = \int \Delta T_x dx = \frac{1}{T_i} \int \Delta T dt. \tag{4.33}$$

v_f is used to tune the current of the charge pump. The period of the oscillator is obtained from

$$T = T_o - \frac{K_f}{T_i} \int \Delta T dt, \tag{4.34}$$

where T_o is the period of the oscillator when the injection signal and feedback are both absent and K_f is the gain of the integrating feedback. Substitute (4.34) into the expression of $a_1(t)$ given earlier

$$a_1(t) = \omega_i \left[\Delta T_o - \frac{K_f}{T_i} \int \Delta T dt \right], \tag{4.35}$$

where $\Delta T_o = T_o - T_i$ is the initial difference between the period of the oscillator and that of the injection signal. Differentiating ϕ_x with respect to x, equating the result to (4.13), and making use of the expression of $a_1(t)$ given earlier yield

$$\frac{dt}{dx} = T + \frac{a}{\omega_i} \sin \phi_x. \tag{4.36}$$

Since in the lock state $dt = T_i dx$ and $\sin\phi_x \approx \phi_x + \frac{a_1}{2}$, Eq.(4.36) is simplified to

$$T - T_i \approx \frac{a}{\omega_i}\phi_x. \tag{4.37}$$

Substitute (4.37) into (4.35)

$$a_1(t) = a_{in}(t) - \frac{aK_f}{T_i}\int \phi(t)dt. \tag{4.38}$$

where $a_{in}(t) = \omega_i \Delta T_o$ is the initial phase angle of $i_i(t)$. Laplace transform of (4.38) gives

$$A_1(s) = A_{in}(s) - \frac{aK_f}{sT_i}\Phi(s), \tag{4.39}$$

where $A_{in}(s)$ is the Laplace transform of $a_{in}(t)$. Substitute (4.31) into (4.39)

$$\frac{A_1(s)}{A_{in}(s)} = \frac{s\left(s + \frac{a}{T_i}\right)}{s^2 + s\frac{a}{T_i} + \frac{K_f}{a}\left(\frac{a}{T_i}\right)^2}. \tag{4.40}$$

Because in the lock state, $\omega_i = \omega$ and $a \approx 4m$, we have

$$\frac{a}{T_i} \approx \frac{4m}{T} = \frac{2}{\pi}m\omega = \Delta\omega_L. \tag{4.41}$$

Eq.(4.40) becomes

$$\frac{A_1(s)}{A_{in}(s)} = \frac{s\left(s + \Delta\omega_L\right)}{s^2 + s(\Delta\omega_L) + \frac{K_f}{a}(\Delta\omega_L)^2}. \tag{4.42}$$

Eq.(4.42) reveals that the injection-locked PLL is a 2nd-order system with its loop bandwidth ω_n and damping factor ξ given by

$$\omega_n = \frac{\Delta\omega_L}{2}\sqrt{\frac{K_f}{m}}, \tag{4.43}$$

and

$$\xi = \sqrt{\frac{m}{K_f}}. \tag{4.44}$$

Because the closed-loop transfer function has a zero at the origin, the steady-state phase error is zero. This differs from the injection-locked relaxation oscillator without the integrating feedback studied earlier. Also, because $\xi\omega_n = \frac{\Delta\omega_L}{2}$ and $\Delta\omega_L$ is directly proportional to the injection index, the larger the injection index, the faster the locking. The loop bandwidth ω_n and damping factor ξ are determined by both the strength of the integrating feedback K_f and the injection strength a. The two poles of (4.42) are given by

$$s_{1,2} = \frac{\Delta\omega_L}{2}\left[-1\pm\sqrt{1-\frac{K_f}{m}}\right]. \tag{4.45}$$

The system has both poles located in the left of s-plane and is stable.

4.3.4 Noise Consideration

The injection signal is transmitted over a wireless channel by a base station, the presence of noise in the signal is inevitable. The noise coupled to the injection signal can be represented a Fourier series. To simplify presentation, let the noise coupled to the injection signal be a sinusoid. The total injection signal in k^{th} oscillation cycle can be written as $i_i(t) = I_i\cos(\omega_i t + \phi_{i,k}) + I_n\cos(\omega_n t + \phi_{n,k})$ where I_n and ω_n are the amplitude and frequency of the noise respectively, and $\phi_{n,k}$ is the phase

angle of the noise $i_n(t)$ at $t = t_k$. When the noise coupled to the injection signal is considered, the cycle-to-cycle phase angle variation can be quantified by

$$\Delta\phi_k = a_1 + a\sin\phi_{k+\frac{1}{2}} + \sigma, \tag{4.46}$$

where σ represents the contribution of the noise coupled to the injection signal to the cycle-to-cycle phase angle variation. Eq.(4.46) reveals that he noise coupled to the injection signal will affect the lock range of the oscillator under injection. Re-writing (4.25) with noise $i_n(t)$ considered

$$\int_t^{t+T_n} X\left[I_c + i_i(t) + i_n(t)\right] dt = 0, \tag{4.47}$$

we have

$$\int_0^{t_k} X\left[i_i(t) + i_n(t)\right] dt = I_c \sum_{j=1}^{k} \Delta T_j. \tag{4.48}$$

Eq.(4.48) reveals that in system with integrating feedback, the accumulated period variation of the oscillator will contain both the effects of the clean injection as well as that of the coupled noise on the oscillator.

It should also be noted that since the injection signal is obtained from an ASK demodulator, high frequency noise components of the injection signal will be to some extent filtered out by the low-pass mechanism of the ASK demodulator [58] and will have smaller effect on the locking of the oscillator.

4.4 Circuit Implementation

Fig.4.6 shows the configuration of the proposed remote frequency calibration system using IL-PLL. The calibrating RF signal is sent by the base station. It is

demodulated and filtered out using C_i prior to its injection. The oscillator is a relaxation oscillator whose oscillation frequency is mainly determined by passive components, minimizing the effect of PVT.

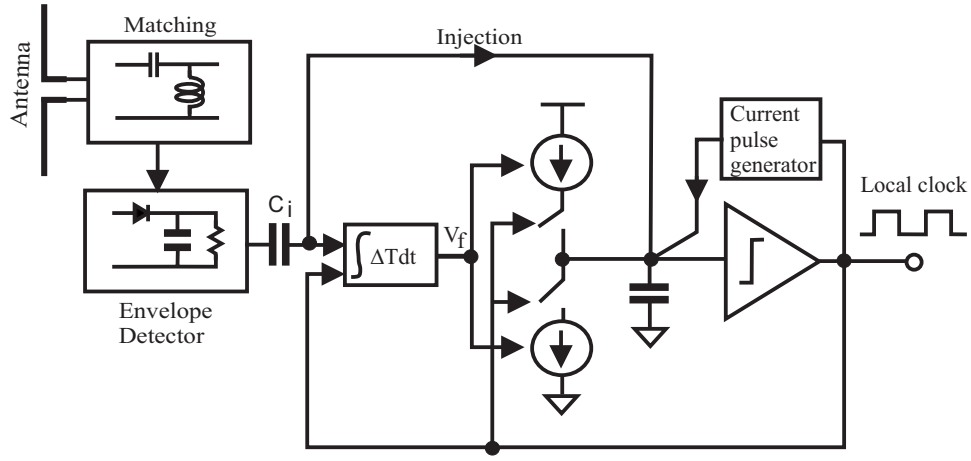

Figure 4.6: Remote frequency calibration of local oscillators of passive wireless transponders using injection-locked phase-locked loops. The charge pump current is controlled by the feedback while the direction of the charge pump current is controlled by the output of the comparator.

4.4.1 Relaxation Oscillator[2]

Schmitt triggers are often employed in relaxation oscillators. The hysteresis of the Schmitt trigger directly affects the frequency of these oscillators. The maximum hysteresis that a Schmitt trigger can provide is given by $\Delta V_{max} = V_{DD} - V_{tn} - |V_{tp}|$, where V_{tn} and V_{tp} are the threshold voltage of nMOS and pMOS transistors, respectively. Since the power of passive wireless transponders is harvested from the radio-frequency wave emitted by their base station, its supply voltage is typically low and time-varying. In our design, V_{DD} is set to 1 V. The hysteresis of a Schmitt trigger implemented in TSMC-0.18μm CMOS technology will be less than 200 mV when $V_{DD} = 1$ V. It was shown in Section 4.2 that the period of the Schmitt trigger relaxation oscillator is given by $T_n = 2\left(\frac{C\Delta V}{I_c}\right)$. The sensitivity of the frequency of the oscillator to V_{DD} is obtained from

[2]Our research regarding this subject has been published in Electronics Letters [59]

$$\frac{\partial f_n}{\partial V_{DD}} = -\frac{I_c}{2C\left(\Delta V\right)^2}\frac{\partial \Delta V}{\partial V_{DD}}, \tag{4.49}$$

where $f_n = \frac{1}{T_n}$. Eq.(4.49) reveals that the smaller the hysteresis ΔV, the more sensitive the frequency of the Schmitt trigger relaxation oscillator to V_{DD} fluctuation.

One way to generate a large hysteresis without using a Schmitt trigger is to use latches in conjunction with two timing capacitors and two voltage comparators [23]. It is, however, difficult to find an appropriate injection node so that the charging and discharging of both timing capacitors can be controlled by the injection signal. To overcome this difficulty, a current pulse generator (Fig.4.7) is proposed. The operation of the current pulse generator is depicted as follows : Assuming that X=logic-0, M1 shuts off and M2 turns on. M5 turns on and M6 is off. C_1 is totally discharged via the path provided by M5. M3 is off and M4 is on. M4 sources the current $i_p = i_{ds4}$ to the output. In the mean time, C_2 is charged by V_{DD}. As a result, v_A rises exponentially with time. When v_A reaches $V_{DD} - |V_{tp}|$, M4 turns off and i_p vanishes. A current pulse is generated. The width of the current pulse can be estimated as the follows : Assume $v_X = 0$ when X is at logic-0 and the voltage drop cross the source and drain of M2 (in triode) is constant and is denoted by V_{sd2}. From

$$V_{sd2} + R_2C_2\frac{dv_A}{dt} + v_A = V_{DD}, \quad v_A(0^-) = 0, \tag{4.50}$$

we have

$$v_A(t) = (V_{DD} - V_{sd2})\left[1 - e^{-\frac{t}{R_2C_2}}\right]. \tag{4.51}$$

The width of the positive current pulse, denoted by τ_p, can be obtained by letting $v_A(t) = V_{DD} - |V_{tp}|$

$$\tau_p = R_2 C_2 \ln\left(\frac{V_{DD} - V_{sd2}}{|V_{tp}| - V_{sd2}}\right) \approx R_2 C_2 \ln\left(\frac{V_{DD}}{|V_{tp}|}\right). \tag{4.52}$$

In a similar way, one can show that when X=logic-1, M3 will sink a current pulse from the output node with the pulse width

$$\tau_n \approx R_1 C_1 \ln\left(\frac{V_{DD}}{V_{tn}}\right). \tag{4.53}$$

The preceding analysis reveals that the current pulse generator will generate a current pulse each time the output of the comparator changes its logic state. When the voltage of the timing capacitor rises to 0.5 V from 0 V, the current pulse generator will set it to V_{DD} before the discharge period begins. When the timing capacitor drops to 0.5 V from V_{DD}, the pulse generator will reset it to 0 before the charging period of the timing capacitor starts. The amplitude of the current pulses must be sufficiently large such that it will charge or discharge the timing capacitor completely. The width of the current pulses is set much smaller as compared with the relaxation time of the timing capacitor such that it has a little impact on both the duty cycle and the period of the output voltage of the oscillator.

The output of the relaxation oscillator is designed to have a 50% duty cycle. The mismatch of the width of current pulses exists mainly due to $|V_{tp}| \neq V_{tn}$, Because the width of the current pulses is much smaller as compared with the relaxation time of the timing capacitor, the effect of the mismatch on the duty cycle of the oscillator is negligible.

4.4.2 Integrating Feedback

It was shown in (4.29) that the accumulated variation of the period of the oscillator under injection can be obtained by integrating the injection current modulated by the output of the comparator. The product $Xi_i(t)$ can be obtained using a transmission-gate passive mixer where X is the modulating signal and $i_i(t)$ is the

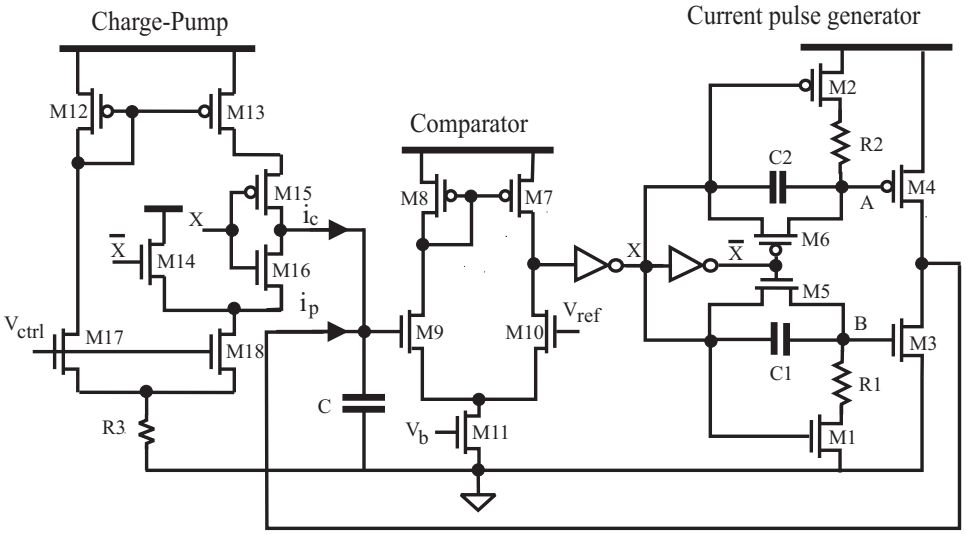

Figure 4.7: Proposed relaxation oscillator. C is the timing capacitor. Time constants R_1C_1 and R_2C_2 set the width of current pulses. Circuit parameters: $W_{1,2,5,6,14-16} = 0.5$ μm, $W_{3,4,9-11}$=1.5 μm, $W_{12,13}$=2 μm, $W_{17,18}$= 1 μm, $L_{7,8}$=1.5 μm, L_{9-11}=1 μm, $L_{12,13}$=3 μm, $L_{17,18}$=8 μm, $R_{1,2}$=60 K, R_3=500 K, $C_{1,2}$=50 fF, C=50 fF, $V_{ref} = V_{DD}/2 = 0.5$ V.

modulated signal. The integration is carried out using a capacitor connected to the output of transmission-gate passive mixer that generates $Xi_i(t)$. Since the injection signal used in the analysis given earlier is a current while the output of the envelope detector is a voltage, a Norton-to-Thevenin source transformation is needed. A dc-blocking capacitor C_i is employed at the output of the envelope detector such that only the ac signal of the desired frequency will be injected into the oscillator. The envelope detector and the dc blocking capacitor can be represented by the Thevenin equivalent shown in Fig.4.8(a). This circuit can be converted to its Norton equivalent circuit shown in Fig.4.8(b). Assume that $v_i(t) = V_i\cos(\omega_i t)$. Its phasor is given by V_i. From the principle of source transformation, the phasor of the current source in the corresponding Norton equivalent circuit is given by $I_i = j\omega_i C_i V_i$. This result shows that $i_i(t)$ leads $v_i(t)$ by $\frac{\pi}{2}$. The corresponding Norton current source can be written as $i_i(t) = \omega_i C_i V_i \cos\left(\omega_i t + \frac{\pi}{2}\right)$.

To ensure that there is no abrupt voltage drop across the switch upon closing, the circuit shown in Fig.4.8(c) is employed. When $X = 1$, the circuit functions the same way as Fig.4.8(b) does. When $X = 0$, the unity-gain voltage buffer ensures

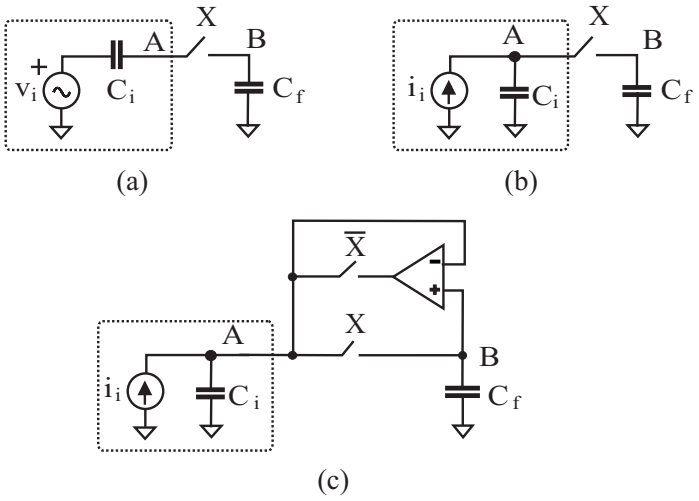

Figure 4.8: (a) Envelope detector is represented by V_i and C_i, where C_i is a dc-blocking capacitor. C_f is the feedback integration capacitor. The sampling switch controlled by X and $\overline{X}$ is implemented using transmission gates. (b) Norton equivalent circuit of that in sub-circuit (a). (c) Simplified circuit of mixing/integrating circuit.

that the voltage of node A remains constant until the next sampling time. Fig.4.9 shows its circuit implementation. When $X = 1$, the output of the amplifier will settle on one of its rails. This will create glitches in the voltage of node A, as seen in Fig.4.10. The duration of the glitches, however, is much small as compared to the duration in which the feedback is on (~ 0.5 μs). By the time $\overline{X} = 1$ interval ends, any transient glitch will have long been adjusted by the feedback, as evident in Fig.4.10. It should be noted that during the time in which a sudden dip of V_A occurs, node A is disconnected from node B. The transient glitches will not propagate to node B. As a result, V_B remains unchanged. So does the oscillation frequency of the oscillator.

4.4.3 Power Consumption

The power consumption of the proposed IL-PLL must be minimized in order for it to be used for passive wireless transponders. The power consumption of the IL-PLL is dominated by the power consumption of the relaxation oscillator and integrating feedback block. The power consumption of the relaxation oscillator is minimized

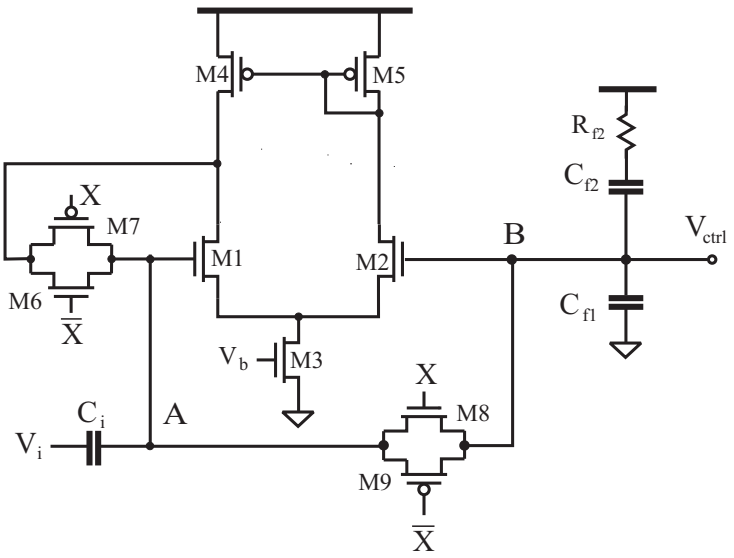

Figure 4.9: Integrating feedback circuit. W_{1-3}= 1 μm, $W_{4,5}$=2 μm, W_6=3 μm, W_7=4 μm, , $W_{8,9}$= 5 μm, $L_{1,2,4,5}$=0.36 μm, L_3=0.72 μm, C_{f1}, C_{f2} and R_{f2} are for providing a proper initial control voltage.

by employing a large tail resistor R_3 in the charge pump and by biasing M_{11} of the comparator in the sub-threshold with V_b≈0.38 V. Note that a large V_b will significantly increase the power consumption of the comparator. An overly small V_b, on the other hand, will severely reduce the speed of the comparator. Similarly, the biasing voltage of the integrating feedback circuit is set to approximately 0.38 V to minimize its power consumption.

4.5 Simulation Results

To validate the results presented in the paper, an injection-locked relaxation oscillator with integrating feedback has been designed in TSMC-0.18μm 1.8V 6-metal 1-poly CMOS technology and analyzed using SpectreRF from Cadence Design Systems using BSIM3V3 RF device models that account for the effect of device parasitics and process variations. The layout of the designed chip and the micro-photo

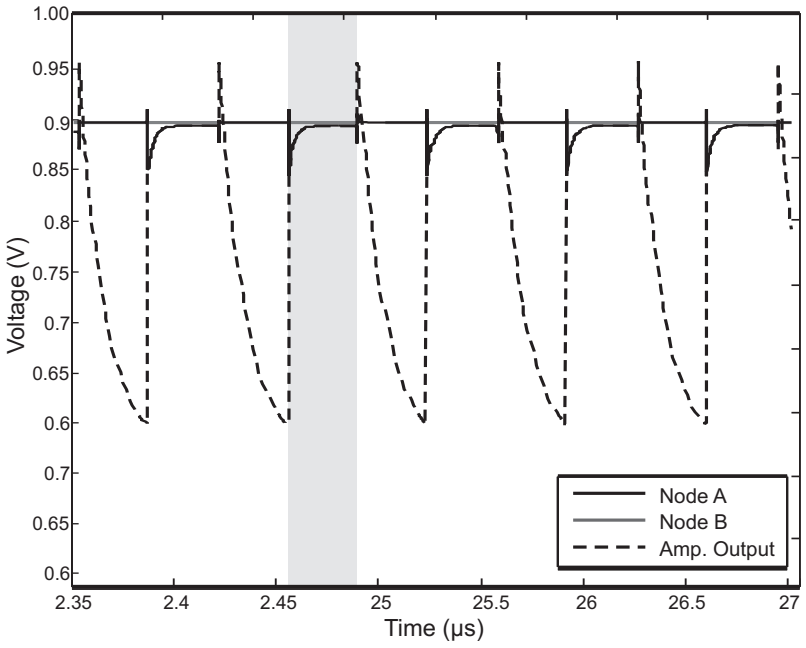

Figure 4.10: Simulated voltages at the output of the amplifier, node A, and node B.

of the fabricated chip are shown in Fig.4.11 and Fig.4.12, respectively.

4.5.1 Injection Locking of Relaxation Oscillator without Integrating Feedback

To examine the injection locking of the relaxation oscillator without integrating feedback, the free-running frequency of the oscillator is varied from 975.9 KHz to 902.9 KHz while injecting a 10 mV amplitude, 1 MHz sinusoidal signal. Considering the 50 nA charge pump current running through the timing capacitor, maximum power drawn from a 10 mV sinusoid injection source is 640 pW. Fig.4.14 shows the simulation results. In the first plot, the free-running frequency of the oscillator is 975.9 KHz. Because frequency displacement is small, the oscillator is locked to 1 MHz. In the second plot, the free-running frequency is set to 969.1 KHz. The oscillator nearly locks to the injected signal but its phase slips eventually. In the the third plot, the free-running frequency is set to 962.4 KHz. The injection signal is outside the lock range. The oscillation frequency of the oscillator approaches

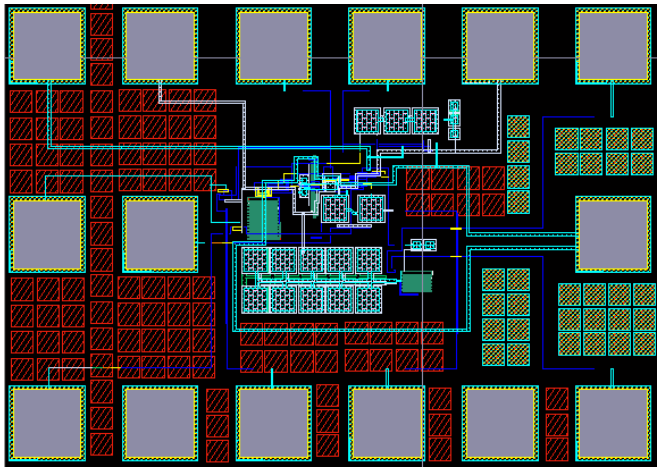

Figure 4.11: Layout of IL-PLL. Pads are arranged as per the probes available to us.

the injection frequency but falls back after a short time. In the last plot, the free-running frequency is set to 902.9 KHz. The injection signal is outside the lock range. This state is known as the fast-beat where the frequency varies sinusoidally with its mean value close to the free-running frequency [22]. Fig.4.13 shows the simulated waveform of the output voltage of the integrator and that of the oscillator. As can be seen that the voltage of the timing capacitor is immediately set to V_{DD} when its voltage exceeds $V_{ref} = 0.5$ V and reset to 0 when its voltage drops below 0.5 V.

4.5.2 Injection Locking of Relaxation Oscillator with Integrating Feedback

The simulation results presented in Fig.4.14 show that when the free-running frequency of the oscillator is less than 969.1 KHz, the oscillator fails to lock to the injected 1 MHz sinusoidal signal. Fig.4.15 plots the simulation results of the oscillator when integrating feedback is present. Although the free-running period of the oscillator is outside the lock range of the oscillator without integrating feedback, the oscillator successfully locks onto the injected signal when the integrating feedback is present.

Fig.4.16 shows the effect of injection index on the locking process. It is seen that the larger the injection index, the faster the locking process. This agrees well with

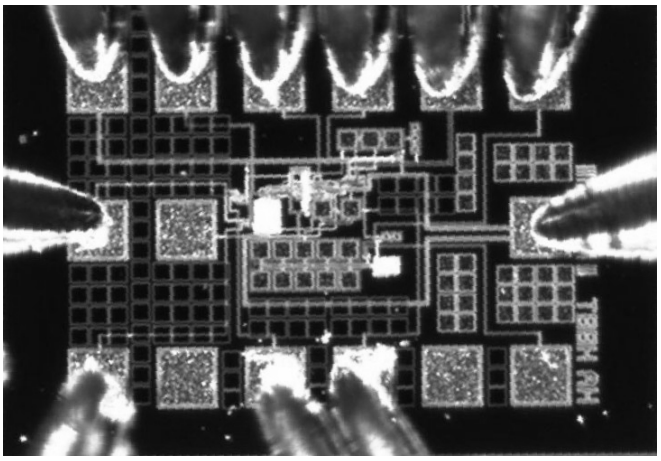

Figure 4.12: Micro-photo of fabricated IL-PLL chip with probes shown.

the theoretical results derived earlier.

Fig.4.17 plots the control voltage of the oscillator with integrating feedback at four process corners. It is seen that the oscillator with integrating feedback locks to the injection signal in less than 200 μs at all process corners.

Fig.4.18 plots the frequency locking of the oscillator with integrating feedback at four process corners. The different initial oscillation frequencies of the relaxation oscillator are the results of the variation of the process parameters at the process corners. As can be seen from the figure that at all the process corners, the oscillator successfully locks to 1 MHz.

Fig.4.19 compares the injection locking of the relaxation oscillator with and without the integrating feedback when the free-running period of the oscillator is set to 902.9 KHz. It is seen that when the integrating feedback is absent, the oscillator fails to lock to the injected 1 MHz signal. However, when the integrating feedback is present, the oscillator locks to the injected signal in less then 100 μs.

The minimum amplitude of the injection signal to ensure that the oscillator with the integrating feedback will lock is found to be 25 mV. Injection signals with large amplitude will improve the lock speed. When the injection signal is removed, the frequency of the oscillator with the integrating feedback drifts at a rate of 5 Hz/ms. This drift is negligible as backscattering from transponders to their base station typically take only a few milliseconds to complete. For the same

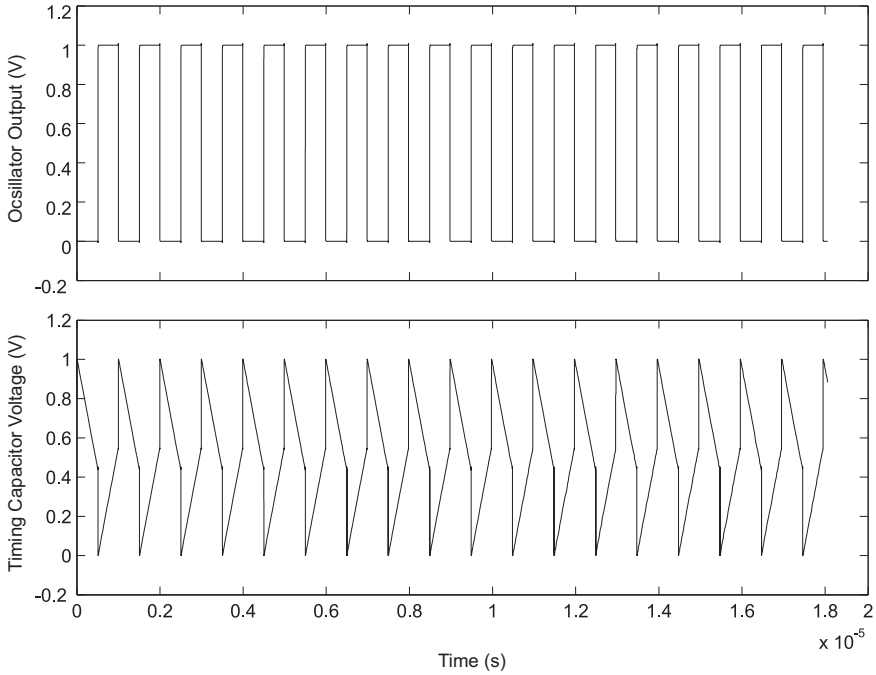

Figure 4.13: Simulated (post-layout) waveform of the output voltage of comparator (top) and that of timing capacitor of proposed injection-locked relaxation oscillator with integrating feedback (bottom).

argument, the effect of temperature variation on the frequency of the oscillator during backscattering can also be neglected safely.

4.6 Measurement Results

The measurement setup for testing the proposed IL-PLL is shown in Fig.4.20. The injection signal is provided by a Agilent E4420B function generator and applied directly to the negative terminal of the timing capacitor. The output of the oscillator is buffered using three inverter stages. The supply voltage of these buffers comes from a separate pad, allowing one to measure the power consumption of the IL-PLL. On-wafer probing is conducted using a Cascade Microtech RF-1 probe station with four MH5 positioners, RF and dc probes. The current consumption of the chip is measured using a HP 34401A digital multi-meter.

Fig.4.21 is the measured output waveforms of the IL-PLL lock at 1.4 MHz captured

using a Tektronix TDS3012B oscilloscope. The distortion in the waveform is caused by the small size of the output buffer of the oscillator and the unexpected large input capacitance of the oscilloscope. It is seen that the frequency of the output voltage of the VCO is the same as that of the fundamental.The proposed IL-PLL can also lock to the harmonics of the input signal, as evident from Fig.4.21.

In order to test the relaxation oscillator and the IL-PLL system separately, a control signal SW that can enable or disable the integrating feedback is included in chip design. When SW=0, the switch connects the control line of the oscillator to the pad and turns off the power supply of the integrating feedback, allowing the relaxation oscillator to be tested separately. Note that in the stand-alone test of the oscillator, the injection signal can still be applied to the oscillator, making it possible to measure the lock range in the absence of the feedback. When SW=1, the control line is disconnected from the pad and the supply voltage to the feedback circuit turns on. In this setup, even though the control line of the oscillator is disconnected from the pad, the pad itself should not be connected to any source such that the leakage of the switch does not corrupt the small signal from the feedback.

Fig.4.22 plots the measured lock range of the oscillator with and without the integrating feedback, together with simulation results. It is seen that the lock range of the oscillator with the integrating feedback increases with the rise of the injection amplitude initially and the rate of increase gradually levels off. The lock range of the oscillator without the integrating feedback, on the other hand, continues to increase with the injection amplitude. Also observed is that the lock range of the oscillator with the integrating feedback is approximately one order of magnitude larger as compared with that without the integrating feedback. The increased lock range is critical to ensure that passive wireless transponders will lock to the injected signal.

Fig.4.22 also quantifies the super-harmonic lock range of the oscillator with and without the integrating feedback at the third harmonic (4.2 MHz) and third harmonic (7 MHz) of the locked frequency.

The minimum supply voltage to ensure the stable operation of the IL-PLL is found to be 1.2 V, slightly more than 1 V used in simulation. Table 4.1 summarizes the

Table 4.1: Performance summary of proposed IL-PLL.

Technology	TSMC-0.18μm 1.8 V 6-metal CMOS
Supply voltage	1.2 V
Injection signal	10 mV (640 pW), 1.4 MHz sinusoid
Lock time	approx. 150 μs at SS corner
	approx. 60 μs at SF corner
	approx. 100 μs at FF corner
	approx. 30 μs at FS corner
Lock range	30 KHz w/o integrating FB (full range)
	430 KHz with integrating FB
Chip area	850 μm $\times$ 600 μm including pads
Power consumption of VCO	525 nW
Power consumption of IL-PLL	960 nW

performance of the system.

4.7 Chapter Summary

The issue of clock frequency calibration in passive transponders along with some of the current techniques were briefly discussed. Theory of injection locking and pulling in non-harmonic oscillators was presented and an analytical model of this phenomenon in relaxation oscillators was derived. A new technique for increasing the locking range of oscillators under injection was introduced. The technique uses an integrating feedback that accumulates the frequency variations caused by the injection and adds that to the intrinsic frequency of the oscillator. Besides increasing the lock-range, this technique also causes the injection-locked frequency to hold after the injection source is removed.

To implement the proposed frequency calibration system, a new ultra-low power relaxation oscillator was designed. Unlike the relaxation oscillator topologies commonly used in transponders [24, 60, 23], the proposed design uses only one timing capacitors which makes it much more suitable for injection locking.

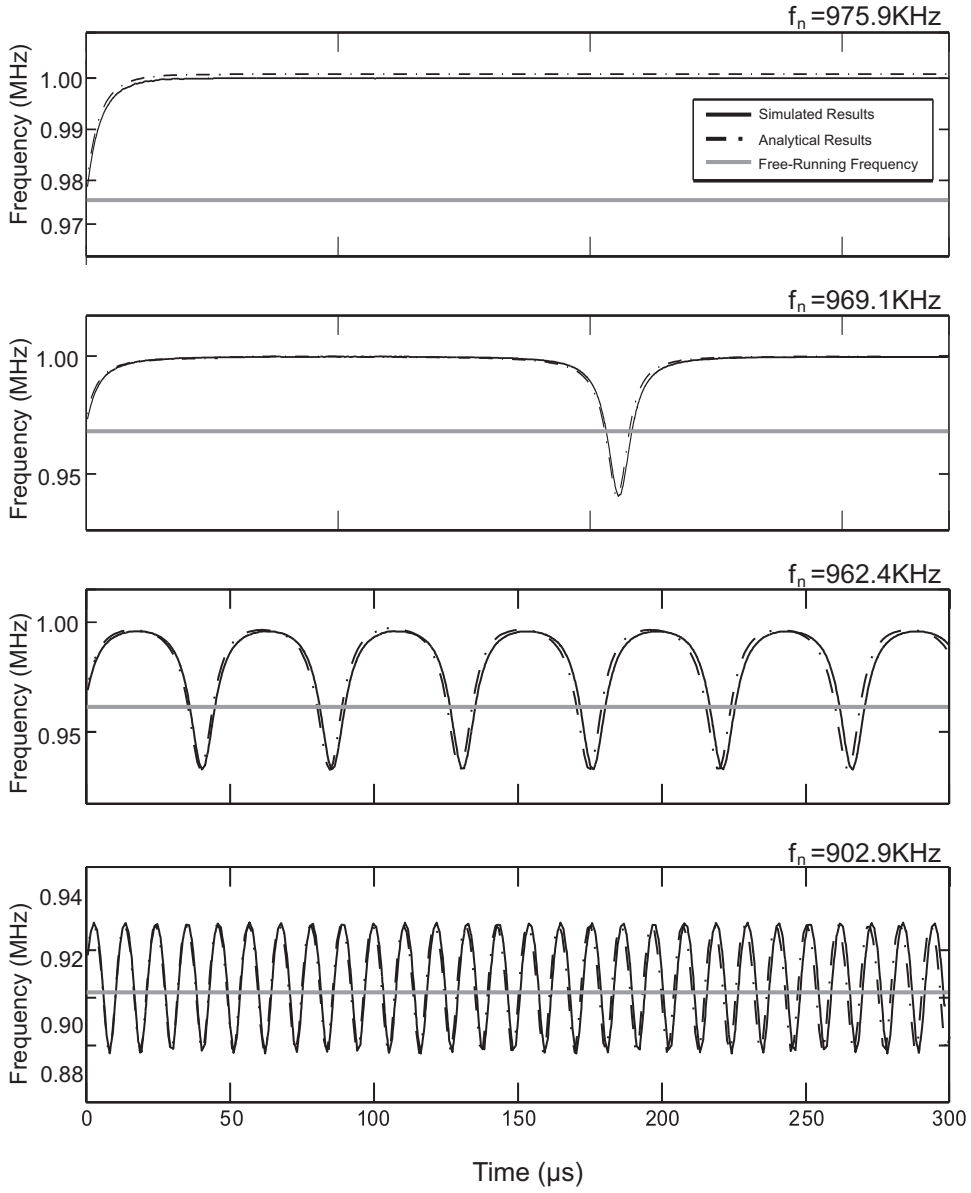

Figure 4.14: Simulated effect of the injection of a sinusoidal current on the frequency of the relaxation oscillator without integrating feedback at various frequency offsets from the injection frequency. Legends : Solid line - simulation results. Dotted line - Analytical results.

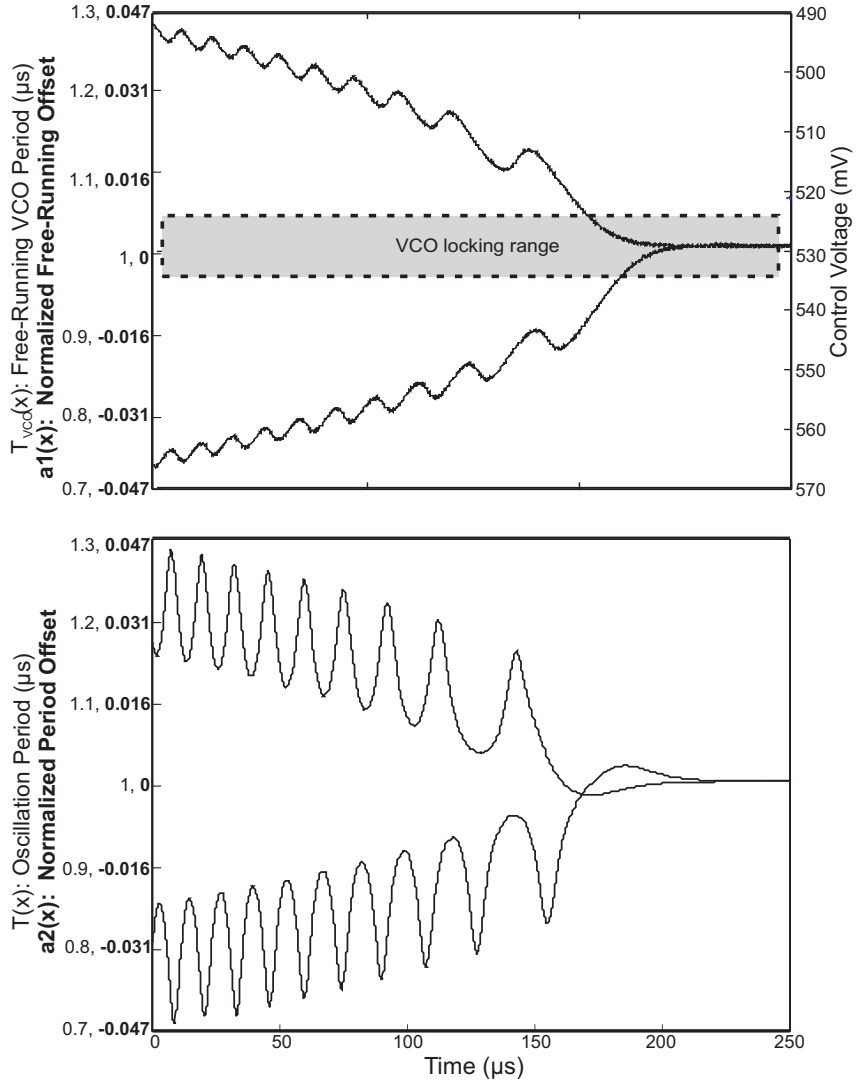

Figure 4.15: Simulated effect of integral feedback on oscillator period outside the lock range. It can be seen that the feedback shifts the period towards the lock range.

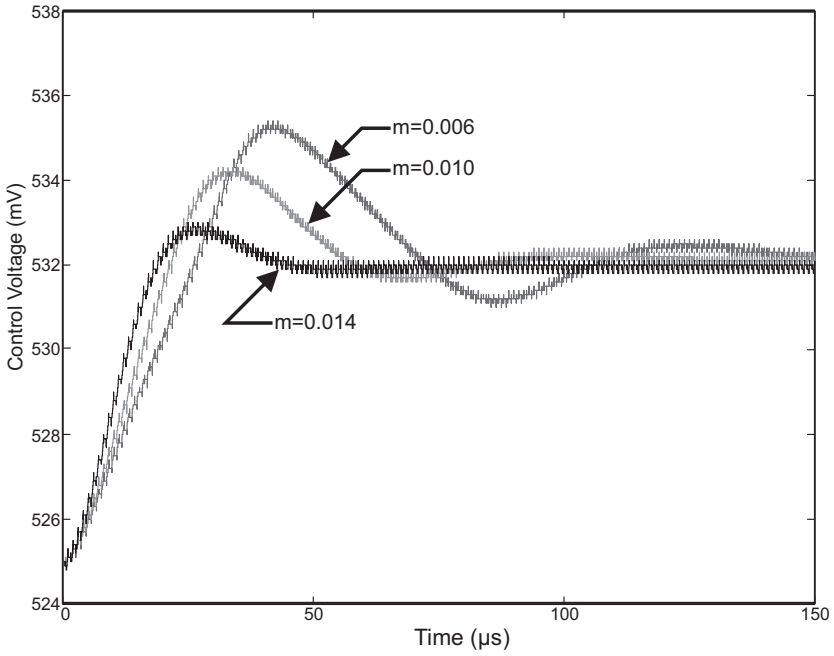

Figure 4.16: Simulated effect of the injection of sinusoidal current on the frequency of the relaxation oscillator at different offsets from injection frequency.

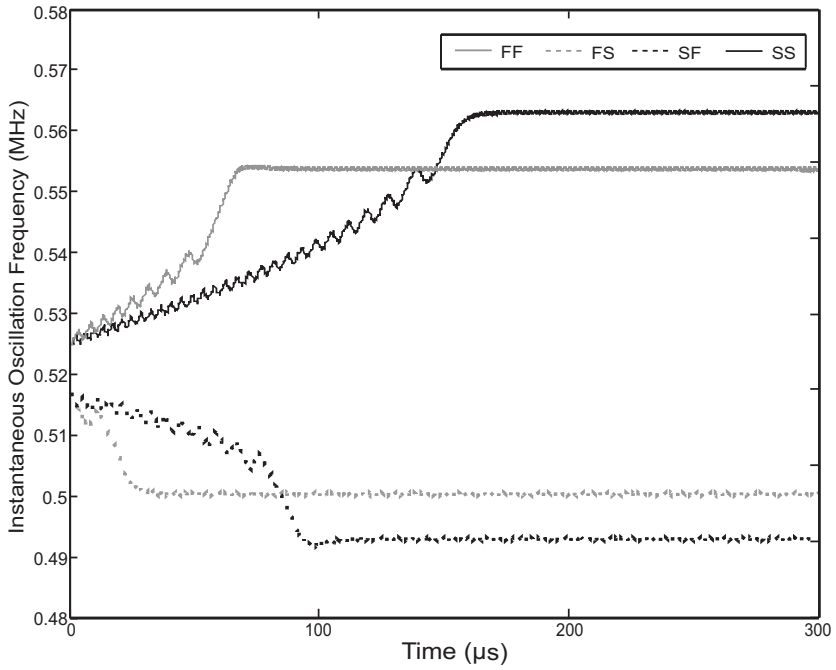

Figure 4.17: Simulated control voltage of proposed injection-locked relaxation oscillator with integrating feedback at process corners. SS - slow nMOS/slow pMOS, FF - fast nMOS/fast pMOS, FS - fast nMOS/slow pMOS, and SS - slow nMOS/slow pMOS (post-layout).

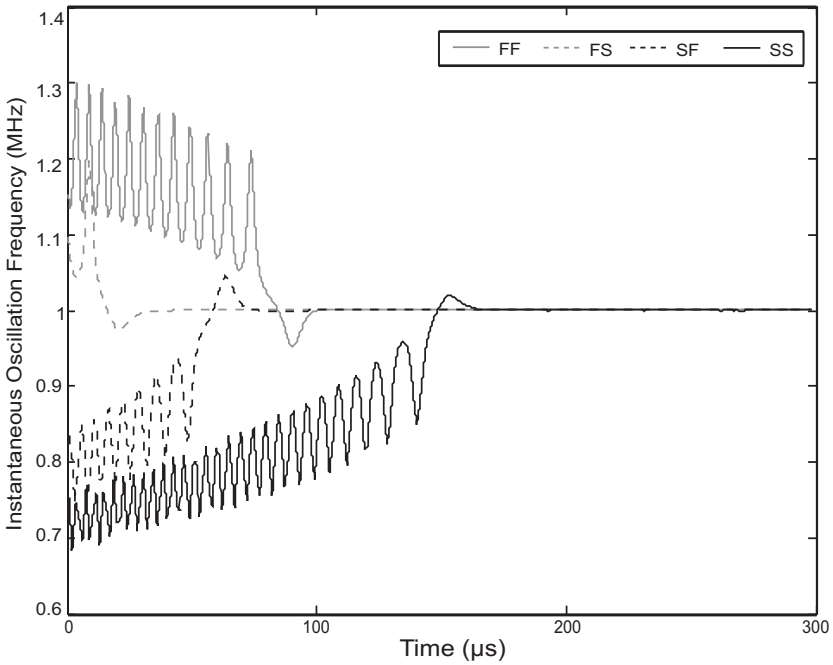

Figure 4.18: Simulated frequency locking of proposed injection-locked relaxation oscillator with integrating feedback at process corners (post-layout).

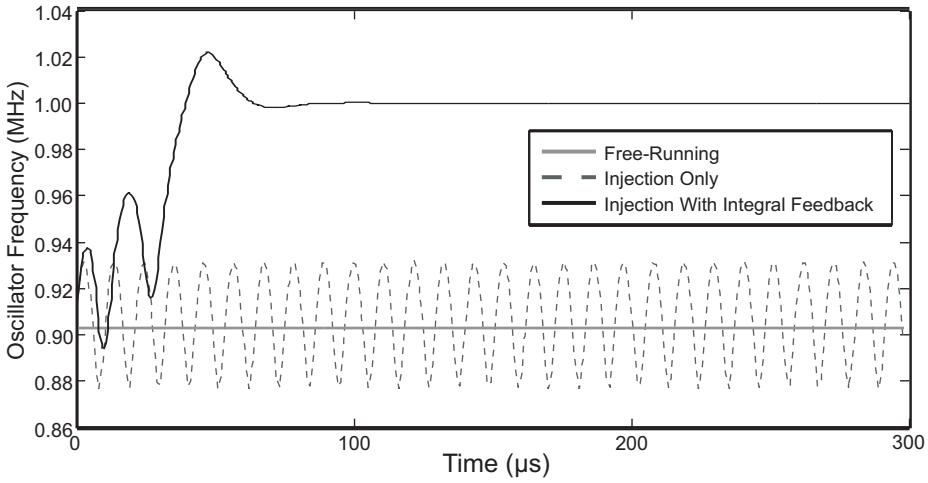

Figure 4.19: Comparison of locking process of relaxation oscillator with and without integrating feedback in the nominal process conditions. Legends : Light-colored solid line - Without both injection and integrating feedback. Dashed line - With injection only. Dark-colored solid line - With both injection and integrating feedback. The small variation of the frequency of the oscillator with integrating feedback after locked is due to the large relative tolerance used in simulation (reltol = 10^{-3}). The variation is removed when a smaller reltol is used.

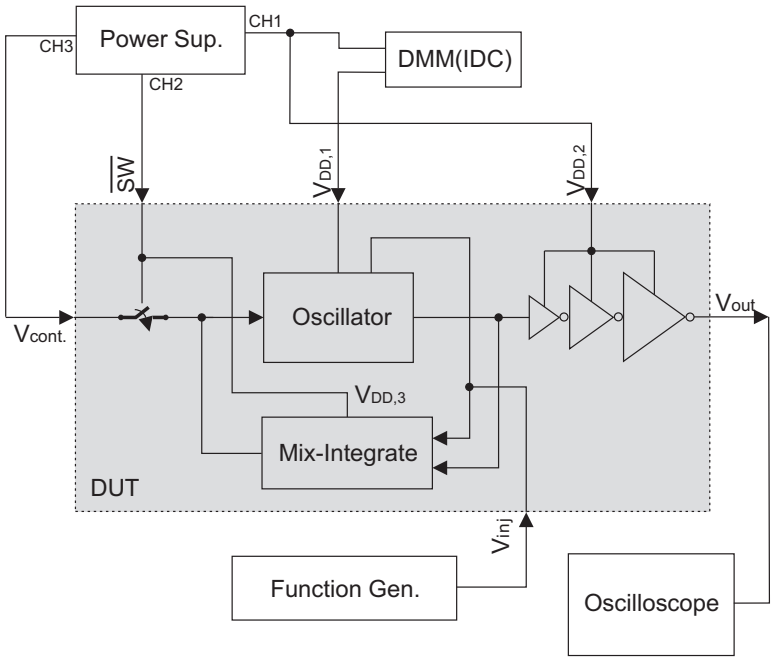

Figure 4.20: Measurement setup.

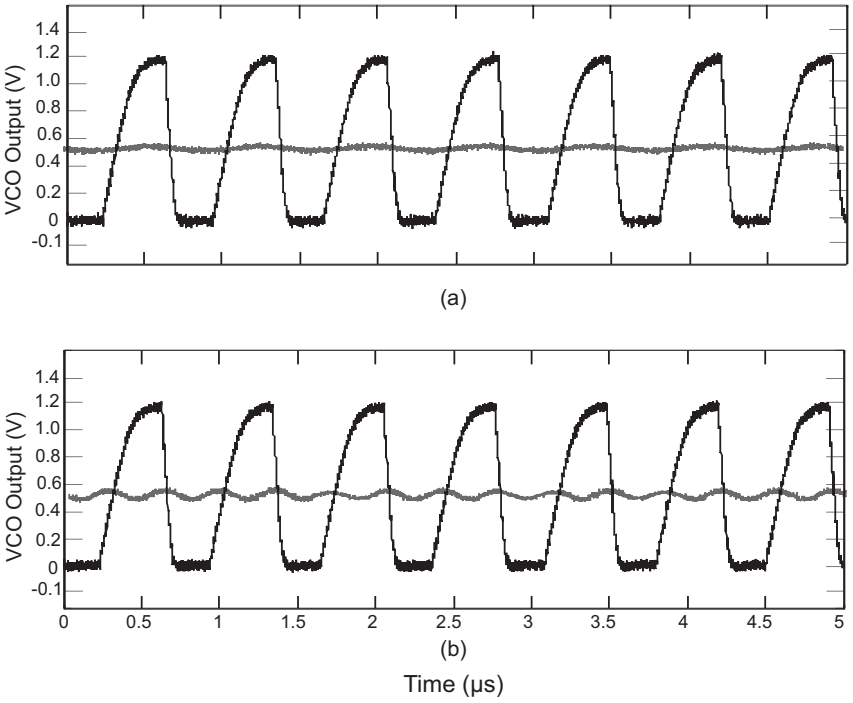

Figure 4.21: Measured waveform of the output voltage (square wave) of the oscillator of the IL-PLL locked at 1.4 MHz with fundamental (top) and the second harmonic (bottom) of the locking frequency. The sinusoid is the injected signal.

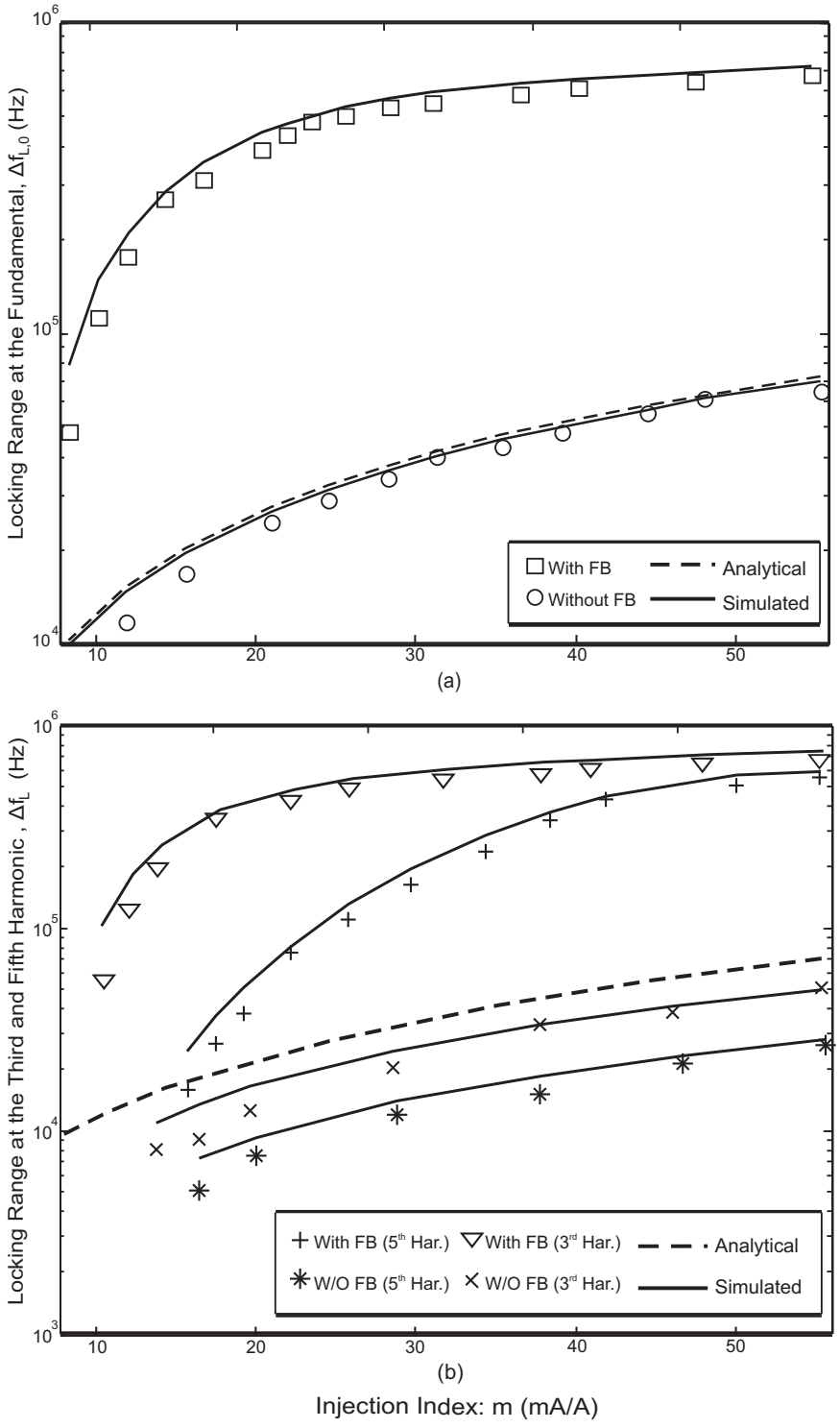

Figure 4.22: Measured locking range of the oscillator and IL-PLL injected with (a) the fundamental, and (b) 3rd and 5th harmonics of the locking frequency. The results from both analytical model and simulation are also plotted for the purpose of comparison.

Chapter 5

Conclusions and Future Work

5.1 Summary

This thesis has made contributions to the area of passive communication circuits and systems. The designs presented were primarily aimed at minimizing the power consumpion/loss in the analog front of passive transponders thereby increasing the amount of power available to the digital back end. The designed proposed in this thesis are summarized as follows.

A new step-up transformer impedance-matching and gain-boosting technique to improve the efficiency of power harvesting of passive wireless microsystems has been presented. The large voltage gain is delivered using a transformer with large turn ratio. The series resistance of the primary winding is made much smaller by using multiple metal layers while the tracks of the secondary winding are made much narrower than that of the primary winding such that both the series and shunt winding losses of the transformer are minimized, which are the major limit on the maximum gain attainable using on-chip matching. The detailed analysis of the proposed method has been presented. Measurement results of the proposed impedance-matching and gain-boosting network–implemented in TSMC-0.18μm 1.8 V 6-metal CMOS technology with thick metal option– have demonstrated that the proposed step-up transformer impedance-matching and gain-boosting technique significantly improves the power sensitivity and efficiency as compared with the widely used LC

matching network.

A remote frequency calibration method that allows a passive UHF wireless transponder to adjust the oscillation frequency of its local oscillator to a desired frequency using a low-power injection-locked phase-locked loop has been proposed. A new relaxation oscillator with a current pulse generator and a single MIM capacitor has also been proposed to generate the effective hysteresis needed for oscillation without using a Schmitt trigger, thereby avoiding the drawback of the high sensitivity of the frequency of conventional Schmitt trigger relaxation oscillators to supply voltage fluctuation. The power consumption of the proposed IL-PLL is minimized effectively by operating both the charge pump and comparator in the subthreshold. Integrating feedback has been employed to increase the lock range and hold the oscillation frequency of the oscillator when the injection signal is removed. A detailed analysis of the injection locking of relaxation oscillators has been presented. The loop dynamics of the proposed IL-PLL have also been investigated in detail. The theoretical results of the proposed IL-PLL presented have been evaluated using both simulation and measurement results. The locking range of the proposed IL-PLL is 13 time larger than that of the stand-alone oscillator. The minimum amplitude of the injection signal required to lock to the injection signal at all process corners has been found to be 25 mV. When the injection signal is removed, the frequency of the oscillator with the integrating feedback drifts at a rate of 5 Hz/ms. This drift is negligible as backscattering from transponders to their base station typically take only a few milliseconds to complete. For the same argument, the effect of temperature variation on the frequency of the oscillator during backscattering can also be neglected safely.

5.2 Future Work

The designs proposed in this thesis were aimed at the development of smaller, more efficient passive wireless devices. The general direction of future work for this research shall be toward the design and development of the entire microsystems such that they will make most of the advantages provided by these essential improvements.

The obvious bottle neck for the development of small RFID tags and transponders is the size of the antenna. The power harvesting technique introduced in this thesis is most effective–as shown theoretically and through simulations– for matching electrically small antennas. Using the technique proposed here, smaller dipole antennas can be efficiently matched to the chip while providing the high impedance transfomation ratio essential for driving ultra-low power devices. Design of electrically small–possibly integrated–antennas will be the most effective step in future developments.

The phase locking technique introduced for frequency calibration in this thesis can be used as an essentional block in ultra-low power data communication. Using the proposed IL-PLL, development of ultra-low power circuits that can effectively demodulate FM and PM signals with small AM subcarries will facilitates construction of more sensitive RF fronts capable of operating at farther distances from the reader.

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