A LOW-VOLTAGE CMOS CURRENT-MODE INCREMENTAL SIGNALING SCHEME FOR HIGH-SPEED PARALLEL LINKS

by

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Abstract

Title of Thesis: **A low-voltage CMOS Current-Mode Incremental Signaling Scheme For High-Speed Parallel Links**

Tao Wang, Master of Applied Science, 2006

Thesis Directed By: Dr. Fei Yuan,
Electrical and Computer Engineering Department

Point-to-point parallel links are widly used in short-distance high-speed data communications. For these links, the design goal is not only to integrate a large number of I/Os in the systems, but also to increase the bit rate per I/O. The cost per I/O has to be kept low as performance improves.

Voltage and timing error sources limit the performance of data links and affect its robustness. These kinds of noise impose greater challenges in parallel data links, such as inter-signal timing skew and inter-signal cross-talk. The use of low-cost schemes, such as single-ended signaling, is effected signaficantly by the voltage and timging noise. Fully differential signaling scheme, two physical paths per signal channel, significantly increases the cost of system. Therefore, overcoming the voltage noise, keeping the cost low are two challenges in high-speed parallel links.

In this thesis, we propose a new current-mode signaling scheme called current-mode incremtnal signaling for high-speed parallel links. Also, the circuits of the receiver called current-integrating receiver are presented. To assess the effectiveness of the proposed signaling scheme, a 4-bit parallel link consisting of four bipolar current-mode drivers, five 10 cm microstrip lines with a FR4 substrate, and four proposed current-integrating receivers is implemented in UMC 0.13μm, 1.2V CMOS technology and analyzed using *SpectreRF* from Cadence Design Systems with BSIM3V3 device models. Simulation results demonstrate that the proposed current-mode incremental signaling scheme and the current-integrating receiver are capable of transmitting parallel data at 2.5 Gbyte/s.

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Chapter 1

Introduction

1.1 Motivation

The exponential growth in both the speed and the level of integration of digital integrated circuits(ICs) has increased the demand for high IC-to-IC communication bandwidth to maximize overall system performance. Traditionally, system designers have addressed this issue by increasing the number of high-speed signals, leading to an increase in both the cost and complexity of systems. In order to maintain a balanced system, however, per-pin interconnection bandwidth must scale with the speed and the level of integration of ICs.

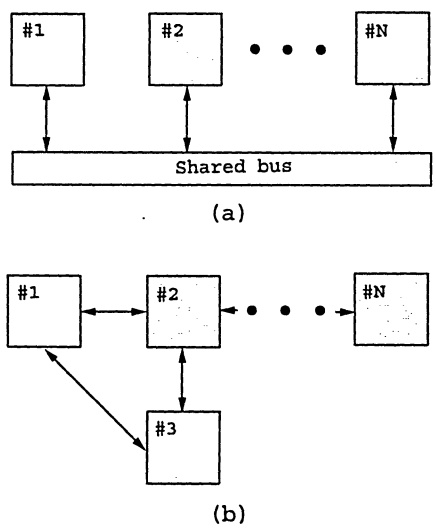


Figure 1.1: (a) Shared buses; (b) Point-to-point links.

As shown in Fig. 1.1, there are two dominant approaches for high-speed signaling: shared buses and point-to-point links. In the conventional shared bus approaches, many links are integrated within a single system to increase the total signaling bandwidth. The large number of links makes the overall overhead (area, power, latency) a key constraint of the design. This constrain dictates that a shared bus approach limits the maximum bandwidth per channel. In contrast, the goal of high-speed point-to-point links is to maximize communication bandwidth and distance of a single link. Point-to-Point signaling links offer an excellent solution for applications that require multi-gigabit per second [1].

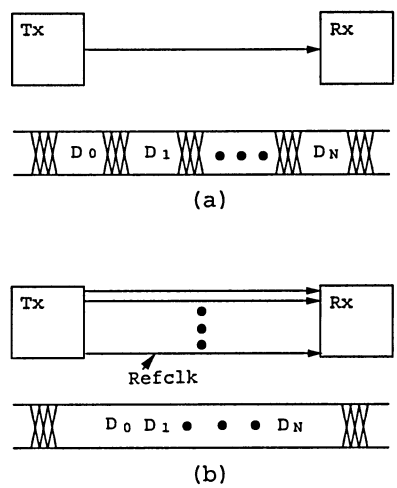


Figure 1.2: (a) Serial links; (b) Parallel links.

As shown in Fig. 1.2, Point-to-Point links can be divided into two classes: serial links and parallel links. A serial link transmits a stream of data along a channel while a parallel link transmits several streams of data over multiple channels. This thesis focuses on parallel links.

Generally, the fully differential signaling scheme is widely used in parallel links to effectively suppress common-mode noise. The need for two physical paths per signal channel, however, significantly increases the cost of implementing this signaling scheme in terms of on-chip interconnect count, off-chip printed circuit board trace count, and chip I/O pin count. Pseudo-differential signaling where a common reference is shared by a set of signal channels,

usually limited to four, can effectively reject common-mode disturbances while keeping the total number of physical paths low. The physical displacement between the signal paths and the common reference path, however, degrades its ability to reject common-mode noise. A voltage-mode incremental signaling scheme was proposed in where only $N + 1$ physical paths are needed for N parallel signal channels. [2] Common-mode rejection is achieved by amplifying the signals of physically adjacent paths with differentially configured receivers. The drawbacks of voltage-mode signaling, such as low signal swing, high switching noise injection, and high sensitivity to supply voltage fluctuation and ground bouncing, as well as the need for N encoders in transmitters or equivalently N peak detectors and decoders in receivers, however, limit its data rates and increase the power consumption. So, the challenge of this thesis is how to efficiently overcome these design difficulties.

1.2 Original Contributions

This thesis presents a new current-mode incremental signaling (CMIS) scheme where data transmitted to the channels are represented by branch currents rather than nodal voltages for multi-Gbps parallel links.

The proposed signaling scheme requires only $N + 1$ physical paths for N parallel signal channels. The current-mode signaling of the proposed scheme not only ensures that the delay of the critical nodes of the links is minimized by lowering both the voltage swing and the impedance of the nodes, it also enables large signal swing in the presence of a low supply voltage. As a result, both the power consumption and switching noise injection are greatly reduced.

A fully differential transimpedance front-end with inductive shunt peaking is proposed to provide a low, tunable, and resistor-free matching impedance to the channels such that not only the signal reflection at the far end of the channels is eliminated, the effect of the large capacitance of the channels on the data rate of the links is also minimized.

A fully differential current-integrating receiver consisting of a transimpedance front-end and an integrator is proposed to effectively suppress transient disturbances coupled to the

channels.

To enable a fast sensing and latching, new fully differential class A and class AB current-mode integrating architecture and sense amplifierclass are proposed.

Publications of this research.

- Tao Wang and Fei Yuan, "A new current-mode incremental signaling scheme with applications to Gb/s parallel links," *IEEE Transactions on Circuits and Systems I - Regular Papers.* Accepted for publication in August 2006.

- Fei Yuan and Tao Wang, "CMOS current-mode integrating receiver for Gbytes/s parallel links," *Microelectronics Journal.* Submitted in June 2006.

- Tao Wang and Fei Yuan, "A new current-mode incremental signaling scheme with applications to Gb/s parallel links," *IEEE Int'l Symp. Circuits and Syst.(ISCAS2006), Kos, Greece.* Accepted for publication in Jan. 2006.

- Tao Wang and Fei Yuan, "A novel current-mode incremental signaling scheme for high-speed parallel links," *IEEE MidWest Symp. Circuits and Systems (MWSCAS2005),* pp.1802-1806, Cincinnati, Aug. 2005.

- Tao Wang and Fei Yuan, "A new CMOS current integrating receiver for Gbyte/s parallel links," *IEEE MidWest Symp. Circuits and Systems.* Accepted for publication in May. 2006.

1.3 Thesis Organization

The thesis is organized as follows:

Chapter 2 describes basical data link schemes and two fundamental challenges in high-speed data communication design: the voltage noise, timing recovering.

Chapter 3 examines electrical signaling schemes for data communications over wire channels.

Chapter 4 introduces the current-mode incremental signaling scheme and describes the intrinsic advantages of current-mode signaling in high-speed data links. A fully differential transimpedance front-end for parallel links is presented.

Chapter 5 details the design of the fully differential current-integrating front-end. Transient disturbances coupled to the channels may significantly alter the amplitude of the received data and result in erroneous results. A current-integrating scheme was proposed to minimize the effect of this kind of high-frequency disturbances.

Chapter 6 introduces a class A sense amplifier with CMOS active inductor shunt peaking. A class AB configured sense amplifier that provides a voltage gain that is twice that of class A sense amplifier is also proposed.

In Chapter 7, a 4-bit parallel links consisting of four bipolar current-mode drivers, five 10 cm microstrip lines with FR4 substrate, four current-integrating receivers are implemented in UMC 0.13μm, 1.2V, 8-metal CMOS technology and analyzed using *SpectreRF* from Cadence Design Systems with BSIM3V3 device models that account for both the parasitics and high-order effects of devices. Simulation results are presented

The thesis is concluded in Chapter 8.

Chapter 2

Background

This chapter gives an overview of electrical signaling schemes for data communications over wire channels. Basic concepts of data communications and fundamental challenges in high-speed data communication design are investigated.

2.1 Fundamentals Of Data Links

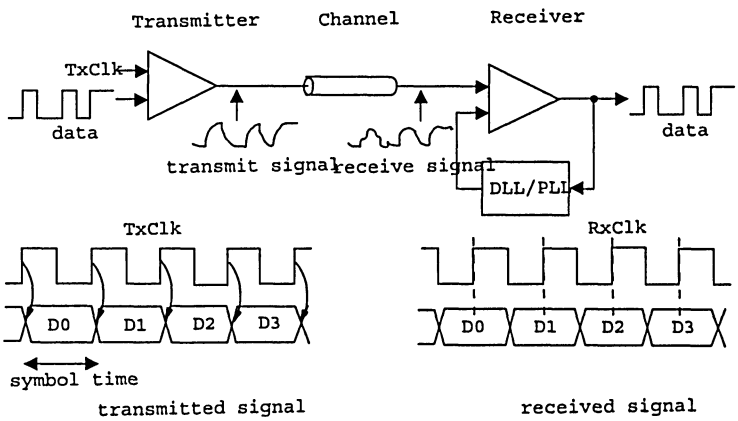


Figure 2.1: Basic data link.

There are three primary components in a data link: a transmitter, a channel, and a receiver. The transmitter converts a digital data sequence into an analog signal and conveys it to the channel. The receiver converts the received analog signal to a digital data sequence. Fig. 2.1 illustrates these key components and their operation.

The transmitted signal is a digital signal, and is transmitted in phase with the transmitter clock, TxClk. The duration between successive signal transitions is called symbol time.

The channel is typically a cable or a printed-circuit board (PCB) trace through which signals propagate from the transmitter to the receiver. The channel is the origin of many voltage noise sources and imposes an increasingly challenging design constraint as data rates continue to increase. For example, the frequency-dependent attenuation of PCB traces or cables distorts the received signal and gives rise to an inter-symbol interference (ISI). Another source of noise comes from impedance discontinuity at both the transmitter and receiver packages. Cross-talk from nearby signals also contributes to noise.

The receiver recovers the data sequence from the received signal stream. The receiver amplifies and smaples the receive signal, using a timing recovery circuit to optimally position the receiver clock, RxClk, to sample the data. The logic stage of this sampled data is determined by a voltage comparator with a reference voltage V_{ref}. Generally, the value of V_{ref} is half of signal swing. The heart of the timing recovery circuit is a phase-locked loop (PLL). The PLL is to lock the output clock to a timing reference using negative feedback, as shown in Fig. 2.2.

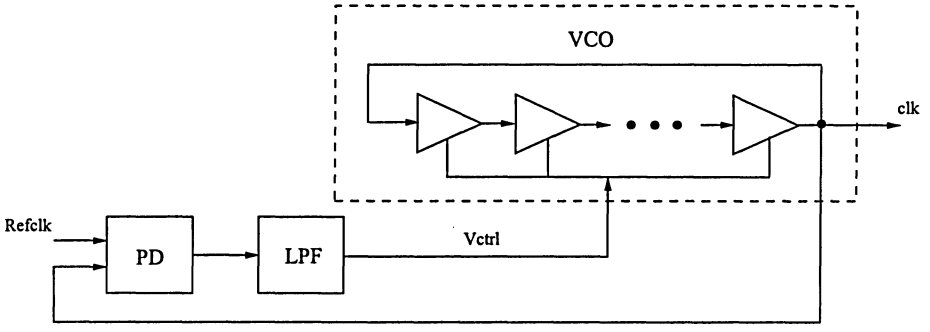


Figure 2.2: Phase-locked loops.

A simple VCO based PLL consists of a phase detector (PD), a low-pass filter (LPF), and a VCO. The PD converts the phase difference between the input and output clocks into an output signal whose average DC voltage level is proportional to the phase error. This signal is smoothed out by the LPF to generate the control voltage (V_{ctrl}), which then drives the

VCO and determines its oscillation frequency.

2.2 Data Format

Transmitters generally have an encoder, while receivers have a decoder. A great variety of encodeing and decoding schemes (a scheme determines what bit patterns should be used to represent the messages to be communicated) exist for data communications. Here, we introduce two basic schemes that are widely used in date communications.

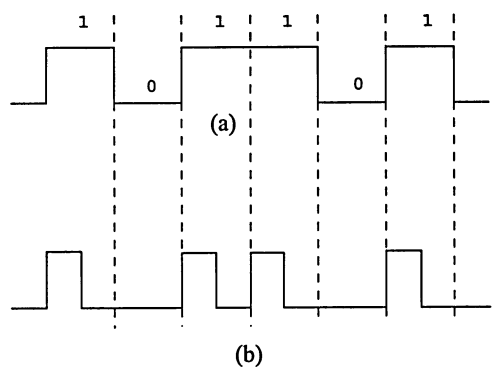


Figure 2.3: (a) NRZ data formats; (b) RZ data formats.

Transmitted signal in digital sequences are "non-return to zero" (NRZ), NRZ differs from "return to zero" (RZ) data format, in which each bit consists of two sections: the first section assumes a value that represents the bit value, and the second setion is always equal to a logical zero, as shown in Fig. 2.3. It is obvious that RZ exhibits a more "transition dentsity" than NRZ does. However, RZ occupies about twice as much bandwidth as NRZ data does. "DC-Balance" coding schemes, such as 8B/10B coding, are used with NRZ to guarantee enough transitions in the symbol stream, making NRZ more effeciently in high speed data communications [4].

2.3 Serial Links and Parallel Links

Point-to-Point links can be divided into two classes: serial links and parallel links. A serial link transmits a stream of data over a channel while a parallel link transmits several streams of data over multiple channels. Serial links are shown in Fig. 2.4. Due to a single channel between the transmitter and the receiver, parallel data of lower data rates are multiplexed to generate a high-speed serial signal. Clock information is embedded in the data, which is sent over the channel. The receiver recovers the embedded clock from the signal transitions and aligns its local clock accordingly for an optimal data detection.

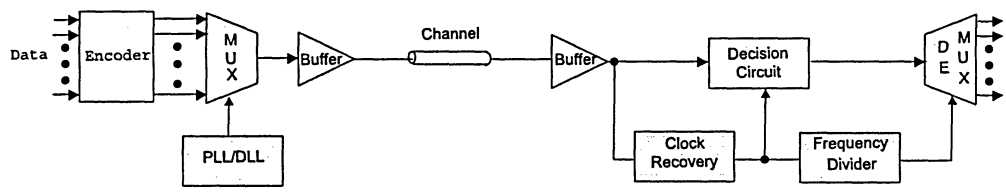


Figure 2.4: Block diagram of serial links.

Parallel links use an explicit channel to transmit the clock. Fig. 2.5 shows the block diagram of source-synchoronous point-to-point parallel links. All data signals ($D_0 \sim D_N$) and a reference clock siganl (refClk) are transmitted synchronously on one/both of edges of TxClk. At the recevier, a phase-locked loop generates a RxClk by delaying the recevied refClk by half the symbol time. This RxClk is then used to sample all incoming data signals in the middle of the data eyes to maximize timing margins.

At the first sight it would seem that a serial link is inferior to a parallel one, because it transmits less data in each clock cycle. However, serial links can be clocked much faster than parallel links, and offer a higher data rate. This is because:

1. Clock skew between different channels of parallel links is not an issue.

2. A serial connection requires a fewer interconnecting cables and hence occupies a less space. The extra space allows for a better isolation of the channel from its surroundings.

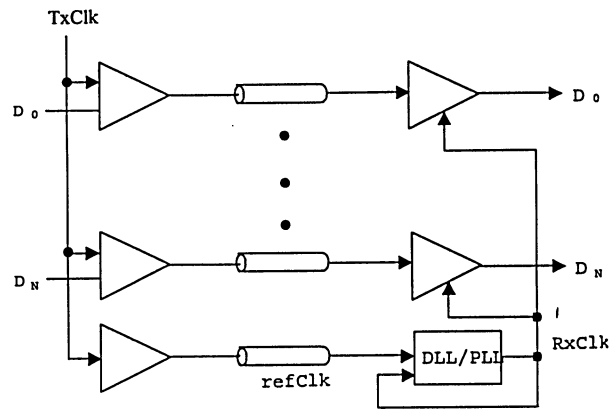


Figure 2.5: Block diagram of source-synchronous parallel links.

3. Crosstalk is reduced because there are a fewer conductors in the proximity.

Serial links are a better option in applications where the cost of communication channels is high and the distance of transmission range is large. However, parallel links have been widely used in short-distance and low-cost applications, such as multiprocessor systems, processor-to-memory interconnections, and network switches. For example, at a given signaling rate, the distance over which one can reliably transmit a signal is limited by the frequency-dependent attenuation of the transmission medium. Due to this reason, for long-distance high-speed serial links, special techniques, such as pre-emphasis and post-equalization, are used to compensate for the channel loss. This will lower the data rate and increase the level of the power consumption.

2.4 Receiver Voltage and Timing Margins

Fig. 2.6 shows the eye diagram of the received signal, formed by wrapping the received signal waveform around one symbol time. The received signal can be sampled at the middle point of the data eye. The voltage margin is the voltage range the receiver can move its decision threshold and can still correctly determine the logic state of the received signal. The timing margin is the time difference the receiver can shift RxClk and can still accurately detect the

logic state of the received data. Ideally, the received signal would have a voltage margin equal to the nominal swing of the transmitted signal, and a timing margin equal to the nominal symbol time. However, the noise coming from the transmitter, the receiver and the channel added to the signal degrade both the voltage margin and time margin, closing the eye and decreasing the BER (bit error rate).

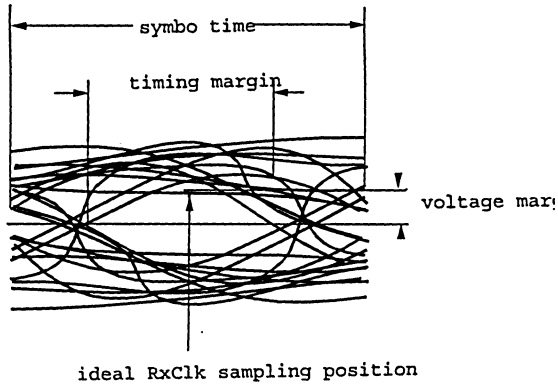


Figure 2.6: Eye diagram of received signal.

2.4.1 Voltage Noise

Voltage noise directly reduces voltage margins. The major source of voltage noise in data communications are channel attenuation, reflections, inter-signal cross-talk, offsets, power supply fluctuation and ground bouncing.

Channel Attenuation

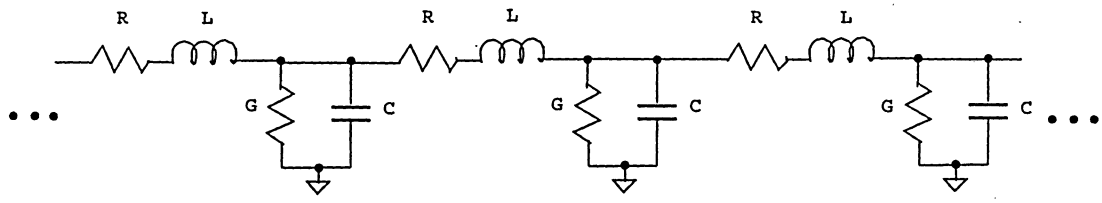


Figure 2.7: Lumped LCRG model of a transmission line.

PC board traces, coaxial cables, and twisted-pair cabels behave as transmission lines that

store and propagate signal energy. These lines can be modeled by a series of lumped LCRG elements as shown in Fig. 2.7.

To simplify analysis, a transmission line can be modeled as a simple RC low-pass filter as shown in Fig. 2.8. For a periodic square wave, a low-pass filter attenuates the high-frequency components, yielding finite rise and fall times. But for a random digital signal, as illustrated in Fig. 2.8, for a single ONE followed by a ZERO, the output does not come close to V_o, but for two consecutive ONEs, it does. A similar effect occurs for ZEROs as well. The output voltage level corresponding to ONEs and ZEROs vary with time, making it difficult to define a decision threshold. This phenomenon is called "inter symbol interference" (ISI). The narrower the bandwidth, the larger the value of R and C, the longer the tails and the greater the ISI [4].

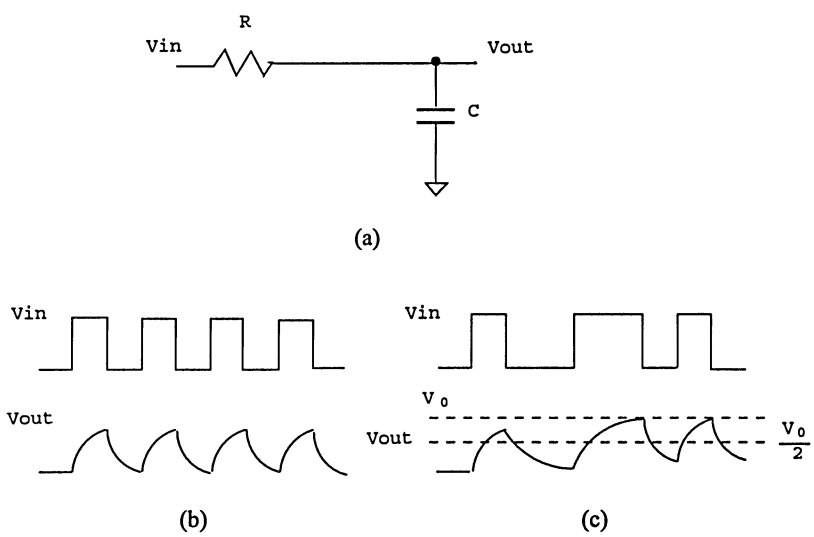


Figure 2.8: (a) RC model of transmission lines; (b) Periodic data response; (c) Random data response.

Another source of ISI comes from the characteristics of the channel that act like a frequency-dependent band-limited filter that disperses the signal. High-frequency currents flow closer to the surface of the conductor, resulting in a higher channel resistance that attenuates the signal (skin effect). Dielectric absorption that can be modeled as a conductance G

between the channel and the ground also increases with signal frequency. Fig. 2.9 shows the time-domain response of a transmission line to an ideal trapezoidal pulse. The pulse suffers more attenuation on its high frequency components than its low frequency components. The lower frequency attenuation of the channel results in a long settling tail. This long settling tail gives rise to an ISI that corrupts future symbols [1, 5].

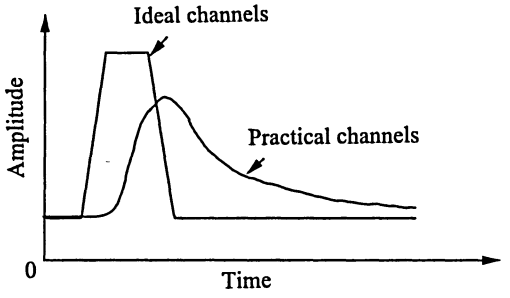


Figure 2.9: Response of a transmission line to a trapezoidal pulse.

Reflections

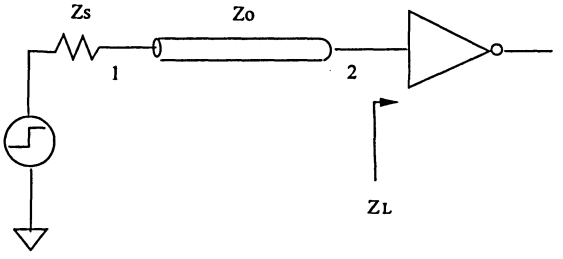


Figure 2.10: No termination at the both ends of line.

Reflection is another source of ISI. It is caused by impedance mismatch at both ends of transmission lines, as shown in Fig. 2.10. The reflection of a signal is given by

$$V^- = \left[\frac{Z_L - Z_o}{Z_L + Z_o}\right] V^+, \tag{2.1}$$

where Z_L is the load impedance at $z = 0$, and $\frac{Z_L - Z_o}{Z_L + Z_o}$ is the voltage reflection coefficient at $z = 0$. Ringing will exist due to the refletions and these signaling systems are slow because

the transmitter must charge up the line as the signal propagates over serveral round trips, as shown in Fig. 2.11.

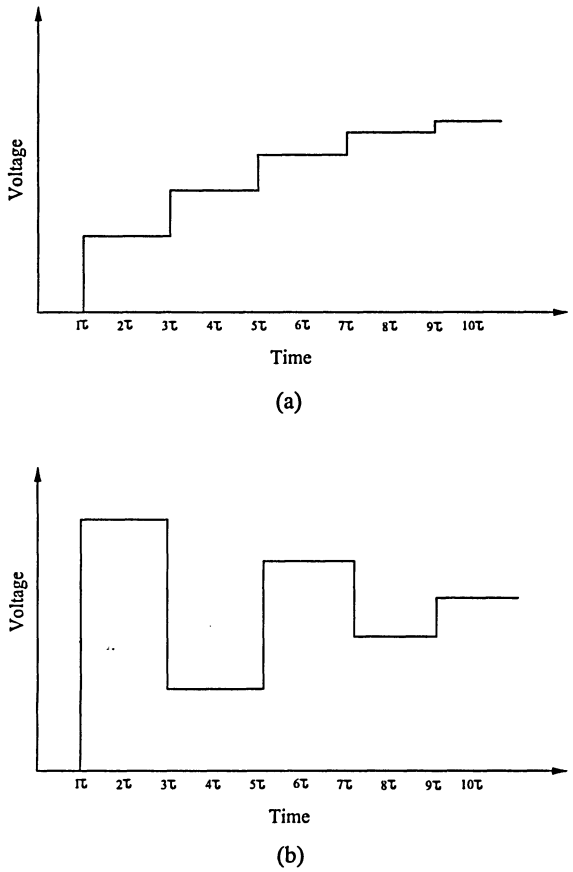


Figure 2.11: Voltage at the far end of the transmission lines with input impedance mismatched. (a) Over-terminated; (b) Under-terminated. τ is the propagation delay of the lines.

Reflection noise becomes more of a problem as signal frequencies increase. When transition times become comparable to signal propagation delays through the bond wires, package traces, and connectors in signal paths, these components can no longer be treated simply as lumped elements, but rather transmission line stubs. They create more impedance discontinuities that introduce more reflections [6, 7].

Cross-Talk

In parallel data links, high-speed signals coupled to/from nearby signals due to mutual capacitances and mutual inductances. Cross-talk depends largely on the physical arrangement of the signal lines. For an instance, in a twisted pair where the two wires carry currents of the same amplitude by opposite polarity, the magnetic flux generated by one wire cancel that from the other wire so that the pair do not radiate electromagnetic energy. The amount of radiation can be further reduced by shielding the signal pair. Inter-signal cross-talk is the worst when unshielded wires are bundled together, unless the cross-talk from all other signals is a common-mode noise to the pair of signals in consideration. Differential architecutres usually are used to lower the inter-signal cross-talks that appear as a common-mode disturbance [8].

Offsets

Even in a carefully matched layout, transistor mismatches can introduce a fixed voltage offset whose amplitud is determined by the transistor sizes, biasing conditions, and process parameters [9]. Transmitter mismatches cause the output signal swing to deviate from the normal value. Recevier mismatches cause the decision threshold voltage to deviate from the normal voltage. Offset-cancellation techniques commonly used in op-amp designs, can be applied to reduce the effect of mismatches [10].

Power Supply Noise and Substrate Noise

As shown in Fig. 2.12, the power supply noise problem has traditionally been thought of as an inductance problem. This problem is becoming more serious as more gates switch at higher frequencies. Also, switching noise can propagate through the common substrate and corrupt sensitive analog circuits.

Power supply noise and substrate noise are not a dominant voltage noise in differential links. Both of them are coupled to the signal pairs at both the transmitter and the receiver are common-mode inputs [11].

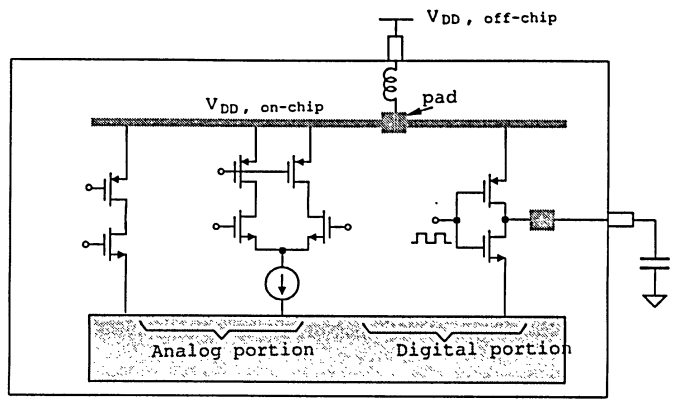


Figure 2.12: Supply voltage fluctuation and ground bouncing in mixed analog/digital circuits

2.4.2 Timing Noise

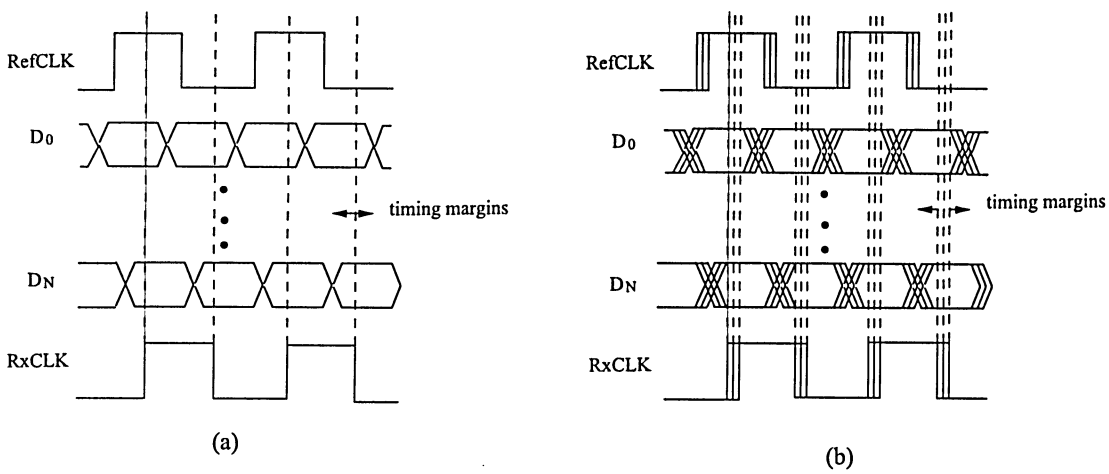


Figure 2.13: Phase noise and timing jitter. (a) Ideal case; (b) Practical case.

The presence of timing errors, shifts the transition edges of the received data signals relative to the transition edges of RefCLK and reduces timing margins. If we assume that RxCLK tracks RefCLK perfectly, as shown in Fig. 2.13 (a), timing margins are still greatly reduced. This is called inter-signal timing skew which is caused by difference in signal propagation delay from the transmitter to the receiver. However, In reality, as shown in Fig. 2.13 (b), the transmitter clock, the receiver clock, and the signal, are all shifted.

Inter-signal timing skew is a static phase error and can be compensated. Most timing jitter is induced by on-chip voltage noise in the signaling system itself. All the major voltage noise sources in data links designs are synchronous in nature, but random data streams make the effect of each, and hence the superimposed voltage noise, 'random'. Each of these components contributes to the shift of the signals.

Precise phase alignment circuits are needed to accurately extract timging information from the received signals and position the receiver clock to the middle point of data eye so that the effects of inter-signal timing skew and jitter are minimized and the receiver timing margins are maximized. Therefore, at the heart of timing recovery of the receiver are phase-locked loops (PLLS).

Chapter 3

Electrical Signaling For Data Transmission Over Wire Channels

A number of electrical signaling schemes have been developed for data transmission over wire channels. Depending upon the physical arrangement of channels, electrical signaling for data transmission over wire channels can be classified into single-ended signaling scheme, fully differential signaling scheme, pseudo-differential signaling scheme, and incremental signaling scheme. They can also be categorized into voltage-mode signaling and current-mode signaling, depending upon whether the information carriers are nodal voltages or branch currents. In this chapter, an examination of the pros and cons of these signaling schemes is provided.

3.1 Singled-Ended Signaling Scheme

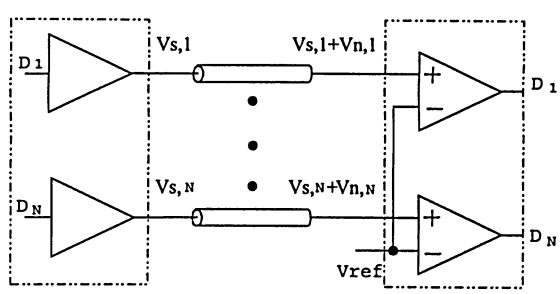


Figure 3.1: Singled-ended signaling scheme.

The basic configuration of the singled-ended signaling scheme is shown in Fig. 3.1. Only one physical line per channel is needed. The signal appearing at the far end of the channel consists of both the transmitted signal $v_{s,k}$ and the noise coupled from neighboring devices to the channels $v_{n,k}$, $k = 1, 2, ..., N$. The logic stage of the received signals is determined by a set of voltage comparators whose reference input V_{ref} is generated at the receiver. The noise coupled from the channels can not be suppressed by the comparators. As a result, the single-ended signaling scheme is very susceptible to noise coupled to the channels.

3.2 Fully Differential Signaling Scheme

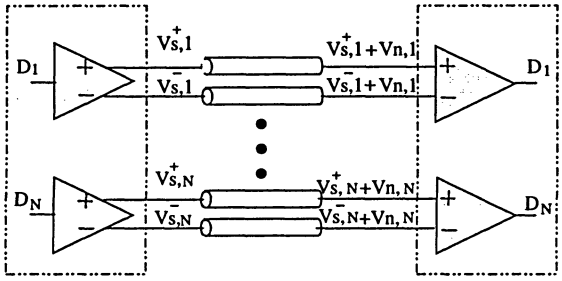


Figure 3.2: Fully-differential signaling scheme.

The fully differential signaling scheme shown in Fig. 3.2 employs two physical lines per channel. These two lines are usually twisted such that the signal appearing at the far end of the channel consists of both the transmitted signals $v_{s,k}^{+}$ and $v_{s,k}^{-}$, and the noise coupled from neighboring devices to the channels $v_{n,k}$ that are approximately equal on twisted conductors. The logic stage of the received signals is determined by a set of fully differential voltage amplifiers with a high common-mode rejection ratio. Because the noise signals coupled from the channels makes their appearance at the receiver as a pair common-mode inputs, they are suppressed largely. The fully differential signaling scheme provides an excellent common-mode noise immunity.

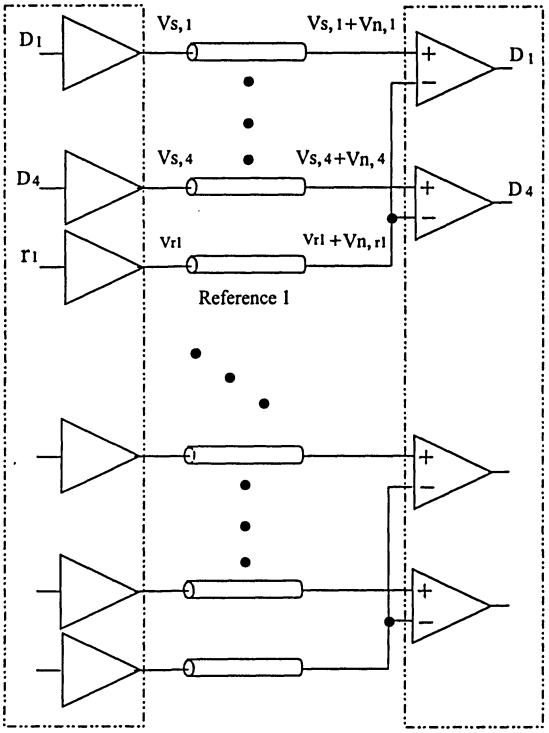


Figure 3.3: Pseudo-differential signaling scheme.

3.3 Pseudo Differential Signaling Scheme

A main drawback of the fully differential signaling scheme is its high hardware cost both in terms of the number of physical lines, the silicon area for routing them, and chip I/O count. The configuration of the pseudo differential signaling scheme shown in Fig. 3.3 is a compromise of the single-ended and the fully differential signaling schemes. In this scheme, a group of physical lines, usually limited to four, share a common reference line routed in parallel with the data lines. The reference voltage is generated on the transmitter and shipped to the receiver. Because these physical lines are located in a small proximity, the noise coupled to these lines including the reference line are approximately the same, i.e. $v_{n,1} \approx ... \approx v_{n,4} \approx v_{n,r1}$. They can be suppressed effectively by the differential receivers. The pseudo differential signaling scheme provides a good common-mode noise immunity with a small overhead.

3.4 Voltage-Mode Incremental Signaling Scheme

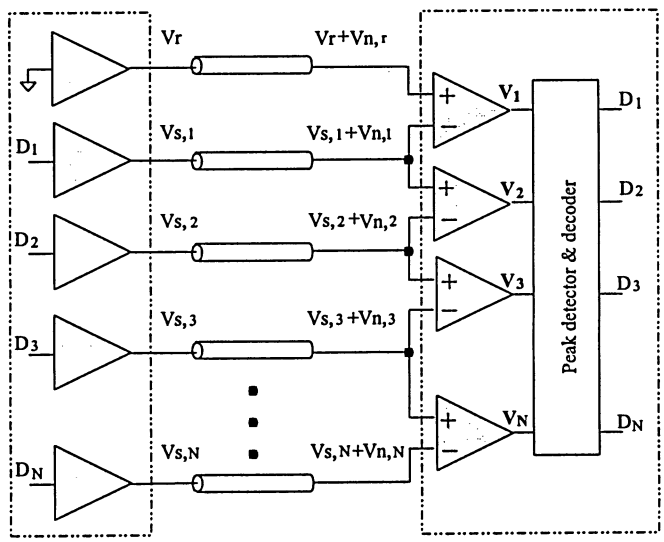


Figure 3.4: Voltage-mode incremental signaling scheme.

To take the fully advantage of the superior signal integrity of the fully differential signal-

ing scheme and at the same time to minimize its hardware cost, a voltage-mode incremental signaling scheme was proposed in [2] where only $N+1$ physical paths are needed for N parallel signal channels, as shown in Fig. 3.4. It denotes noisy signal at the receiver, $V_{S,k}+V_{n,k}$. There is some redundancy inherent in transmitting N signals over $2N$ signal paths. This redundancy is eliminated by having the signals appear incrementally as the difference between adjacent signal paths.

$$V_k = (V_{S,k-1} + V_{n,k-1}) - (V_{S,k} + V_{n,k}). \tag{3.1}$$

Using this scheme, the signals still appear differentially between two adjacent wires, so all of the noise-rejection advantages of fully differential signals are obtained using only $N+1$ signal paths for number of N transmitted signals.

Encoder/transmitter and decoder/receiver are needed for this signaling scheme. The signal path values are encoded according to the following equation:

$$V_{S,k+1} = (V_{S,k} + D_k) \mod 2, \tag{3.2}$$

where D_k is the information symbol being encoded. The receiver must then intepret the received signals by:

$$D_k = V_k \mod 2. \tag{3.3}$$

The modular addition in encoder at the transmitter can be performaed by an exclusive-OR operation

$$V_{S,k+1} = V_{S,k} \oplus D_k. \tag{3.4}$$

Common-mode rejection is achieved effectively by amplifying the signals of physically adjacent paths with differentially configured receivers. To recover the logic stage of the received signals, N encoders at the transmitter side or equivalently N peak detectors and decoders at the receiver side are needed. The drawbacks of voltage-mode signaling including

low signal swing, high switching noise injection, high sensitivity to supply voltage fluctuation and ground bouncing, and the need for additional circuitry for either encoding at the transmitters or decoding at the receivers, however, increase the power consumption and limit its data rates.

Chapter 4

Current-Mode Incremental Signaling

This chapter introduces a new current-mode signaling scheme called current-mode incremental signaling (CMIS) to overcome the design difficulties associated with voltage-mode incremental signaling in parallel links.

4.1 Current-Mode Signaling

Current-mode signaling where information carriers are branch currents has been used widely in high-speed serial links [13, 14, 15, 16, 17, 18]. As compared with voltage-mode signaling, current-mode signaling offers the following intrinsic advantages critical to high-speed data links:

1. *Low-Voltage* - Because information carriers of current-mode circuits are branch currents rather than nodal voltages, the swing of nodal voltages can be made small while keeping the branch currents large. This is achieved by lowering the impedance of the nodes. Current-mode circuits can operate effectively in the presence of a low supply voltage. On the contrary, the information carrier of voltage-mode circuits is nodal voltages whose swing is directly proportional to the supply voltage. The supply voltage must be high enough in order to have a large signal swing.

2. *Small Propagation Delay* - The average rise/fall time of a purely capacitive node, denoted by Δt, is determined from

$$\Delta t = \frac{C_n \Delta V_n}{I}, \tag{4.1}$$

where I is the average current charging/discharging the node, C_n is the capacitance of the node, and ΔV_n is the voltage swing of the node. A small Δt can be obtained by minimizing the voltage swing at the node or maximizing the current charging and discharging the capacitance of the node. The small voltage swing of current-mode circuits lowers the amount of time to charge and discharge the capacitor of the nodes, resulting in a small propagation delay.

3. *Signal Integrity* - As pointed out in [13, 14], the current conveyed to the channels by current-mode transmitters are well defined with a little effect from the supply voltage fluctuation and ground bounding. On the contrary, the output voltage of voltage-mode transmitters, such as static inverters, is a strong function of the supply and reference voltages. In addition, although terminated with a series resistor, the variation of the output impedance of voltage-mode transmitters gives rise to a signal reflection at the transmitter end unless the resistance of the series termination resistor is significantly larger than the output impedance of the transmitter.

4. *Low power* - Although current-mode transmitters and receivers consume static power arising from the existence of static biasing current sources and a small voltage swing of their nodes, the dynamic power consumption of these circuits is low. Moreover, the total power consumption of these systems is independent of frequency. On the contrary, the power consumption of voltage-mode transmitters and receivers, such as those that are based on static inverters, mainly comes from dynamic power consumption and is proportional to the frequency. As pointed out in [19], at multi-Gb/s data rates, the total dynamic power consumption of static voltage-mode logic circuits well exceeds the static power consumption of corresponding current-mode logic circuits.

5. *Low switching noise* - The total current drawn from the supply voltage and the total current injected to ground rail by current-mode transmitters are constant. This not

only minimizes switching noise, the noise injected to the substrate via parasitic junction capacitances is also minimized due to the small voltage swing of the nodes of current-mode circuits.

4.2 Current-Mode Incremental Signaling

The architecture of the proposed current-mode incremental signaling scheme is shown in Fig. 4.1. The transmitter consists of a set of N bipolar current-mode drivers for a N-bit parallel link. Each driver conveys two currents of the same amplitude but opposite polarity to the channels such that not only the effect of V_{DD} fluctuation on the channel currents is minimized, the noise injection from the drivers to the substrate is also minimal. Although the direction of the output currents of the drivers is controlled by the logic state of the parallel inputs, The currents flowing in the channels are determined from the mesh current of each mesh. For the inputs shown in the figure, the currents flowing in the channels and the voltage drop across the termination resistors are tabulated in Table 4.1, where A_v is the voltage gain of the differential amplifier at the receiver. It is evident that an one-to-one mapping between the polarity of the voltage drop across the termination resistors and the logic stage of the input of the corresponding drivers exists.

Table 4.1: Input-output mapping of parallel link of Fig. 4.1 with the current-mode incremental signaling scheme.

Input	Mesh current	Channel current	V_{out} of receiver
$D_1 = 1$	I	$I_1 = I$	$V_o = (R_T I)A_v$
$D_2 = 1$	I	$I_2 = 0$	$V_o = (R_T I)A_v$
$D_3 = 0$	$-I$	$I_3 = -2I$	$V_o = -(R_T I)A_v$
...	...	...	...
$D_N = 1$	I	$I_{N+1} = -I$	$V_o = (R_T I)A_v$

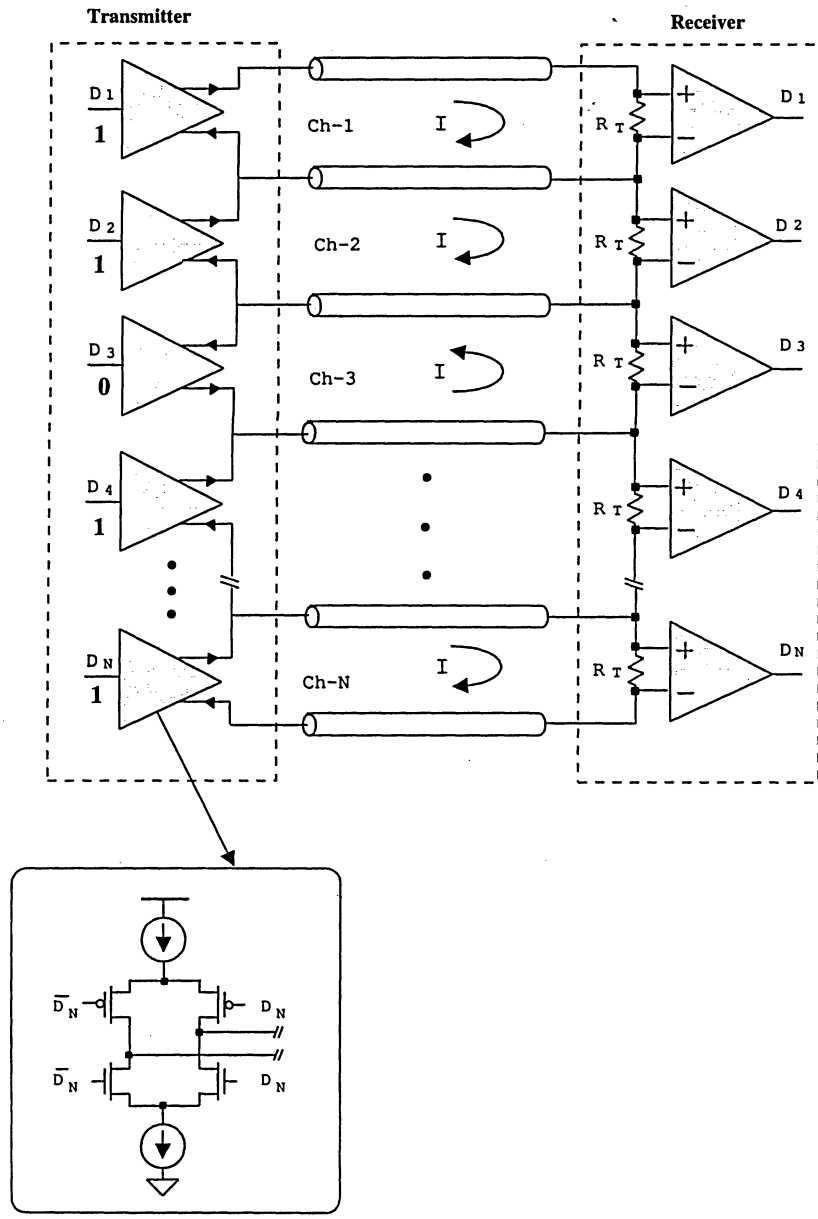


Figure 4.1: Current-mode incremental signaling scheme.

4.3 Fully Differential Transimpedance Front-End

A major drawback of the preceding parallel links is the need for a passive resistor R_T at the input of the receiver for both channel termination and current-to-voltage conversion. Not only the thermal noise of the termination resistor deteriorates the signal-to-noise ratio of the links, the large variation of the resistance of the resistors and their parasitics of the resistors gives rise to a signal reflection at the far end of the channels. To eliminate these drawbacks, on-chip termination resistors with a tunable resistance are desirable, as shown in Fig. 4.2.

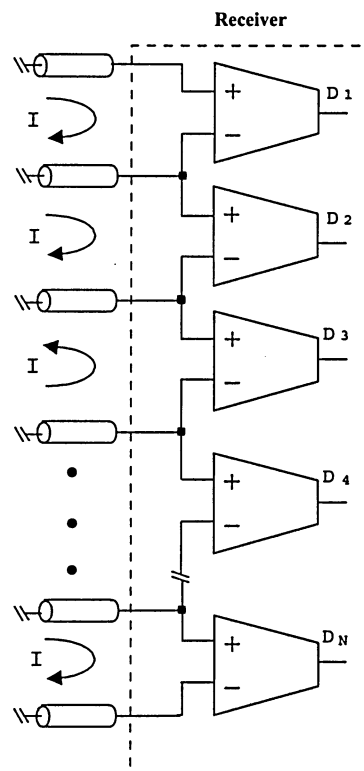


Figure 4.2: Fully differential transimpedance front-end with a built-in tunable termination.

On-chip termination resistors implemented using MOSFETs in the deep triode offer good linearity, the variation of the terminal voltage of the resistors, however, must be kept small. Termination resistors based on the symmetric load increase the voltage range [20]. As shown by Fig. 4.3, the need for two pMOS transistors, however, results in both a large chip area

and increased the level of the noise. Other approaches such as digital trimming can not tune the impedance continuously to obtain a perfectly matching impedance. In addition, they require a prohibitively large chip area [21].

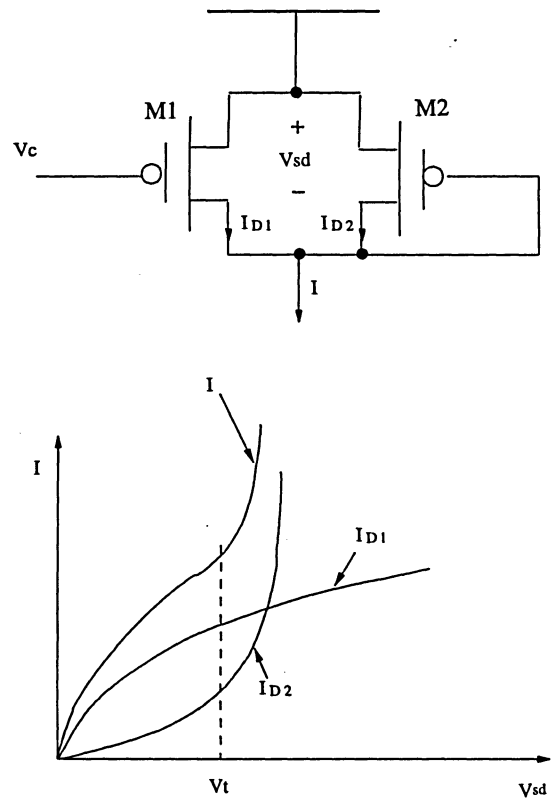


Figure 4.3: Symmetric pMOS load.

In this chapter, a fully differential transimpedance front-end with a built-in tunable termination is proposed. Shown in Fig. 4.4, the front-end is common-gate configured with local voltage feedback formed by $R_{1\sim2}$ and $M_{5\sim6}$. The input impedance of the amplifier is given by

$$R_{in} \approx \frac{1}{g_{m_{1,2}}(R_{1,2}g_{m_{5,6}})}. \tag{4.2}$$

The low input impedance ensures a small time constant at the input node in spite of a large channel capacitance. The dimension of the feedback transistors $M_{5,6}$ should be made

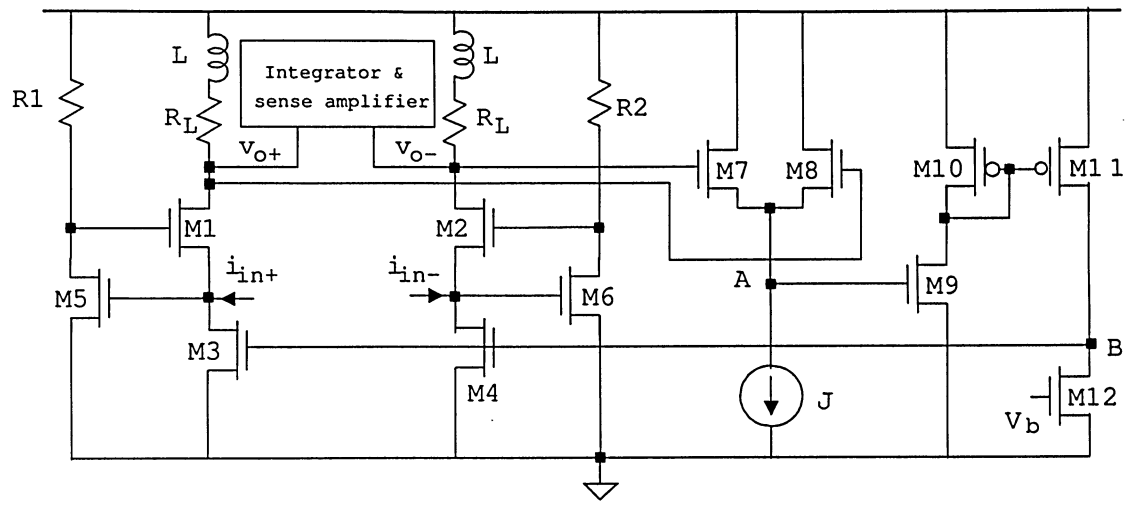


Figure 4.4: Transimpedance front-end with common-mode feedback.

small to minimize the additional capacitance added to the input nodes. R_1 and R_2 should also be kept small to minimize the time constant of the feedback loop. To lower the input impedance and at the same time to boost the gain of the transimpedance amplifier, $g_{m1,2}$ should be made large. This, however, is echoed with a large capacitance at the output node. To offset this effect, Inductive shunt peaking is employed at the output nodes to sharpen the rising and falling edges of the output voltage [22].

Generally, high-gain fully differential amplifiers require a means of defining the output common-mode level. For example, as shown in Fig. 4.5, the output common-mode (CM) level of the differential pair with diode-connected loads is $V_{DD} - |V_{TP}|$, where V_{TP} is the threshold voltage of transistor $M_{3,4}$. However, the output common-mode level of the differential pair with current-source loads is not well-defined. Ideally, each of the input transistors carries a current of $\frac{I_{SS}}{2}$, the CM level depends on how close I_{D3} and I_{D4} are to this value. In practise, mismatches in the PMOS and NMOS defining I_{SS} and $I_{D3,4}$ create a finite error between $I_{D3,4}$ and $\frac{I_{SS}}{2}$. Suppose, for example, that the drain currents of M_3 and M_4 in the saturation region are slightly greater than $\frac{I_{SS}}{2}$. As a result, to satisfy Kirchoff's current law at the output nodes, both M_3 and M_4 must enter the triode region so that their drain current fall to $\frac{I_{SS}}{2}$. Conversely, if the drain currents of M_3 and M_4 in the saturation region are slightly

less than $\frac{I_{SS}}{2}$, then the voltage at the output nodes must drop to produce a current equals to $\frac{I_{SS}}{2}$.

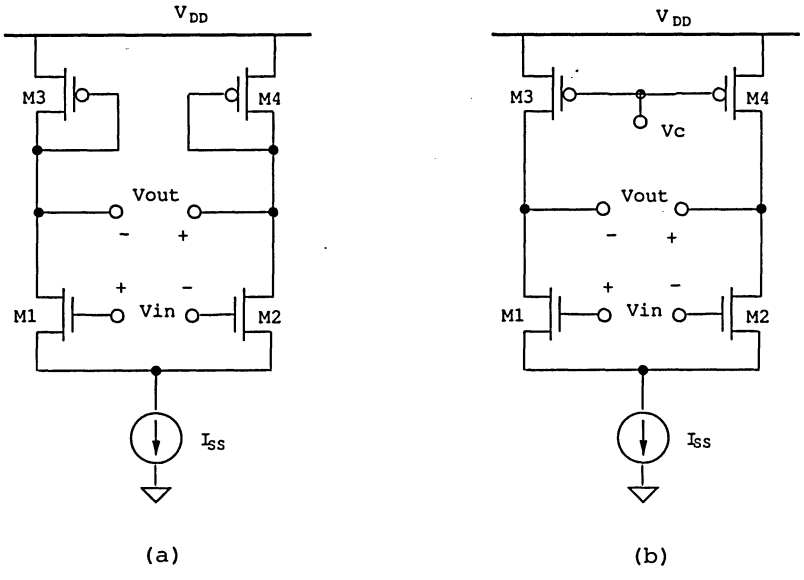


Figure 4.5: (a) Differenital pair with diode-connected; (b) current-source loads.

Transistors $M_{7,8}$ and the current source J form a common-mode voltage sensing network whose output voltage is insensitive to the differential output voltage of the front-end. When the common-mode component of v_{o+} and v_{o-} increase, v_A rises and i_{D9} increases accordingly. Because M_{12} biased in the deep triode region and behaves as a resistor, v_B increases. The biasing current of $M_{1,2}$ lowers the common-mode component of v_{o1} and v_{o2}. As a result, the common-mode component of v_{o+} and v_{o-} drops.

Fig. 4.6 shows the output voltage of the transimpedance front-end with a differential input current of 2 mA. L is varied from 0 to 2 nH with step 0.5 nH. It is seen that the shunt-peaking inductors increase the bandwidth of the amplifier. The input impedance of the transimpedance front-end with two input terminals connected together is also shown in the Fig. 4.7. Note that this input impedance is the joint effect of two input branches. Because each channel is shared by two neighboring transimpedance front-ends, the impedance seen by the channel is only half of that of each single-ended branch of the transimpedance front-end.

It is evident that the input impedance can be tuned by varying the biasing condition.

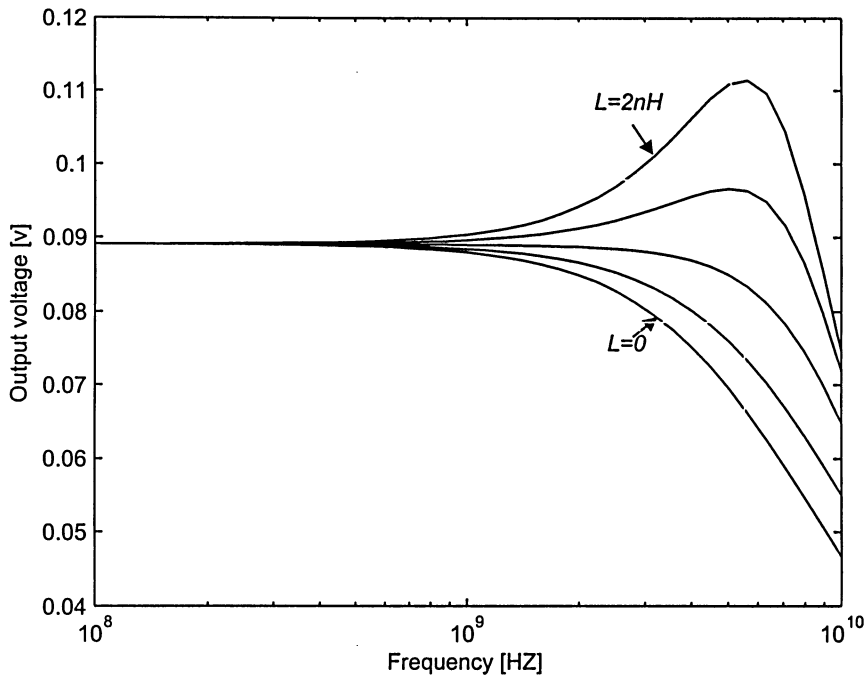


Figure 4.6: Frequency response of the output voltage of the transimpedance front-end with common-mode feedback

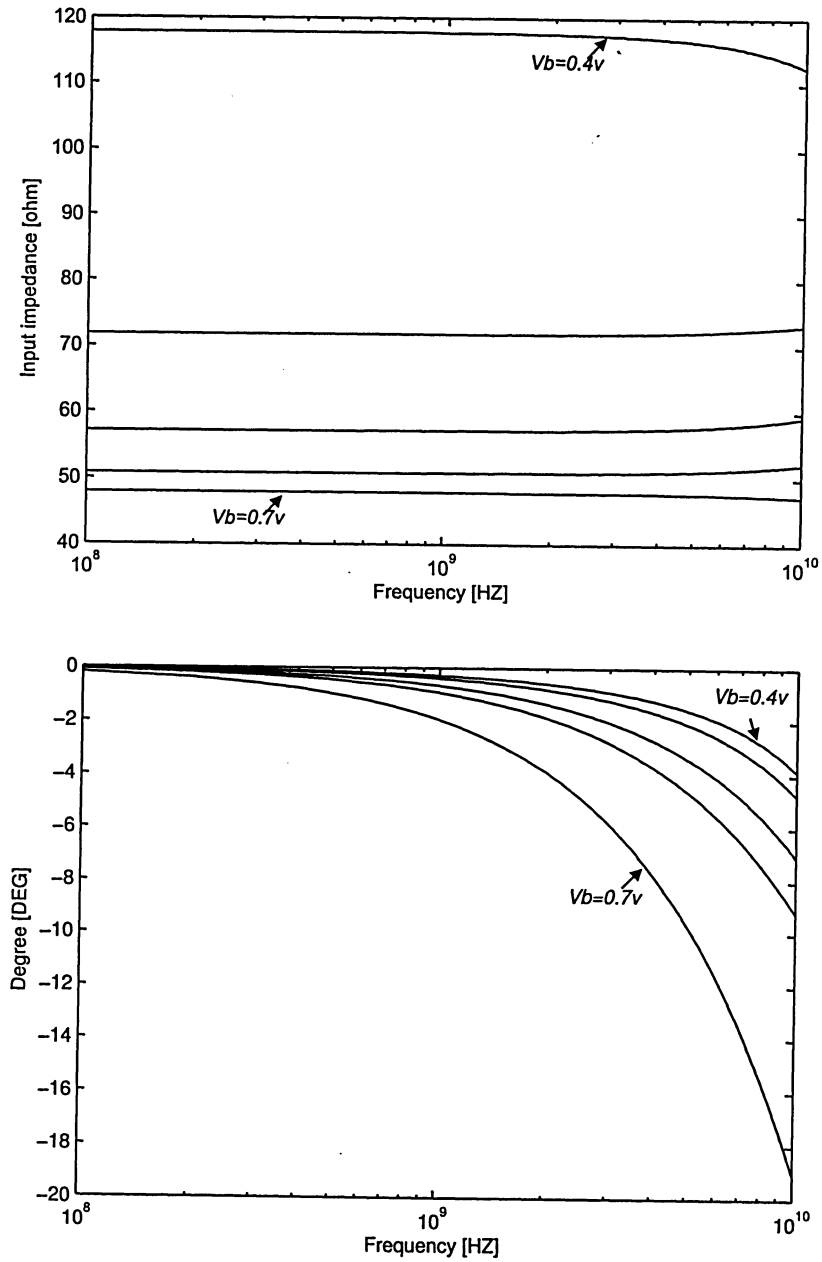


Figure 4.7: The magnitude (top) and phase (bottom) of the input impedance of transimpedance front-end.

Chapter 5

Fully Differential Current-Integrating Front-End

In conventional phase-picking source-synchronous parallel links, a clock signal is transmitted in phase with data via a separate line that is in parallel in data lines. Data recovery is achieved by delaying the received clock signal by half the symbol time at the receiver so that the received data can be sampled at the middle point of data eyes to maximize timing margins. Transient disturbances coupled to the channels may significantly alter the amplitude of the received data signals at the time instants where sampling takes place and result in erroneous results. As illustrated graphically in Fig. 5.1 [23, 24].

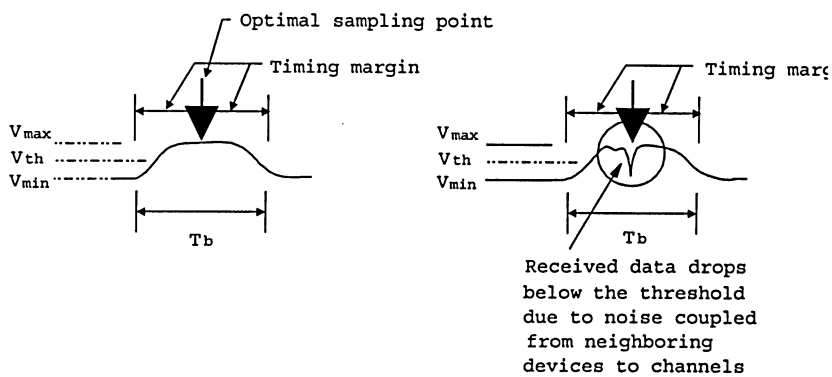


Figure 5.1: Data recovery. (a) Without noise disturbances; (b) With noise disturbances at sampling point.

5.1 Oversampling Scheme

One approach is to sample the received signal multiple times during one symbol time - a technique called oversampling. This approach takes a majority vote of all the samples. Hence the oversampling factor should be an odd number of at least three. The idea is illustrated in Fig. 5.2.

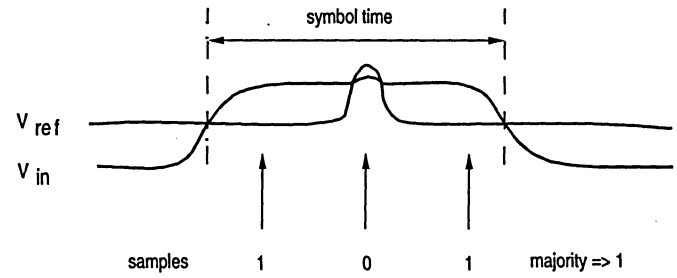


Figure 5.2: Oversampling as a means to overcome high-frequency noise.

Oversampling with majority-voting mechanisms can effectively eliminate this problem, however, at the cost of power, chip area, and increased switching noise [25]. Moreover, this approach becomes difficult to implement when data rates reach multiple Gb/s.

5.2 Current Integrating

A current-integrating scheme was proposed to minimize the effect of high-frequency disturbances coupled to the channels. This scheme is the analog equivalent of majority voting. This method requires only a single clock defining the sampling/integrating period. Fig.5.3 illustrates the concept of current integrating receiver. When ϕ is high, the current switch (SW1) steers to one branch of the integrator and charge the respective capacitor. At the end of the integrating period, the polarity of the ouput differential voltage ΔV indicates whether the input signal was mostly low or high during the integrating period. When ϕ is low, the reset switch (SW2) is on, equalizing the integrator output and preparing for the next data period. Transient noise that causes the input to cross the reference voltage will not effect the correct reception of the signal as long as the duration of the transient noise

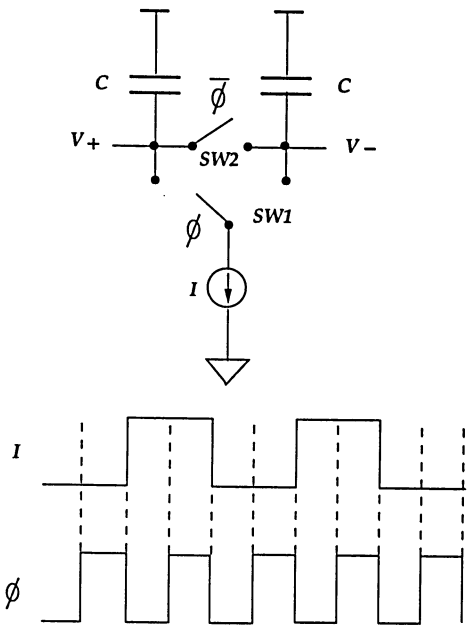


Figure 5.3: Idealized current integrating receiver.

is less than half the valid symbol period. The logic state of the received data is determined by a voltage comparator whose inputs are the output voltage of the integrating capacitors and a reference voltage V_{ref}. The voltage swing of the inputs must be sufficiently large such that the tail/head currents can be steered between the two arms of the differential pairs. The integrating receiver presented in this chapter differs from the voltage-mode integrating receivers in the following aspects :

1. The inputs of the receiver are currents. This enables the receiver to be used in current-mode data links. The receiver provides a continuous and tunable matching impedance to the channels, eliminating the need for a lumped termination resistor for both channel termination and current-to-voltage conversion.

2. The transistors of the receiver are operated in the saturation region, avoiding the speed penalty of turning on/off the transistors completely.

5.3 Ideal Current-Integrating Receiver

The simplified schematic of the proposed current-integrating front-end is shown in Fig. 5.4. Capacitors C_1 and C_2 are integrating capacitors. $M_{7,8}$ are current-source loads. This ensures that the dominant pole of the amplifier is at the output with the pole frequency given by $\omega_o \approx \frac{1}{r_{o7,8}C_{1,2}}$. When the switch is open, the received differential currents are integrated on C_1 and C_2 via the transimpedance amplifier. The polarity of $\Delta v_c(t) = v_{c1}(t) - v_{c2}(t)$ at the end of the integration phase indicates whether the incoming signal is mostly low or high during the integration phase.

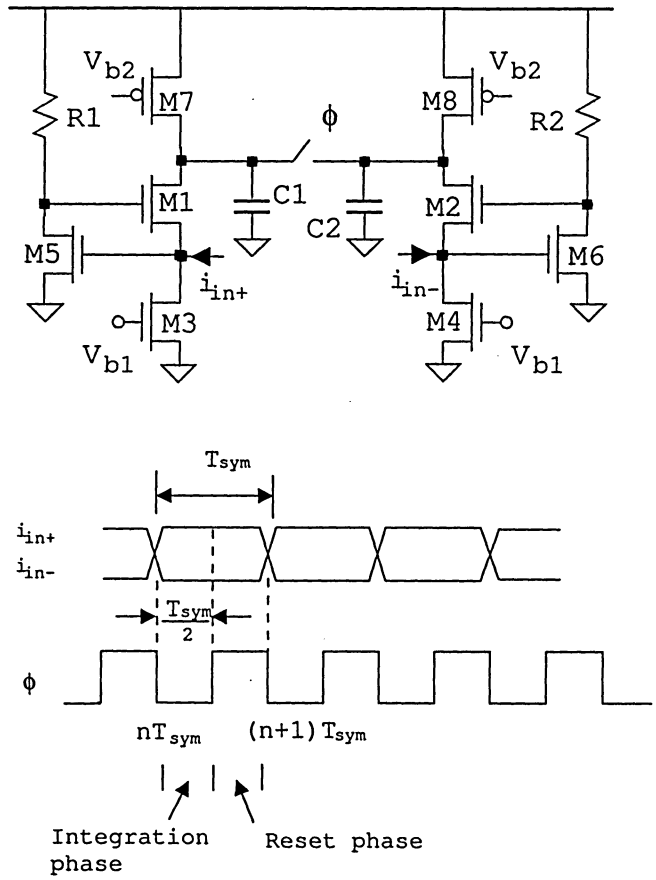


Figure 5.4: Schematic of current-integrating front-end with ideal reset switches.

During the reset phase where the switch is closed, the change of C_1 and C_2 is equalized.

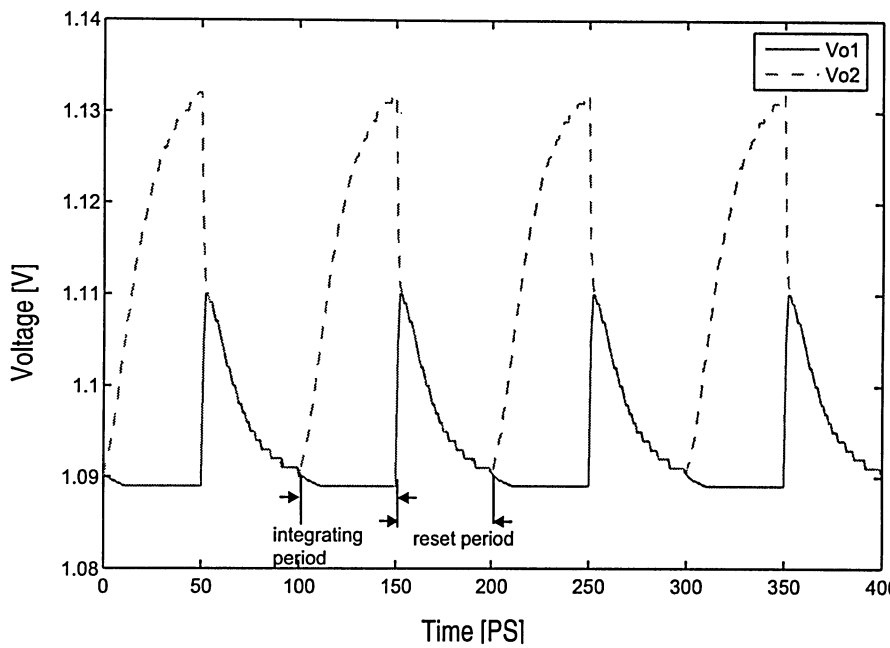


Figure 5.5: Simulated output voltage of the transimpedance front-end with ideal reset switch.

The reset period must be larger than the transient time of $V_{C1,C2}$, which is a function of $C_{1,2}$, switch equivalent impedance, and the DC voltage drop of source and drain of $M_{7,8}$, to ensure that V_{C1} and V_{C2} are equal at the end of the reset phase. Fig. 5.5 plots Δv_c with $i_{in}^{+} = 2\text{mA}$ and $i_{in}^{-} = 0$. i_{in}^{+} varies from 0 to 2 mA periodically with period 100 ps and 50% duty cycle while $i_{in}^{-} = 0$. It is seen that at the end of the integrating phase, Δv_c correctly shows the polarity of the input signal. During the reset phase, the law of charge conservation ensures an instantaneous charge equalization between C_1 and C_2

$$v_{c1,c2}(nT + \frac{T^{+}}{2}) = \frac{1}{2}\left[v_{c1}(nT + \frac{T^{-}}{2}) + v_{c2}(nT + \frac{T^{-}}{2})\right], \tag{5.1}$$

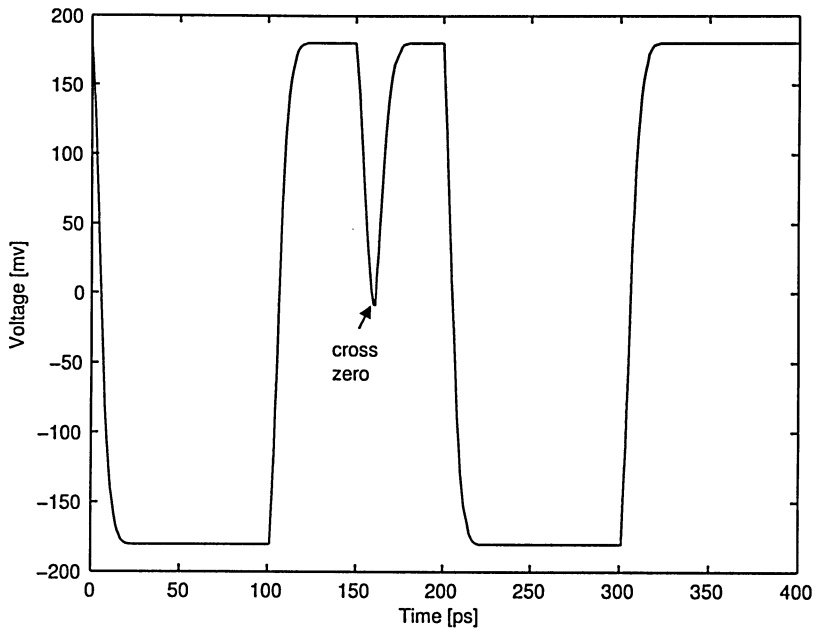
where the superscripts $-$ and $+$ denote the time instant just before and after the reset switch is closed, respectively. After the charge equalization, v_{c1} and v_{c2} decrease exponentially to their DC value.

Transient disturbances whose duration is significantly less than the integration phase have a little impact on the final voltage of the capacitors. This is demonstrated in Fig. 5.6 in the presence of a 1mA, 10ps duration input current noise signal. It is observed that the output voltage of the transimpedance front-end drops below the reference voltage whereas that of the current-integrating front-end only suffers from a small dip with no change in the polarity at the end of the integration phase.

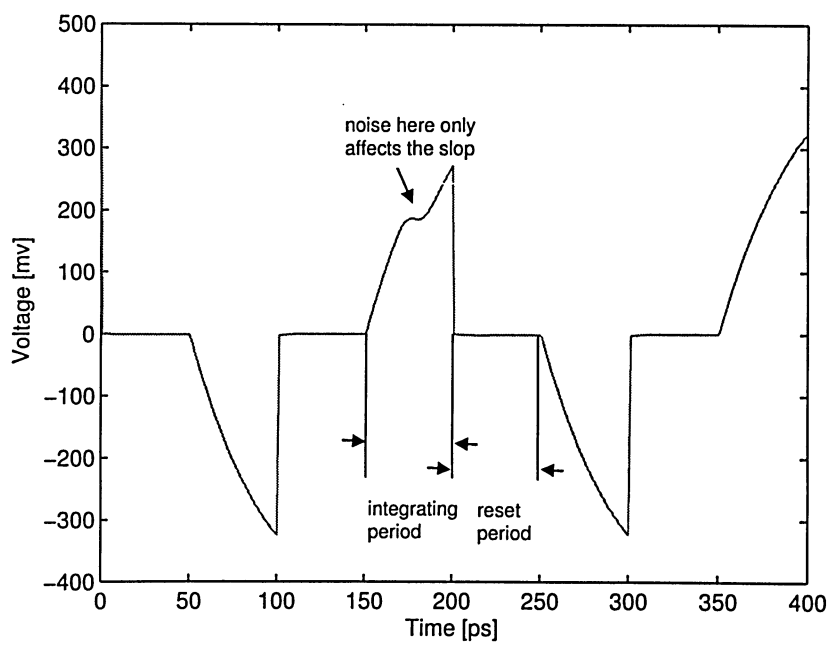
5.4 Reset Schemes

When the channel resistance of the reset switch is considered, the preceding instantaneous charge re-distribution between C_1 and C_2 becomes impossible. Instead, charge equalization is governed by the RC time constant of the reset loop consisting of C_1, C_2 and R_{on}. Also because $i_{in}^{+} = 2\text{mA}$ while i_{in}^{-}=0, v_{c1} and v_{c2} at the end of the reset phase differ by the voltage drop across R_{on} of the switch, i.e.

$$v_{c1}(nT + \frac{T^{+}}{2}) - v_{c2}(nT + \frac{T^{+}}{2}) = R_{on}I. \tag{5.2}$$



(a)



(b)

Figure 5.6: (a) Simulated output voltage of transimpedance front-end; (b) simulated output voltage of the current integrating front-end.

Equalization of v_{c1} and v_{c2} can not be achieved. To overcome this problem, a novel approach is proposed as shown in Fig. 5.7. When ϕ =0, the receiver performs current integration. When ϕ =1, C_1 and C_2 are isolated from the front-end by $TG_{2,3}$, V_{C1} and V_{C2} are equalized via TG_1. The size of the transmission-gates should be carefully chosen such that the time constants satified the timing requirement in both the integrating and reset phases. Fig. 5.8 shows the Δv_O of the transimpedance front-end with TG reset switches. i_{in}^+ varies from 2 mA to -2 mA periodically with period 100 ps and 50% duty cycle while $i_{in}^- = 0$. The voltage is DC-shifted by 1.09V.

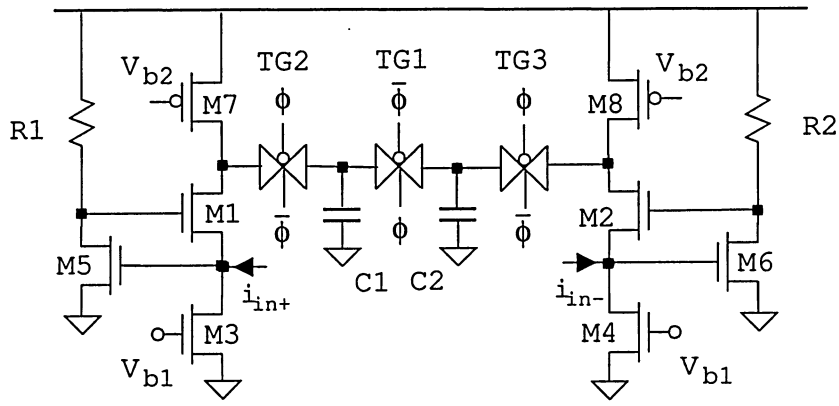


Figure 5.7: Schematic of current-integrating front-end with TG reset switches.

This schematic can be applied in the random signal transmission system. But we still have to consider an extreme case which one channel current is always flow in and the neighbor one is always keep zero. For example, if $i_{in}^+ = 2$ mA and $i_{in}^- = 0$ continue for a large number of clock periods, although the charge of C_1 and C_2 is equalized in the reset phase, the increase in the net charge of C_1 and C_2 results in a continuous level-up of v_{c1} and v_{c2}, as shown in Fig. 5.9. To solve this problem, the voltage of $C_{1,2}$ at the end of reset phase can be clamped to a pre-defined voltage, as demonstrated in Fig. 5.10.

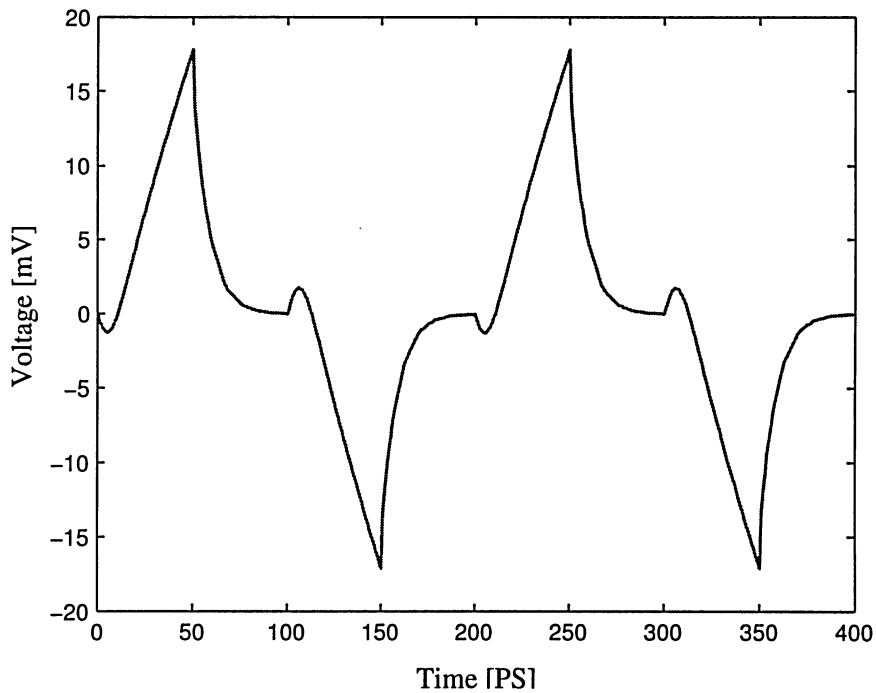


Figure 5.8: Simulated output voltage of the transimpedance front-end with TG reset switch.

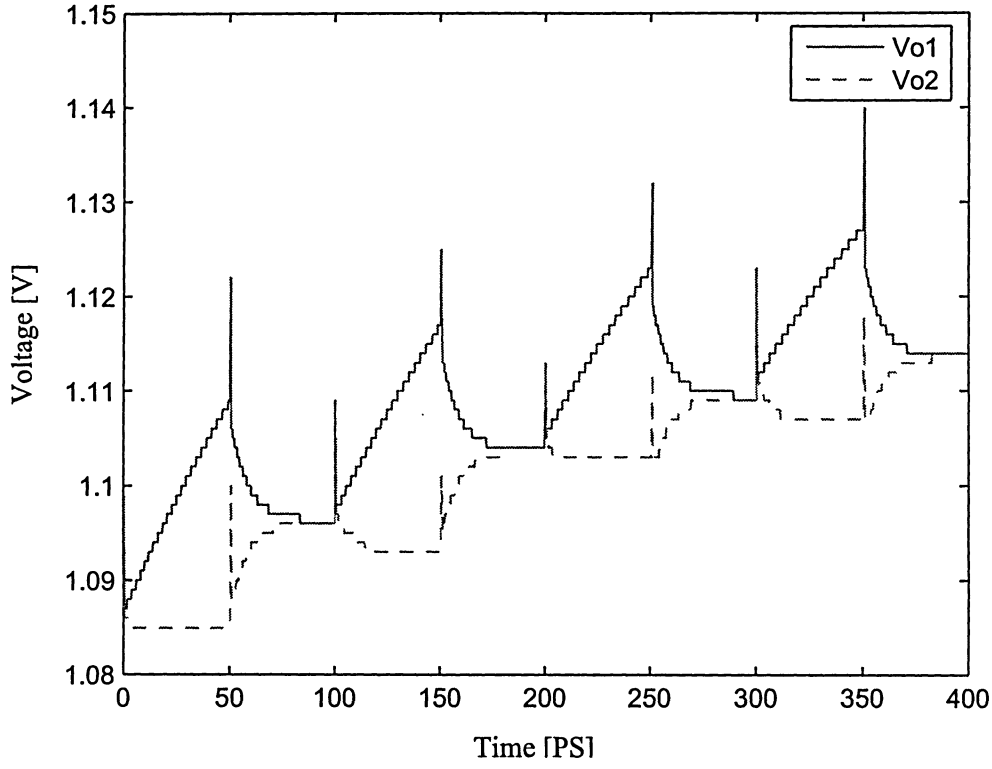


Figure 5.9: Simulated output voltage of the transimpedance front-end without voltage clamping.

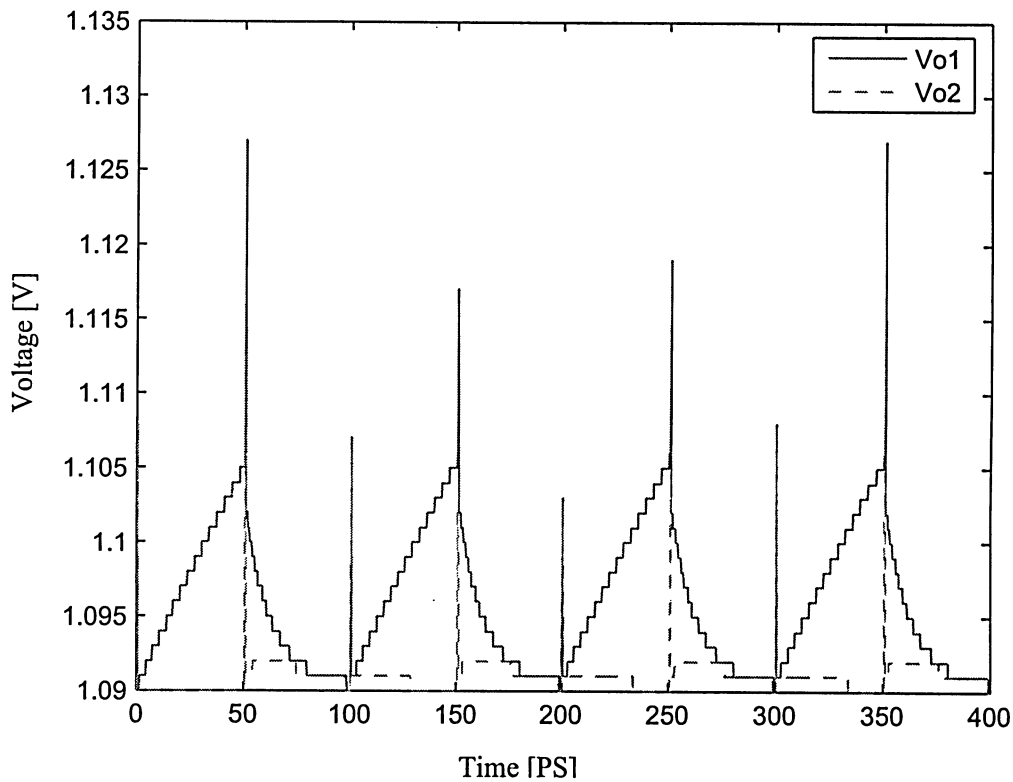


Figure 5.10: Simulated output voltage of the transimpedance front-end with voltage clamping.

Chapter 6

Sense Amplifier

It is seen from Fig. 5.10 that the voltage of $C_{1,2}$ at the end of the integration phase is rather small. Because the maximum or minimum value of the differential current-integrating output voltage is:

$$\Delta v_O = \pm(I \times t_b)/C, \tag{6.1}$$

where I is the current, t_b is the half of symbol time, and C is the capacitance of the integrating capacitor.The output voltage of the integrator is small due to the following reasons:

1. The variation of the output voltage of the transimpedance front-end caused by the input currents with ± 2 mA current swing is small.

2. The duration of the integration phase is less than the symbol time.

3. The transistors of the transimpedance front-end are all biased in the saturation.

An amplifier that amplifies the voltage of the integrating capacitors at the end of the integration phase to full swing with the settling time less than $T_{sym} - \tau_{int}$ is critically needed, where τ_{int} is the integration time. Fig. 6.1 is the block diagram of the current-integrating receiver with a sense amplifier.

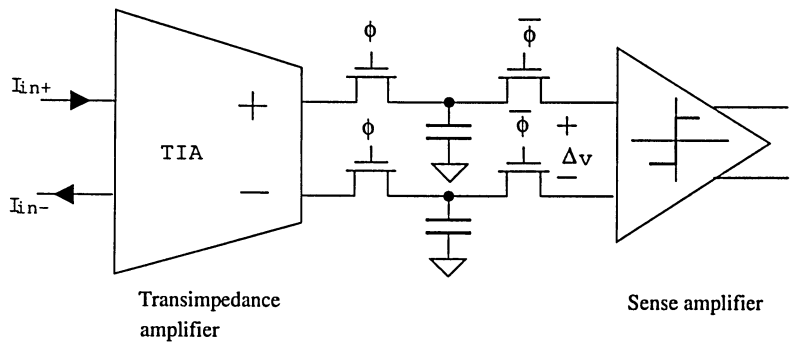


Figure 6.1: Current-integrating front-end with sense amplifier.

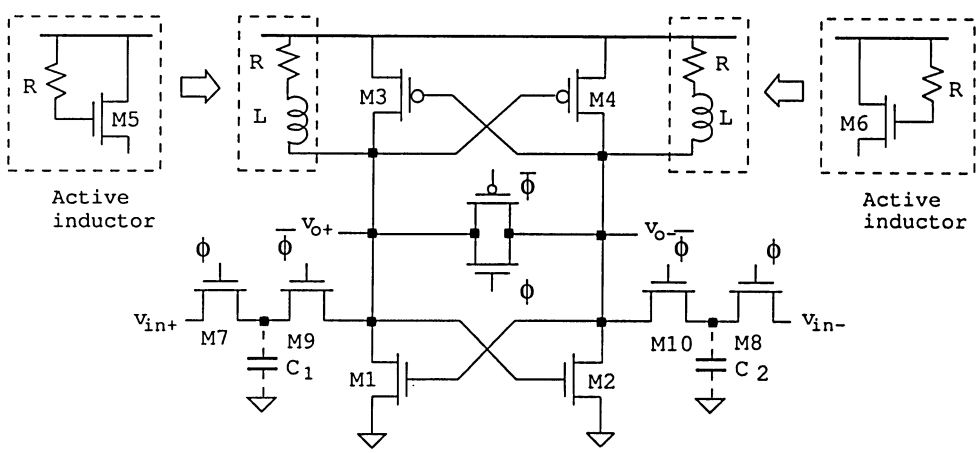


Figure 6.2: Sense amplifier.

6.1 Class A Sense Amplifer

We notice that sense amplifiers that are widely used in SRAM and Gbps serial links possess these attributes [27]. The schematic of the class A sense amplifier proposed in this thesis is shown in Fig. 6.2. The sense amplifier consists of a pair of cross-coupled static inverters controlled by an equalization switch. The equalization switch is realized using a transmission gate to take the advantage of its low equivalent channel resistance and low voltage drop. Inductor shunt-peaking is employed at the output node of the inverters to speed up transient response of the inverters. The active inductor implementation of the shunt-peaking network is also shown in the figure. The operation of the sense amplifier is depicted as the followings :

6.1.1 Integration Phase

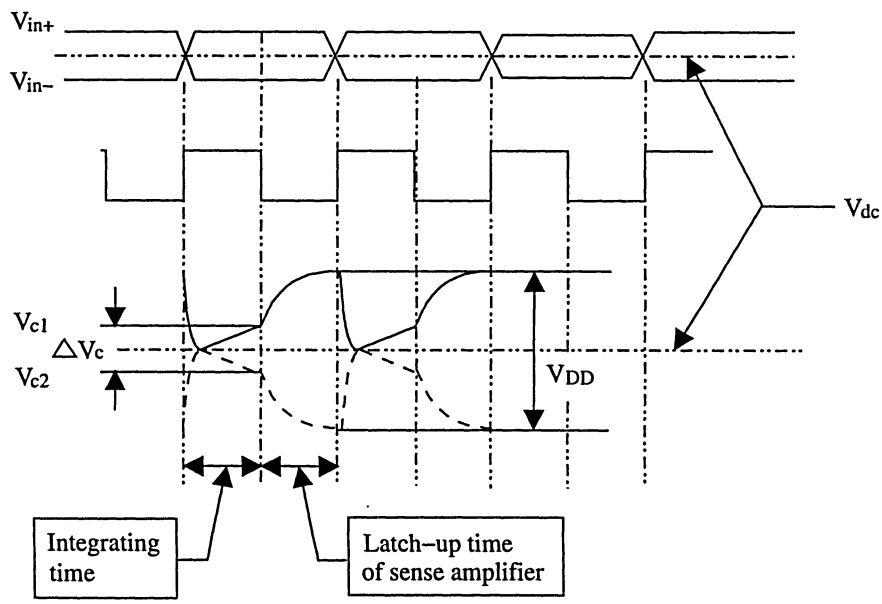


Figure 6.3: Operation of sense amplifier.

In Fig. 6.2, when $\phi = 1$, the differential output voltages of the preceding transimpedance front-end are integrated on capacitors C_1 and C_2 with the time constant given by $R_{on7,8}C_{1,2}$

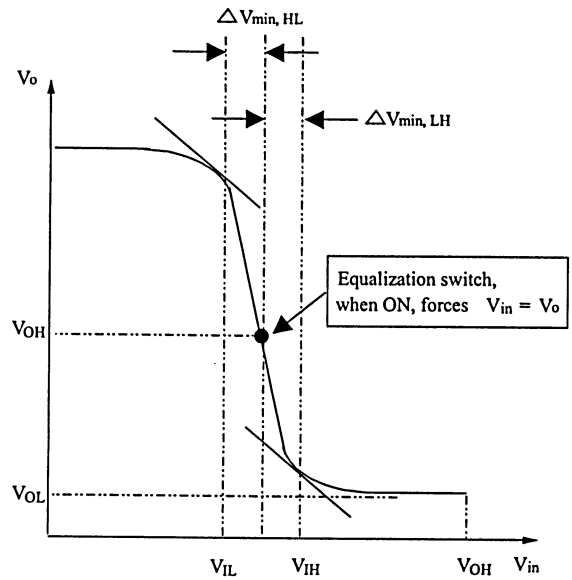


Figure 6.4: Voltage transfer characteristic of static inverters.

as shown in Fig. 6.3. Note that C_1 and C_2 are realized using the intrinsic and parasitic capacitances of the transistors connected to the nodes. The inverter pairs are isolated from the transimpedance front-end and the integrating capacitors, and are equalized by the transmission gate. The operating point of the inverters is forced to the middle of their state transition region where the input and output of the inverters are identical, as illustrated graphically in Fig. 6.4. Both the nMOS and pMOS transistors of the inverters in this case are in the saturation and each inverter consists of two common-source amplifiers with the voltage gain

$$A_v = -(g_{m,n} + g_{m,p})(r_{o,n} || r_{o,p}), \quad V_{IL} \leq v_{in} \leq V_{IH}, \tag{6.2}$$

where $g_{m,n}$ and $g_{m,p}$ are the transconductance of the nMOS and pMOS transistors of the inverter, respectively, and $r_{o,n}$ and $r_{o,p}$ are the output impedance of the nMOS and pMOS transistors, respectively. Note that the voltage gain is approximately twice that of a simple common-source amplifier. For each static inverter, when the variation of the input voltage of the inverter, denoted by Δv_{in}, satisfies

$$\Delta v_{in} > \Delta V_{min,HL} \text{ or } \Delta V_{min,LH}, \tag{6.3}$$

where $\Delta V_{min,HL}$ and $\Delta V_{min,LH}$ are defined explicitly in Fig.6.4, the output of the static inverter will switch from one logic state to the other. Because the cross-coupled static inverter pair form a positive feedback, a variation of the input voltage of the inverter pair that is smaller than $\Delta V_{min,HL}$ or $\Delta V_{min,LH}$ will first be amplified. When (6.3) is satisfied, a complete switch of the output voltage of the inverter pair will take place.

6.1.2 Latch-Up Phase

As shown is Fig. 6.2, when $\phi = 0$, capacitors C_1 and C_2 are disconnected from the transimpedance front-end. The cross-coupled static inverters are enabled with the turning off of the transmission gate and amplify the voltage of C_1 and that of C_2 at the end of the integration phase. The latch-up time, which is the time for the cross-coupled inverters to establish their logic states, depends upon the transconductance, the output impedance, and the gate capacitance of the transistors of the inverter pair and the channel resistance of $M_{10,11}$. It is rather difficult to reduce the latch-up time by manipulating the width of the transistors of the inverter pair simply because the capacitance and channel resistance are conflicting parameters. To speed up the transition, as shown in Fig. 6.2, the charge time of the output nodes is determined by the second-order RLC system instead of only first-order RC system. The large improvement in the rise and fall times reveals that inductor shunt peaking, a technique that is widely used for bandwidth enhancement of amplifiers [22].

6.1.3 Self-Biased Active Inductor

Inductors realized using an on-chip spiral layout suffer from a number of drawbacks including extremely area consuming, a small inductance, and a strong interaction with the substrate. The shunt-peaking inductors can be implemented using self-biased active inductors which is shown in Fig. 6.2. Neglecting C_{gd} and the second-order effects of the transistor, its small signal equivalent circuit is shown in Fig. 6.5.

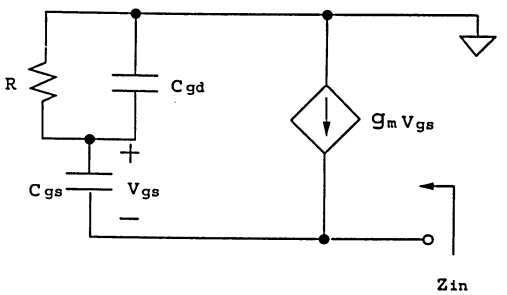


Figure 6.5: Small signal equivalent circuit of active inductor.

We can see that the input impedance of this active inductor is [26]

$$Z_{in}(s) = \frac{1 + sC_{gs5,6}R}{g_{m5,6} + sC_{gs5,6}}, \tag{6.4}$$

where $g_{m5,6}$ and $C_{gs5,6}$ are the transconductance and gate-source capacitance of the active inductor transistor $M_{5,6}$, respectively.

So the equivalent inductance L_s and series resistance R_s given by

$$R_s(\omega) = \frac{g_{m5,6} + \omega^2 C_{gs}^2 R}{g_{m5,6}^2 + \omega^2 C_{gs5,6}^2}. \tag{6.5}$$

The active inductor is inductive in the frequency range $\omega_z < \omega < \omega_p$, where $\omega_z = \frac{1}{RC_{gs}}$ and $\omega_p = \frac{g_m}{C_{gs}}$. If $g_{m5,6}R \gg 1$,

$$L_s(\omega) \approx \frac{R}{\omega_{t5,6}\left[1 + \left(\frac{\omega}{\omega_{t5,6}}\right)^2\right]}, \tag{6.6}$$

where $\omega_{t5,6} = \dfrac{g_{m5,6}}{C_{gs5,6}}$ is the device cut-off frequency of $M_{5,6}$. Several comments are made with respect to these two formulas:

1. The series inductance of the active inductor $L_s(\omega)$ is directly proportional to R and can be tuned by varying R.

2. Because $\omega_{t5,6}$ is large, the effective inductance of the self-biased active inductor $L_s(\omega)$ is small.

3. The self-biased acitve inductor has a non-zero series resistance $R_s(0) = 1/g_m$ and $R_s(\infty) = \mathrm{R}$. R_s is largely dominated by g_m, especially at low frequencies.

As shown in Fig. 6.2, the self-biased active inductor can be connected in parallel with a pull-up PMOS transistor to eliminate the loss of voltage swing. This is achieved by the pull-up PMOS load takes over once the self-biased active inductor enters its cut-off region when $V_o^+, V_o^- < V_{DD} - |V_{TP}|$. Where $|V_{TP}|$ is the threshold voltage of $M_{5,6}$.

6.2 Class AB Current-Mode Integrating Receiver

A new fully differential class AB current-mode integrating receiver is proposed in this section. The receiver consists of a class AB integrating stage and a class AB sense amplification stage which provide a voltage gain that is twice that of class A sense amplifier, enabling a fast sensing and latching.

6.2.1 Class AB Integrator

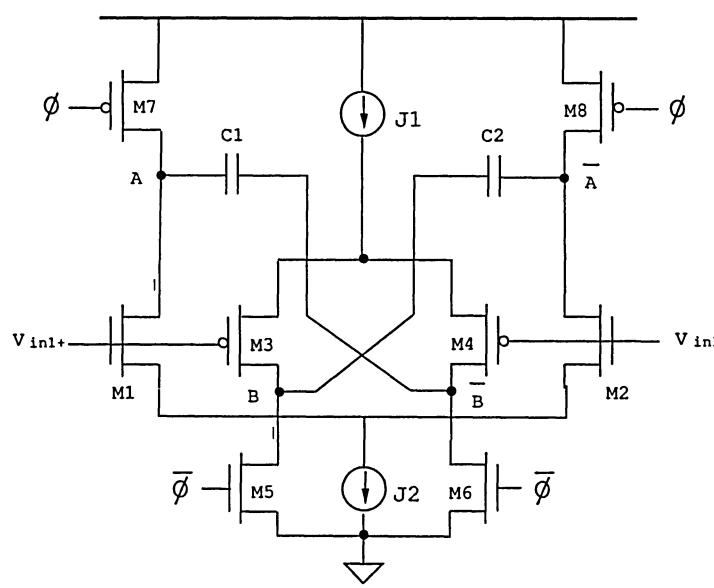


Figure 6.6: Class AB integrator.

The schematic of the proposed class AB integrator is shown in Fig. 6.6. The inputs of the integrator are from the preceding transimpedance front-end. The dc value of v_{in+} and v_{in-} is such that transistors $M_{1\sim4}$ are always in the saturation to avoid speed penalty from turning on/off transistors completely. When there is a differential input voltage exists, $v_{in+} = \frac{\Delta v}{2}$ and $v_{in-} = -\frac{\Delta v}{2}$. v_A drops while $v_{\overline{A}}$ rises. Similarly, v_B rises while $v_{\overline{A}}$ drops. Assume that the impedance of nodes A and $\overline{A}$ is Z_A and that of nodes B and $\overline{B}$ is Z_B, we have

$$\Delta V_A = -g_{m1,2} Z_A \frac{\Delta v}{2}, \tag{6.7}$$

$$\Delta V_{\overline{A}} = g_{m1,2} Z_A \frac{\Delta v}{2}, \tag{6.8}$$

$$\Delta V_B = g_{m3,4} Z_B \frac{\Delta v}{2}, \tag{6.9}$$

$$\Delta V_{\overline{B}} = -g_{m3,4} Z_B \frac{\Delta v}{2}. \tag{6.10}$$

If $g_{m1,2} = g_{m3,4} = g_m$ and $Z_A = Z_B = Z$, we obtain the variation of the voltage cross capacitors C_1 and C_2

$$\Delta V_{c1} = \Delta V_A - \Delta V_{\overline{B}} = 2 g_m Z \frac{\Delta v}{2}, \tag{6.11}$$

$$\Delta V_{c2} = \Delta V_{\overline{A}} - \Delta V_B = 2 g_m Z \frac{\Delta v}{2}. \tag{6.12}$$

It is seen that the class AB integrator doubles the voltage across the integrators.

6.2.2 Class AB Sense Amplifier

The schematic of the proposed class AB sense amplifier is shown in Fig. 6.7. The sense amplifier consists of a NMOS re-generative stage composed of M_1 and M_2 and a PMOS re-generative stage composed of M_5 and M_6. Transmission gates are equalization switches. The operation of the sense amplifier is depicted briefly as the followings : When $\phi = 1$,

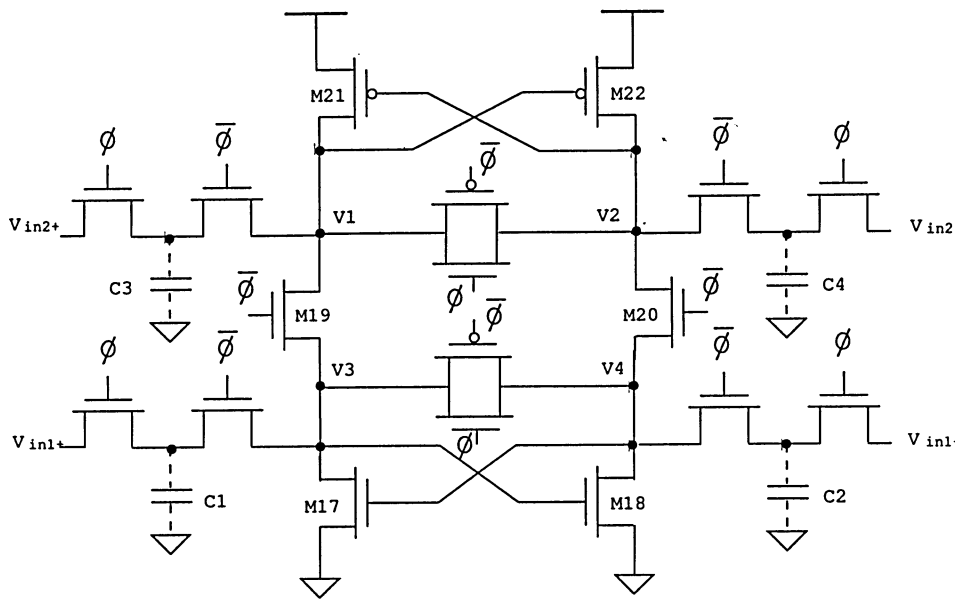


Figure 6.7: Class AB sense amplifier.

$V_1 = V_2$ and $V_3 = V_4$. The operating point of the re-generative amplifiers to the middle of their state transition region such that a small variation of the input voltage will enable the output of the re-generative amplifier to flip from one state to the other. The input signals are integrated on four capacitors $C_{1\sim4}$, which are the intrinsic capacitances of the transistors. When $\phi = 0$, the re-generative amplifiers amplify the input signals held by $C_{1\sim4}$ and withhold the resultant output. The speed of the re-generative amplifiers is determined by the time constant RC at the output node of the amplifiers.

Chapter 7

Simulation Results

To assess the performance of the proposed current-mode incremental signaling scheme and the current-integrating receiver, a four-bit parallel link consisting of four bipolar current-mode drivers, each conveys a ± 2 mA differential current to the channels, five microstrip lines of length 10 cm with FR4 substrate [35], and four current-integrating receivers is implemented in UMC 0.13μm 1.2V CMOS technology, as shown in Fig. 7.1.

The circuit parameters of class A are tabulated in Table 7.1, and those of class AB are tabulated in Table 7.2. The mutual coupling between the channels is neglected. The link is analyzed using *SpectreRF* from Cadence Design Systems with BSIM3.3V device models that count for both the parasitics and high-order effects of MOSFETs. Because the three inner channels are shared by neighboring receivers, the impedance seen at the far end of these three channels are $Z_{in}/2$, where Z_{in} is the single-ended input impedance of the transimpedance front-end of the receivers. The impedance encountered at the far end of the two outer channels is only Z_{in}. Impedance asymmetry is countered at the two outer receivers. Although the impedance asymmetry can be removed by changing the biasing condition of the two outer transimpedance front-ends, the fully differential operation of these front-ends will be eliminated. This difficulty can be overcome by adding impedance-balancing networks at both the near and far ends of the two outer channels, as shown in Fig. 7.1, where $\frac{1}{2}$TIA denotes half of the transimpedance front-end with common-mode feedback. The added impedance-balancing networks ensure that

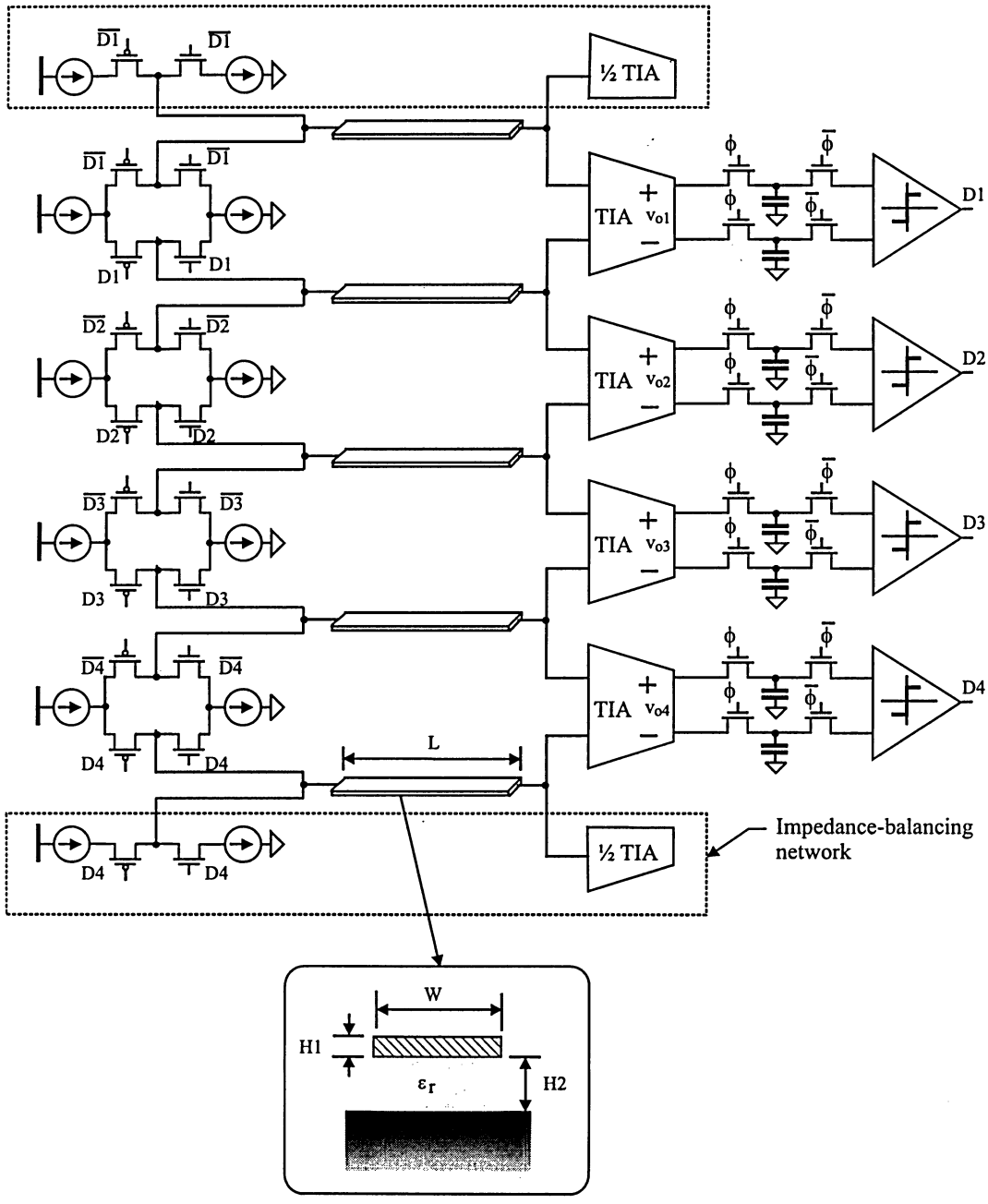


Figure 7.1: 4 channel source synchronized parallel link using current integrating receivers.

1. The impedance seen by each channel at the far end of the channel is identical and is given by $Z_{in}/2$.

2. The sum of the currents flowing through the cross-section of the channels is zero, minimizing the electromagnetic interference exerted from the channels to neighboring devices.

Table 7.1: Circuit parameters of transimpedance/current-integrating front-end with class A sense amplifier. $L = 0.13\mu$m for all transistors

Blocks	Parameter	Value
Transimpedance /current-integrating front-end	$W_{1,2}$	30 μm
	$W_{3,4}$	20 μm
	$W_{5,6}$	1 μm
	$W_{7,8}$	10 μm
	$W_{9\sim12}$	10 μm
	$R_{1,2}, R_T$	50 Ω
	V_{b1}	0.6 V
	V_{b2}	0.65 V
Channel model	Type	Microstrip
	Microstrip line width W	200 μm
	Microstrip line length L	10 cm
	Microstrip line height H_1	50 μm
	Model frequency range	0-20 GHz
	Dielectric constant ϵ_r	5
	Dielectric thickness H_2	500 μm
Sense amplifier	$W_{1,2}$	30 μm
	$W_{3,4}$	20 μm
	$W_{5,6}$	variable
	$W_{7\sim10}$	10 μm
	W_{TG}	10 μm
	R	500 Ω

7.1 Transimpedance Front-End

The voltage at the far end of the channels, i.e. the inputs of the transimpedance front-ends are plotted in Fig. 7.2 with impedances match from the front-ends, where $V_b = 0.6$ V.

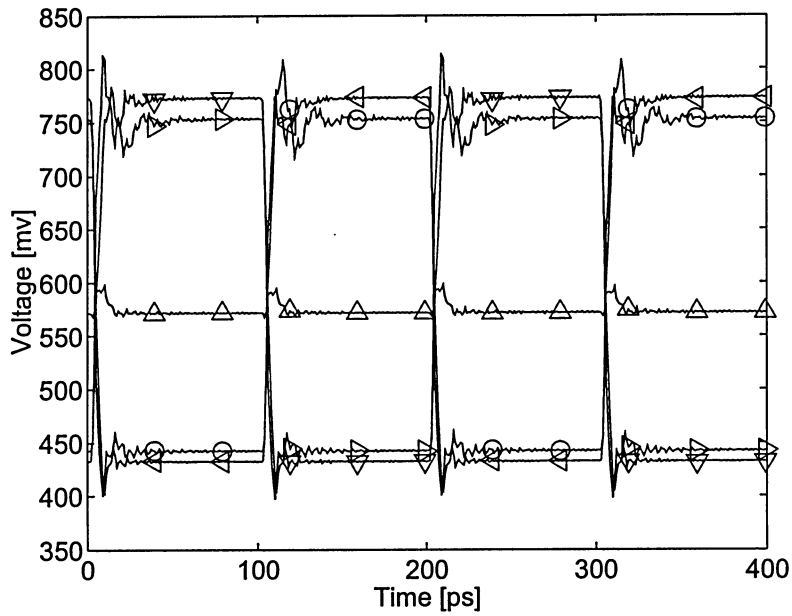


Figure 7.2: Simulated input voltage of a four-bit parallel link with transimpedance front-end when matching impedances are presented. Legends : ◯ : v_{in1}, △ : v_{in2}, ▽ : v_{in3}, ◁ : v_{in4}, and ▷ : v_{in5}.

Table 7.2: Circuit parameters of transimpedance/current-integrating front-end with class AB sense amplifier. $L = 0.13\mu$m for all transistors

Parameter	Value
V_{DD}	$1.3V$
$W_{1\sim2}$	30μm
$W_{3\sim4}$	20μm
$W_{5\sim6}$	1μm
$W_{7\sim8}$	10μm
$W_{9\sim10}$	5μm
$W_{11\sim12}$	10μm
$W_{13\sim14}$	20μm
$W_{15\sim32}$	10μm
$R_{1\sim2}$	50Ω
$R_{3\sim4}$	500Ω
V_{bias}	0.6V
V'_{bias}	0.65V
TG_nMOS	10μm
TG_pMOS	10μm

Also, the voltage of inputs of the transimpedance front-ends are plotted in Fig. 7.3 without impedances match from the front-ends.

At the output of transimpedance front-ends, Figs. 7.4 shows the output voltage of a four-bit parallel link when matching impedances are presented.
Also, the voltage of outputs of the transimpedance front-ends are plotted in Fig. 7.5 without impedances match from the front-ends.

It is seen that the ringing of the voltage is small when matching impedances are present. The ringing increases when the input impedance drifts away from the matching impedances.

7.2 Current-Integrating Front-End

The output voltage of the current-integrating receiver without the sense amplifiers is plotted in Fig. 7.6. It is seen that the voltage varies with time exponentially during the integration phase and returns to the value set by the preceding transimpedance front-end at the end of the reset (evaluation) phase. When the channel resistance of the reset switch is considered,

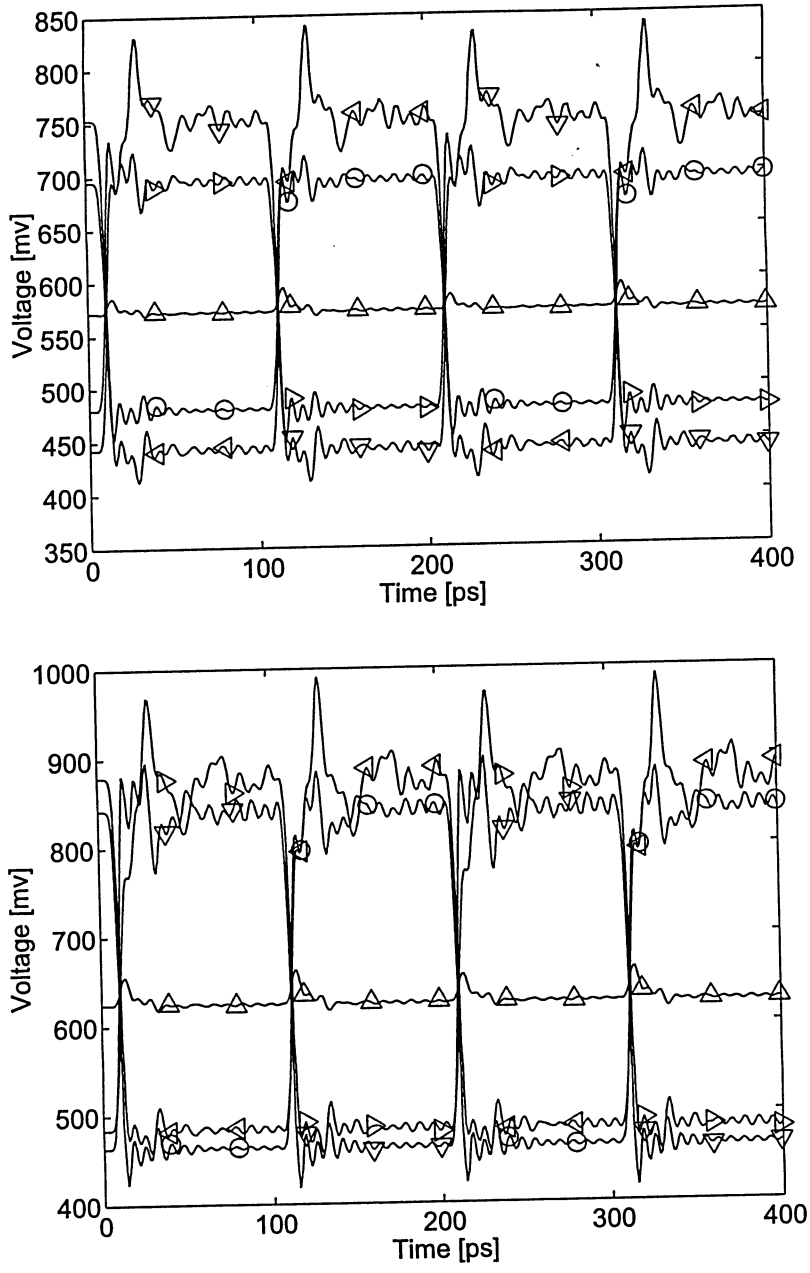


Figure 7.3: Simulated input voltage of a four-bit parallel link with transimpedance front-end when matching impedances are not presented. Top : $V_b = 0.5$V. Bottom - $V_b = 0.8$ V. Legends : ○ : v_{in1}, △ : v_{in2}, ▽ : v_{in3}, ◁ : v_{in4}, and ▷ : v_{in5}.

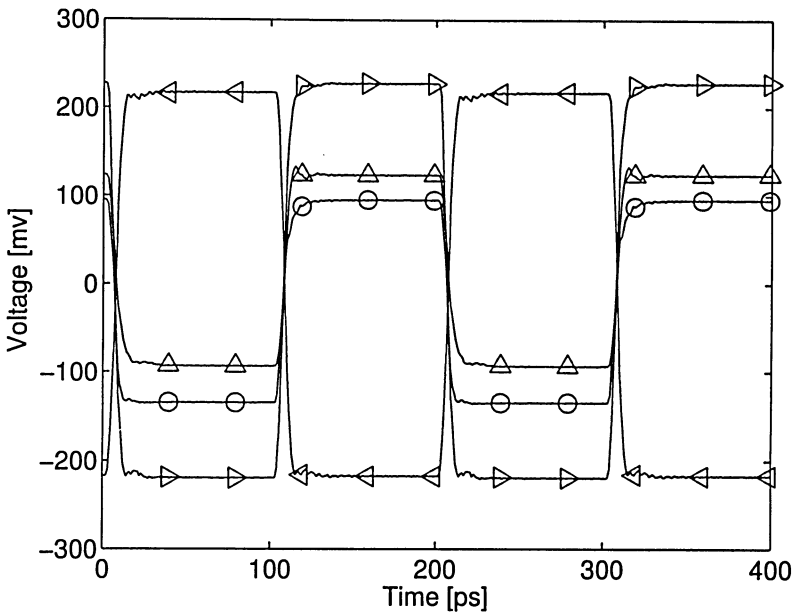


Figure 7.4: Simulated output voltage of a four-bit parallel link with transimpedance front-end when matching impedances are presented. Legends : ○ : v_{o1}, △ : v_{o2}, ◁ : v_{o3}, ▷ : v_{o4}.

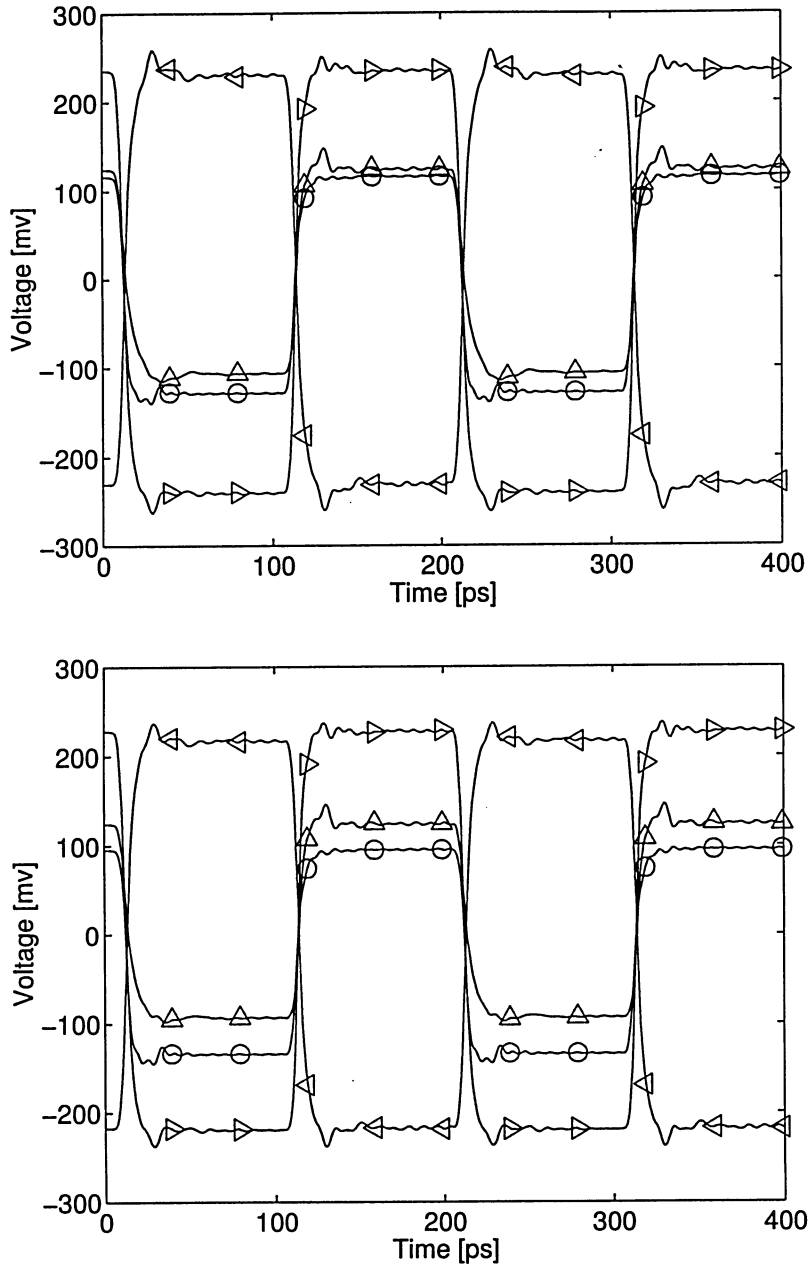


Figure 7.5: Simulated output voltages of a four-bit parallel link with transimpedance front-end when matching impedances are not present. The voltage is DC-shifted by 1.09V. Top - $V_b = 0.5$ V. Bottom - $V_b = 0.8$ V. Legends : ○ : v_{o1}, △ : v_{o2}, ◁ : v_{o3}, and ▷ : v_{o4}.

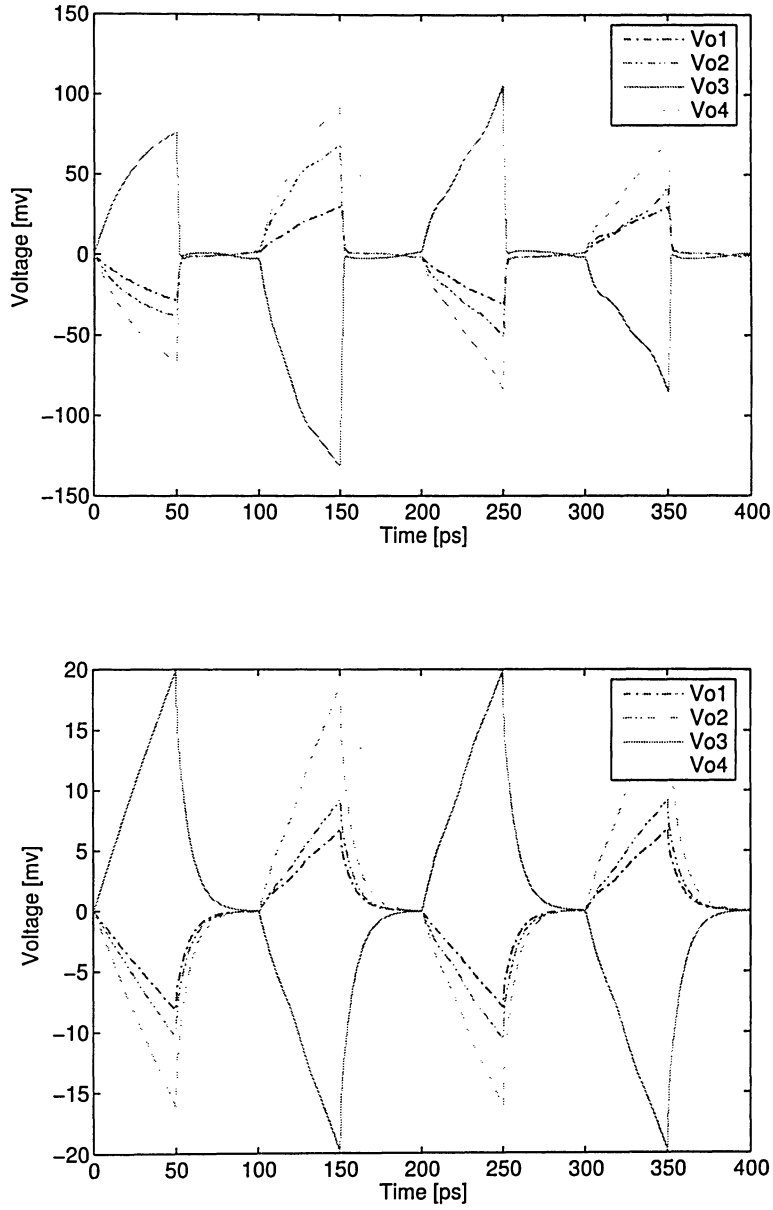


Figure 7.6: Simulated output voltages of a four-bit parallel link with current-integrating front-end and integrating capacitors (without the sense amplifiers). The voltage is DC-shifted by 1.09V. Top - with ideal reset switches; Top - with TG reset switches.

the output voltage is smaller as compared with that with ideal reset switches. In both case, the variation of the voltage across the integrating capacitors is small.

7.3 Class A Current-Mode Integrating Receiver

Fig. 7.7 plots the output voltage of the current-integrating receiver with the sense amplifiers. It is seen that the output voltage of the receivers is clamped at $V_{DD}/2$ approximately during the integration phase and reaches full swing at the end of the evaluation phase. This observation agrees with the theoretical analysis given earlier. The improvement in the transient behavior of the output voltage of the receiver due to the use of peaking inductors is evident, especially when the inductance of the peaking inductors is large. The output voltage of the receiver with the self-biased shunt-peaking active inductors is also plotted in Fig. 7.7. The speed improvement is comparable to that with the passive peaking inductors. The performance of the current-integrating receiver is summarized in Table 7.3.

Table 7.3: Performance of current-mode integrating receiver

Technology	UMC-0.13 μm 1.2 V
Data rate	2.5 Gbyte/s
Input current	$\pm$2 mA
Output voltage swing	1.2 V peak-to-peak
Current drawn from V_{DD}	9.1 mA
Transistor area	$302\times0.13\mu m^2$
Power consumption	10.92 mW

7.4 Class AB Current-Mode Integrating Receiver

Fig. 7.8 plots the voltage of the integrating capacitors of both class A and class AB current-mode integrating receiver. It is seen that the voltage cross the integrating capacitors of the class AB receiver is twice that of the class A receiver. The output voltage of the class AB current-mode integrating receiver is shown in Fig. 7.9. The employment of the class AB

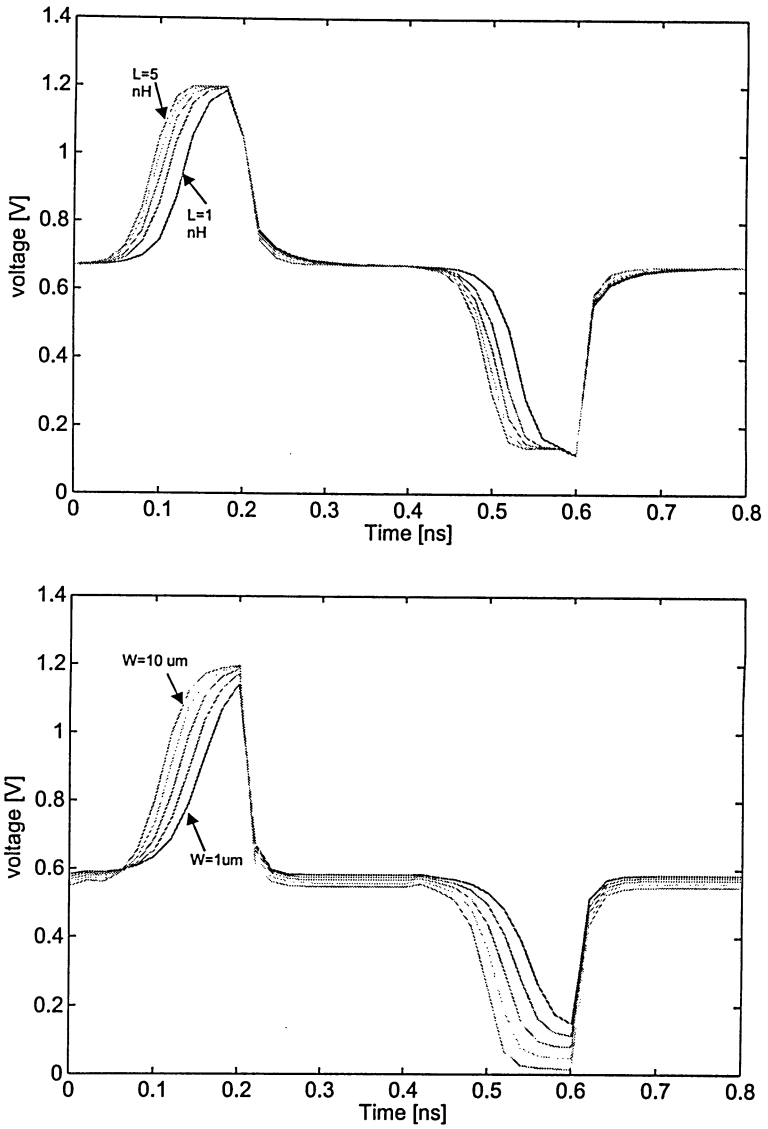


Figure 7.7: Simulated output voltage of a four-bit parallel link. Top - passive shunt-peaking inductors. L is varied from 1nH to 5nH with step 1nH; Bottom - active shunt-peaking active inductors. $W_{5,6}$ are varied from 1μm to 10μm with step 2.25μm.

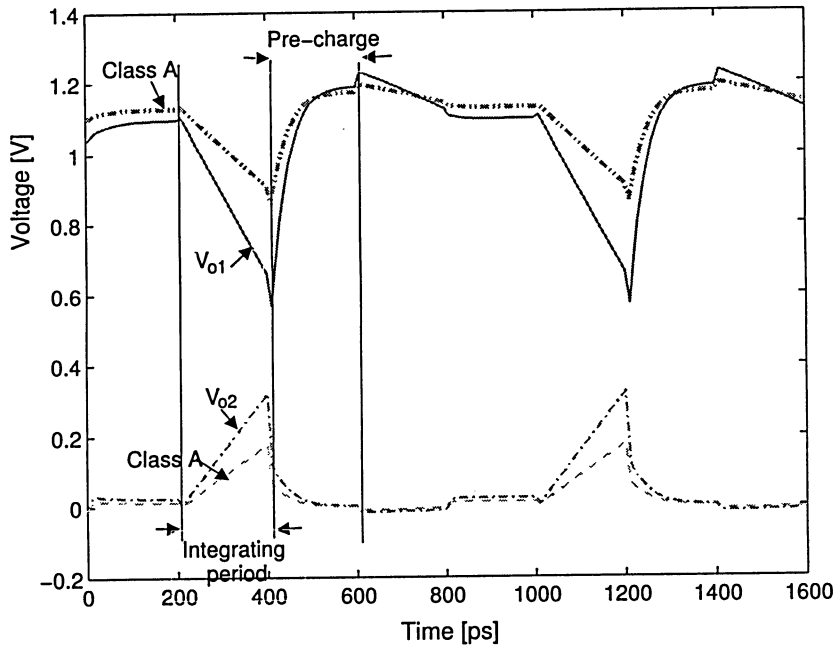


Figure 7.8: Comparison of the voltage across integrating capacitors of class AB current-mode integrating and class A current-mode integrating.

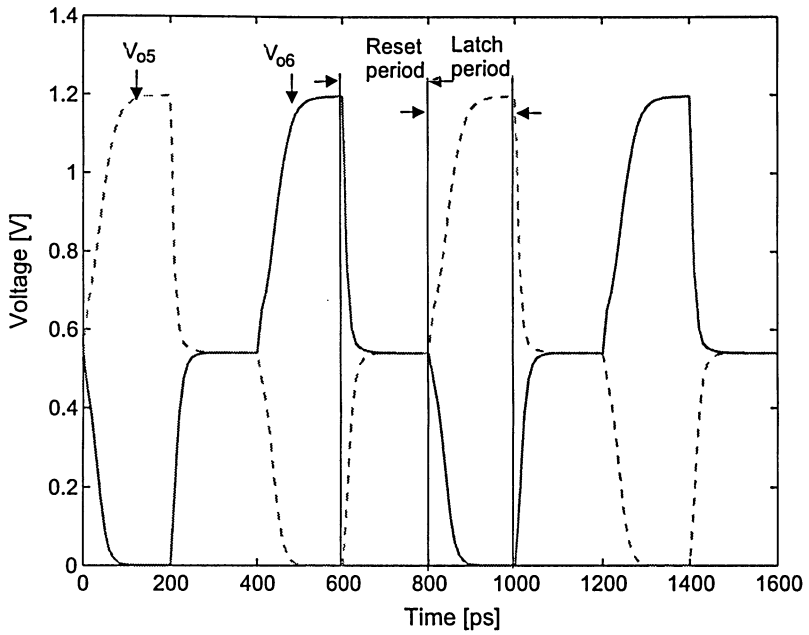


Figure 7.9: Output voltages of the class AB current-mode integrating receiver.

sense amplifier snsures that the output voltage of the receiver reaches full swing in less than 200ps,indicating that the proposed class AB current-mode integrating receiver is capable of sensing the recovering parallel data at 2.5GBytes/s.

Chapter 8

Conclusions

In this thesis, we have described the basic data link schemes. Also, we have detailed two fundamental challenges in high-speed data communication design: the voltage noise and time recovering. The sources of voltage and timing errors limit the performance of the data links and affect their robustness. For example, voltage noise sets the minimum signal swing, and hence power, required for robust link operation, and may cause bit errors. In high-speed parallel links, the major voltage noise sources are channel attenuation and inter-symbol interference, offset, reflections, cross-talk, and power supply noise. Many possible solutions, such as, fully differential signaling scheme, pseudo differential signaling scheme, and voltage-mode incremental signaling scheme, exist to reduce the affection of these noise sources or minimize their impacts on the system performance. However, almost every scheme requires adding extra hardware or increasing the per I/O cost, therefore conflicting with the low cost per I/O requirement that is essential for mass integration of parallel I/Os. Hence, every design involves trade-offs among performance and cost.

In this thesis, a new low-voltage current-mode incremental signaling scheme and a new fully differential current-integrating receiver has been presented. The signaling scheme utilizes the intrinsic advantages of current-mode signaling that is critical to high-speed data links. The current-integrating receiver consisting of a transimpedance front-end, an integrator, and a sense amplifier with active inductor shunt peaking offers the key advantages of a low and tunable input impedance for channel termination, large bandwidth, and ef-

fective suppression of transient noise coupled to the channels. It is implemented in UMC 0.13μm, 1.2V CMOS technology and analyzed using *SpectreRF* from Cadence Design Systems with BSIM3V3 device models. Simulation results have demonstrated that the proposed low-voltage current-mode incremental signaling scheme and the current-integrating receiver are capable of transmitting parallel data at 2.5 Gbyte/s.

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