Complex Incremental $\Sigma\Delta$ ADC

by

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Complex Incremental ΣΔ ADC

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Abstract

This thesis examines the theory and design of incremental Sigma-Delta (ΣΔ) modulators when applied to complex oversampling analog-to-digital converters (ADCs). Two different types of approaches for the complex ADC are analysed and compared.

The first system is a traditional complex bandpass over-sampling ADC with incremental (time limited) ΣΔ architecture. This system uses cross-coupling switch capacitor (SC) integrators and quadrature two channel inputs.

The second system uses a low-pass architecture with time interleaved integrators. This system does not have a mismatch between the in-phase and quadrature phase (I/Q) output channels. The input is frequency shifted down to DC during the conversion.

A graphical user interface (GUI) design toolbox was created to design and simulate the two types of systems. The bandpass second-order system was fabricated in an IBM 130nm CMOS process with a 83kHz two channel input and 10kHz bandwidth at an OSR of 24.

Acknowledgements

First, I would like to acknowledge and thank my parents, Igor and Alla, for their support and help throughout my life. I am also very grateful to my grandmother, Nina, whose constant motivation has helped me realized my full potential.

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Most of all, I could not have completed this thesis without the support and encouragement of my fiancée, Melissa Gauvin. Thank you for never giving up on me; your moral support was invaluable through the difficult times.

Dedication

This paper is dedicated to my father, Igor Peker, who instilled in me the drive and discipline required to tackle any task with enthusiasm and determination.

Contents

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List of Abbreviations

$\Sigma\Delta$	Sigma-Delta
$I\Sigma\Delta$	Incremental Sigma-Delta
ADC	Analog-to-Digital converters
BP	Bandpass
BW	Bandwidth
CIC	Cascade-Integrator-Bomb
CM	Common Mode
CMFB	Common mode feedback
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DNL	Differential Non-Linearity
ENOB	Effective Number of Bits
FB	Feedback
FF	Feed-Forward
GUI	Graphical User Interface
I	In-Phase
IF	Intermediate Frequency
IRR	Image Rejection Ratio
LO	Local Oscillator
LP	Low-Pass

LSB Least Significant Bit

NG Noise Gain

NMOS N-Channel Metal-Oxide-Semiconductor

NTF Noise Transfer Function

OSR Oversampling Ratio

OTA Operational Transconductance Amplifier

PMOS P-Channel Metal-Oxide-Semiconductor

PSD Power Spectrum Density

PWM Pulse Width Modulation

Q Quadrature Phase

S/H Sample and Hold

SAR Successive Approximation

SC Switched-Capacitor

SIS Self-Image Signal

SQNR Signal-to-Quantization-Noise Ratio

SS State Space Model

STF Signal Transfer Function

Chapter 1

Introduction

Technology is moving towards digital hardware and systems. Automated techniques have made digital hardware easier to produce and test. Since digital software is easier to reconfigure or reuse, it allows for fast turnaround time. Analog equivalent circuits in industry applications such as data acquisition, controls, digital thermometer, compact disk, and digital radio receivers cannot match up. Considering that the physical world is analog, sensors and actuators, which measure in continuous time, have to be converted to digital, discrete time and amplitude. For this reason, a analog-to-digital converter (ADC) is a crucial component of almost every device we use. A sub set of converters is over-sampling ADCs, which use over-sampling to shape quantization noise. This thesis focuses on over-sampling ADC, with regard to both theory and design.

High-speed ADCs operate at intermediate frequencies (IF) , ranging from a megahertz to hundreds of megahertz. There are many different types of ADCs architecture, and so classification is important. One such classification is the ratio of sampling rate, (f_s) and bandwidth (B), which is refereed to as oversampling ratio (OSR). Since Nyquist-theorem states that $f_s \geq 2B$ must be true for any sampler to preserve the input signal without aliasing, the OSR is defined as $f_s/2B$. A converter that operates at $OSR = 1$ is running at Nyquist-rate.

Most high-speed converters operate at a very high OSR and the final output is then digitally filtered and decimated to produce a Nyquist rate for the subsequent digital processing. Only the frequency response of the input is preserved during the conversion. The performance is judged by the resolution of the output, bandwidth and power consumed during the conversion.

Most applications have very different requirements regarding resolution, bandwidth and power consumption. For instance, Microcontrollers have medium requirements for all three categories. By contrast, in the automotive industry, although neither the power consumption nor the bandwidth requirements are a major concern, the resolution requirements are high. As in automotive industry, cell phones require high bandwidths for data transfer but power consumption in cell phones is important.

Today's trends are moving towards the integration of analog and mixed signal systems onto one chip. Low precision analog elements and on chip noise limit the resolution of Nyquist rate converters. In order to overcome these limitations, over-sampling converters such as Sigma-Delta ($\Sigma\Delta$) converters are used

to improve resolution.

1.1 Motivation

ΣΔ modulators, referred to as noise-shaping converters, perform conversion at a high OSR. The disadvantage of using high OSR is reduced bandwidth (BW) and increased power consumption. When low power and high absolute accuracy are required, incremental ΣΔ converters (a special ΣΔ topology) are used. The integrators in the sigma delta and incremental converters differ because the latter one requires a reset every T_s. As a result of this reset, an incremental converter operates like a Nyquist converter, allowing a one-to-one conversion [1]. Noise shaping is minimalized by the resets, and so, in order to improve performance and reduce conversion time, higher order filters are utilized.

Since a high throughput in communication is needed, quadrature or complex systems are employed. ΣΔ is frequently used for these applications because it maintains the spectrum of the input, has a large dynamic range and tolerates process variations. There are two types of ΣΔ modulators for real IF inputs: complex bandpass (BP) ΣΔ modulators and complex low-pass (LP) ΣΔ modulators with built-in IF mixers.

A drawback of the complex modulators is the mismatch between the in-phase and quadrature phase (I/Q), which adversely affects its image rejection ratio (IRR) and signal-to-quantization-noise ratio (SQNR) . The complex signal processing differs from a regular modulator because it is not centred at DC. When the IF signal is converted down near DC (in order to avoid DC offset and 1/f noise), an adjacent radio channel becomes the image signal.

To eliminate I/Q mismatch, dynamic element matching methods have recently been proposed. These methods, which reduce the matching problem between the digital-to-analog converter (DAC) in the feedback path, are only a partial solution[2]. Complex LP typology, proposed in [3],has shown that the use of shared input sampling capacitors reduced I/Q mismatch. However, since there are still two paths, some mismatch may still occur.

The next section shows resent publications in both incremental and complex ΣΔ modulators but no overlap between the two exists. To apply incremental ΣΔ mode to complex modulators is the motivation for this thesis, since it has never been done before. Both complex BP and complex LP typologies are designed to implement incremental mode.

1.2 Current Literature

1.2.1 High-Speed Incremental A/D Converters

When incremental ΣΔ was first introduced in 1987 [4], it did not receive much attention until a Ph.D thesis by Mákus [5] demonstrated good performance for higher order architectures and filters. Over the last decade, there has been considerable research in the field of incremental ADCs, as reflected in Table 1.1. The modulators with the highest sampling frequencies are continuous time, as to be expected.

Ref.	Technology	Architecture	Sampling Frequency	Signal Bandwidth	OSR	SNDR	Power
[1]	0.6 μm	3rd-order	30.72 kHz	60 Hz	512	121.93 dB	0.6 mW
[6]	0.18 μm	3rd-order	10 MHz	1.1KHz	230	81.5 dB	6.6 mW
[7]	0.18 μm	2nd-order	45.2 MHz	0.5MHz	45	86.3 dB	38.1 mW
[8]	0.5 μm	1st-order	512 kHz	500 Hz	1024	59 dB	20 μW
[9]	0.18 μm	8th-order	50 MHz	8.33 MHz	3	40.3 dB	151 mW
[10]	Simulation	2nd-order	120 kHz	1 kHz	128	98 dB	N/A
[11]	0.13 μm	2nd-order	5 MHz	1.67 kHz	1500	89.9 dB	83 μW
[12]	90 nm	2nd-order	1 MHz	977 Hz	256	74 dB	6.75 μW
[13]	0.15 μm	3rd-order	320 kHz	2 kHz	320	65.3 dB	96 μW

Table 1.1: Recently published experimental results for $I\Sigma\Delta$ modulators.

Incremental $\Sigma\Delta$ modulators do not outperform traditional $\Sigma\Delta$ modulators unless the OSR is low and the noise shaping is minimal [9]. The main advantage of incremental converters is the one-to-one conversion, allowing multiplexing of different inputs to be done without cross talk. In this paper a fourth-order cascade incremental $\Sigma\Delta$ ($I\Sigma\Delta$) ADC is used to multiplex I/Q channels for a mismatch-free quadrature ADC.

1.2.2 Bandpass $\Sigma\Delta$ ADC

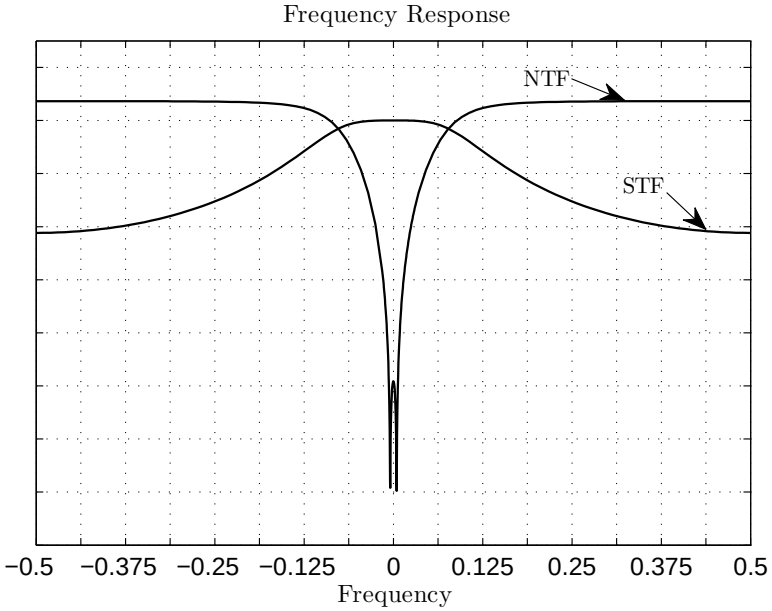


Figure 1.1: NTF spectrum for low-pass $\Sigma\Delta$.

$\Sigma\Delta$ modulators use over-sampling to create noise shaping to improve the accuracy of the conversion.

Signal and noise have different transfer functions. The signal transfer function usually has a gain of 1 in the band of interest allowing the signal to pass through the system. In higher order systems the signal transfer function (STF) has attenuation for out of band noise and at aliasing frequencies. Noise transfer function (NTF) is the key characteristic of ΣΔ modulators. Instead of having white noise or folding noise due to quantization, ΣΔ modulators reduce quantization noise from the band of interest and push it to higher frequencies, as shown in Fig. 1.1.

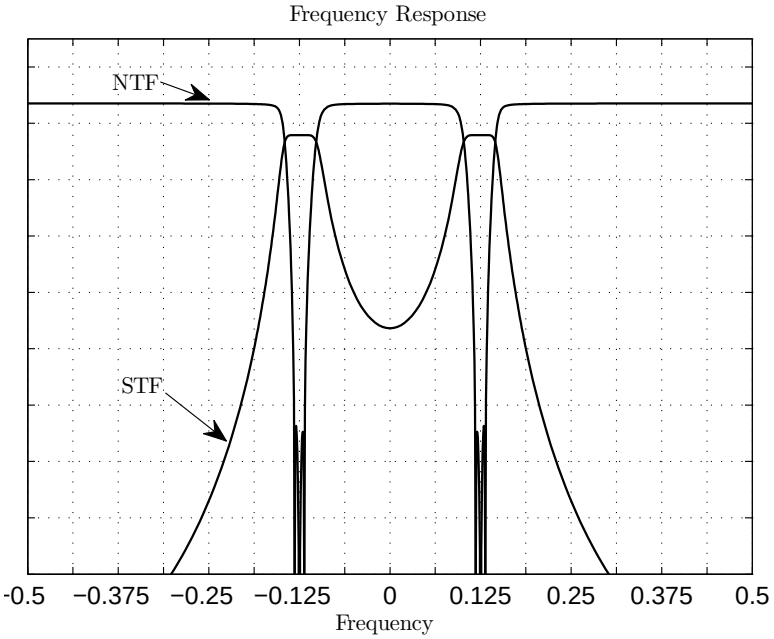


Figure 1.2: NTF spectrum for bandpass ΣΔ.

NTF and STF in bandpass modulators are centred around a frequency that is not zero. Usually, to simplify the math, the center frequency is selected to be $f_s/4$,as explained in Chap. 3. The spectrum of bandpass modulators is shown in Fig. 1.2. The STF for this type of system attenuates out of band signals.

A sub category of bandpass ΣΔ are the complex bandpass modulators. These modulators use complex filters, as opposed to regular ones, to shape noise from positive or negative frequencies, but not both. The NTF and STF spectrum representation can be seen in Fig. 1.3.

In the last several years there has been considerable research on bandpass and complex ΣΔ modulators. Table 1.2 shows recent work on the bandpass and complex Sigma-Delta modulators.

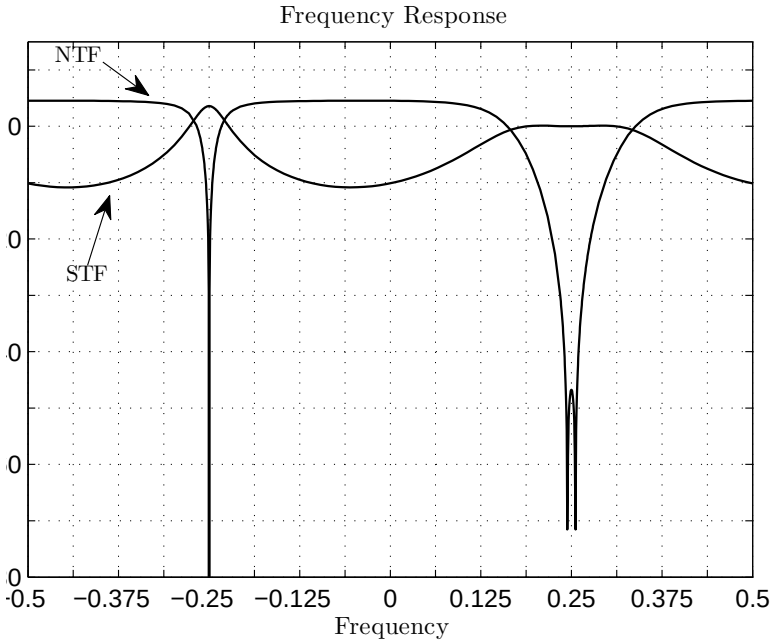


Figure 1.3: NTF spectrum for complex bandpass $\Sigma\Delta$.

1.3 Thesis Organization

This thesis is divided into 6 chapters: Chapter 2 introduces the operation as well as the advantages and disadvantages of $I\Sigma\Delta$ ADCs. Chapter 3 presents the operation of complex BP and LP $\Sigma\Delta$ modulators. Chapter 4 presents the original work into implementing incremental mode to complex $\Sigma\Delta$ modulators. Chapter 5 presents experimental results of a test chip fabricated in an IBM 130 nm process. Finally, Chapter 7 concludes the thesis.

Ref.	Technology	Architecture	Sampling Frequency	Signal Bandwidth	OSR	SNDR	Power
[14]	0.35 μm	3rd - order	3.4 MHz	200 kHz	32	57 dB	37.2 mW
[15]	0.18 μm	4th - order	264 MHz	8.5 MHz	6	71 dB	375 mW
[16]	90 nm	2-2 MASH	340 MHz	20 MHz	32	69 dB	56 mW
[17]	65 nm	5th - order	436 MHz	N/A		14 dB	18 mW
[18]	0.35 μm	2nd - order	60 MHz	1 MHz	3	63 dB	16 mW
[19]	0.35μm	2nd - order	50 MHz	1 MHz	50	60 dB	28 mW
[20]	0.25 μm	3rd - order	150 MHz	2 MHz	32	63.9 dB	2.7 mW
[21]	0.18μm	5th - order	64 MHz	2 MHz	16	82 dB	9 mW
[22]	90 nm	6th - order	3 GHz	60 MHz	2	40 dB	40 mW
[23]	90 nm	3rd - order	4 GHz	50 MHz	4	53.6 dB	69 mW
[24]	0.25 μm	3rd - order	2 MHz	200 kHz	5	86.8 dB	2.7 mW
[25]	0.18 μm	6th - order	800 MHz	10 MHz	4	68.4 dB	160 mW
[26]	0.18 μm	4th - order	100 MHz	3 MHz	16	57.8dB	11.8 mW
[27]	0.18 μm	5th - order	128 MHz	2 MHz	32	60.3dB	9 mW
[28]	65 nm	3rd - order	80 MHz	10 MHz	16	84.5 dB	4.2 mW
[28]	65 nm	2rd - order	80 MHz	5 MHz	16	84.6 dB	4.2 mW

Table 1.2: Recently published experimental results for bandpass and complex $\Sigma\Delta$ modulators.

Chapter 2

Incremental Mode ΣΔ

This chapter focuses on the basics of incremental ΣΔ converters. ΣΔ modulators will be discussed first. This will be followed by the presentation of the operation of first-order incremental ΣΔ converters. The operation of higher-order converters and various decimation filters for incremental ΣΔ converters will be examined.

2.1 ΣΔ Converters

2.1.1 First-Order ΣΔ Converter

A first-order ΣΔ modulator is simply a loop filter with an integrator and a low resolution quantizer, as shown in Fig. 2.1. The system must have a high OSR to maintain low noise in the band of interest. The quantizer is modelled as a noise source, E1. For a first-order system, the integrator is a SC circuit with the transfer function,

$$\frac{V_o(z)}{V_{in}(z)} = \frac{z^{-1}}{1 - z^{-1}}. \tag{2.1}$$

It follows that the output of the system in Fig. 2.1 is given by

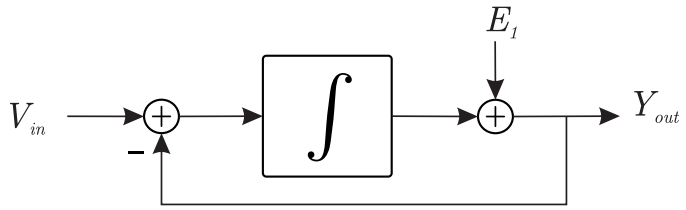


Figure 2.1: System diagram of ΣΔ modulators loop filter.

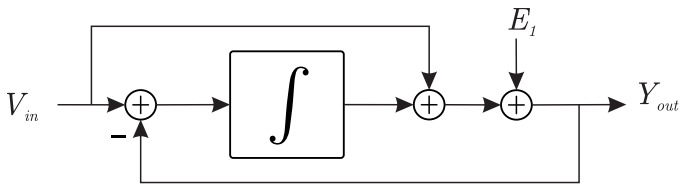


Figure 2.2: System diagram of ΣΔ modulators loop filter using feed-forward.

$$Y(z) = \frac{z-1}{z}\left[X(z) - Y(z)\right] + E(z) \tag{2.2}$$

from which we have

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{2.3}$$

where the Y(z) is the output bit stream from the quantizer and X(z) is the input of the modulator. The NTF and STF of the system are given by

$$STF = \frac{Y(z)}{X(z)} = z^{-1}, \tag{2.4}$$

$$NTF = \frac{Y(z)}{E(z)} = 1 - z^{-1}. \tag{2.5}$$

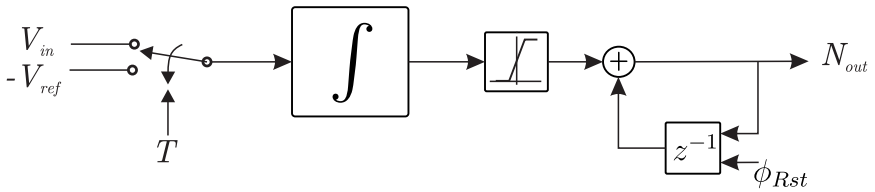
The signal passes through unattenuated but has a delay, while the noise is attenuated at low frequencies. Using a feed-forward architecture, shown in Fig. 2.2, allows the input enters the delay-free path so that no delay will exist for the signal. The integrator does not see the input signal due to negative feedback and only the error enters the integrator. In some cases, the error may be correlated with the input. For higher resolution internal quantizers, the error is less dependent on the input[9].

High-order integrators can be used to further suppress quantization noise from the band of interest. If higher-order modulators are used, stability becomes a design problem. The high gain of the integrators may saturate the quantizer and the negative feedback will not keep the system stable.

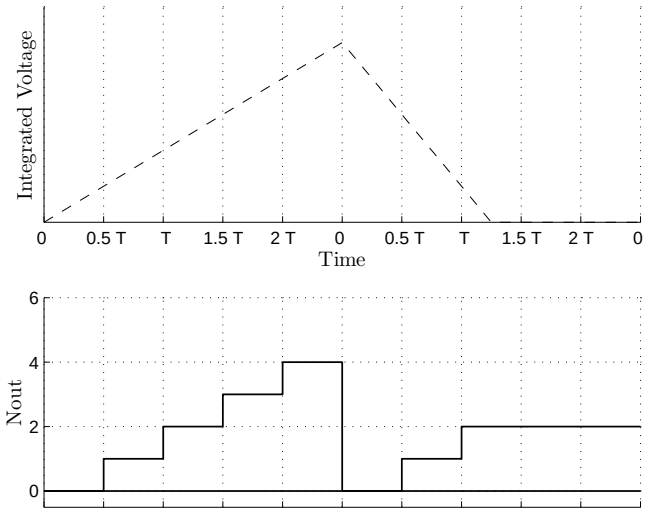
The decimation for a ΣΔ modulator is usually preceded by a LP comb filter, which removes all high frequency quantization noise. The LP filter is important and its performance requirements are application dependent. A moving average filter can also be used. For example, the bit stream from a one bit quantizer is 0 1 0 0 1 0 0 0, and the average of the 8 bits is 2/8 or $0.25FS$.

2.2 Incremental ΣΔ Converters

First-order incremental ΣΔ modulators, which achieved a 16-bit resolution, were first introduced by Robert et al. in 1978 [4]. The operation of these converters is similar to that of dual slope Nyquist-rate converters, which will be discussed first.



(a)Architecture



(b)Output

Figure 2.3: Block diagram of dual-slope converters.

2.2.1 Dual-Slope Converters

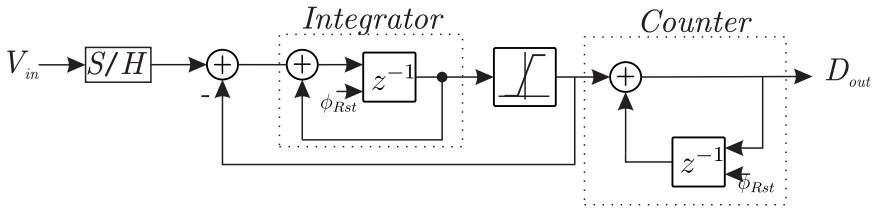
Dual-slope converters are useful for high-accuracy, high-linearity conversion with a low offset, and gain errors [29]. 2^{N+1} cycles are required for one conversion to achieve a N-bit resolution. When a high resolution is needed, the conversion time is long.

The operation of a dual-slope converter for a DC input is shown in Fig. 2.3a. First the input, v_{in}, is integrated for T, which equals to $N = 2^{n_{bits}}$ periods of the sampling clock. A negative reference voltage, $-V_{ref}$, is then integrated for another T, as shown in Fig. 2.3b. The number of clock cycles which it takes to reach zero is N_{out} and $T_0 = N_{out} * F_s$. For a constant input

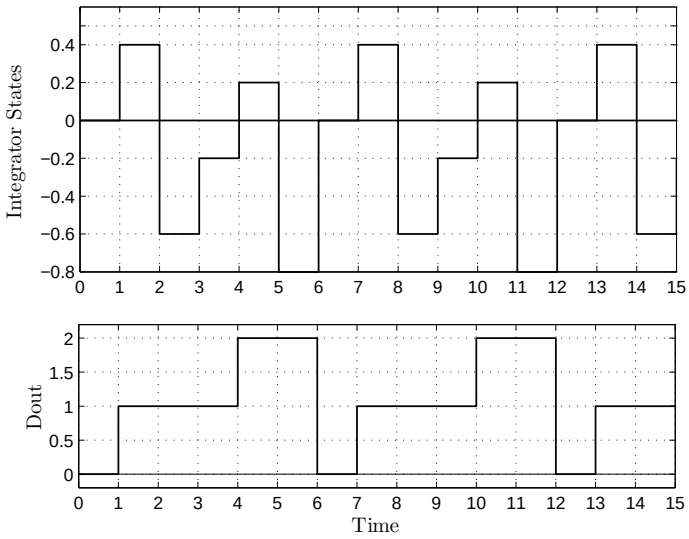
$$\frac{V_{in}}{V_{ref}} = \frac{T}{T_0} + \frac{\varepsilon}{N} = \frac{N_{out}}{N} + \frac{\varepsilon}{N}, \tag{2.6}$$

where the error, caused by the finite clock frequency, ε, satisfies $0 \leq \varepsilon < 1$. If the input varies with time then the RC circuit of the integrator filters out the input.

Other disadvantages of this type of system is the need for large capacitor and resistor values because



(a) Architecture



(b) Integrator states and digital output

Figure 2.4: First-order incremtntal ADC with OSR of 6.

the integrator must settle in a fraction of a clock cycle.

2.2.2 First-Order Incremental Converters

A first-order incremental ADC is a hybrid between a first-order ΣΔ modulator and a dual-slope ADC. The difference between a ΣΔ modulator and $I\Sigma\Delta$ modulator is that the integrator is reset after each conversion, and the input is sampled for each conversion. Also, the decimation filter can be a counter as in the dual-slope converters. Using this type of decimation filter will not suppress any signal that falls between $f_s/(2 \cdot OSR)$ and $f_s/2$ and will alias back into the signal band[9].

The delaying integrator is constructed using a delay cell in a feedback loop to achieve the transfer function in Eq.(2.1. The comparator is used as a the low-resolution quantizer. The comparator swing is from zero to V_{ref} because the input has a unipolar input. The comparator should have a full swing of $-V_{ref}$ to V_{ref} if negative inputs need to be converted. The counter is used to convert the output bit stream ($Y(z)$) to the digital representation (D_{out}). A representation of a counter is a non-delaying

integrator.

The operation of the first-order incremental modulator running at an OSR of 6 can be seen in Fig. 2.4. The constant positive input is integrated until it is larger than 0, the comparator goes high and a V_{ref}, in this case 1, is subtracted from the input. The counter is incremented each time the comparator goes high. To obtain a resolution of N bits, the integrator runs for $2^N - 1 = OSR$ number of clock cycles, half as many as dual-slope converter. At this point, the integrator and counter are reset for the next conversion.

After OSR clock cycles, the output of the integrator becomes

$$Y = OSR \cdot V_{in} - D_{out} \cdot V_{ref} \tag{2.7}$$

where D_{out} is the final counter sum. Since V must satisfy $-V_{ref} < V < V_{in}$, it follows that

$$D_{out} = n\left(\frac{V_{in}}{V_{ref}}\right) + \varepsilon \tag{2.8}$$

where $\varepsilon \in [-1, 1]$. The residual error at the output of the integrator is given by

$$V = -2\varepsilon_q V_{ref} \tag{2.9}$$

where $\varepsilon_q \in [-0.5, 0.5]$ is the quantization error of the conversion. Using ε_q, an extra bit can be obtained with one extra cycle and a zero input [30].

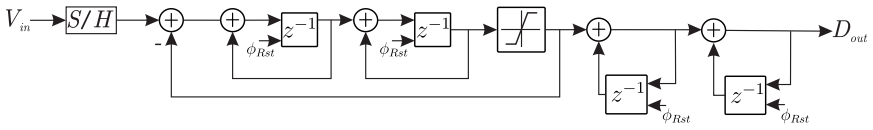
The distance between the pulses from the comparator is inversely proportional to the input voltage, and can be seen as a pulse width modulation (PWM) . The counter can be replaced by a more complicated post filter, which monitors the bit stream from the comparator.

2.2.3 Higher-Order Converter

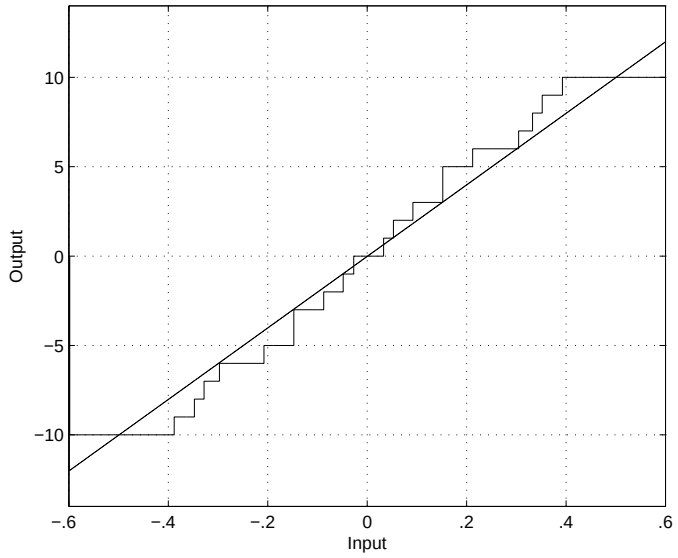
Incremental converters are a subset of oversampled converters and can utilize higher order design techniques in the same way that ΣΔ can. Higher order modulators can either be implemented in a single-stage structure or a cascade architecture. Each has their own advantages and disadvantages which will be discussed here.

Single-Stage Incremental ADC

The single-stage architecture is implemented with multiple integrators in series. Since integrators have a large gain, the stability of the system becomes an issue[30]. The negative feedback of the loop filter allows the system to remain stable for small inputs. The architecture of a second-order system is shown in Fig. 2.5a. The modulator is running at an OSR of 7 and uses a flash ADC with 3 output levels to improve performance. The integrators are reset after each conversion. The operation and output of the system are shown in Fig. 2.5b. The system also has an NTF of $(1 - z^{-1})^2$ and a bipolar input. The large integrator swing creates differential non-linearity (DNL) errors for large inputs, thereby limiting the modulator to only $\pm 0.6FS$, where the error is within $0.5LSB$.



(a) Architecture



(b) Input vs. Output for an OSR of 6 and a 3 level quantizer

Figure 2.5: Second-order single-stage incremtntal A/D conveter.

At high OSRs, the valid input range can be calculated the same way as ΣΔ stability for a given input amplitude, which is [31],

$$max \mid V_{in} \mid = \frac{N + 1 - \mid\mid h(n) \mid\mid_1}{N - 1} \tag{2.10}$$

for an N-level quantizer where $\mid\mid h(n) \mid\mid_1$ is the first norm of the NTF $H(z)$. For IΣΔ Eq. (2.10) is sufficient to find the input range, but depending on the OSR, the system may be stable at higher input ranges. Simulation can determine the largest input swing, such as the system shown in Fig. 2.5b.

Caldwell [9, Appendix A], in a detailed analysis, shows that the number of effective output levels is

$$N_{inc,ss} = \alpha(N-1)\frac{(M+L-1)!}{L!(M-1)!} + 1 \tag{2.11}$$

for a L^{th} order single-stage. Using N quantizer levels and an OSR of M, the resolution is $log_2(N_{inc,ss})$. The coefficient α is the maximum input signal that does not saturate the quantizer and, as mentioned above, is usually less than unity.

To improve the resolution, the order of the system can be increased, as in Eq. (2.11). However, increasing the order will reduce the stability of the system. For incremental converters, the input range is higher than that of ΣΔ because the integrators are reset after OSR clock cycles and do not have time to saturate. Input feed-forward architectures can also be used to improve the integrator swing [32].

Cascade Incremental ADC

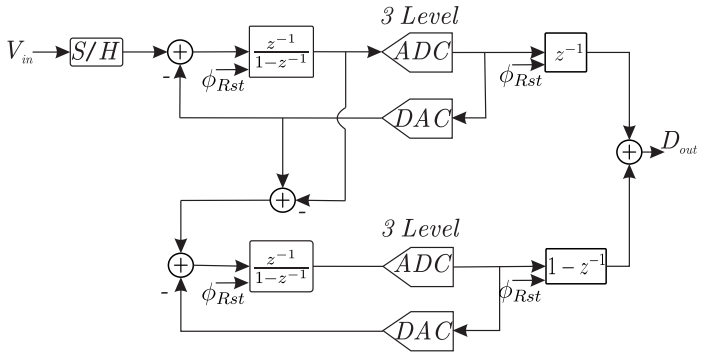
A second-order cascade modulator, first introduced in [30], has as its main advantage that the error from the first stage is fed to a second stage. Only the first integrator in a cascade architecture sees the input while the second only integrates error, which results in a small integrator swing. Fig.2.6a shows a cascade 1-1 with a 3 level quantizer and an OSR of 7. The cascade 1-1 modulator has a dynamic range higher than V_{ref}, as can be seen in Fig. 2.6b. The output has a perfect staircase structure, with error within ±0.5 LSB, as shown in Fig. 2.6c.

The order of the system can also be increased to improve resolution by further feeding the error from the second stage into the third, and so on. Since the error between each stage is small, the stability is not affected as it is in single-stage architecture. Also interstage gain and multi-bit quantizers can be used to increase the resolution [9].

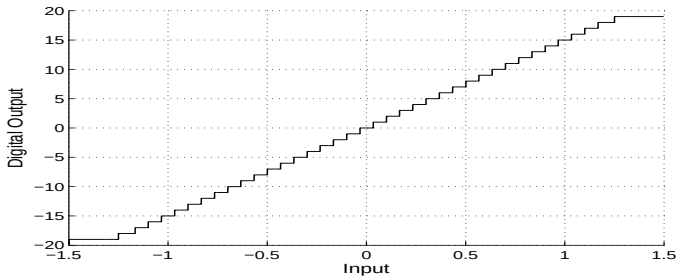
The quantizer is increased to have 3 quantization levels, which are $1, 0, -1$. These levels are chosen because the feedback DAC is able to convert the 3 levels with minimal gain error. This is important to note because the gain error is an added noise but since it is in the feedback loop it will not be noise shaped.

Caldwell [9, Appendix A], in a detailed analysis of a cascade architecture for an L^{th} order , showed that the number of effective output levels is given by

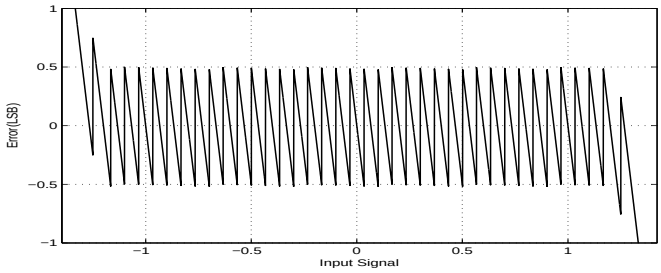
$$N_{inc,ss} = \alpha(N-1)^L\frac{(M+L-1)!}{L!(M-1)!} + 1. \tag{2.12}$$



(a) Architectur



(b) Output versus input for OSR of 7 using a 3 level quantizer



(c) Error of LSB

Figure 2.6: Cascade 1-1 IΣΔ with an resulting in 35 output levels.

Using N quantizer levels and an OSR of M, the resolution is $log_2(N_{inc,ss})$. The coefficient α is still the maximum input before the system saturates, but for a cascade architecture it is unity or larger. Eq.(2.12) assumes that the interstage gain for all stages is $N-1$, which means that the maximum number of output levels is larger for the same order system and α.

The ADC discussed in this thesis is a 4^{th}-order cascade of 1^{st}-order stages with an NTF of $(1-z^1)^4$. Cascade of higher order stages can be implemented, but is outside the scope of this thesis.

2.3 Decimation Filters for IΣΔ

Extensive research has been done in the area of decimation filters for IΣΔ, since a lot of information is available during the conversion process. There are many different approaches to decimation filters, a few of which will be presented here.

2.3.1 Cascade of integrators

As previously demonstrated, using accumulators (or non-delaying integrators) with the same order as the loop filter would be the simplest decimation filter. However, higher order can achieve better results. In the case of the first-order incremental, Fig.2.4 shows that at least 2^N clock cycles are required to achieve N-bit resolution.

The transfer function of the first order decimation filter is $\frac{1}{1-z^{-1}}$ when converted to the s domain is that of a first order sinc-filter which has zeros at multiples of $1/OSR \cdot T_{clk}$ [5]. Also there is attenuation at higher frequencies. The decimation process then folds all the frequencies down to DC which means that any signals between $f_s/2 * OSR$ and $f_s/2$ are aliased down to DC without attenuation.

Roberts, in [30], stated that using a second-order filter for a first-order converter increases resolution and the average accuracy, but the quantization error at DC remains the same. This is also proven by [5, Fig. 3.4]. Higher order will still have the same quantization error at DC which means that ENOB remains the same.

The dead zone at zero input can be explained by looking at the operation of first order incremental 2.4. If the input is small, the integrator does not trigger the comparator and no feedback is applied. To eliminate this problem, the comparator needs to be excited, using a dither before the comparator, as shown in Fig. 2.7. This technique is commonly used in ΣΔ design [5, 33].

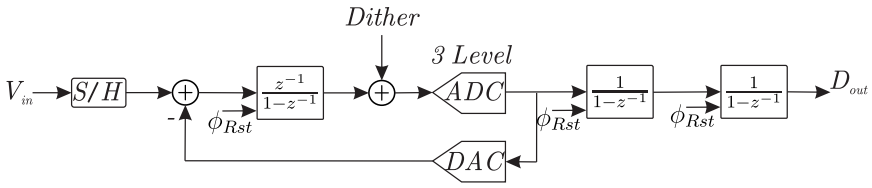


Figure 2.7: First-order incremental with dither and second order decimation filter.

2.3.2 CIC filters

Lth-order cascade-integrator-comb (CIC) filters have also been used in incremental decimation [32]. This type of filters are popular in ΣΔ design because the internal quantizer must have more levels to achieve stability. A detailed analysis can be found in [5].

2.3.3 Extended-Range

As mentioned before, the residual error on the last integrator can be used to further improve the resolution of IΣΔ ADCs. The error can be feed into a separate system which converts the quantization noise which then the error is subtracted from the main path. This requires that the two paths have no dc biasing which will be added error in the system.

In [7] the residual error is fed into a Nyquist-rate ADC, such as a successive approximation (SAR) ADC, then combined with the IΣΔ ADC output. The SAR ADC runs at a much lower speed so its power consumption is lower.

2.3.4 Optimal Filtering

In cascade architectures, the information is stored in each path, and the residual errors from each stage are used to improve resolution. An optimal filter is constructed using the data from each path separately. Since the $I\Sigma\Delta$ is reset after each conversion, the stream of bits is limited and an optimal filtering algorithm can be used to increase the resolution. By using this technique, an optimal filtering algorithm was developed by [34].

Chapter 3

Complex $\Sigma\Delta$

Complex $\Sigma\Delta$ modulators, which converts real IF signals, can be divided into two categories: complex BP $\Sigma\Delta$ modulators and complex LP $\Sigma\Delta$ modulators. The former use two paths which require careful matching. The latter, does not have any cross talk between the two paths and down-conversion is performed by a built-in mixer.

In this chapter both types of systems will be discussed in detail also the advantages and disadvantages of each will be discussed.

3.1 Complex Bandpass Approach

Bandpass $\Sigma\Delta$ modulators operate in a similar way as LP $\Sigma\Delta$ modulators do. In contrast to Nyquist-rate converters, BP $\Sigma\Delta$ modulators have improved linearity, reduced anti-alias filter complexity, and robust analog implementation [35]. The poles in BP modulators are achieved by having cross-coupling between two integrators. Usually the poles are located at $f_s/4$ to simplify the frequency shift after the conversion.

Complex signals and systems are represented by pairs of real signals, and can be filtered and manipulated as real signals. A complex BP $\Sigma\Delta$ modulator operates on the in-phase or quadrature phase simultaneously, and treats these two phases as a complex analog signal $I+jQ$. The input can be thought of as

$$x(n) = x_R(n) + jx_I(n) \tag{3.1}$$

where x_R is the real or in-phase (I) and x_I is the imaginary or quadrature (Q) phase signal. The imaginary symbol $j = \sqrt{-1}$. In an actual physical system, both signals are real.

Consider the quadrature mixer in Fig. 3.1, which has a real input. The input is $x(n) = x_R(t)$ where $x_I = 0$, and the output is

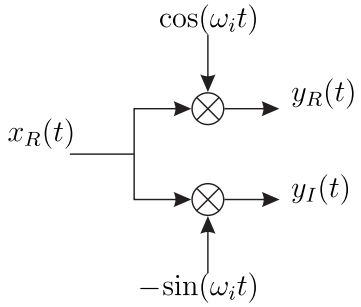


Figure 3.1: Quadrature mixer.

$$\begin{aligned} y(t) &= x_R(t)\cos(\omega_i t) - x_R(t)\sin(\omega_i t) \\ &= x_R(t)\left[\cos(\omega_i t) - \sin(\omega_i t)\right] \\ &= x_R(t)e^{-jw_i t}. \end{aligned} \tag{3.2}$$

Then, taking Fourier transform,

$$Y(\omega) = X_R(\omega + \omega_i), \tag{3.3}$$

shows that an ideal quadrature mixer results in a simple frequency shift of the input signal with no images occurring [36]. If the input was complex and centred around ω_i then the output of the quadrature mixer would be a DC signal. More details on complex signal processing can be found in [36].

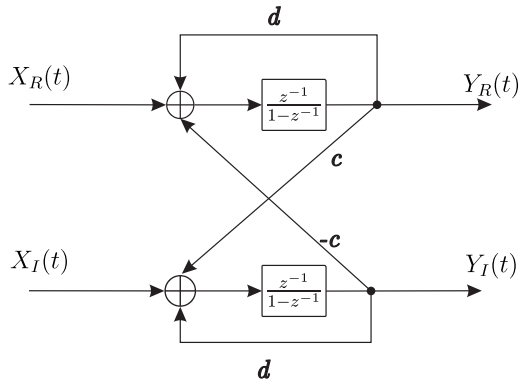
By using a complex filter in a ΣΔ loop, the effective signal bandwidth is cut in half, because only single side band is of interest. This doubles the overall OSR, improving the SQNR. It also allows the selection of NTF poles and zeros to minimize any error in the system [35].

3.1.1 Realizing Complex Poles

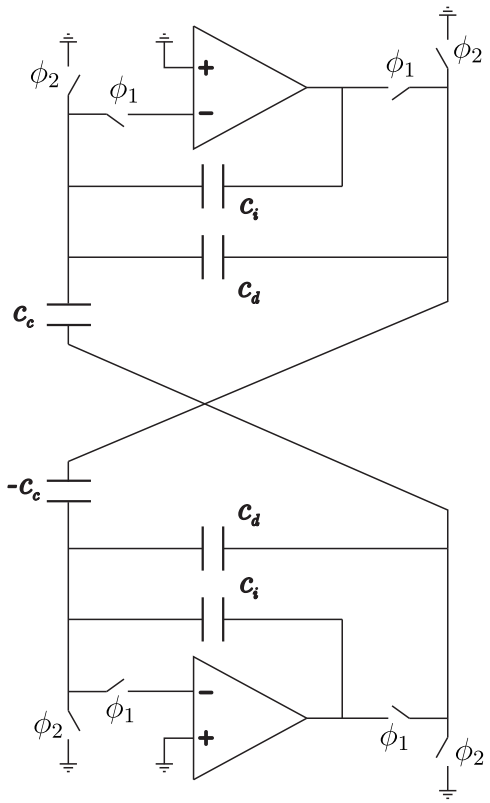
If in LP ΣΔ modulators, the loop filter is comprised of integrators, which shape noise away from DC, it follows that quadrature ΣΔ modulators will have a loop filter comprising of complex integrators to shape noise away from complex frequencies. The block diagram and schematic diagram of a complex resonator is shown in Fig. 3.2. This type of filter can be realized using a switched-capacitor (SC) filter, which was first proposed by [35].

A complex filter with a single pole at real-axis coordinate $(1 + d)$ and imaginary-axis coordinate c has the transfer function

$$\frac{Y(z)}{X(z)} = \frac{1}{z - 1 - d - jc}. \tag{3.4}$$



(a) Block level diagram.



(b) Signal-ended circuit realization.

Figure 3.2: Cross-coupling structure of complex integrators.

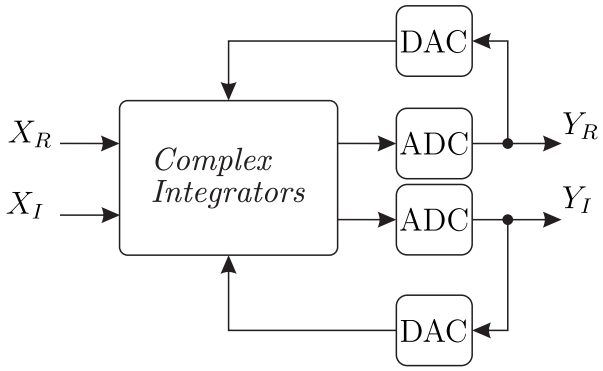


Figure 3.3: Architecure of complex ΣΔ ADC.

and in rectangular form is

$$\frac{Y(z)}{X(z)} = \frac{z - 1 - d + jc}{(z - 1 - d)^2 + c^2} \tag{3.5}$$

Realization of Eq.(3.4) can be done efficiently using a state space model, given in [37]. The network can be constructed using real blocks in the two-channel system shown in Fig. 3.2b. One of the cross-coupling coefficients, c , is negative since the imaginary term of the coefficient is being multiplied by the imaginary channel output ($j \cdot j = -1$). Negative capacitance can be achieved by using a differential SC architecture.

Constructing one complex pole requires two integrators, which means that second-order complex resonators require four integrators. Since there are twice the number of integrators, the power consumption is doubled.

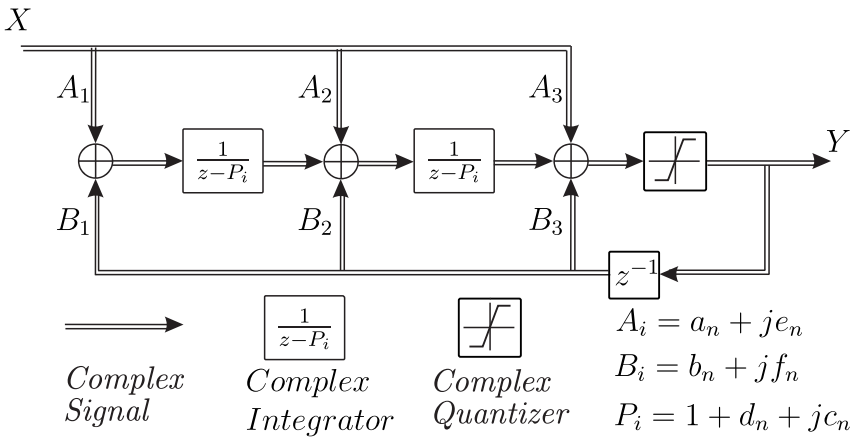
A major concern is capacitor matching between the two paths. Any mismatch will create gain errors in the real and imaginary paths which, in turn, will reduce SQNR and IRR.

3.1.2 Complex ΣΔ Structure

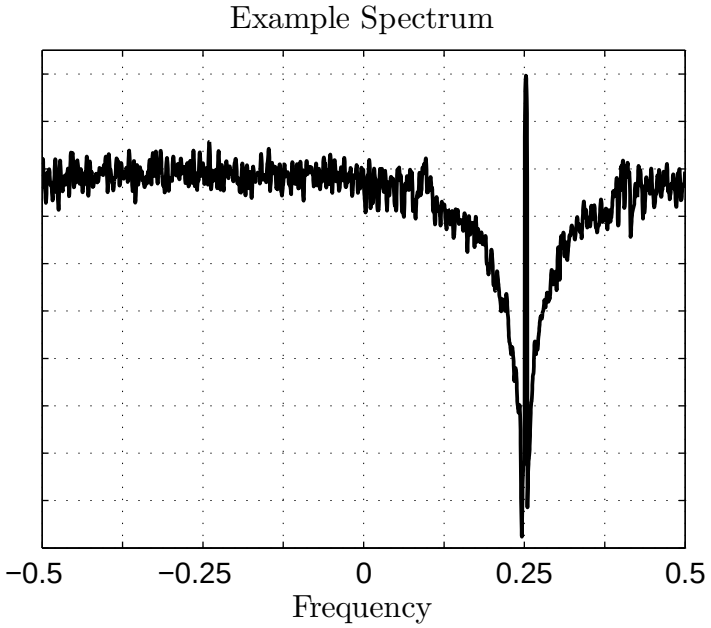
A general structure of a complex ΣΔ is shown in Fig. 3.3. The ADCs are low resolution quantizers to reduce the complexity and DC biasing of the feedback DAC. The general structure allows for the input and feedback to be cross-coupled internally between I and Q paths. The cross-coupling is a key feature of this design, which will be discussed here.

The structure of a second-order complex ΣΔ modulator is shown in Fig. 3.4. The double line represents a complex two-path signal. The system can be extended to any order but stability due to integrators saturation becomes an issue, as discussed in Sec. 2.1.

While a BP modulator must have poles and zeros centred around DC, complex BP modulators do not have this limitation. The distributed input and feedback allow designers the ability to place poles and zeros at both the positive and negative frequencies. The SNR and bandwidth can be maximized this way [35]. The notches in the NTF can be used to suppress image signals.



(a) System diagram.



(b) Frequency response for OSR of 24 and bipolar quantizer.

Figure 3.4: Second-order complex ΣΔ modulator.

The transfer function of the loop filter is important for stability analysis. The complex A coefficients set the zeros of the STF, which can be used to filter blockers and aliasing signals. The zeros of the complex NTF are set by the complex poles as mentioned in Sec. 3.1.1. The complex quantizer gives 1-bit outputs for each channel, which is cross coupled back to each stage using SC circuits just like the complex integrators. The complex B coefficients set the positions of the NTF and STF poles. The z-plane equations can be found in [35, Apendix A].

The general structure allows the placement of the NTF poles across the band of interest. Many BP ΣΔ modulators do not allow this freedom, because they are constrained to having poles at a fixed $f_s/4$. The drawback of spacing out poles is the increased number of different sized capacitors [36].

Finally, the complex modulator can convert a real signal (imaginary is equal to zero) requiring only half as many NTF zeros. The results and description can be found in [35, Sec. 3.3.3].

3.1.3 Complex Demodulation

The decimation filter for the BP and complex BP modulators, is implemented by a frequency shifter followed by a LP filter and decimation on each path. The LP filter is crucial because it removes the out of band quantization noise before the folding in the decimation process [33].

The frequency shift, which is simple to perform on a complex signal, can be seen in Fig. 3.5. The θ_0, which is the center frequency, is usually $\pi/2$ to allow implementation using simple hardware [38]. A frequency shift can be described mathematically as a multiplication of the signal with

$$\begin{aligned} e^{-j\theta_0 n} &= cos(\theta_0 n) - jsin(\theta_0 n), && \textbf{where } n = 0, 1, 2, \ldots \\ &= (1, \frac{1}{\sqrt{2}}, 0, -\frac{1}{\sqrt{2}}, -1, -\frac{1}{\sqrt{2}}, 0, \frac{1}{\sqrt{2}}, \ldots) \\ &+ j(0, \frac{1}{\sqrt{2}}, 1, \frac{1}{\sqrt{2}}, 0, -\frac{1}{\sqrt{2}}, -1, -\frac{1}{\sqrt{2}}, \ldots), \end{aligned} \tag{3.6}$$

where $n = 0, 1, 2, \ldots$. Since the output of the modulators is also complex, the shifting is multiplying two complex signals

$$[i(n) + jq(n)]e^{-j\theta_0 n} = [i(n) + jq(n)][cos(\theta_0 n) - jsin(\theta_0 n)]. \tag{3.7}$$

The baseband signals are

$$i_0(n) = i(n)\left[cos(\theta_0 n) + q(n)sin(\theta_0 n)\right] \tag{3.8}$$

and

$$q_0(n) = q(n)\left[cos(\theta_0 n) + i(n)sin(\theta_0 n)\right]. \tag{3.9}$$

The filtering is done in a multi-stage structure to reduce the overall complexity. Usually an FIR filter

is used for each decimation stage for stability and linear phase. The decimation filter is designed in a reconfigurable digital architecture, which allows it to have different specifications for different standards.

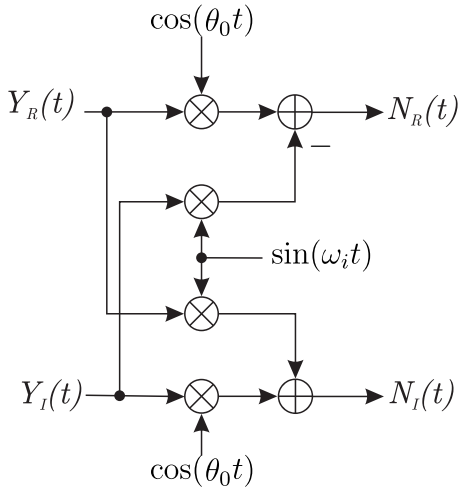


Figure 3.5: Complex frequency shifting for complex demodulation.

3.2 Complex Low-Pass Approach

As mentioned previously, the main drawback of the complex modulator is I/Q mismatch, which affects IRR and SQNR. Not only is self image a problem, images from adjacent radio channels are also problematic because the complex system is not centred around DC. Papers that have eliminated parts of I/Q mismatch, were published[36, 39, 40], but none present a complete solution to the problem. A partial solution was introduced by [3] using two LP ΣΔ modulators for each channel and frequency shifting, using the input sampler, also known as LP complex ΣΔ modulators, as seen in Fig. 3.6.

The LP complex modulator has shown the most promise because the input sampling capacitors are shared for both I and Q paths. This structure allows the mismatch to be zero for the first stage. Mismatch in all other stages is considered noise, and although it is shaped away from the band of interest, may still pose a problem.

Input is chosen to be at $\pi/2$, which is the same for a BP. As a result, the samples are $1, 0, -1, 0, \ldots$ and $0, 1, 0, -1, \ldots$ for I and Q respectively. The IF mixer shown in Fig. 3.6 has a simple sampling scheme, which is performed at the input. This scheme will be discussed later. The frequency of the two LP modulators can be reduced by half because the alternative samples are zeros, which are added in post processing.

Compared to complex BP modulators, LP modulators have the advantage of lower power consumption [3]. The two sub-modulators shown in Fig. 3.6 operate at half the sampling rate, and half as many integrators are needed for the same order. The need for two LP modulators doubles the power consumption and yet, the total power consumption is still halved.

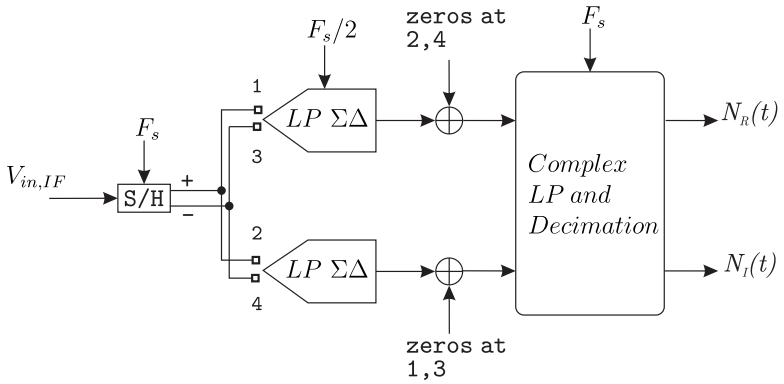


Figure 3.6: Low-pass complex ΣΔ architecture.

Fig. 3.7 shows the sampling scheme for complex LP modulators, in which the input sampling capacitors can be seen. Only the first stage is shown for simplicity. Also, the feedback DAC capacitors are combined with the input capacitors by using alternative phase clocks. This further reduces the mismatch.

The time sharing of capacitors C_1 and C_1' between channels I and Q as well as the feedback DAC is the underlining principle of the mismatch suppression. As pointed out in [40] only the input and feedback DAC elements will adversely affect the image rejection of the modulator. Any mismatch between C_{in} and C_{in}' will be suppressed by the common-mode rejection of the integrating Op-Amp.

One drawback of the system in Fig. 3.7 is the phase errors of the sampling clocks, which can reduce the image rejection of the modulator. This problem is minimized by allowing the falling edges of ϕ_{A1} and ϕ_{A2} to occur later than rising edge of ϕ_{B1} and ϕ_{B2} [41].

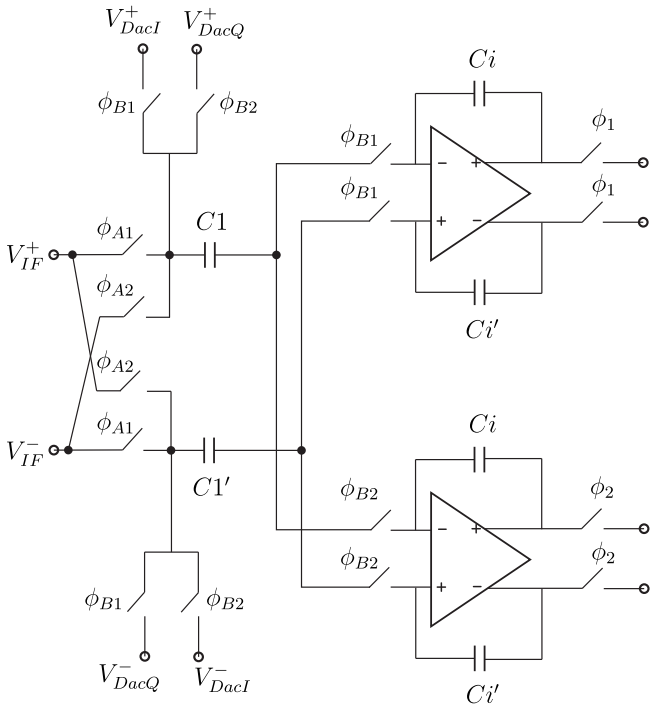
3.2.1 Complex Input

The sampling scheme for a real input has only $\pm IF$ which allows only one pair of sampling capacitors. For a complex input, two pairs of complex sampling capacitors must be used because the two channels see different inputs for the same clock cycle. In Fig. 3.8 the quadrature sampling scheme for an input at $\pi/2$ is presented. The complex input and local oscillator (LO) are

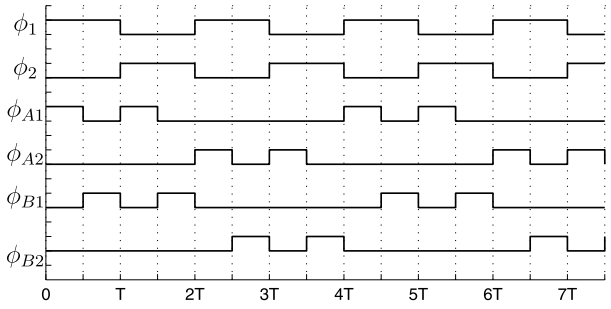
$$X(n) = x_I(n) + jx_Q(n) \tag{3.10}$$

$$LO = cos(n\pi/2) + jsin(n\pi/2) \tag{3.11}$$

respectively, where $n = 0, 1, 2, 3 \ldots$. The output is the multiplication of the two signals which is



(a) Schematic



(b) Timing diagram

Figure 3.7: Sampling scheme for a low-pass $I\Sigma\Delta$ ADC (only first stage shown).

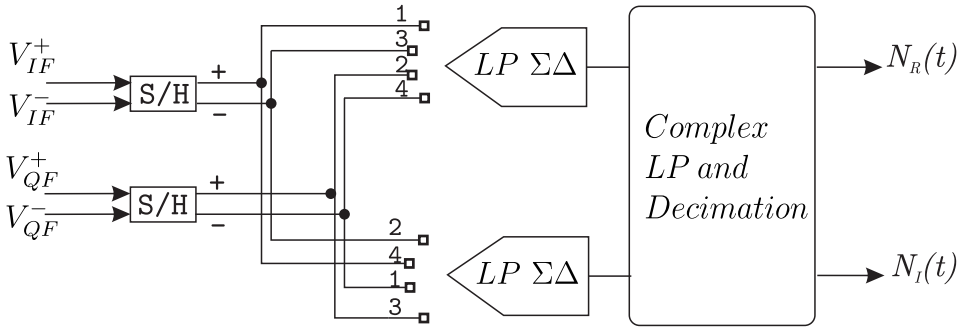


Figure 3.8: Quadrature sampling scheme of low-pass complex ΣΔ.

$$\begin{aligned} x_I(n) + jx_Q(n) &\left[cos(\frac{n\pi}{2}) + jsin(\frac{n\pi}{2})\right] \\ &= \left[x_I(n)cos(\frac{n\pi}{2}) - x_Q(n)sin(\frac{n\pi}{2})\right] \\ &+ j\left[x_Q(n)cos(\frac{n\pi}{2}) + x_I(n)sin(\frac{n\pi}{2})\right]. \end{aligned} \tag{3.12}$$

Since both paths are now baseband, a LP $I\Sigma\Delta$ ADC can be used for each channel.

The error in both paths still exists because the paths are independent of each other. No cross-coupling exists between the two channels, and the main errors occur due to self image [42]. This type of system achieved 70dB of image rejection with 0.1% capacitor mismatch.

Chapter 4

Complex Incremental Sigma Delta

This chapter is the new work on incremental ΣΔ ADCs which is the application of incremental typology in complex modulators. $I\Sigma\Delta$ ADCs have never been applied to complex ΣΔ which means that comparison will be done with the complex ΣΔ ADCs. A complex BP incremental modulator will be introduced and analysed. This will be followed by the presentation of complex LP incremental modulators, with a new multiplexing scheme. The advantages of each design will be discussed.

4.1 Bandpass Approach

The main difference between ΣΔ modulators and incremental modulators are the resetting resonators. Since continuous time resonators cannot be reset, this paper will only look at discreet time systems using switched capacitors (SC). The system in Fig. 3.4 is modified to operate in the incremental mode. This is achieved by resetting the integrators after each conversion, and reconstructing the output bits stream before it enters the decimation filter.

The new system can be seen in Fig. 4.1. The output of the modulators is shifted to baseband first, using a complex frequency shifter from Fig. 3.5, so that a simple decimation filter can be used. In this case the decimation filter is a counter with moving average decimation. The incremental modulators have reset spurs at multiplies of the reset frequency which is equal to

$$f_{RST} = \frac{f_s}{2 \cdot OSR}. \tag{4.1}$$

If f_{RST} falls in the band of interest, the input signal will be lost. Therefore, if f_{RST} is smaller than the bandwidth of the input, the reset spur will affect the final output. The output of the modulator before the frequency shift can be seen in Fig. 4.2.

The LP filter and the decimation operate at the same reset frequency as the modulators. As a result of this, the reset spurs are reduced during decimation. This is only true for $I\Sigma\Delta$ modulators. Since the output is digital, the delay in clock phases at the output will have little effect on the final SNR.

Since the discrete resonators have cross-coupling between the I/Q paths, a complex resetting scheme

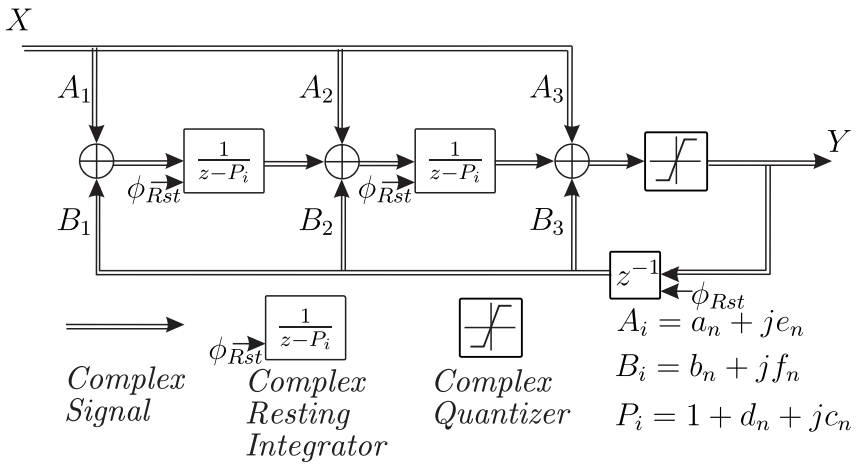


Figure 4.1: Complex LP IΣΔ architecture.

cannot be implemented. The reset spurs from each path will cross multiply with each other, creating unwanted noise.

4.2 Low-Pass Approach

The incremental ΣΔ has many more advantages when the signal is near DC because the reset spurs and decimation can be controlled. In this section, the considerations for both real and complex IF inputs are examined.

4.2.1 Low-Pass Incremental with Real IF

A real IF input is sub-sampled before the LP ΣΔ ADC at $f_s/4$. As discussed in Sec. 3.2, $\pi/2$ coefficients are $0, 1, -1$,and so the capacitors do not require scaling. ΣΔ modulators must have a continuous input signal to allow for noise shaping, which ensures that switching noise does not corrupt the input signal. This section will show that these restrictions do not apply to an incremental converter due to a one-to-one conversion.

Since an IΣΔ ADC converts the input sample in one sampling period, it is ready for the next conversion as soon as the next sample is held. This means that the converter does not have memory and so it can convert both I and Q channels without causing cross talk. This type of system can be seen in Fig. 4.3, where both I and Q channels use the same ADC and a simple multiplexer to split the channels after the ADC. There is no mismatch between the I and Q channels because the same ADC converts both, and amplitude scaling is performed in digital post filters, which does not suffer gain errors.

In the traditional sigma delta ADC, negative gain is achieved by using a differential SC, as described in Sec. 3.2. Incremental modulators do not need to preserve the input because they do not have memory. The negative scaling can be implemented in digital post filtering. This simplifies the analog portion of

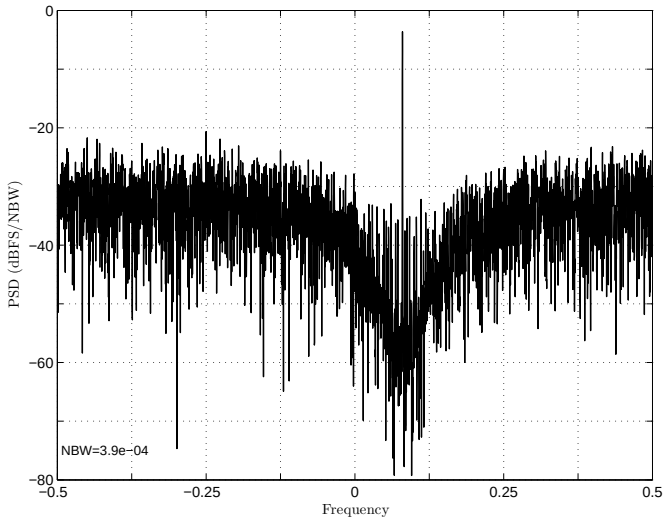


Figure 4.2: Output spectrum of the Complex LP IΣΔ having reset spurs.

the design as well as removing any mismatches which may occur due to scaling.

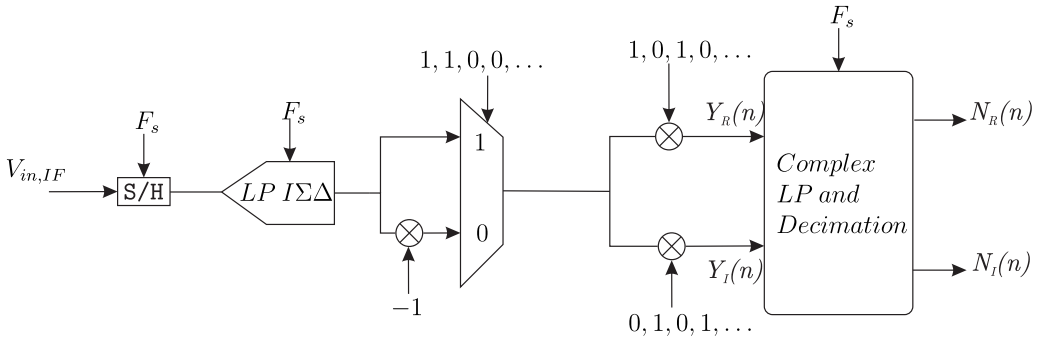


Figure 4.3: One path complex LP IΣΔ for center frequency $\pi/2$ with real IF input.

The new system can be seen in Fig. 4.4, which uses digital filters to perform the reconstruction of the I/Q channels. The assumption that the center frequency should be chosen to be $\pi/2$ no longer applies. If the center frequency becomes $\pi/3$ and the modulator is running at

$$F = \frac{F_C * F_S}{2\pi} F = 3/2F_S$$

The sequences for the signal reconstruction becomes $1, \frac{1}{2}, -\frac{1}{2}, -1, -\frac{1}{2}, \frac{1}{2}$ and $0, \frac{1}{2}, \frac{1}{2}, 0, -\frac{1}{2}, -\frac{1}{2}$, for I and Q respectively. These sequences can be implemented with a shifter inside the multiplexing scheme. Only one ADC performs the conversion for I/Q channels, and so no mismatch exists. This system can be extended to any input center frequency and still has perfect matching.

Since only frequency shifting is performed, the self-image signal (SIS) is still present in the final

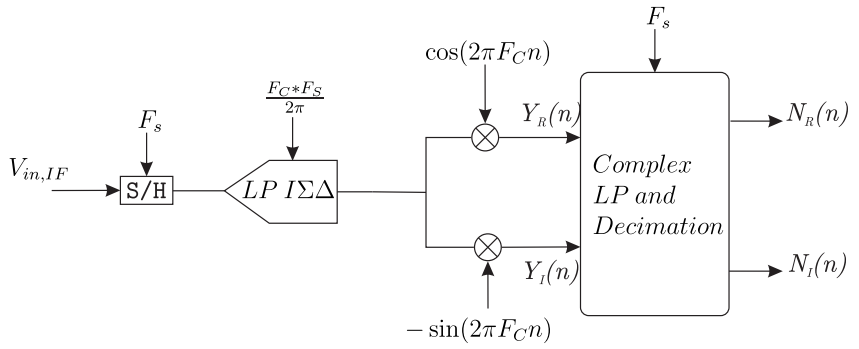


Figure 4.4: One path complex LP IΣΔ for any center frequency with real IF input.

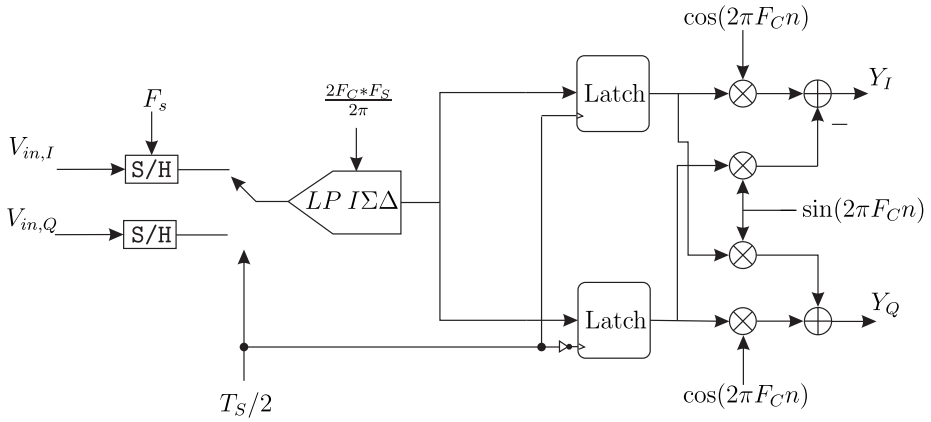


Figure 4.5: One path complex LP IΣΔ for any center frequency with complex IF input.

output but is shifted to higher frequencies. Frequency wrapping of the SIS does occur and a LP filter can be used followed by a decimation by 2. The final BW is halved because of this effect and these signals are not counted in the SQNR calculations.

4.2.2 Low-Pass Incremental with Complex IF

In a complex IF input, the quadrature input is no longer zero complicating the overall system, explained in Sec. 3.2.1. As explained in the previous section, the negative gain can be applied in post filtering. Also, the conversion of the I/Q channels can be time-interleaved so that all the components are shared and the two output signals are ready at the same time. The modulator must run at twice the frequency to convert both I/Q inputs.

The proposed system can be seen in Fig. 4.5. Both I/Q input channels are sampled using the same clock to remove phase errors during the conversion. This system can also be extended to any center frequency by adjusting the sampling rate of the modulator and the digital re-constructor.

The system in Fig. 4.5 also has a tunable center frequency of the modulator. This is possible

because the frequency shifting is done in digital domain where there are no gain errors. The LP $I\Sigma\Delta$ can dynamically change its sampling frequency to match the new center frequency, then the digital reconstruction does the same.

The proposed system has the drawback of increased frequency of the ADC, which must be able to handle two conversions in one sampling period, a small price to pay for having a tunable center frequency. The the complexity of the digital post filter is also increased. Another drawback of is that the sample and hold (S/H)will increases the complexity of the anti-aliasing pre-filter.

Chapter 5

Design Example

The previous chapter discussed the theory of complex IΣΔ modulators and two different types of implementations. In this chapter, a graphical user interface (GUI) for designing and optimizing incremental and ΣΔ modulators is introduced. Circuit level design is discussed in order to illustrate implementation.

5.1 Design Toolbox

A graphical user interface (GUI) was built for three main reasons: to optimize the poles and zeros of a higher order ΣΔ modulator, to simulate the ideal performance of the incremental versus the traditional ΣΔ modulator, and to compare the performance of the ideal model with that of the transistor level circuit. The GUI was constructed using MATLAB [43]. The optimization of the system was performed using the Sigma-Delta Toolbox [44]. All ideal systems were simulated using SimuLink [45].

The NTF and STF were generated using the order of the system, the OSR, and the type of modulator (low-pass, complex, or bandpass). The z-domain equations were converted to state space (SS) model using MATLAB. The SS model was directly used for variables in SimuLink to compare results of the mathematical model to that of an ideal system.

The GUI can run pre-set SimuLink models or user-defined designs so that comparison between single-stage and cascade architectures can be tested. The ΣΔ mode can be compared to the incremental mode for both types of architectures. Also, feed-forward could be added to any type of system.

The GUI allows the user to set the input voltage, run time and other important parameters. Since performance and stability are critical issues, the GUI allows the user to sweep OSR and gain.

The GUI was used to import Cadence [46] simulation results during the design of the test chip. The Cadence results were verified using the ideal system model in SimuLink. The comparison was done during the three stages of the design process: the ideal block level, the transistor level and the extracted layout before production. This allows the user to verify that the functionality of ADCs.

More details of GUI can be found in Appendix A.

5.2 Design of Complex BP IΣΔ Modulators

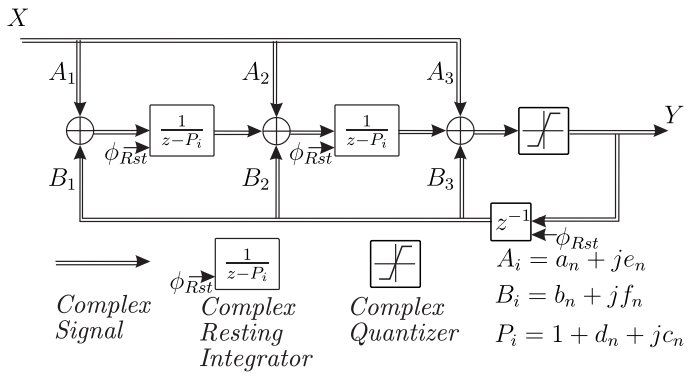


Figure 5.1: Architecture of second-order complex BP IΣΔ.

Incremental ADC is primarily used for the conversion of a sample and hold signal. If the signal is periodic, it requires that the sample and hold be removed, which alters the STF. The STF of the system will be convoluted with a sync function because of the resets, details can be found in [9]. In a complex BP IΣΔ, the signal is periodic and therefore the S/H is removed from the input.

A second-order system, Fig. 5.1, is designed in this section. The complex integrators are constructed using cross coupled switched capacitor (SC) circuits with a differential architecture to allow negative capacitance, discussed in Sec. 3.1.1. The feedback from the both I and Q quantizers are also cross-coupled to the allow precise positioning of NTF poles and zeros.

The parameters of the modulator are obtained using the GUI. There are three complex coefficients, which determine the complex NTF and STF. They are the complex feed in coefficients, $A = a + je$, the feed-back coefficients, $B = b + jf$, and the poles of the NTF, $P = 1 + d + jc$.

The SS model is extracted from the NTF, using the GUI. The NTF is

$$NTF = \frac{(z - (0.8678 + 0.4968i))(z - (0.8642 + 0.5031i))}{(z - (0.2953 - 0.1323i))(z - (0.03306 + 0.3219i))} \tag{5.1}$$

The SS model is

$$ABCD = \begin{bmatrix} 0.8642 + 0.5031i & 0 & 1 & -0.4937 - 0.8696i \\ 1 & 0.8678 + 0.4968i & 0 & -1.7321 - 1i \\ 0 & 1 & 0 & 0 \end{bmatrix}. \tag{5.2}$$

The coefficients derived from the SS model are $A_1 = 1$, $A_2 = 0$, $B_1 = 0.4937 + 0.8696j$, and $B_2 = 1.17321 + 1j$. Coefficient P is derived using the zeros of the NTF, in this case one. Simulation results of the second-order system can be seen in Figure 5.2. This system is tested using the SimuLink block and an OSR of 24.

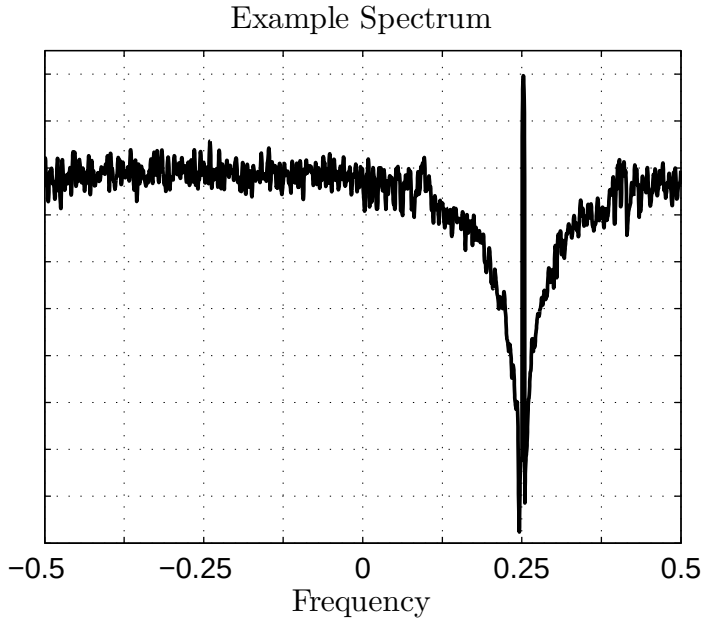


Figure 5.2: Simulation results of second-order complex BP IΣΔ.

5.2.1 Circuit Design

The circuit was designed for a 0.13μm IBM process. The system was first simulated in Cadence and then imported into MATLAB to compare with SimuLink simulation results using the NTF in Eq.(5.2). To ensure that the amplifier outputs will not exceed the reference levels, the capacitors were scaled down.

A 1.2V power supply, centred around a common-mode (CM) of 0.6V. The reference voltages for the feedback of the DAC were set to 0V and 1.2V. The amplifier swing was set to $1.2V_{p-p}$, which gives $\pm 0.6V$ around the $0.6V_{CM}$ for positive and negative output of the amplifier.

Capacitor sizes were set using kT/C as the minimum to satisfy noise requirements and minimize the capacitor area. The NTF derived in the last section is used to calculate the capacitor values, [35, Appendix A]. The table 5.1 summarizes the design parameters. All circuit simulations were performed in Cadence.

The clocking scheme is presented in Fig. 5.3. The non-overlapping clock generator provides six phases and a latch signal. These six phases include four versions of phase 1 (ϕ_1, $\bar{\phi}_1$ and the delayed version ϕ_{1d} and $\bar{\phi}_{1d}$) and two versions of phase 2 (ϕ_2 and $\bar{\phi}_2$). The clock generator also produces a latch signal for the SR latched comparator.

Comparator

The comparator for the modulator requires that the output is held using an SR latch. The comparator offset is not crucial since the loop filters will eliminate any DC component. The artefacts will be out of

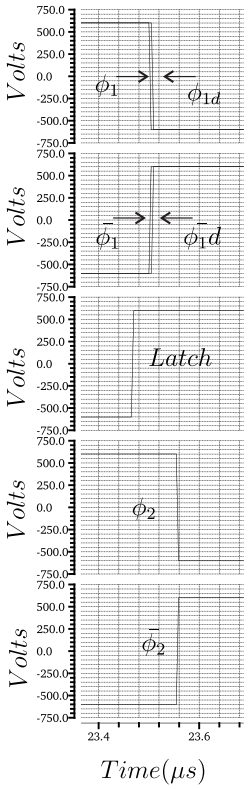


Figure 5.3: Clocking scheme for the complex ΣΔ.

band noise, which will be filtered out in post filtering.

The schematic is shown in Fig. 5.4. When ϕ_2 is high, the comparator is reset, and is ready for the next comparison. N3 ties N4 and N5 latches together and P1 and P2 drains are pulled to VDD through N3 and N4. The rising edge ϕ_1 releases the PMOS and NMOS latches and allows the output to latch onto the input of N1-N2. The output is inverted (buffered) before the SR latch. The sizes of the transistors is given in Table 5.2

The SR latch can be seen in Fig. 5.5. The signal is held at the output when the latch signal is low. The output directly controls the DAC in the feedback path. When the latch signal is high, the output latches onto the input (Table 5.3.)

Clock Generator

A standard non-overlapping clock generator is used to create the six required phases of the clock and the latch signal. It consists of two cross-coupled NOR gates and four delay cells, as shown in Fig. 5.6. The delay cells determine the non-overlapping period and the cross-coupling ensures that both phases are in synchronized. The latch signal is also generated by this system. The latch signal must be high before ϕ_2 to allow the SR latch to settle before the comparator is reset. The delayed version of ϕ_1 is needed to

Vin Real	$83kHz$	$1.2V_{peak}$
Vin Img	$83kHz$ 90°Phase shift	$1.2V_{peak}$
Sampling rate	$1M$	2 Phase
VDC	$0.7V_{FS}$	
Vref+/-		1.2V/0V
Delay	$5ns$	
Integrating Cap	$1pF$	Used to set the rest of the capacitor sizes
Cap a1	$1pF$	real signal input stage 1
Cap a1	Unused	real input input stage 2
Cap b1	$219.5fF$	real feedback stage 1
Cap b2	$1.732pF$	real feedback stage2
Cap c1	$624.7fF$	Imaginary of Complex integrator stage 1
Cap c2	$363.9fF$	Imaginary of Complex integrator stage 2
Cap d1	$219.1fF$	Real of Complex integrator stage1
Cap d1	$68.6fF$	Real of Complex integrator stage2
Cap e1/2	Unused	image signal input
Cap f1	$975.6fF$	complex feedback stage 1
Cap f2	$988.6fF$	complex feedback stage 2
Cap x	$1pF$	Inter-stage gain

Table 5.1: Second-order complex ΣΔ design parameters

Component	Size	Component	Size
N1	3/1	P1	48/1
N2	3/1	P2	48/1
N3	4/1	P3	2/1
N4	2/1	P4	2/1
N5	2/1	P5	8/1
N6	4/1	P6	8/1
N7	4/1		

Table 5.2: Transister sizes for the comparator using scaling factor $4\mu/120n$.

Latch	S	R	Q	$\bar{Q}$
0	x	x	Q	$\bar{Q}$
1	1	0	1	0
1	0	1	0	1

Table 5.3: Truth table for SR latch.

reduce charge injection at the input of the integrator. The signals are then buffered to be strong enough to drive the transmission gates. The simulation results for the clocks is shown in Fig. 5.3 with a $5pF$ load.

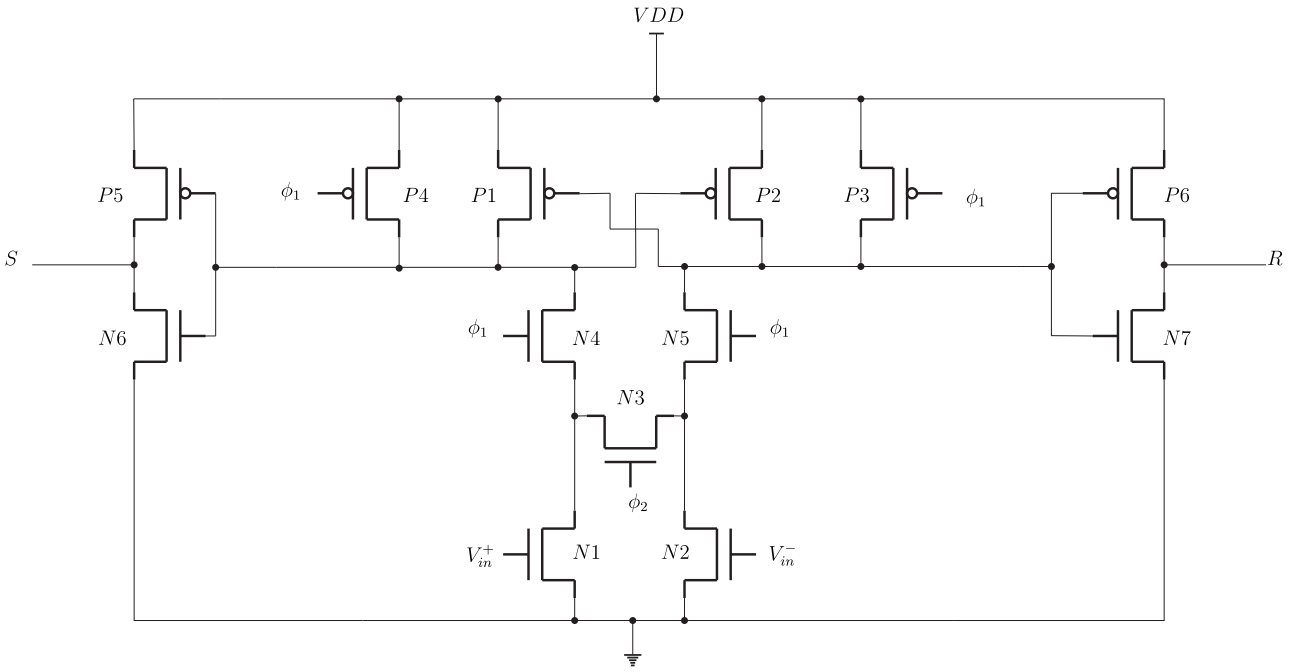


Figure 5.4: Schematic of the comparator.

Input Switching Structure and Transmission Gate

The input is sampled and held using a sampler (Fig. 5.7). It is important to ensure that the transmission gates do not have leakage, and that associated waveforms are correct. The input transmission gates use delayed clock signals to reduce the charge injection [30]. The input is sampled onto the capacitor during ϕ_{1d} and is then pulled to V_{CM} to allow the DAC charge to be subtracted from the integrating capacitor during ϕ_2.

The integrator is shown in Fig. 5.8. Resetting the integrator for the $I\Sigma\Delta$ mode is possible by pulling both terminals of the integrating capacitor to V_{CM}. The output of the integrator has a sample and hold structure so that the signal is available to the next stage during both clock phases. The two systems

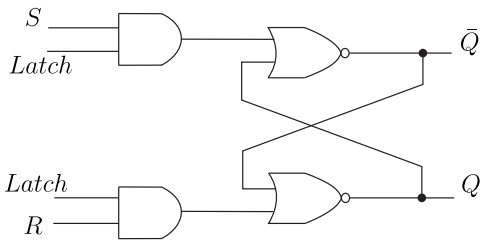


Figure 5.5: Schematic of the SR latch.

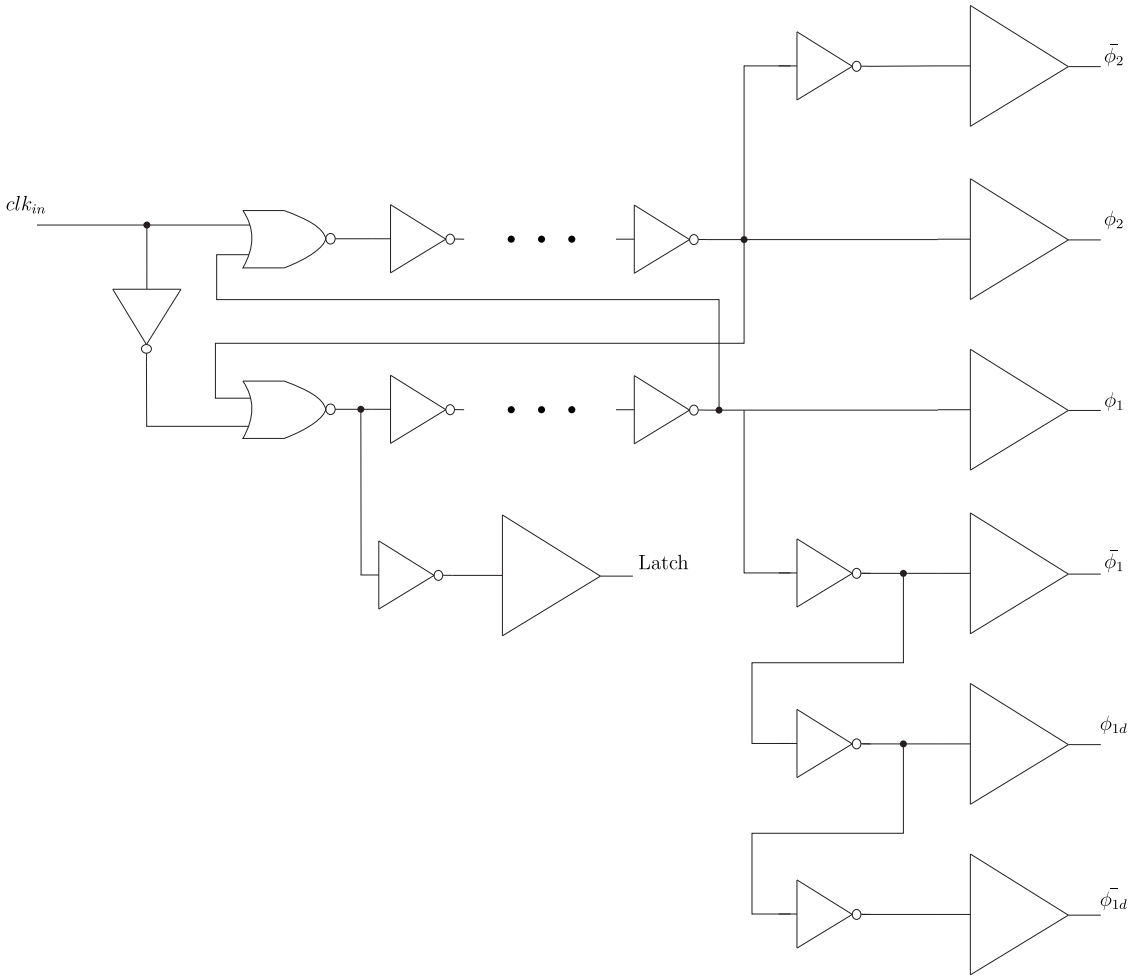


Figure 5.6: Schematic of the Clock generator.

were tested by sampling a sinusoidal and observing the settling time of the integrator output (Fig. 5.9).

1-Bit DAC

The comparator drives a 1 bit DAC in both the real and imaginary channels. The DAC feeds either a positive or negative differential reference voltage to be subtracted from the integrators. The switching circuit is the same structure as the input sampler but uses the second phase to subtract rather than added, shown in Fig. 5.10. The NAND and NOT gates are used to clock the latched comparator output using ϕ_2.

Operational Transconductance Amplifier (OTA)

The biasing circuit was designed off-chip as a result of the limited time available for the layout.

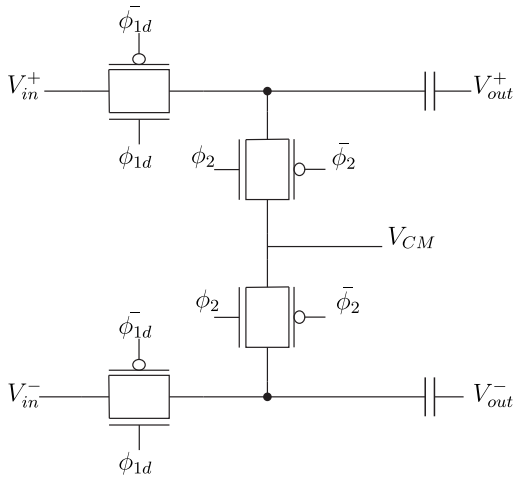


Figure 5.7: Schematic of the input sampling gates and capacitors of the complex ΣΔ.

The OTA for the modulator is fully differential, with built in common mode feedback (CMFB). The OTA is a two stage amplifier for the maximum gain. The schematic is shown in Fig. 5.11 The first stage of the amplifier is a cascode load differential amplifier which gives a large gain and a low output swing.

The second stage is a class AB amplifier. A pair of 50fF capacitors were used for compensation in this Op-Amp because the bias for the AB amplifier comes from the differential stage. The estimated slew-rate caused by the compensation capacitor is 400mV/ns, which is within the speed requirements. The AB type amplifier is used to allow for a full swing of the amplifier from ground to VDD.

The CMFB circuit is also presented in Fig. 5.11. The design has a gain of approximately 8, which is large enough to balance the output. Since the loop gain is large, a capacitor is needed to stabilize the CMFB loop. The CMFB is important to keep the differential voltage of the OTA at a constant value. If the common mode voltage wanders too high or too low, the amplifier may shut off.

The stability of the OTA must be ensured because there is feedback from the AB stage through the CMFB. The stability were ensured by testing the OTA with a step response while the OTA drives a 250fF load. The capacitor sizes are adjusted to meet 1MHz sampling clock.

Mode Selection and Clock Divider

Finally, the mode selection and clock divider were designed in a custom digital style. The mode selection is a signal from outside the chip which turns on the clock divider. The clock divider was used to create the reset signal for the incremental mode. When the signal is high, the system is in the incremental mode, which resets the OTA every 24 clock cycles. When the signal is low, the modulator is in the ΣΔ mode. The ΣΔ mode means the system is free-running and so there is no reset of the integrators. The clock divider circuit is shown in Fig. 5.12. The clock divider uses D flip-flops, NAND and NOT gates to create the *Rst* signal.

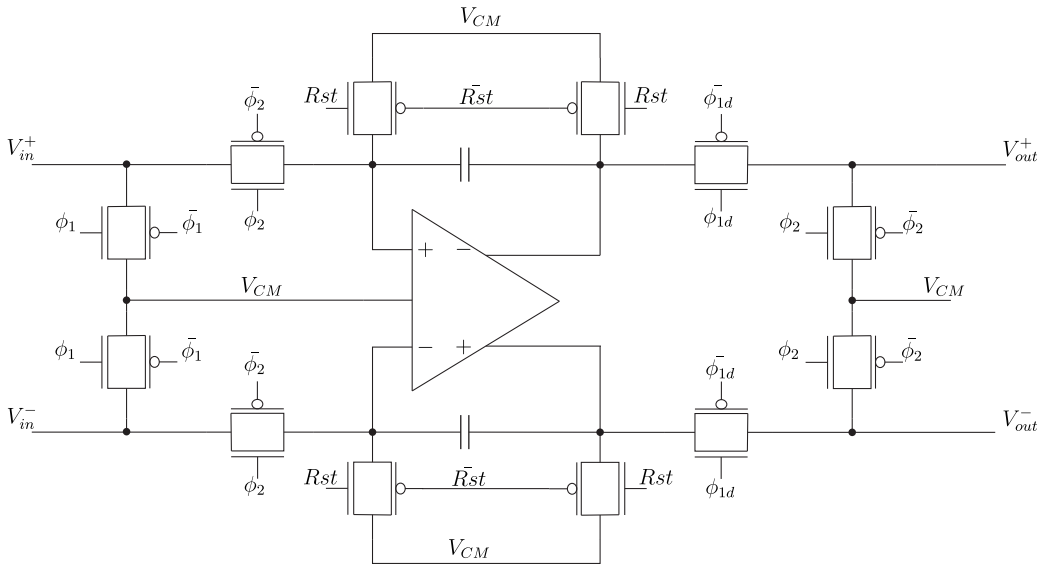


Figure 5.8: Schematic of the amplifier sampling gates and capacitors of the complex ΣΔ.

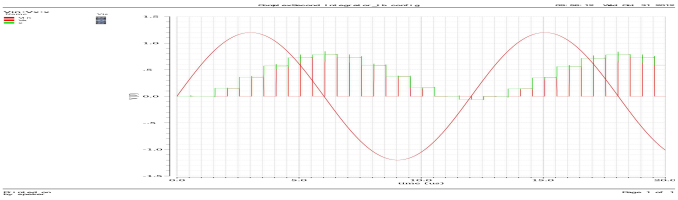


Figure 5.9: Simulation results of the integrator and input sampler for a sinusoidal input.

5.2.2 Layout Techniques

A special care was taken when floor-planning the modulator since the matching between the real and imaginary paths is important. The differential signals in each signal path were carefully matched. All devices such as OTA, input sampler and capacitors have mirror symmetry. Also, the I/Q paths have mirror symmetry for matching the two paths.

When designing the capacitors a special care was taken to ensure the exact ratio between the capacitors is minimized, as specified in Tab. 5.1. Any mismatch in the capacitors will shift the poles and zeros of the NTF, reducing the noise shaping of the modulator which, in turn, reduces SNR.

The clock generator was positioned at the center of the two paths to allow all clock signals to be equidistant from each path. The clock as well as the DAC signals run down the center of the chip so that the delays are equal for both I/Q channels.

The delay to stage two is shorter than the delay to stage one. The reason for this is that stage two needs to finish sampling the output of stage one before stage one changes its state. The input sampler has a longer delay than that of stage one for the same reason.

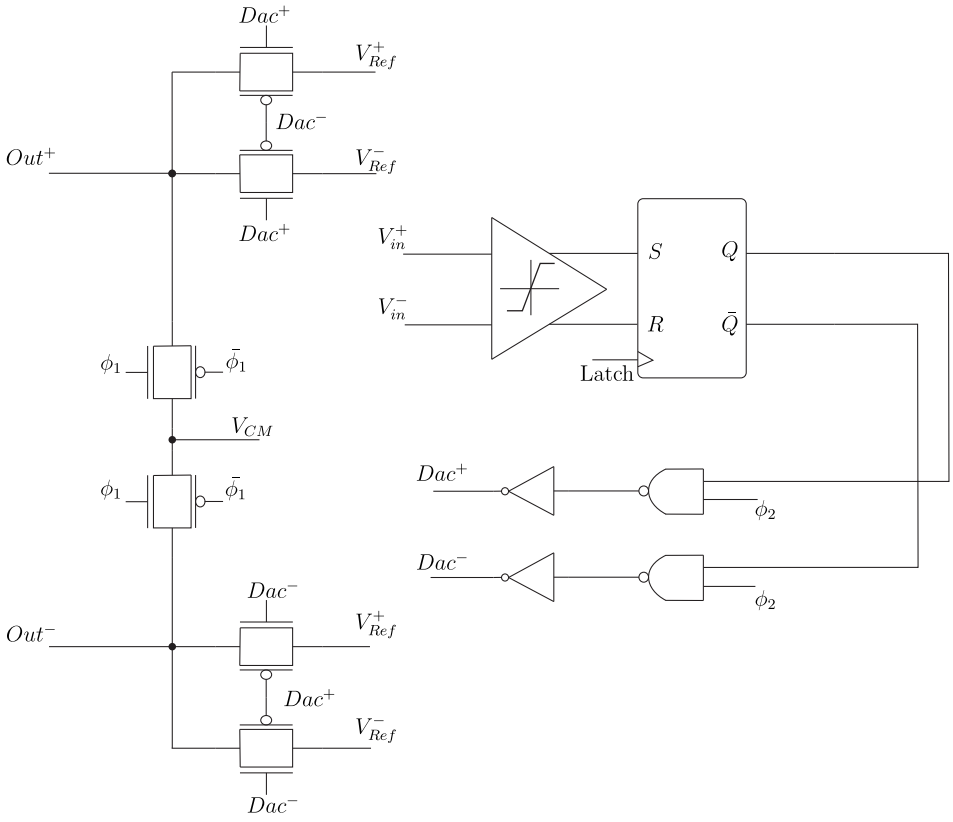


Figure 5.10: Schematic of the feedback DAC.

All analog signals run perpendicular to the digital signals to reduce any cross talk from the digital signals. Finally, the pads are positioned equidistant to the I/Q channels to ensure that the signal path for the I channel has the same parasitics as the Q channel before the input sampler.

An output buffer was added after the comparator so that the output pins can drive the 50Ω load of the oscilloscope. Since the output is a one bit digital signal, simple inverters are used. The final layout can be seen in Fig. 5.13.

5.3 Design of Low-Pass Incremental

The complex incremental ΣΔ modulator uses a 4th order cascade of first-order integrators for each ADC. The ADC is running at an OSR of 7 and implements 3-level quantizers. The final NTF of the ADC is $(1 - z^{-1})^4$. The ADC can be seen in Fig. 5.14, and the decimation filter which matches the order of the system is shown in Fig. 5.15. The four paths are combined before the decimation filter to allow complicated filters to be used.

The reconstruction of the signal and noise before the decimation filter allows the system performance to be dynamically changed depending on constraints, such as speed, power and performance. The

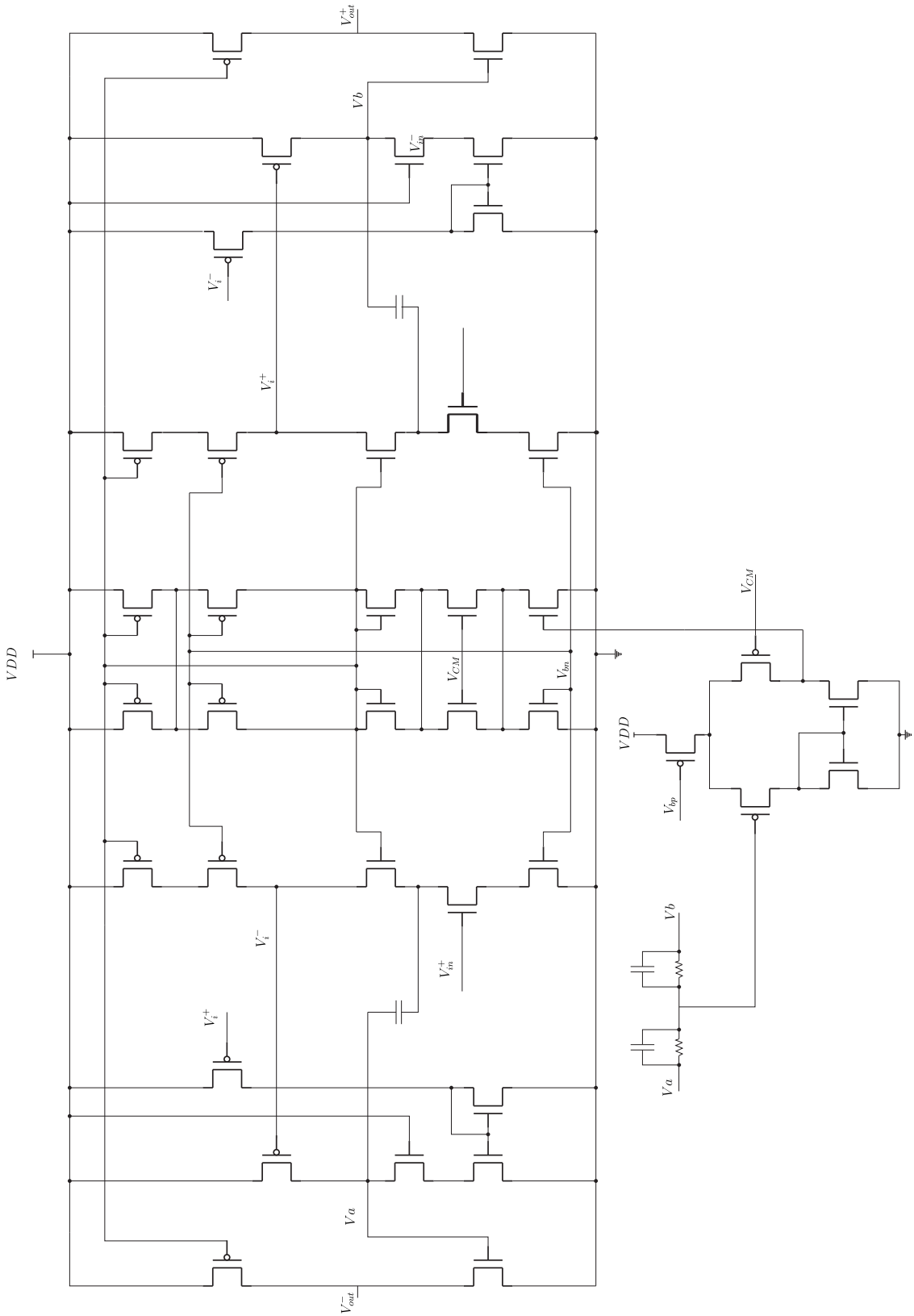


Figure 5.11: Schematic of a two stage OTA with decoupling capacitors and CMFB.

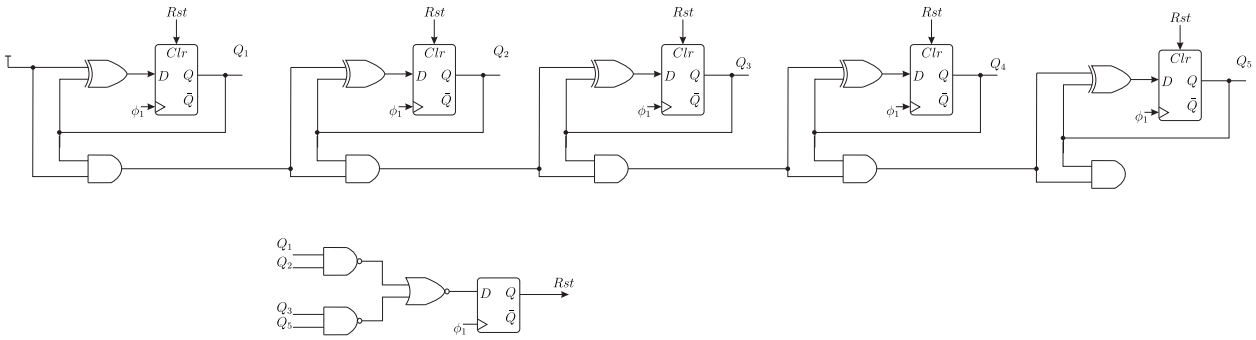


Figure 5.12: Schematic of the clock divider used for the resetting clock.

constraints can be adjusted by changing the decimation filter for a better accuracy or a higher precision, as discussed in Sec. 2.3.

To calculate the SNR of the ADC Eq.(2.12) is used. The ADC has an interstage gain of one, which reduces the $(N-1)^L$ term to $(N-1)$. The final SNR is $48.24dB$ when $\alpha = 1$.

The 4th order cascade ADC can convert inputs of up to $1.4V_{ref}$ while maintaining a perfect staircase shape, as seen in Fig. 5.16a. It follows from Sec. 2.3 that the system can achieve a higher SNR, as seen in Fig. 5.16b.

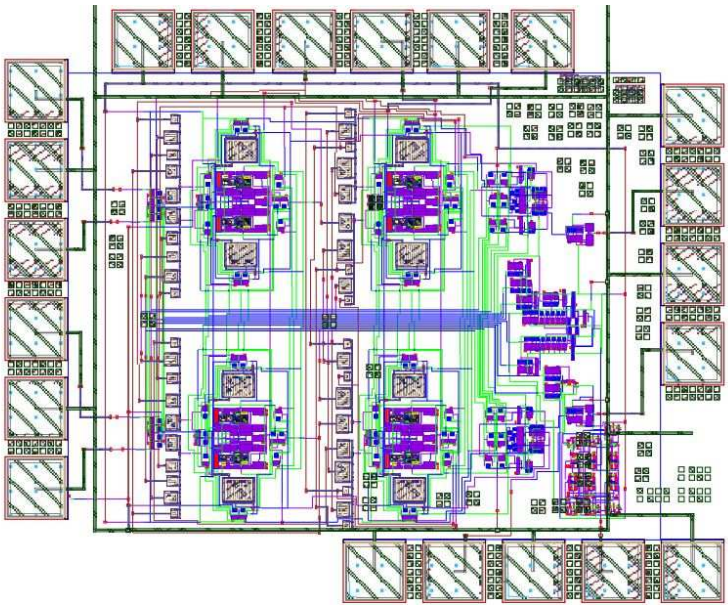


Figure 5.13: Final layout before fabrication.

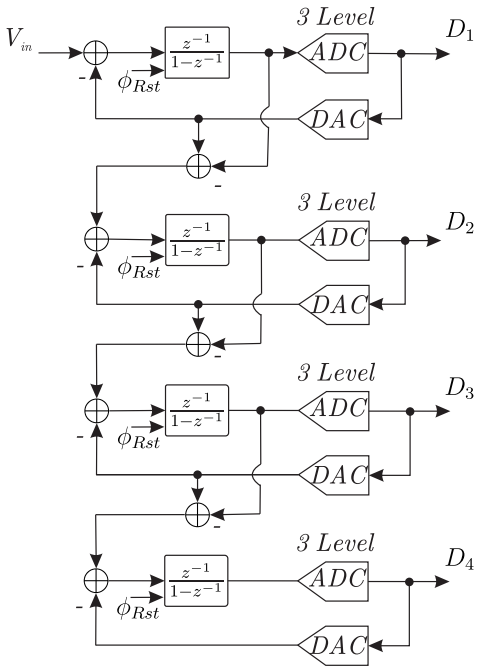


Figure 5.14: cascade 1-1-1-1 IΣΔ using a 3 level quantizer.

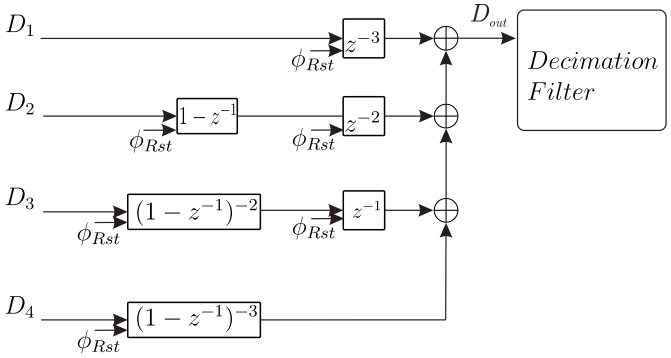
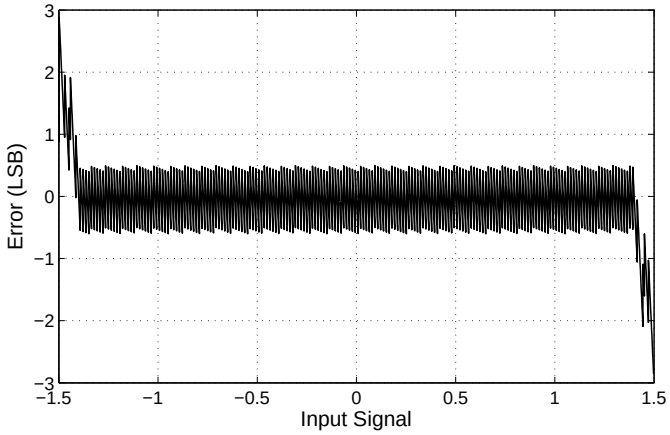
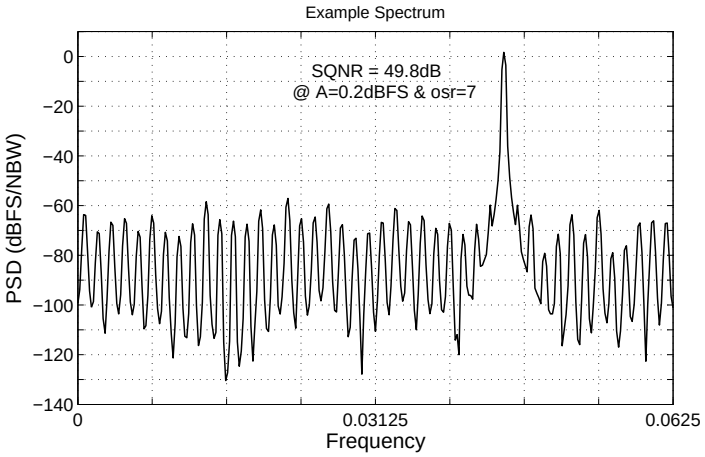


Figure 5.15: Decimation filter for cascade 1-1-1-1 implementing a fourth order cascade of accumulators.



(a) Error of LSB for DC input with OSR of 7.



(b) Output spectrum for sinusoidal input.

Figure 5.16: cascade 1-1-1-1 simulation results.

Chapter 6

Results

The BP $I\Sigma\Delta$ approach discussed in Sec. 5.2 was fabricated in an IBM $130nm$ CMOS process. The system is set up to test both $\Sigma\Delta$ and incremental modes in order to compare the two results. The test set-up will be described in Sec. 6.1, followed by a discussion of the results of each mode, in Sec. 6.2. The LP approach, Sec. 5.3, is not fabricated due to funding cuts. Only simulation results will be discussed in this chapter.

6.1 Test Setup

6.1.1 Chip

The chip was fabricated in an IBM $130nm$ CMOS process. The Cadence tools were provided by CMC and layout support is provided by Kaben Wireless Silicon.

The final chip size is $1.3mm$ by $1.4mm$ and no packaging is used. Table 5.1 summarises the operation of the test chip.

6.1.2 Equipment

The free die was tested using a Cascade Microtech RF-1 Probe Station with two 6-pin DC probes with $-10dB$ attenuation and two differential analog probes with bandwidth of 100kHz to 100MHz.

The input was generated using the LF output of the Tektronix Oscilloscope TDS3000 (500MHz, 2 channels). A phase shifter was used to create the quadrature signal. The differential signals were created using transformers, as seen in Fig. 6.2. The R was selected to be $10k\Omega$ to maintain $0dB$ gain. The R_1 and C were calculated to the center frequency of $83kHz$ using

$$\Delta\theta = \arctan\left(\frac{1}{\omega R_1 C}\right), \tag{6.1}$$

where $\Delta\theta$ is 90°. R_1 was implemented using a potentiometer to adjusted the phase for non-idealization of the capacitor and Op-Amp. The third terminal of the transformer was grounded to make sure that

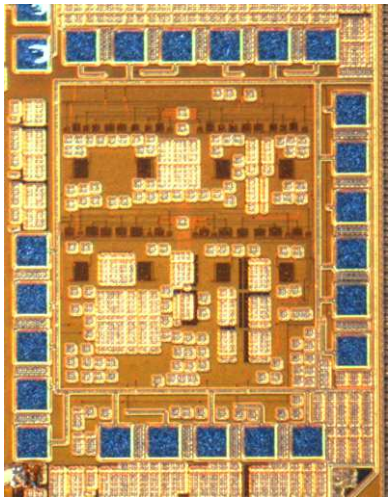


Figure 6.1: Two stage complex BP ΣΔ fabricated chip photo.

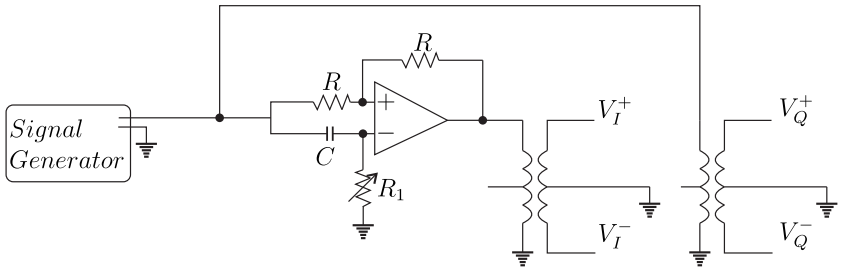


Figure 6.2: Creating differential signals for testing of the fabricated chip.

the two phases were common grounded.

The lab set-up for testing the chip can be seen in Fig 6.3. The DC power supply was used to create the power and biasing signals. The common mode voltage was also created using the DC power supply.

A 4-terminal BKPRECISION oscilloscope was used to verify the output bit streams as well as save the data to be post processed in Matlab. An Agilent Spectrum Analyzer N9320B (Up to 3GHz) verified that the bit streams contained both the noise and signal. Only one channel was needed to see the bins of the output spectrum.

The clock was generated outside the chip using an Agilent Pattern Generator(81130A,660MHz). All cables used for testing have less than -2dB attenuation. The final test set-up was verified to have a noise floor of -120dB.

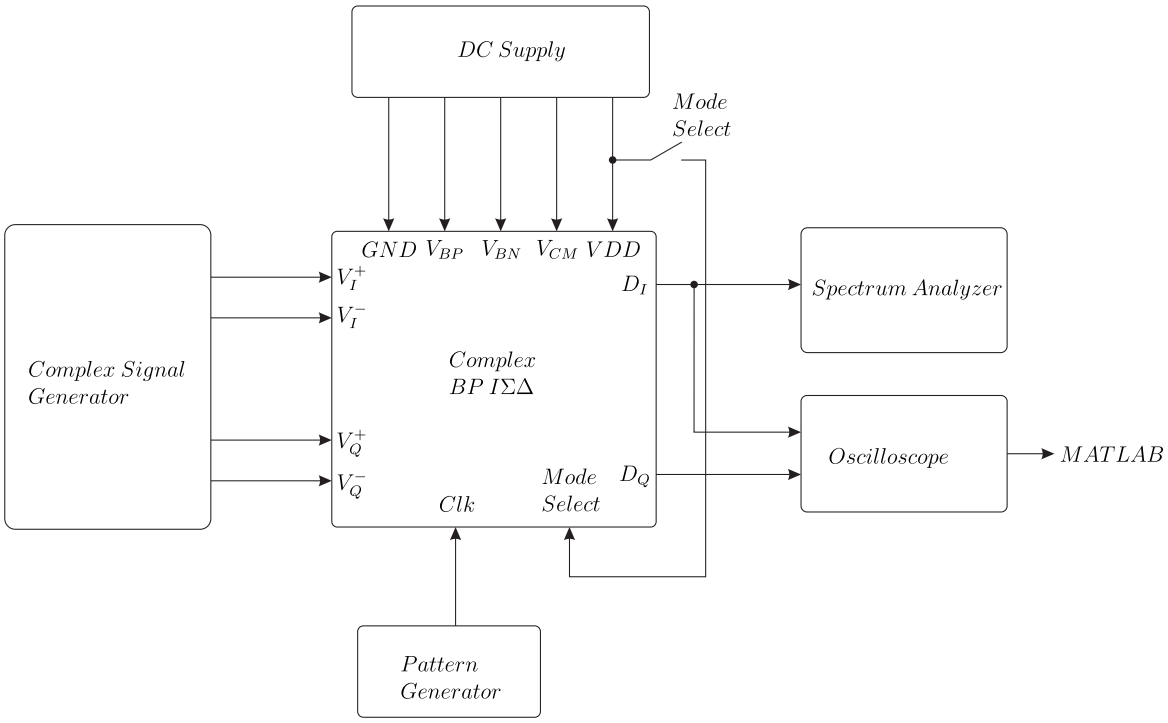


Figure 6.3: Lab set up for testing of the fabricated chip.

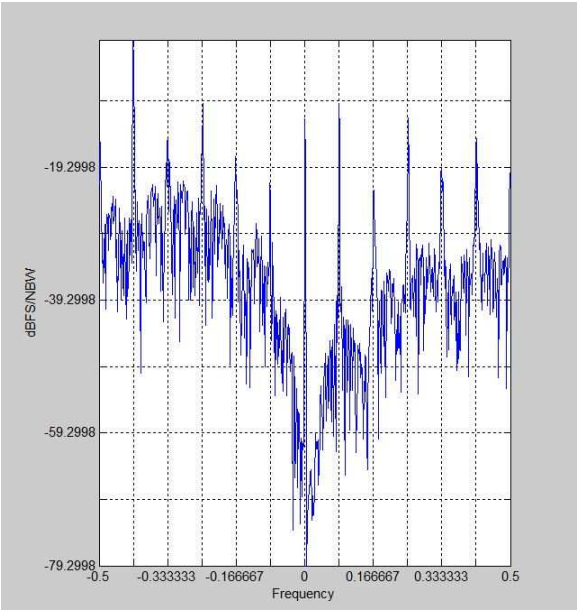


Figure 6.4: Results for the fabricated chip in ΣΔ Mode.

6.2 Results of Bandpass Complex ΣΔ ADC

The spectrum Analyzer was used to capture the frequency of the input it was compares with the output spectrum of the ADC. The output shows that the fabricated chip did perform noise shaping as well as maintaining the center frequency.

6.2.1 ΣΔ Mode

The output spectrum for the ΣΔ Mode can be seen in Fig. 6.4. The noise shaping can be clearly seen along with the two notches. The notches are spaced out around the center frequency indecating that capacitor mismatch has shifted the NTF zeros.

The DC component is due to the bit stream being centred around V_{CM}. The DC spear will not be used in the SQNR calculation.

The spears at the multiples of the input frequency are present because the interconnects did not have any ground shielding. The spurs are outside the bandwidth of the modulator and will be filtered out. The remaining spurs reduced the SQNR to just $12dB$.

6.2.2 Incremental ΣΔ Mode

The output spectrum of the incremental mode can be seen in Fig 6.5. The output has a DC component same as the ΣΔ mode. The multiples of the reset frequency can be seen in the spectrum.

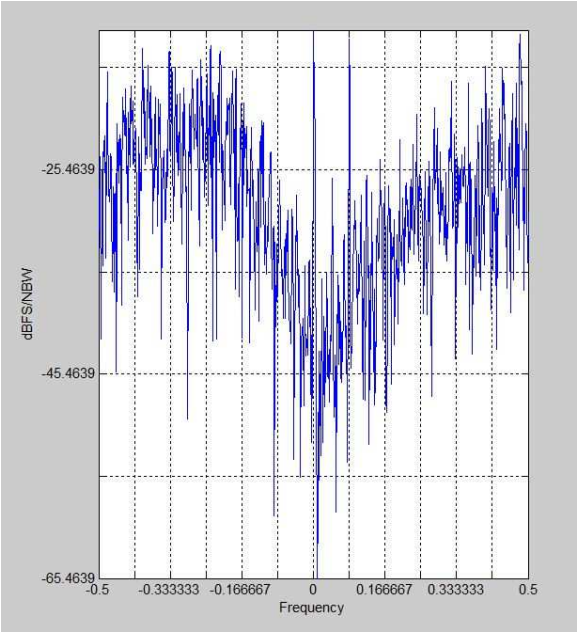


Figure 6.5: Results for the fabricated chip in IΣΔ Mode.

No notches can be seen because the incremental mode does not have noise shaping. Due to the lack of clear notches reduces the total SQNR. The final SQNR is $9dB$ over the bandwidth of the system.

6.3 Results of Complex Low-Pass $I\Sigma\Delta$ ADC

Using the cascade 1-1-1-1 from Sec. 5.3, the LP complex ΣΔ modulators are simulated using Simulink. The ADC is designed using the GUI interface from App. 1. The ADC achieves an IRR of more than 60dB over a range of $140kHz$. In addition, the SQNR of these modulators is 50 dB. The input signal is a real IF which allows the complexity of the time interleaving to be relaxed, as seen in Sec. 4.2.2.

For simplicity, the input center frequency is $f_s/4$ because the digital reconstruction after the decimation filter can be achieving using multiplexers alone, as seen in Sec. 4.2.1. The input is a real signal with $F_{IF} = 1MHz$ and $BW = 70KHz$ therefore the S/H takes a sample once every $1\mu s$. The integrators are running at $F_{int} = 7MHz$ for an OSR of 7, and reset at the same time as the S/H, which then takes a new sample. The decimation filters have three units of delay, as explained in sec 4.2.1. Since the IΣΔ has a one to one conversion, the digital output comes out at $1MHz$.

The digital multiplexer runs at the same frequency as the S/H but with a delay of approximately $524ns$ or 3 integration cycles. The output is multiplexed using $+1, 0, -1, 0, \ldots$ for I and $0, +1, 0, -1, \ldots$ for Q. The final SQNR is 47dB, as seen in Fig. 6.6. The IRR is 57.1dB which is equal to the noise floor. The modulator has a uniform SQNR for the entire BW of the input, as shown in Fig. 6.7. The deviation is only $4dB$ for the entire range of inputs.

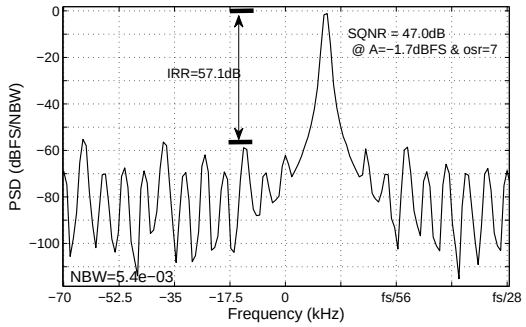


Figure 6.6: Output of complex LP Incremental ΣΔ with OSR of 7 after post filtering .

The type of modulators determines the maximum SQNR. Better performance can be obtained if higher order cascade IΣΔ are used. Another way to increase the SQNR is to increases the OSR which can be done dynamically at the cost of power consumption. Finally, the type of decimation filters can determine the noise floor of the system.

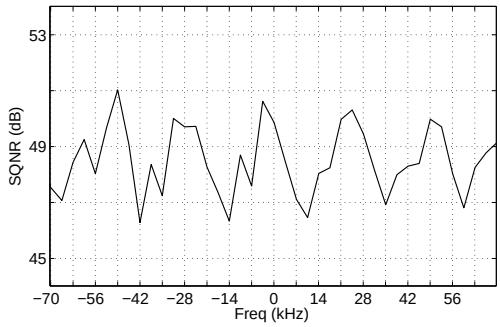


Figure 6.7: SNR vs output signal frequency for a complex LP IΣΔ.

Chapter 7

Conclusion

This thesis looked at different implementations of complex incremental sigma-delta analog-to-digital converters. It showed that it is feasible to use incremental ADCs at a low OSR for complex signals. Incremental converters can have zero I/Q mismatch when both channels are time interleaved on the same path. Time interleaving is only possible for LP incremental a$\Sigma\Delta$ modulator which maintains a one-to-one conversion.

7.1 Summary

For the first time incremental modulators was used to construct complex BP and complex LP $\Sigma\Delta$ ADCs. The pros and cons of using an incremental versus a traditional $\Sigma\Delta$ modulator were presented. Simulation and circuit-based design techniques were also presented along with the complex signal theory.

The contribution of this paper is the application of incremental data converters for complex signals and systems. Both BP and LP incremental systems were introduced and implemented to show the strengths and weaknesses of each type. Finally, a chip level design and testing was presented to show the applications of the theory.

The BP incremental has potential applications but mismatch and noise problems must first be addressed. Also, the complexity of circuits allows for errors to occur. They cannot be fixed in post filtering because incremental modulators do not have noise shaping.

As for the LP incremental $\Sigma\Delta$ modulator, the modulator is simple and does not require complicated sub-systems. The post filter can be simplified to a multiplexer and a few adders. Implementation can be done in FPGA or a reconfigurable application specific block. With the cascade architecture, the system is stable and can reach a high resolution with a low OSR.

A GUI-based design kit was developed to simplify the design of oversampling ADCs. The GUI is built in Matlab and uses SimuLink for testing. The kit is designed to assist in the development of the ADC. First is the mathematical representation of the $\Sigma\Delta$ modulator with the placement of poles and zeros. Second is the simulation of the design, using ideal blocks for feasibility and timing considerations.

Finally, the testing of transistor level circuits by importing data from Cadence Virtuoso.

7.2 Possible Future work

This thesis did not cover cascade architectures with higher order stages or extended range systems. These systems can improve the performance of the incremental ADC with minimal increases in complexity.

The LP system can be extended to have complex inputs or even multi-channel inputs which would increase the complexity of the time interleaving as well as the frequency. Maintaining one path for all signals would mean that the no mismatch would occur.

Appendix 1

Graphical User Interface

1.1 Introduction

The graphical user interface (GUI) was developed in Matlab [43] to simplify the testing of complex $\Sigma\Delta$ modulators. The GUI runs functions from the Sigma-Delta Toolbox [44]. SimuLink [45] systems are also available to test Sigma-Delta modulators in the GUI.

The main features of this system are:

1. Different typologies of $\Sigma\Delta$ modulators are set up manually.
2. SimuLink blocks are automatically set-up to have the same constraints as the mathematical model.
3. Cadence simulation date are processed to show bits and spectrum of the input, output and each stage of the modulators.
4. Sigma-Delta toolbox demos and examples are available.
5. The $\Sigma\Delta$ variables are set for both Incremental and $\Sigma\Delta$ modes.
6. Simulink parameters are set inside the GUI.

This program was created to help with the design of different types of $\Sigma\Delta$ typologies. The GUI is meant to help bridge the gap between the design and verification steps. The user is able to utilize the Sigma-Delta Toolbox to place poles and zeros of the NTF and STF. All of the modulator parameters can be changed to meet any design specifications.

Once the ideal system type has been finalized, its performance can be compared with a system in Simulink where ideal blocks are used. In SimuLink, single or cascade type systems can be tested with the same order and OSR. Even feed-forward architecture can be tested. Extended range and post filters can be added to meet design specifications.

Finally, real simulation results from Cadence can be imported to compare simulation results. This is very important for complicated typologies where each stage output must be compared. Cadence design

Figure 1.1: Initial start up GUI.

is performed in three stages: ideal, circuit level and extracted layout. To achieve high SNR and IRR, all three stages of the design must perform in the same way that the SimuLink system does.

1.2 Getting Started

The GUI is run from an initial screen, as shown in Fig. 1.1. All settings, preferences and configurations are available through this interface. The available options are:

1. File
   (a) Open – Opens a saved working environment.
   (b) Save – Saves all environment settings for the system and simulation.
   (c) Open Cadence Preferences – Opens saved preferences for different tests and typologies.
   (d) Save Cadence Preferences – Saves current preferences.
   (e) Templates – Load a design template.
   (f) Exit – Exits all open windows and deletes all unsaved variables.
2. Edit
   (a) Undo – Reverting any changes to variables or settings.
   (b) Redo – The opposite of Undo.
   (c) Close All Figures – Closes all open figures.
3. Tools
   (a) Example – Opens window to run Sigma-Delta Toolbox examples.
   (b) Demo – Opens window to run Sigma-Delta Toolbox demos.
   (c) Preferences – Opens a window to set which SimuLink system to use and which results to show.

Figure 1.2: GUI for running ΣΔ Toolbox examples.

(d) Import Preferences – Opens a window to set names of the Cadence environment variables.

4. Options

   (a) Design Parameters – Opens window to set Sigma-Delta Toolbox variables for an ideal system.

   (b) Sim Parameters – Opens a window to control all SimuLink simulation preferences.

5. Help

   (a) Introduction

   (b) Tutorial

   (c) Documentation

The GUI also has four buttons, grouped in twos, to run each of the simulations. The first two buttons are for Cadence testing and the second two are for Matlab simulations. The "Import data" button selects a file with Cadence simulation results to be loaded into Matlab. Before this can occur, "Import Preferences" must be set. The "Graph data" button takes the FFT of the results and graphs them for the user.

The simulation buttons are used to run Toolbox functions or SimuLink files. The "Start Sim" button must be pressed first to create the STF and NTF equations. The "Start Simulink" button then takes the NTF equations and converts them to an SS model to determine which SimuLink model to use. Both buttons generate graphs for the input and output of the system being simulated.

1.3 Toolbox Functions

The Sigma-Delta Toolbox comes with pre-set examples and demos to show the full functionality of the toolbox. The GUI allows the user to run these functions through a separate interface. The examples can be run from Tools → Examples (see Fig. 1.2). The Demos can be accessed through Tools → Demos (Fig. 1.3).

1.3.1 Determining NTF

The Toolbox uses eight different variables to determine the NTF and STF of the modulator being designed. These variables are

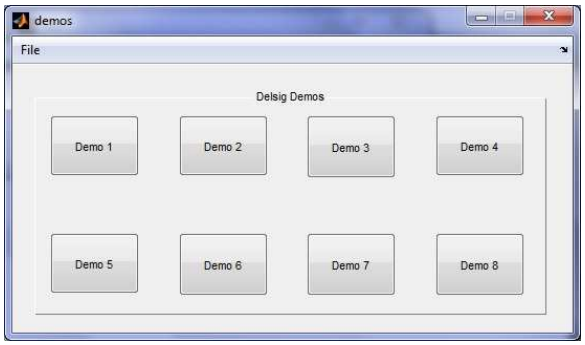


Figure 1.3: GUI for running ΣΔ Toolbox demos.

- Order
- OSR
- M
- Noise Gain
- Image Noise Gain
- f0 – Center frequency for bandpass and complex systems
- Complex
- Form – Feedback (FB) or feed-forward ()

All eight of these values can be set in the Design Options available in the main GUI Options → Design Options or "Ctrl+ P" (Fig. 1.4). The save and exit button must be utilized for the changes to take effect. The NTF and STF can be predefined and the system will use the Matlab variable, holding the z-domain equation, inside the Design Option window.

The simulation outputs three windows, each showing different results. The first window is the ideal NTF and STF, which contains two graphs. In the one on the left, the poles and zeros are graphed in a z-domain, and in the one on the right, frequency response is shown. An example is shown in Fig. 1.5. The z-domain graph clearly shows a complex second order system at $\pi/2$ and the frequency response shows noise attenuation of $-50dB$ at pass-band, and $-3dB$ at the self image frequencies.

The second window shows a time domain response of the same system. The graph on the left shows the frequency response and the one on the right shows the SQNR for a sweep of the input amplitude. The example in Fig. 1.6 shows the frequency response of a system with an SQNR of $69.2dB$. This system is running at an OSR of 64 with an input of $-3dB$. The peak SQNR is $71.2dB$ at an input of $-1.1dB$. The SQNR graph also shows that the quantizer and/or integrator saturation limits the performance of the ADC. To improve the ideal performance, the system setting can be adjusted. This can be achieved by increasing the number of quantization levels of the flash ADC or the OSR.

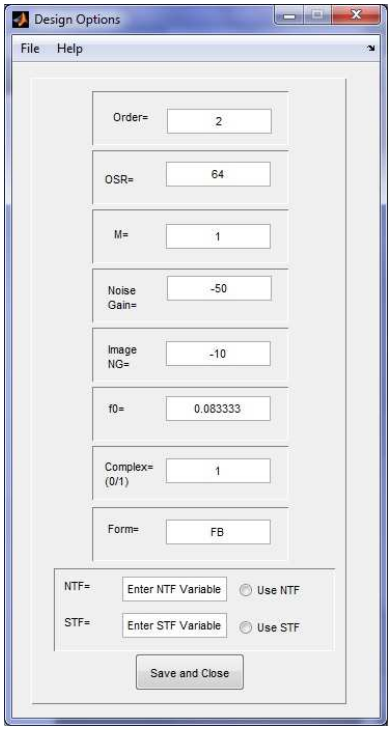


Figure 1.4: GUI for setting design Options in the Delta-Sigma Toolbox.

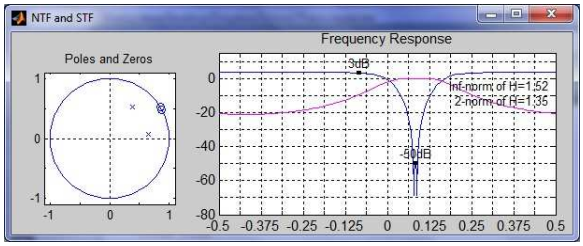


Figure 1.5: Example results for second-order complex ΣΔ modulator.

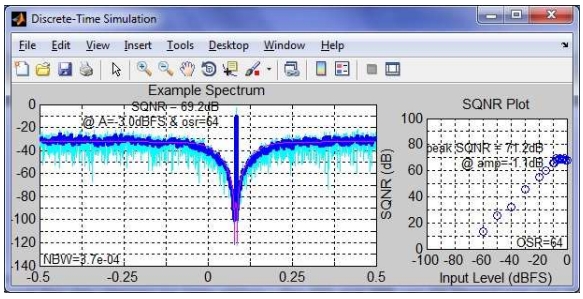


Figure 1.6: Example results of the time domain for second-order complex ΣΔ modulator.

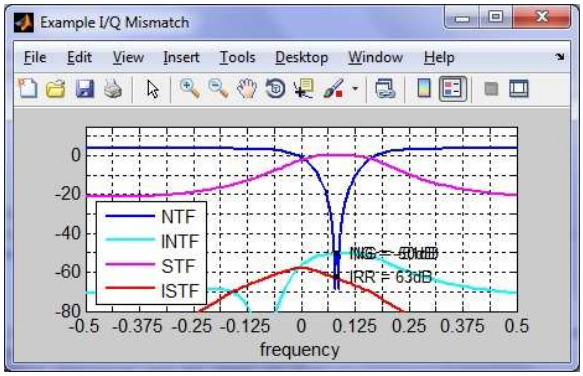


Figure 1.7: Example results of miss match error for second-order complex $\Sigma\Delta$ modulator.

The third window is an I/Q mismatch graph, which shows the NTF and STF for both the I and Q channels with 10% mismatch. In this case, the noise gain (NG) is $-50dB$ and the IRR is $66dB$. This helps the designer when creating the circuit design where channel matching is a concern. An example of this is shown in Fig. 1.7.

1.3.2 SimuLink Simulations

To run pre-set SimuLink models, the NTF for the correct order and type of system must first be set by running the "Start Sim". The GUI uses the NTF to create an SS model which is then used to set the interstage and feedback gains. A third order model is shown in Fig. 1.8. The integrators sampling rate, which is normalized to one, is set to the correct OSR by the GUI.

The simulation parameters can all be controlled in the "Simulation Parameter" GUI, which is accessed through Options $\rightarrow$ Sim Parameters. The GUI, in Fig. 1.9, sets the length of the simulation to allow for better resolution of the FFT. The input frequency shift from the center frequency allows the user to see the change in the SNR for the entire bandwidth of the system. Input voltage can be set for both AC and DC simulations. Finally, the two modes of operation, incremental and $\Sigma\Delta$, are selected. If the incremental mode is selected, the "reset samples" variable is used to set the resetting of the integrators, which is usually the OSR.

Since the pre-set models may not be sufficient to meet all designs typologies, the GUI allows the user to specify the model. Access to these options can be found in Tools $\rightarrow$ Preferences and the pop-up window which is shown in Fig. 1.10. The right hand side allows the user to select which simulation outputs will be displayed. In addition, the sweep of the reset rate section allows the user to sweep the OSR of an incremental mode modulator. The smoothing factor is used to show the moving average of the FFT output.

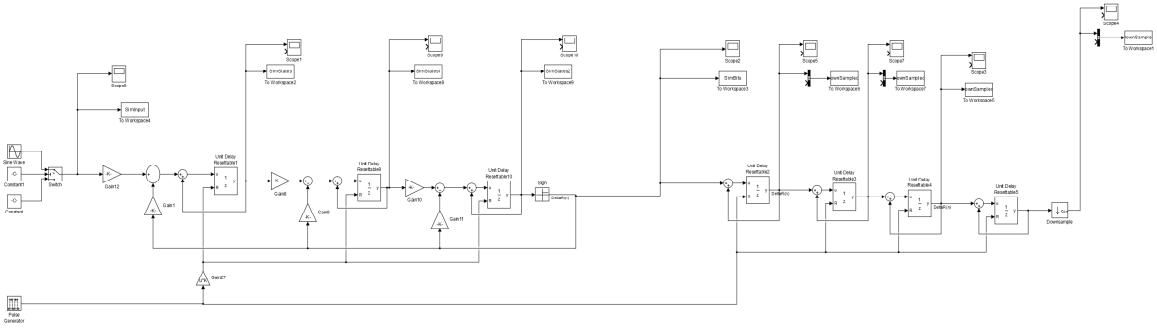


Figure 1.8: SimuLink model of a third-order modulator used by the GUI.

Figure 1.9: Parameters for the simulation of the ideal SimuLink model.

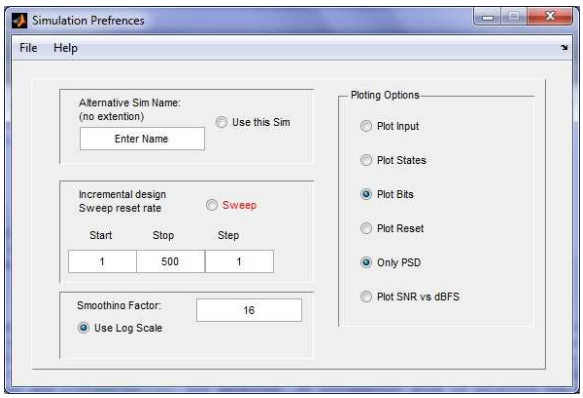


Figure 1.10: Parameters for results of the ideal SimuLink model.

1.3.3 Cadence Importing

The circuit level simulations are performed in the Cadence icfb environment, which simulates the Spice model. This allows the performance of the modulators to be simulated with second and third order non-linear effects. Comparing the states of each integrator output allows the designer to ensure that the system is performing properly.

The designer must tell the GUI the names of each signal to be imported from Cadence so that proper outputs can be displayed. A GUI interface is available in Tools → Importing Preferences (Fig 1.11). If the system uses I and Q channels, the Quadrature option must be selected. The down sampling is needed to convert the continuous signal to a digital signal, with one sample for each sampling period. The run time option is used to reduce the number of states displayed, to facilitate easier comparison with SimuLink.

The "Import Data" button on the main window allows the user to select the appropriate file containing the Cadence data. The "Graph Data" button is used to graph the states specified in the Import Preferences GUI.

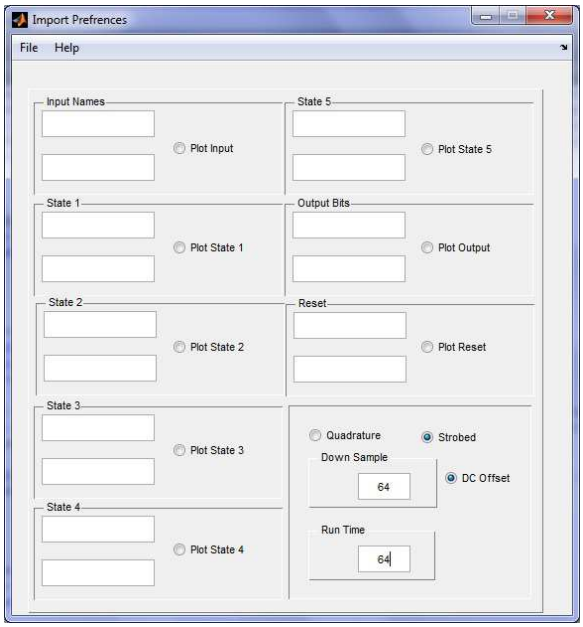


Figure 1.11: Preferences for importing Cadence results.

1.4 Extra Features

Maintaining consistency throughout the design process is essential. Each window in the GUI has the save and open option. When working with each stage separately, the user is able to load the save state at a moment's notice or send design parameters to a different user. Also, all variables throughout the design kit can be saved at the same time through the main window, using File → Save, or CTRL+S. In addition, the save state can be loaded using File → Open, or CTRL+O. Opening a saved file, in any of the environments, will delete all previous data.

1.5 Final remarks

This tool was created to help the user design an oversampling ADC for high speed applications. All mathematical models are based on ΣΔ toolbox by R. Schreier. Before using the GUI, the user must be familiar with the toolbox. The SimuLink models were designed to help compare incremental and ΣΔ modes of operation.

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