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A low-voltage CMOS current-mode differential front-end for optical communications

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A Low-Voltage CMOS Current-Mode Differential Front-End for Optical Communications

by

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Master of Applied Science, 2003
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Abstract

This thesis deals with the design of a low-voltage fully-differential CMOS current-mode preamplifier for optical communications. An in-depth comparative analysis of the building blocks of low-voltage CMOS current-mode circuits is carried out. Two new bandwidth enhancement techniques, namely inductor series-peaking and current feedback, are introduced and implemented in the design. The feedback also reduces the value of the series-peaking inductor. The minimum supply voltage of the amplifier is only one threshold voltage plus one pinch-off voltage. The preamplifier has a balanced differential topology such that the effect of bias-dependent mismatches is minimized and the amplifier is insensitive to the switching noise caused by the digital circuitry. Negative differential current feedbacks are implemented to boost the bandwidth and increase the dynamic range. The design is based on 0.18 μm CMOS technology. It has the bandwidth of 3.5 GHz and provides 66 dB differential transimpedance gain with standard 50 Ω loads.

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Chapter 1

Introduction

1.1 Overview

Optical fiber communication systems have been greatly developed with the blossom of Internet and Intranet networks. Optical communication systems are to carry a large volume of data across the networks. The primary application of such systems is in long distance telecommunication networks. For example, the telephone systems in Europe are connected to those in the North America through a fiber system installed across the Atlantic Ocean. Multimedia applications such as advanced graphics, audio, video conferences are driving the adoption of optical data links for short haul optical communications as well. The exchange of data using optical fiber communications gives a number of advantages over metal-wired cable systems. These are higher bandwidth, lower attenuation, smaller bit error rates (BERs), and less electromagnetic signal interface [1]. The cost of manufacturing and installing optical fiber cables is now less than that of metal cables for applications over 100 Mbps.

A transmitter and a receiver, connected by the fiber cable, constitute a generic optical communication system. The transmitter consists of a current drive circuit and an optical emitter, while the receiver consists of an optical detector and an amplifier circuit. The fiber cable is the transmission medium. The light experiences attenuation

as it travels through long distance or low cost fibers. Thus, the receiver must exhibit wide bandwidth, high sensitivity and low noise. Our research is focused on the design of the front-end preamplifier which is the most challenging part in optical communication systems.

Currently, most high-speed optical receiver designs are using bipolar or GaAs MESFET transistors [2], which give wider bandwidth. However, standard CMOS technology provides advantages such as low power and low cost. It also gives high degree of integration, which makes it possible to integrate the front-end preamplifier and the clock and data recovery circuits into a single chip. The f_T of MOS devices has also been improved significantly such that it is feasible to use CMOS for the optical front-end. The cost of an optical receiver built by GaAs is about 10 times that of a CMOS receiver. The rapid expansion of optical communication networks, especially the trend of "fiber-to-user" and "fiber-to-home", has brought more research interests on the design of low-cost, high-speed and low-noise optical receivers using standard CMOS technologies. In this thesis, a low-voltage current-mode CMOS preamplifier is designed using TSMC (Taiwan Semiconductor Manufacture Company) 0.18 μm mixed-signal CMOS technology.

Transimpedance, high-impedance and low-impedance are three conventional configurations of preamplifiers of optical receivers. They convert the current from the photodetectors to a voltage signal. Intrinsically, all of the above configurations are based on voltage-mode operation. Recent advance in CMOS technology, mainly driven by low-power applications, has significantly lowered the supply voltage. The reduction in threshold voltages, however, is rather moderate in order to sustain needed noise margins. As a result, the performance of voltage-mode circuits is affected greatly. CMOS current-mode circuits offer many attractive advantages over their voltage-mode counterparts.

The key performance feature of current-mode circuits is their inherent wide bandwidth. Transistor are used almost up to f_T in a current amplifier [3]. Other advantages include low supply voltage requirement, large dynamic range, and tunable input impedance [4]. These characteristics make the current-mode circuits particularly attractive for high-speed computer I/Os [5], and low-cost fiber communications [6].

The objective of this research is to design and build a current-mode front-end amplifier for optical receivers using standard CMOS technology. The aimed data rate is 5Gbps, which matches the rate of OC-96. The transimpednace gain is expected to reach 66dBΩ (2KΩ) to sustain a large noise margin. The amplifier is intended to work with the minimum supply voltage requirement, and a differential configuration is adopted to minimize the switching noise caused by the clock and data recovery circuitry. The dynamic range of the amplifier must be large enough to accomodate different link distances. Other design objectives include minimum mismatch effects, and low power consumption.

TSMC 6-metal, 0.18 μm, 1.8 V mixed-signal CMOS technology is used for the design. Spectre from Cadence Design Systems with BSIM3V3 device models [7] is the CAD tool used for analysis. The designed chip is currently being fabricated by TSMC via CMC (Canadian Microelectronics Corporation).

1.2 Original Contributions

This thesis designs a new low-voltage, wide-band, high gain, large dynamic range, and fully differential CMOS current-mode preamplifier for optical communications. Leading by a comprehensive analysis of the characteristics of current-mode circuits, several new topologies and design strategies are introduced to support the final circuit design.

The major contributions of the thesis are summarized as follows:

- An in-depth comparative analysis of the characteristics of various low-voltage CMOS current-mode configurations is conducted, and many useful insights are obtained.

- A new inductor series-peaking technique to boost the bandwidth of current amplifiers is developed and implemented in the design of the preamplifier.

- A new current feedback technique to lower the input impedance, boost the bandwidth, and reduce the value of the series-peaking inductance is developed and implemented in the design of the preamplifier.

- A two-stage fully balanced current amplifier to achieve a larger bandwidth with the same gain, and to minimize the mismatch effects of current mirrors is proposed. A current-branching mechanism to reduce the power dissipation and increase the output impedance of current amplifiers is introduced.

- A differential current-mode configuration to minimize the effect of switching noise caused by the digital circuitry is proposed. A new negative differential current feedback to boost the bandwidth, and increase the dynamic range of the differential amplifier is implemented.

These original contributions have been published in one journal paper [8] and several conference proceedings [9] [10] [11] [12] [13].

1.3 Thesis Organization

The thesis consists of 7 chapters and is organized as follows:

In chapter 2, we give a brief review of optical communication systems. The characteristics of photodetectors are depicted. The performance requirements and design

challenges of optical receivers are described. Conventional structures of optical receivers are reviewed and analyzed. A primitive current-mode approach for optical front-end preamplifiers is proposed.

In chapter 3, we give a in-depth comparative study of the characteristics of various low-voltage current-mode circuits. Design issues, such as input impedance, bandwidth, dynamic range, and noise performance are examined both analytically and quantitatively. It reveals that most configurations fail to function properly at high frequencies. The current-mirror amplifier with current feedback offers the best performance.

Chapter 4 introduces two new bandwidth enhancement techniques for current-mode circuits. The inductor series-peaking technique boosts the bandwidth by utilizing the resonance characteristics of LC network formed by placing an inductor in series with the capacitor constituting the dominant pole. The technique is demonstrated in both of the current-mirror amplifier configuration and the optical preamplifier configuration. The current feedback increases the bandwidth by taking the advantage of negative feedback theory. A new sampling mechanism is introduced to acquire the feedback current. It shows that the employment of both the inductive peaking and current feedback further increases the bandwidth, and the current feedback can significantly reduces the value of the peaking inductor. Both the inductor series-peaking and the current feedback techniques do not affect the supply voltage and the DC biasing conditions.

Chapter 5 introduces several topologies and design strategies to improve the performance of current-mode circuits. It shows that a two-stage amplifier configuration has a higher bandwidth than that of a single-stage one. The accuracy of current-mode circuits is severely affected by the errors caused by the mismatches of current mirrors. Analysis shows that a fully balanced configuration can minimize the DC bias-induced mismatch error, which is the dominant portion of the output offset current. A current-branching

configuration is introduced to reduce the power consumption of the circuit, and to increase the output impedance. To minimize the effect of power and ground fluctuations caused by the switching of the digital portion of the receivers, we propose a fully differential current-mode configuration. Negative differential current feedback is employed to boost the bandwidth and improve the dynamic range of the differential amplifiers. A common-mode feedback configuration is proposed to increase CMRR and to stabilize the DC biasing condition.

Chapter 6 presents a new low-voltage fully differential CMOS current-mode preamplifier with the preceding circuit techniques implemented. It examines the design techniques, selection of circuit parameters, and the layout strategies. Simulation results are shown to demonstrate the performance of the preamplifier.

In chapter 7, the thesis is summarized and the directions of future research are discussed.

Chapter 2

Background

This chapter gives an overview of the structure of optical communication systems, the characteristics of photodetectors, and the configuration of front-end amplifiers. It discusses the receiver design requirements, and reviews the principal structures of the preamplifiers. Followed by discussion on the challenges of the front-end design, we propose a current-mode approach.

2.1 Generic Optical Communication Systems

Fig. 2.1 shows the basic elements of optical fiber communication systems. On the transmitter side, a drive circuitry accepts the modulated data and delivers large electrical current to the laser diode or light emitting diode (LED). Laser diodes or LEDs then convert the electrical signals into optical signals, and launch them into an optical fiber. The fiber, made from pure glass, is the high-speed propagating medium for optical signals. The device responsible for converting the optical signal back to an electrical signal is an optical receiver. A typical fiber optical receiver consists of an optical detector, a low-noise amplifier, and other circuitry used to recover the clock and data.

There are two widely adopted standards for synchronous fiber-optic transport systems. SONET (Synchronous Optical NETwork) is the North America standard, and

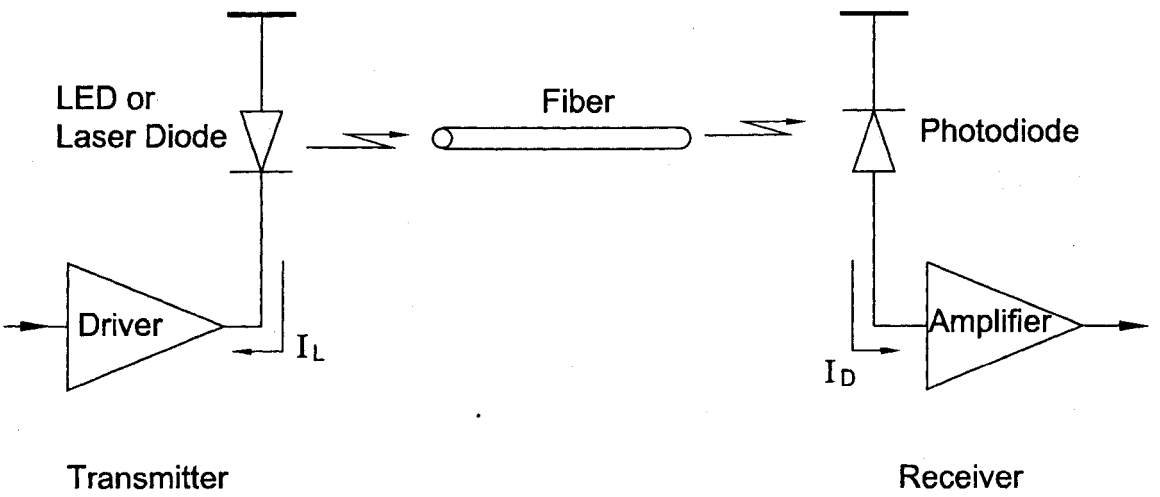

Figure 2.1: Simple optical communication system

SDH (Synchronous Digital Hierarchy) is a similar standard used by the rest of the world [1]. Table 2.1 shows the data rates of SONET and SDH. Although the bandwidth of the fiber is capable of 10^6 Gbps with 1 Km communication distance, due to the speed limitation of the electrical devices, 2.5Gbps (OC-48) optical system was the state of the art design in the past few years and 10Gbps (OC-192) is emerging.

Table 2.1: Commonly used SONET and SDH transmission rates

SONET Level	SDH equivalent	Line rate (Mb/s)
OC-1	–	51.84
OC-3	STM-1	155.52
OC-12	STM-4	622.08
OC-24	STM-8	1244.16
OC-48	STM-16	2488.32
OC-96	STM-32	4976.64
OC-192	STM-64	9953.28

There are three popular wavelengthes used in fiber communications. The first-generation links operated at around 850 *nm*. 1310 *nm* and 1550 *nm* wavelengthes

were adopted with the development of optical sources and photodetectors because of their low attenuation in optical fibers as shown in Fig. 2.2 [2]. The launched optical signals will be progressively attenuated and distorted with increasing distance because of scattering, absorption, and dispersion in the glass material [2]. The attenuated and distorted signals have made the design of the front-end optical receivers to be the most challenging part of an optical communication system.

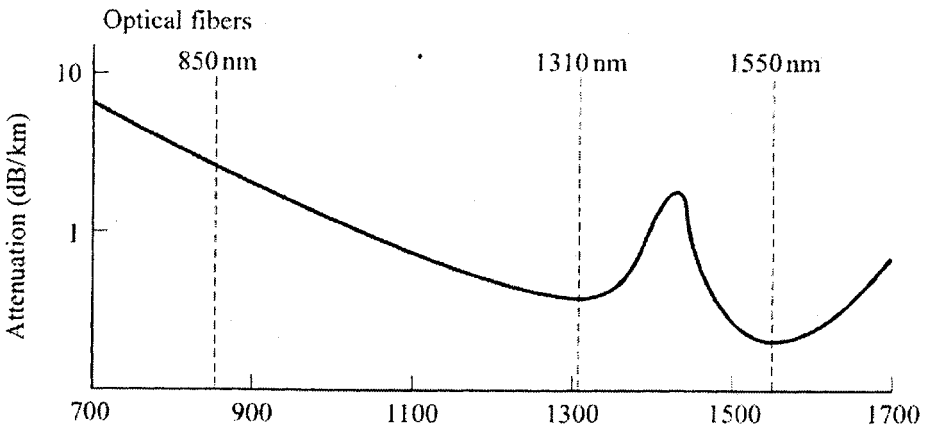

Figure 2.2: Attenuation in optical fibers

2.2 Photodetectors

A photodetector is a transducer that converts the incident optical power into an electrical current. Semiconductor photodiodes are ideal for high-speed optical communications because of their superior frequency response, low dark currents and high quantum efficiency [14]. The principal photodiodes used in fiber optical systems include semiconductor positive-intrinsic-negative (PIN) photodiodes and avalanche photodiodes (APDs). A PIN photodiode is a semiconductor positive-negative (p-n) structure with an intrinsic region sandwiched between the other two regions. It is normally operated by applying a reverse-bias voltage. The magnitude of the reverse-bias voltage depends on the photodi-

ode application, but typically is less than a few volts. An avalanche photodiode (APD) is a photodiode that internally amplifies the photocurrent by an avalanche process. The sensitivity of APD detectors is usually higher than that of PIN detectors. However, a large reverse-bias voltage is needed to apply across the APD's active region.

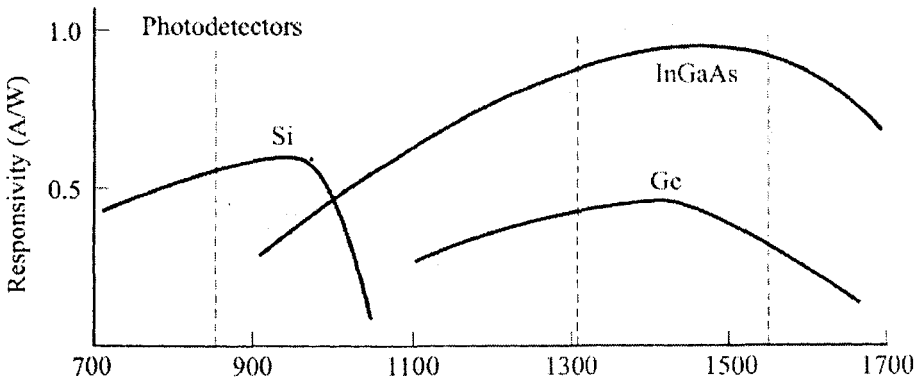

Figure 2.3: Responsivity of photodetectors

The small-signal equivalent circuit of an PIN photodiode is shown in Fig. 2.4. The photodiode capacitance C_d consists mainly of the junction capacitance and parasitic capacitance of packaging. The series resistance R_s is very small comparing with the load resistance. Small C_d is needed to achieve high-speed response. A thick active area can lower the photodiode capacitance. However, a thick active region increases the transit time and decreases the responsivity of the photodiode. Practically, the photodiode capacitance is quite large (in the range of 100 to 500 fF) [15]. In general, the photodiode capacitance is the dominant factor of the frequency response of an optical receiver.

The photocurrent i_s, is generated through the creation of electron-hole pairs when photons from the incident light penetrate the diode. The relationship of the photocurrent and the incident optical power is given by

$$i_s = R_r P \qquad [\text{A}] \qquad (2.1)$$

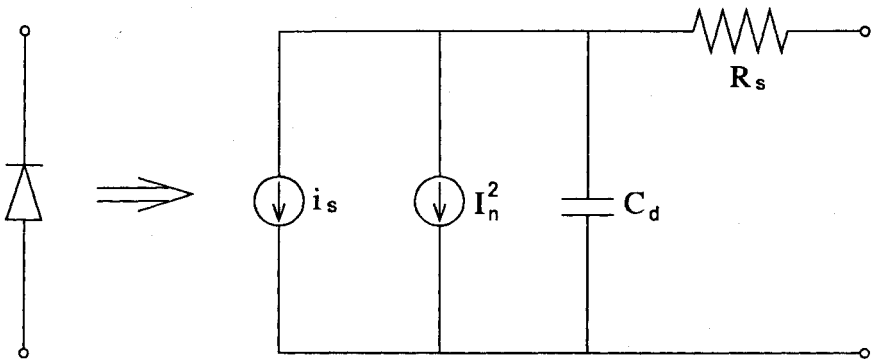

Figure 2.4: Small signal equivalent circuit of PIN photodiodes

where P is the average optical power incident on the photodiode and R_r is the responsivity of the photodiode and is given by

$$R_r = \frac{\eta q}{h\nu} \qquad [\text{A/W}] \tag{2.2}$$

where η is the quantum efficiency (usually in the range of 0.6 to 0.9), q is the electron charge (1.69×10^{-19} C), and $h\nu$ is the photon energy. The responsivity is a function of wavelength. As shown in Fig. 2.3 [2], the material of the photodiode must match the light wavelength to maximize the power efficiency. At a given wavelength (a given value of $h\nu$), the responsivity is constant, so the photocurrent i_s is proportional to the optical power P. The typical value of R_r is around 0.85 A/W for InGaAs detectors at 1310 nm.. Table 2.2 shows the maximum and minimum input optical power and their respective photocurrent for SONET OC-48 receivers. The definition of long-distance (LR), intermediate-distance (IR) and short-distance (SR) optical links is given in Appendix A. It is seen that, in all the three type links, the photocurrent generated by the minimum input power is quite weak.

The photodiode also generates un-negligible noise power I_n^2 into the downstream preamplifier. This noise consists of thermal noise, dark current noise, and quantum

Table 2.2: Minimum and maximum input power and their respective photocurrent of OC-48 receivers

(with R_r=0.85 A/W)

—	Long Distance	Intermediate Distance	Short Distance
P_{max} (dBm)	-10	0	-3
Current (μA)	85	850	426
P_{min} (dBm)	-26	-18	-18
Current (μA)	2.14	13.47	13.47

noise [14]. Although low-noise photodiodes are essential for high-performance optical receivers, the noise of the preamplifier is usually the dominant contributor to the noise of the receiver.

2.3 Optical Preamplifiers

2.3.1 Preamplifier Performance Parameters

The front-end amplifies the photocurrent so that it can be used by following clock and data recovery circuits. It plays a crucial role in determining the overall performance of the receiver such as gain, bandwidth, noise, and dynamic range.

(i) **Gain** – Since the photocurrent generated by the photodiode is small, the gain of the preamplifier must be large enough. Large preamplifier gain helps to overcome the noise of the subsequent stage. Therefore, the design of the subsequent stage, typically a 50-Ω driver or a limiting post-amplifier, can be simplified [15]. The gain trades with bandwidth and dynamic range. The tendency of increasing data rate and decreasing power supply voltage have limited the transimpedance gain from several kilo-Ohms to a few hundred Ohms.

(ii) **Bandwidth** – Due to the inevitable large photodiode capacitance, the total input capacitance of the preamplifier, C_{in}, consisting of the photodiode capacitance, pad capacitance, and input transistor parasitic capacitances, usually dominates the frequency response of the receiver. The bandwidth is determined by the time constant $\tau = R_{in}C_{in}$ at the input. The rising time of the step response is given by $t_r = 2.2R_{in}C_{in}$ [16]. SONET employs Non-Return-to-Zero (NRZ) as its data format. With $t_r = \frac{1}{2}$Bit-Time, it is given that

$$f_{-3dB} = \frac{1}{2\pi R_{in}C_{in}} = \frac{2.2}{2\pi t_r} = \frac{2.2}{2\pi \times \frac{1}{2}\text{Bit-Time}} = \frac{2.2}{\pi} \times \text{Bit-Rate} \tag{2.3}$$

For example, the data rate of SONET OC-96 is about 5 Gbps, the minimum bandwidth requirement of the optical receiver is 3.5 GHz.

(iii) **Noise** – The receiver sensitivity is the minimum amount of optical power required to achieve a specific receiver performance. For digital transmission at a given data rate, this performance is characterized by the maximum bit-error rate (BER) [2]. In analog systems, for a given modulation and bandwidth, it is described by the minimum signal-to-noise ratio (SNR). The relationship between BER and SNR [15] [17] [18] is given by

$$\text{BER} = \frac{1}{\sqrt{2\pi}Q}\exp(-\frac{Q^2}{2}) \tag{2.4}$$

where

$$Q = \frac{1}{2} \times \text{SNR} = \frac{1}{2} \times \frac{\text{Signal}_{pp}}{\text{Noise}_{rms}} \tag{2.5}$$

SONET standard requires the BER not less than 1×10^{-10}. From Table 2.2, -18dBm incident optical power generates a 13.47 μA_{pp} photocurrent (with R_r=0.85 A/W). Thus

to achieve a BER less than 1×10^{-10}, the input current noise, including the input referred current noise of the preamplifier and the noise of the photodiode, must be lower than 1.06 μA_{rms}.

Table 2.3: The relationship between BER and SNR

BER	10^{-7}	10^{-8}	10^{-9}	10^{-10}	10^{-11}	10^{-12}	10^{-13}	10^{-14}
SNR (A/A)	10.4	11.2	12.0	12.7	13.4	14.1	14.7	15.3

(iv) **Dynamic Range** – Dynamic range of the receiver refers to the range of optical power levels over which the receiver operates within the specification. Table 2.2 shows that the power specifications vary dramatically according to the transmission distance. Receivers that have large dynamic range are essential to the flexibility of variable-distance links. However, Recent advance in CMOS technology has significantly lowered the supply voltage, while the threshold voltages of MOS devices have only been reduced moderately. As a result, the input and output signal swings are strictly limited. Low-voltage amplifiers tolerating high signal swing are crucial in up-to-date optical receiver design.

2.3.2 Conventional Preamplifier Structures

Optical preamplifiers convert the current from photodiodes into a voltage signal. As depicted in Fig. 2.5 and 2.6, there are three typical preamplifier configurations, namely low-impedance, high-impedance, and transimpedance amplifiers. Low/high impedance preamplifiers have the same topology. Their transfer function is given by

$$\frac{V_o(s)}{I_{in}(s)} = -\frac{AR}{1 + sRC_{in}} \tag{2.6}$$

where R is the termination resistance, C_{in} is the total input capacitance consisting of

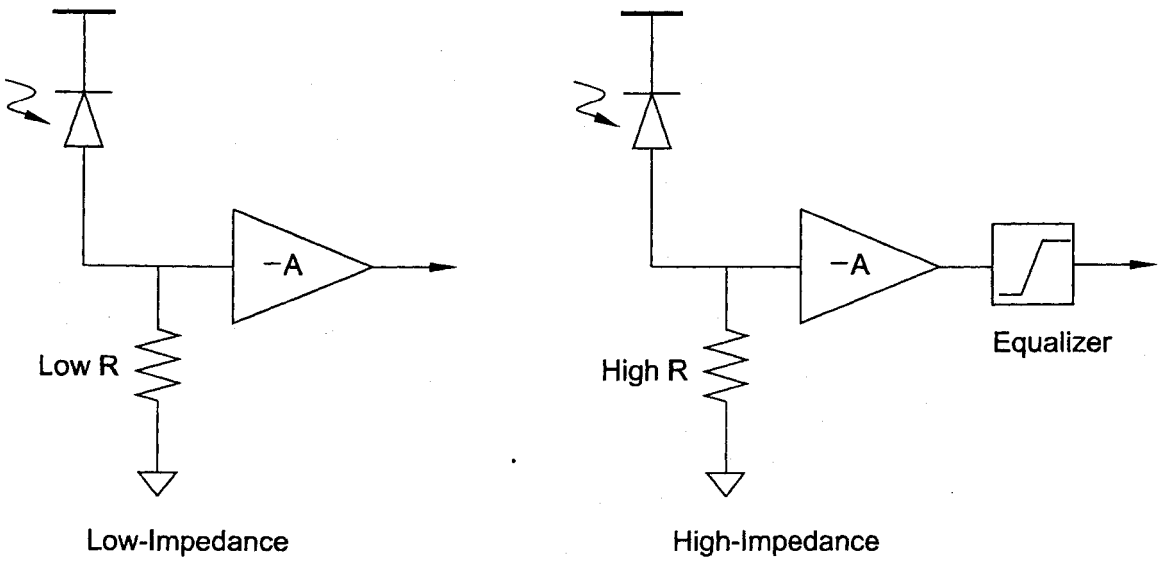

Figure 2.5: Low impedance and high impedance amplifiers

photodiode capacitance C_d and preamplifier parasitic input capacitance. The bandwidth is given by

$$f_{-3dB} = \frac{1}{2\pi RC_{in}} \tag{2.7}$$

As depicted in Section 2.2, the photodiode capacitance C_d is usually large. As a result, the total input capacitance usually dominates the frequency response of the preamplifier. Thus, low-impedance configuration exhibits a better high-speed performance. This configuration also has a good dynamic range. The noise performance of this configuration is poor. This is because the thermal noise of the termination resistor R is directly referred to the input, and its noise current power density is given by

$$\overline{i_{n,R}^2} = \frac{4kT}{R} \qquad [A^2/\text{Hz}] \tag{2.8}$$

where k is the Boltzmann's constant ($1.38\times10^{-23}J/K$) and T is the absolute temperature degree in Kelvin. The smaller the value of R, the higher the noise current. High-

impedance amplifiers improve the noise performance at the expense of both the dynamic range and bandwidth. Usually, this configuration needs an equalizer to enlarge the bandwidth.

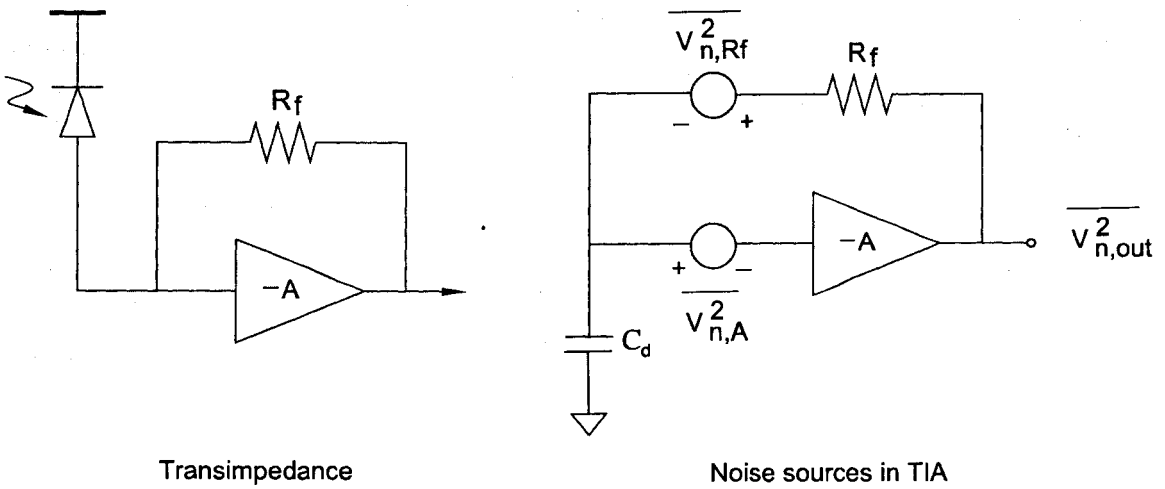

Figure 2.6: Transimpedance amplifier and its noise sources

Transimpedance amplifiers (TIAs) shown in Fig. 2.6 is a compromise of low-impedance and high-impedance approaches. R_f is a shunt-shunt feedback resistor [19], and the transfer function is given by

$$\frac{V_o(s)}{I_{in}(s)} = -\left(\frac{A}{A+1}\right)\frac{R_f}{1+s\dfrac{R_f C_{in}}{A+1}} \tag{2.9}$$

The bandwidth is given by

$$f_{-3dB} \approx \frac{A}{2\pi R_f C_{in}} \tag{2.10}$$

It is seen that the transimpedance gain is approximately equal to the resistance of R_f, and the bandwidth is boosted by the voltage gain.

From Fig. 2.6, the output noise voltage is given by

$$V_{n,out}(s) = \frac{V_{n,R_f} + (sR_fC_d + 1)V_{n,A}}{1 + \frac{sR_fC_d}{A}} \tag{2.11}$$

where $V_{n,A}$ is the input referred noise voltage of the voltage amplifier, V_{n,R_f} is the noise voltage of the feedback resistor. It can be shown that if $C_d = 0$, then $V_{n,out} = V_{n,R_f} + V_{n,A}$, yielding the input referred noise current of the transimpedance amplifier

$$\begin{aligned} \overline{I_{n,in}^2} &= \frac{\overline{V_{n,R_f}^2} + \overline{V_{n,A}^2}}{R_f^2} \\ &= \frac{4kT}{R_f} + \frac{\overline{V_{n,A}^2}}{R_f^2} \end{aligned} \tag{2.12}$$

The input referred noise voltage of the voltage amplifier is divided by R_f, but the noise of R_f is directly referred to the input.

Much research has been done on CMOS transimpedance amplifiers. The common-gate transimpedance amplifier [20] features large bandwidth, but its dynamic range is small and the input referred noise is high. Regulated cascode configuration [21] was introduced to increase the bandwidth and reduce the noise of the common-gate amplifiers, but this configuration has small gain and high power consumption. Most CMOS transimpedance amplifiers use the common-source configuration [22] as shown in Fig. 2.7(a).

As depicted in Section 2.3.1, the transimpedance gain ($\approx R_f$) is about a few hundred Ohms to a few kilo-Ohms. Only poly resistors and diffusion n+/p+ resistors, whose sheet resistance is small, are suitable to be used to build such a relatively small feedback resistor. Unfortunately, CMOS passive resistors have very poor accuracy. For example, the error of the poly resistors is about $\pm 20\%$, and that of the diffusion n+/p+ resistors is about $\pm 30\%$ [23]. Thus, the transimpedance gain is very difficult to be accurately specified, resulting in uncontrolled amplifying performance. It is even more challenging

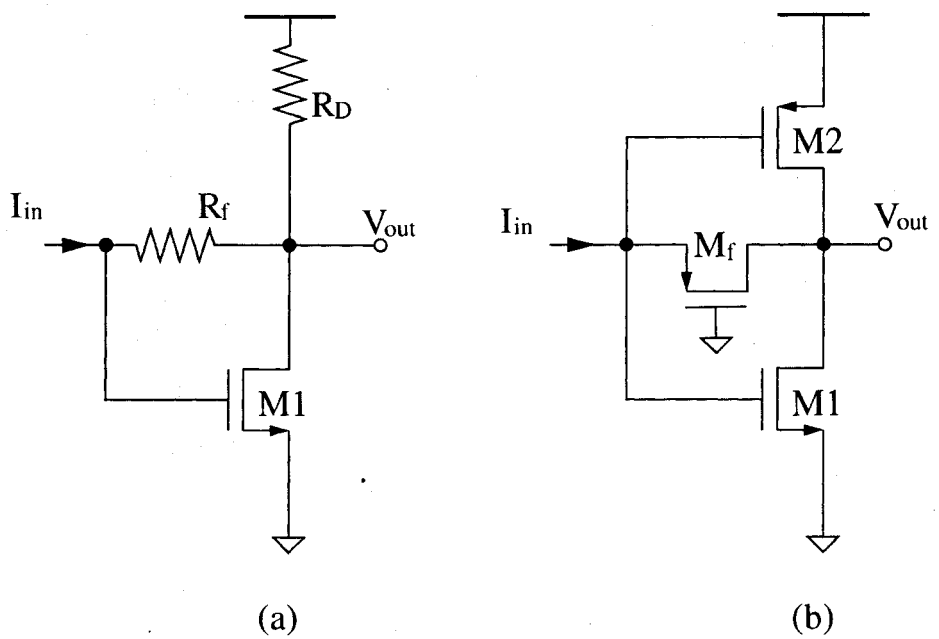

Figure 2.7: CMOS transimpedance amplifiers
(a)Common-source amplifier, (b)Invertor amplifier

in designing an analog signal processing system where accuracy is strictly required. Another disadvantage of the common-source transimpedance amplifier is that the output voltage has to be restrained to ensure that the transistor is working in the saturation region. Thus, the dynamic range of this configuration is small [24].

An invertor transimpedance amplifier as shown in Fig. 2.7(b) [25] was introduced recently. Active feedback is employed in this configuration. The feedback PMOS transistor M_f works in the linear region. The major disadvantage of this circuit is that the transistor M_f working in the linear region has a large drain-to-substrate parasitic capacitance [25]. It introduces a large loading capacitance at the output node.

2.3.3 Current-Mode Approach

Voltage amplifiers are employed in the conventional preamplifiers. The gain-bandwidth product of the amplifiers limits the bandwidth of the voltage amplifiers as well as the

bandwidth of the whole preamplifier. The optimal voltage gain in the invertor transimpedance amplifier is only about 3 [25]. Thus, a small and accurate feedback resistor is critical for the high performance wide-band preamplifiers.

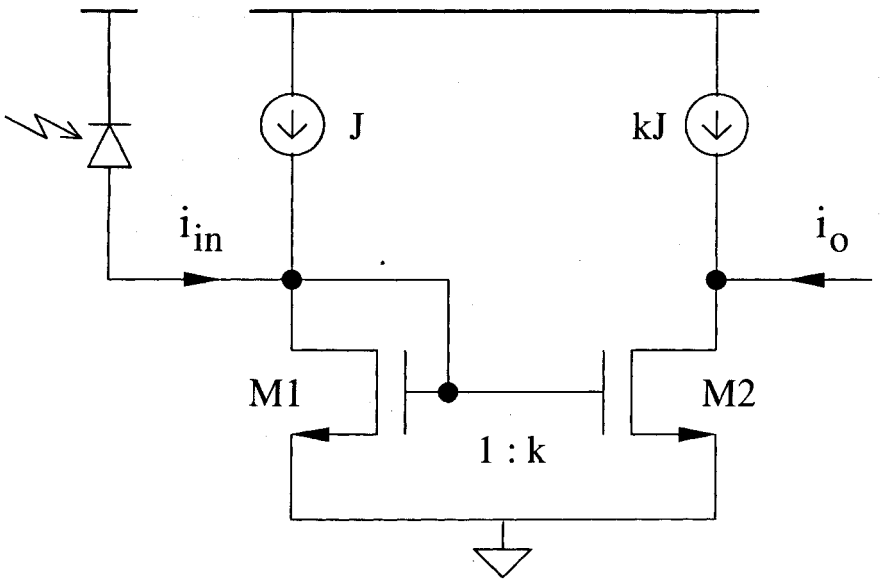

Figure 2.8: Current-mode approach of optical fron-end

The intrinsic advantages of current-mode circuits including large bandwidth, low supply voltage requirement, tunable input impedance, and large dynamic range [3] [4], make them particularly attractive for low-cost optical communications. Current-mirrors are the building blocks of current-mode circuits. Fig. 2.8 shows a primitive current-mode approach for an optical front-end. No necessary passive components are adopted. The current source may be implemented by PMOSs with a DC gate voltage. The minimum requirement of the supply voltage is about $V_{T,n}+V_{sat,p}$, where V_T is the threshold voltage and V_{sat} is the pinch-off voltage. The input impedance is given by

$$R_{in} \approx \frac{1}{g_{m1}} = \frac{1}{\sqrt{2\mu_n C'_{ox}(W/L)_1 J}}, \tag{2.13}$$

where μ_n is the surface mobility of the channel of NMOS, C'_{ox} is the gate oxide capaci-

tance density. A desired low impedance is achievable by increasing the biasing current J or by increasing the channel width of M_1.

The current gain at low frequencies is given by

$$k = \frac{(W/L)_2}{(W/L)_1}\left(\frac{v_{GS2} - V_{T2}}{v_{GS1} - V_{T1}}\right)^2 \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS2}}, \tag{2.14}$$

where λ is the channel length modulation parameter, v_{GS} and v_{DS} are the gate-source and drain-source voltages, respectively. Neglecting the mismatches, we obtain $k = \frac{(W/L)_2}{(W/L)_1}$. The current gain simply equals to the size ratio between the output and input transistors. The higher the current, the larger the size of output transistors, resulting in larger parasitic capacitances. As long as the parasitic capacitances of the transistors are much smaller than that of the photodiode, the increase in the current gain has a little effect on the bandwidth.

The input referred noise current power density of the current mirror amplifier is given by

$$\begin{aligned} \overline{I_{n,in}^2} &= 4kT\gamma g_{m1} + \frac{4kT\gamma g_{m2}}{k^2} \\ &= 4kT\gamma g_{m1}(1 + \frac{1}{k}) \end{aligned} \tag{2.15}$$

where γ equals 2/3 for long-channel transistors and may be larger for submicron MOSFET [26]. If $k \gg 1$, the noise from M_2 can be neglected.

It is seen that a low input impedance requires both a large biasing current and a large input transistor. To achieve a high current gain, both the biasing current and the transistor size at the output branch becomes extremely large, resulting in high power dissipation and large parasitic capacitances (maybe comparable to the photodiode capacitance). The performance of current-mode circuits deteriorates due to mismatches, and their dynamic range is limited by the biasing current. In the following chapters,

we will give an in-depth analysis on CMOS current-mode circuits, and introduce several new topologies and design strategies to improve the performance of those circuits.

Chapter 3

Comparative Study of Low-Voltage CMOS Current-Mode Circuits

Current mirrors are the building blocks of CMOS current-mode circuits [4]. Due to the significantly lowered supply voltage by advance technology, the performance of many effective current-mode circuits, such as cascode [27] and class-AB current mirrors [28], is affected severely.

This chapter presents a comparative study of the characteristics of low-voltage CMOS current-mode circuits for optical communications both analytically and quantitatively. It examines design issues including input impedance, bandwidth, dynamic range, and noise performance for low-voltage CMOS current-mode circuits. A new current mirror with current feedback to lower the input impedance and increase the bandwidth is proposed (more discussions on this configuration are given in Section 4.3). The performance of these current mirrors is assessed using Cadence Spectre and the results are presented.

3.1 Input Impedance

Low input impedance is essential for optical preamplifiers because the parasitic capacitance of photodiodes is usually much larger than the input capacitance of preamplifiers. As a result, the dominant pole of optical preamplifiers is usually determined by the par-

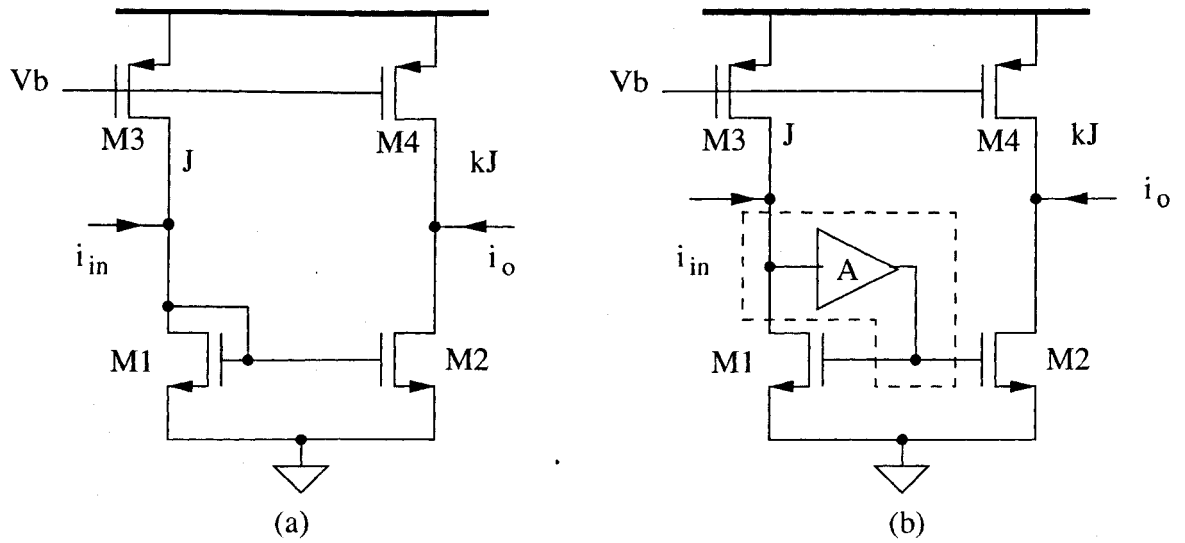

Figure 3.1: (a) Basic current mirror (BASIC); (b) Low input-impedance current mirror (LI-IMP)

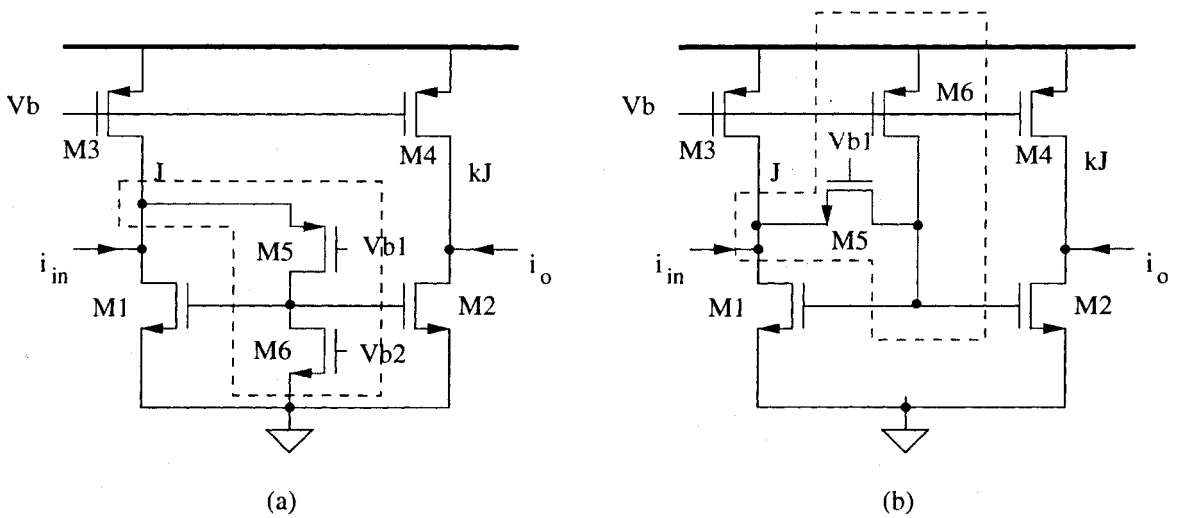

Figure 3.2: Current mirrors with common-gate feedback (CGFB)

asitic capacitance of photodiodes and the input resistance of preamplifiers. The *basic current mirror* shown in Fig. 3.1(a) has the input impedance of

$$R_{in} = \frac{1}{g_{m1} + (1/r_{o1})} \approx \frac{1}{g_{m1}}, \tag{3.1}$$

where g_m is the transconductance and r_o is the output resistance of the MOS transistors.

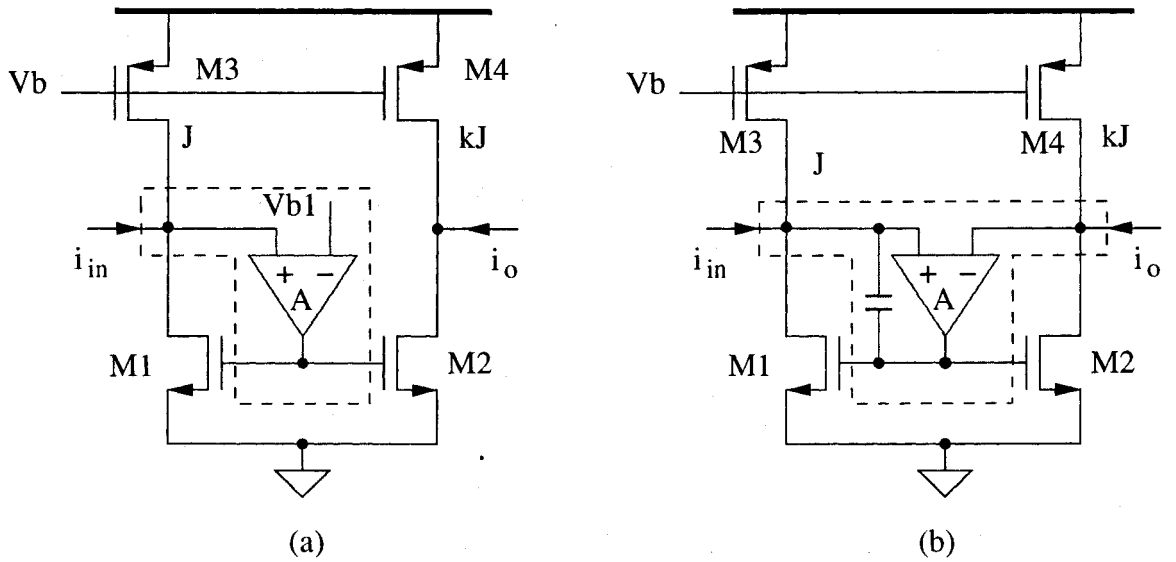

Figure 3.3: (a) Mirror with active feedback (ACTIVE). (b) Bootstrapped current mirror (BSTRP)

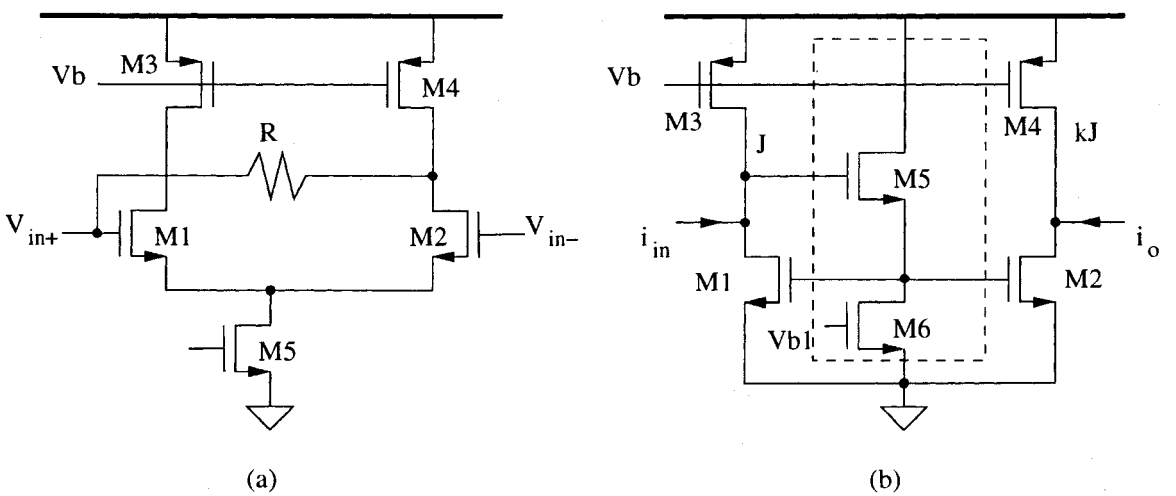

Figure 3.4: (a) Auxiliary differential-input single-output Opamp. (b) High bandwidth current mirror (HBW)

The input impedance can be reduced by inserting a voltage amplifier between the drain and gate of M1, as shown in Fig. 3.1(b), leading to the *low input-impedance current mirror*. The input impedance of the LI-IMP mirror at low frequencies is given by

$$R_{in} = \frac{1}{Ag_{m1} + (1/r_{o1})} \approx \frac{1}{Ag_{m1}}. \tag{3.2}$$

The voltage amplifier can be implemented using common-gate configuration to take the advantage of its immunity from Miller effect, as shown in Fig. 3.2. It can be shown that the input impedance of the CGFB mirrors at low frequencies is approximately given by

$$R_{in} \approx \frac{1}{g_{m1}(r_{o6}g_{m5})}, \tag{3.3}$$

much smaller as compared with that of the basic mirror.

The amplifier can also be differentially configured as shown in Fig. 3.3(a) [29]. To achieve both a low input impedance and a high output impedance, the bootstrapped CMOS current mirror proposed in [30] and shown in Fig. 3.3(b) can be used. This configuration, however, suffers from poor stability at high frequencies. A compensation capacitor is needed as shown and the mirror becomes the basic mirror at high frequencies. The implementation of the auxiliary differential amplifier is shown in Fig. 3.4(a) with bandwidth approximately 692MHz. A drawback of the differential amplifier approach is that it requires a higher supply voltage.

Table 3.1: Input and output impedances at low frequencies
(the output impedance of biasing current source is assumed to be infinite)

Mirror	Input Impedance	Output Impedance
BASIC	$1/g_{m1}$	$r_{o2}\|\|r_{o4}$
CGFB	$1/(r_{o6}g_{m5}g_{m1})$	$r_{o2}\|\|r_{o4}$
HBW	$1/g_{m1}$	$r_{o2}\|\|r_{o4}$
RES	$1/g_{m1}$	$r_{o2}\|\|r_{o4}$
ACTIVE	$1/(Ag_{m1})$	$r_{o2}\|\|r_{o4}$
BSTRP	$1/(Ag_{m1})$	$(Ag_{m1}r_{o1})r_{o2}$
CFB	$1/[g_{m1}(1+k\beta)]$	$r_{o2}\|\|r_{o4}$

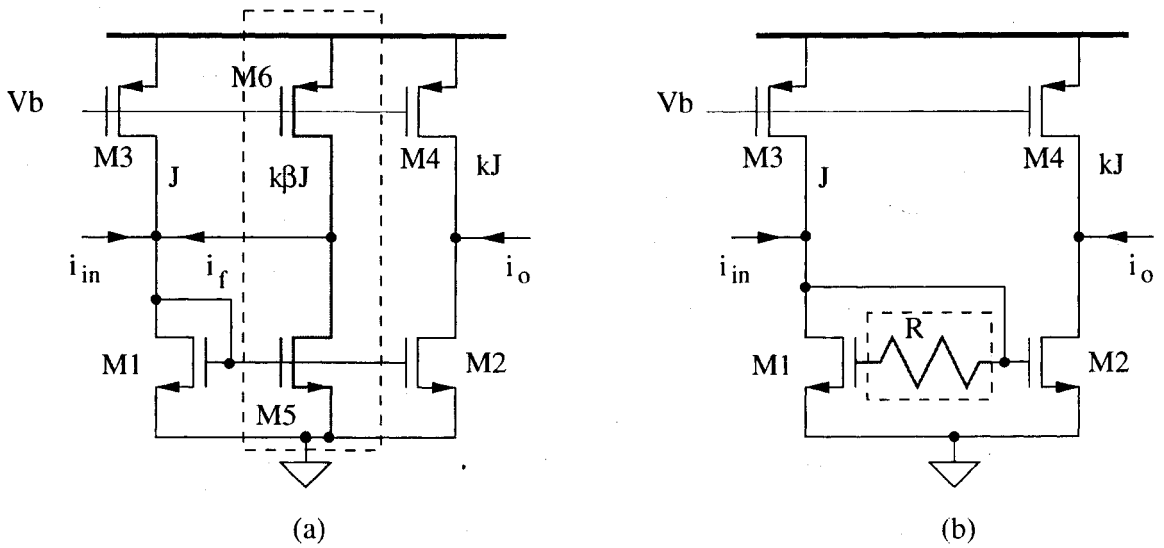

Figure 3.5: (a) Current mirror with current feedback (CCFB). (b) Current mirror with resistor (RES)

It is well known that current-current feedback is capable of reducing input impedance and increasing bandwidth. To sample the output current without adding more elements between V_{DD} and ground, an additional branch is added in parallel with the output transistor to sample the output current. The sampled output current is then fed back to the input, as shown in Fig. 3.5(a). It can be shown that the input impedance of the CCFB mirror is given by

$$R_{in} = \frac{1}{g_{m1}(1 + k\beta)}, \tag{3.4}$$

where k and β are the gain of the forward and feedback paths respectively.

The input and output impedance of the mirrors are tabulated in Table 3.1. To quantify the input characteristics, these mirrors were implemented using TSMC 0.18μ CMOS technology with circuit parameters given in Table 3.2, and simulated using Spectre with BSIM3v3 device models. The amplifier in LI-IMP current mirror is implemented using an ideal VCVS with gain of 5. The results are plotted in Fig. 3.6. The impedance of the

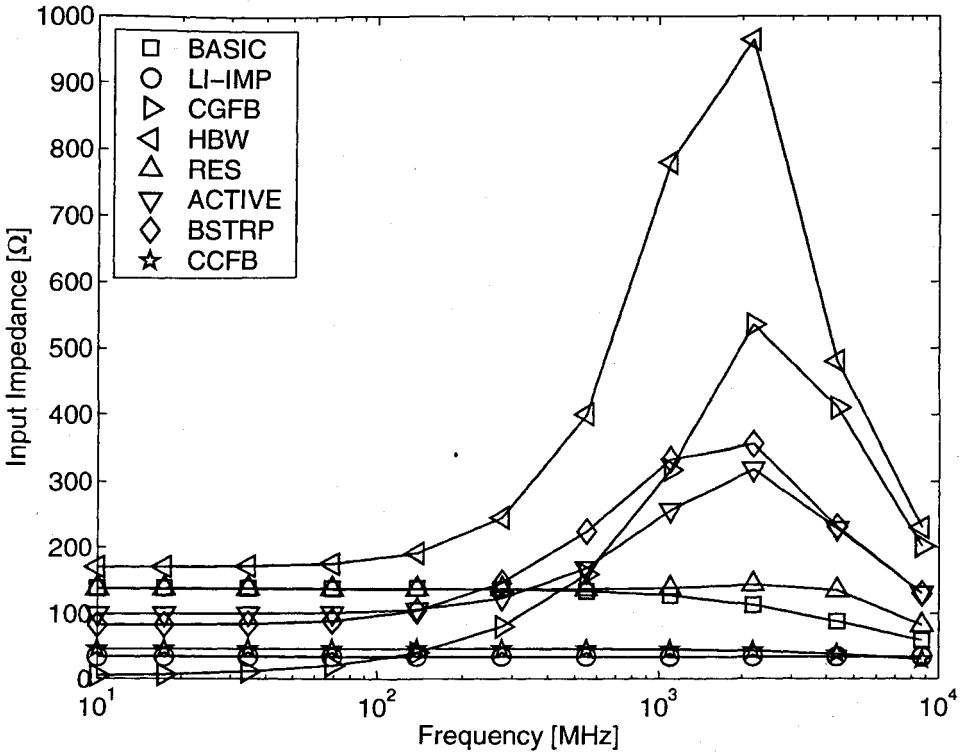

Figure 3.6: Input impedance

Table 3.2: Channel width (μm) of devices
($L_{min} = 0.18\mu$m is used for all devices)

Mirror	M1	M2	M3	M4	M5	M6
BASIC	25	100	25	100		
CGFB	25	100	25	100	40	
HBW	25	100	25	100	20	
RES	25	100	25	100		
ACTIVE	25	100	25	100		
BSTRP	25	100	25	100		
CFB	25	100	25	100	50	50
Opamp	2	2	2	2		

basic mirror at low frequencies is 137Ω. LI-IMP mirror gives a lower and constant input impedance of 35Ω. The input impedance of CCFB mirror is 46Ω and decreases with frequency. CGFB mirror provides the lowest input impedance at low frequencies only.

At high frequencies the input impedance of CGFB, HBW, active and bootstrapped mirrors is significantly high, revealing that they are not suitable for optical communications where signal frequency is in the range of GHz.

3.2 Bandwidth

The bandwidth of the basic mirror is given by

$$\omega_{-3dB} = \frac{g_{m1}}{C_{gs1} + C_{gs2}}. \tag{3.5}$$

It can be adjusted by changing the bias current. The bandwidth of CGFB mirror can be obtained from its transfer function

$$\frac{I_o(s)}{I_{in}(s)} = \frac{\dfrac{g_{m2}g_{m5}}{C_{gs5}(C_{gs1} + C_{gs2})}}{s^2 + s\dfrac{g_{m5}}{C_{gs5}} + \dfrac{g_{m1}g_{m5}}{C_{gs5}(C_{gs1} + C_{gs2})}}. \tag{3.6}$$

with the poles located at

$$p_{1,2} = \frac{g_{m5}}{2C_{gs5}}\Big[-1 \pm \sqrt{1 - 4\Big(\frac{g_{m1}}{C_{gs1} + C_{gs2}}\Big)\Big(\frac{C_{gs5}}{g_{m5}}\Big)}\Big]. \tag{3.7}$$

It is seen that under the condition $\dfrac{g_{m1}}{C_{gs1} + C_{gs2}} = \dfrac{1}{4}\Big(\dfrac{g_{m5}}{C_{gs5}}\Big)$, the circuit has two identical real poles. The bandwidth is given by $\omega_{-3dB} = \dfrac{g_{m5}}{2C_{gs5}}$, approximately 2 times that of the basic current mirror.

The mirror shown in Fig. 3.4(b) is derived from [31] and is called the *high-bandwidth current mirror*. The source follower is employed to suppress the capacitance at the input node. From the transfer function

$$\frac{I_o(s)}{I_{in}(s)} = \frac{\frac{g_{m2}g_{m5}}{C_{gs5}(C_{gs1}+C_{gs2})}\left(s\frac{C_{gs5}}{g_{m5}}+1\right)}{s^2 + s\frac{g_{m1}}{C_{gs1}+C_{gs2}} + \frac{g_{m1}g_{m5}}{C_{gs5}(C_{gs1}+C_{gs2})}}, \tag{3.8}$$

we obtain the two poles

$$p_{1,2} = \frac{g_{m1}}{2(C_{gs1}+C_{gs2})}\Big[-1 \pm \sqrt{1 - 4\Big(\frac{g_{m5}}{C_{gs5}}\Big)\Big(\frac{C_{gs1}+C_{gs2}}{g_{m1}}\Big)}\Big]. \tag{3.9}$$

Under the condition $\frac{g_{m1}}{C_{gs1}+C_{gs2}} = \frac{1}{4}\Big(\frac{g_{m5}}{C_{gs5}}\Big)$, two identical real poles are obtained. It is seen that the added transistor M5 introduces a zero and does not affect the real part of the poles. The bandwidth is given by $\omega_{-3dB} = \frac{g_{m1}}{2(C_{gs1}+C_{gs2})}$ approximately, only half of the bandwidth of the basic mirror.

To avoid using active devices at the input, which may cause unwanted oscillation, a resistor can be inserted between the gates of the input and output transistors, as shown in Fig. 3.5(b) [32]. With the transfer function given by

$$\frac{I_o(s)}{I_{in}(s)} = \frac{g_{m2}(sRC_{gs1}+1)}{RC_{gs1}C_{gs2}\Big(s^2 + s\frac{C_{gs1}+C_{gs2}}{RC_{gs1}C_{gs2}} + \frac{g_{m1}}{RC_{gs1}C_{gs2}}\Big)}, \tag{3.10}$$

it can be shown that when $R = \frac{1}{g_{m1}}$, the zero and one of the poles cancel out, resulting in a first-order system with the pole at $s = -\frac{1}{RC_{gs2}}$. The bandwidth of the circuit is much larger in this case. Further analysis in Section 3.4, however, reveals that the resistor increases the output noise of the circuit significantly. To increase the bandwidth without employing noisy resistors, CCFB mirror can be used. The current gain of the CCFB mirror is given by

$$\frac{I_o(s)}{I_{in}(s)} = \frac{\frac{g_{m2}}{g_{m1}(1+k\beta)}}{s\Big[\frac{C_{gs1}+C_{gs2}+C_{gs5}}{g_{m1}(1+k\beta)}\Big]+1}, \tag{3.11}$$

from which we obtain the bandwidth

$$\omega_{-3dB} = \left(\frac{g_{m1}}{C_{gs1} + C_{gs2} + C_{gs5}}\right)(1 + k\beta). \tag{3.12}$$

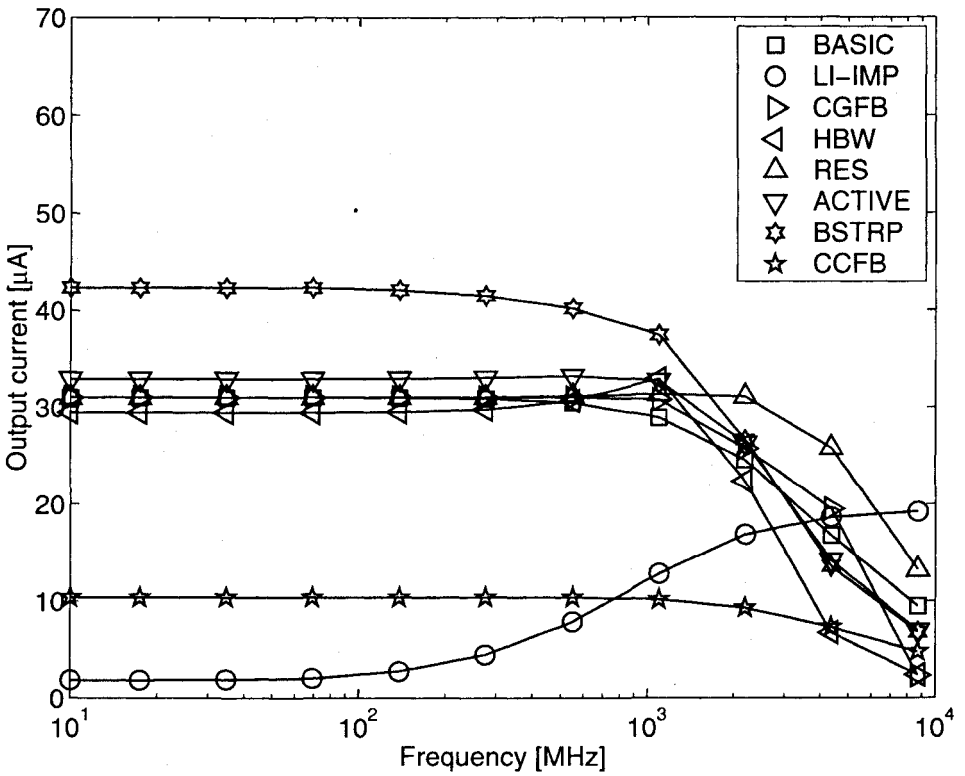

Figure 3.7: Output current
(with $I_{in} = 10\mu$A)

It is seen that the bandwidth is increased by a factor of $(1 + k\beta)$ approximately. The bandwidth of the active and bootstrapped current mirrors is the same as that of the basic mirror because the bandwidth of the differential amplifier is smaller. Fig. 3.7 shows the output current of these mirrors. The basic mirror has bandwidth of 2.7 GHz. The bandwidth of the mirror with common-gate feedback provides bandwidth of 2.65 GHz. The bandwidth of HBW-mirror is approximately 2.3 GHz. The bandwidth of the mirror with a 1kΩ resistor is approximately 5.43 GHz. The values of k and β of the

mirror with CCFB are 4 and 0.5, respectively. Simulation results show that the CCFB mirror has the bandwidth of 4.3 GHz.

3.3 Dynamic Range

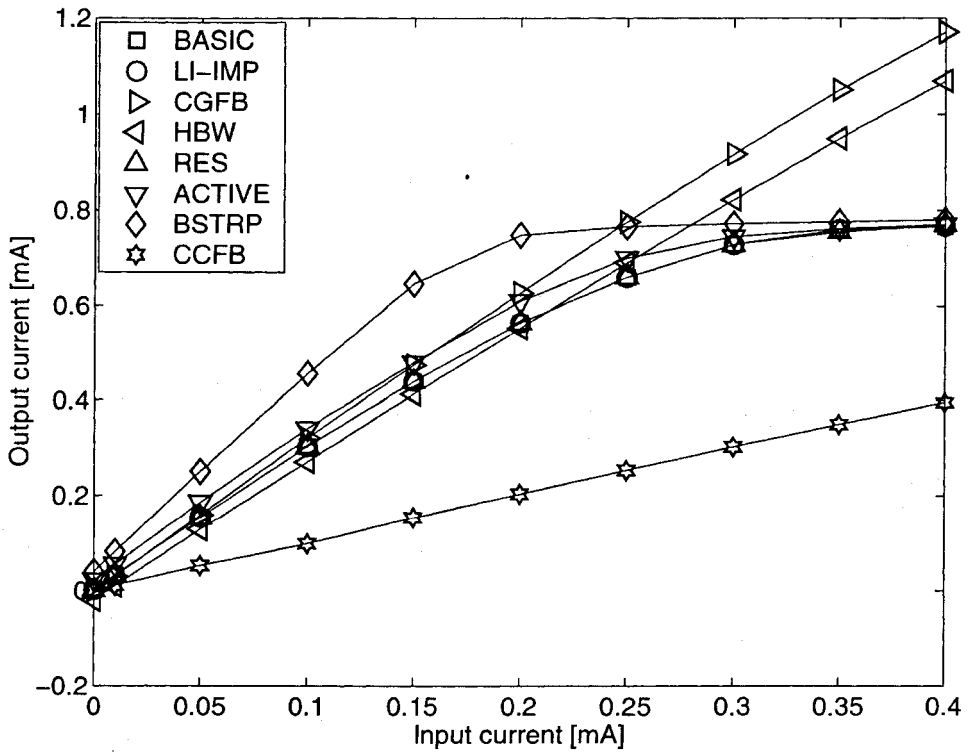

Figure 3.8: Dynamic range
($J = 0.73$ mA, $kJ = 2.9$ mA),
(the plots of CGFB and HBW are shifted down by 0.6mA for comparison)

The dynamic range of the current mirrors are examined by varying the input current from 0 to 0.4 mA (55% of J) and measuring the corresponding output current. Active current mirrors are used as the output loads. The results are plotted in Fig. 3.8. It is seen that the dynamic range of BASIC current mirror is about 27%J. CCFB current mirror provides the largest dynamic range while bootstrapped current mirror has the smallest dynamic range.

3.4 Noise

Using small-signal analysis, the power of the input-referred noise voltage generator $\overline{v_n^2}$ and that of the input-referred noise current generator $\overline{i_n^2}$ of the current mirrors are derived and tabulated in Table 3.3. It is seen that (i) if the current gain of the mirror is large, both the contribution of the noise of M2 and the input-referred voltage noise generator are negligible. (ii) The effect of the noise of the feedback transistor M5 in both HBW and CGFB mirrors is marginal. (iii) The noise of the mirror with a compensation resistor is significantly larger as compared with that of other mirrors. (iv) The input-referred noise of CCFB mirror is higher than that of the basic current mirror due to the reduction of the current gain and the noise of the feedback device.

Table 3.3: Input-referred noise generators

Mirror	$\overline{i_n^2}$	$\overline{v_n^2}$
BASIC	$\overline{i_{n1}^2} + \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{i_{n2}^2}$	$\frac{\overline{i_{n2}^2}}{g_{m2}^2}$
CGFB	$\overline{i_{n1}^2} + \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{i_{n2}^2}$	≈ 0
HBW	$\overline{i_{n1}^2} + \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{i_{n2}^2} + \left(\frac{g_{m1}}{g_{m5}}\right)^2 \overline{i_{n5}^2}$	$\frac{\overline{i_{n1}^2}}{g_{m1}^2} + \frac{\overline{i_{n2}^2}}{g_{m2}^2}$
RES	$\overline{i_{n1}^2} + \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{i_{n2}^2} + (g_{m1}R)^2 \overline{i_{nR}^2}$	$\frac{\overline{i_{n2}^2}}{g_{m2}^2}$
ACTIVE	$\overline{i_{n1}^2} + \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{i_{n2}^2}$	$\overline{\hat{v}_n^2} + \frac{\overline{i_{n2}^2}}{Ag_{m2}^2}$
BSTRP	$\overline{i_{n1}^2} + \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{i_{n2}^2}$	$\overline{\hat{v}_n^2} + \frac{\overline{i_{n2}^2}}{Ag_{m2}^2}$
CCFB	$\overline{i_{n1}^2} + \left[\frac{g_{m1}^2(1+k\beta)^2}{g_{m2}^2}\right] \overline{i_{n2}^2} + \overline{i_{n5}^2}$	$\frac{\overline{i_{n2}^2}}{g_{m2}^2}$

3.5 Summary

An in-depth investigation of the small and large-signal characteristics of low-voltage CMOS current mirrors has been presented. The ideal LI-IMP current mirror effectively lowers the input impedance. Practical implementation of LI-IMP current mirror, however, suffers from large input impedances at high frequencies. CCFB and RES current mirrors provide low and monotonically decreasing input impedances. Among the current mirrors investigated, only CCFB and RES give significant improvement in bandwidth. BASIC, CGFB, and HBW current mirrors offer low noise. RES has the highest noise, mainly due to the thermal noise of the added resistor. The noise of CCFB is higher than that of BASIC due to its reduced current gain. CCFB current mirror provides the largest dynamic range whereas bootstrapped current mirror has the lowest dynamic range.

Chapter 4

New Bandwidth Enhancement Techniques for CMOS Current-Mode Circuits

This chapter introduces two new bandwidth enhancement techniques, namely inductor series-peaking and negative current feedback, for low-voltage CMOS current-mode circuits.

Although inductors are commonly associated with narrow-band RF circuits, they are useful in broad-band circuits as well. The proposed inductor series-peaking technique boosts the bandwidth by utilizing the resonance characteristics of LC network formed by placing an inductor in series with the capacitor constituting the dominant pole. Two configurations are investigated. In the first configuration where the dominant pole is due to the gate-source capacitance of the output branch of current-mirror amplifiers. The peaking inductor is added between the gates of the input and output transistors. In the second configuration, the current amplifier is used as a pre-amplification stage of optical receivers. In this case, the parasitic capacitance of the photo diode and that of the packaging of the chip constitute the dominant pole. The peaking inductor is placed at the input node of the amplifier. Both the bond wire inductance and on-chip spiral inductance can be used to realize this inductor.

The current feedback increases the bandwidth by taking the advantage of negative feedback theory. A new sampling mechanism is introduced to acquire the feedback current. The employment of both the inductive peaking and current feedback further increases the bandwidth. Another notable advantage of the current feedback is that it significantly reduces the value of the peaking inductor, which is not only area-greedy but also has a strong interaction with the substrate. Both the inductor series-peaking and the current feedback techniques do not affect the supply voltage and DC biasing conditions.

Before introducing the new techniques, we begin with a brief review of two existing bandwidth enhancement techniques. The first is inductive shunt-peaking technique for voltage-mode circuits, and the second is resistive-compensation technique for current-mode circuits.

4.1 Inductive Shunt-Peaking and Resistive Compensation

Both inductive shunt-peaking and resistive-compensation techniques enhance the bandwidth by creating a zero to compensate the dominant pole.

As shown in Fig. 4.1, neglecting the parasitic capacitances, the transfer function of this simple common-source voltage amplifier (with $L = 0$) is given by

$$\frac{V_o(s)}{V_{in}(s)} = \frac{g_m R}{1 + sRC}. \tag{4.1}$$

The bandwidth is determined by a single dominant pole, which is determined by the output load resistance R and load capacitance C.

The inductive shunt-peaking technique introduces an inductor L in series with the load resistance and in parallel with the load capacitance. The transfer function is given

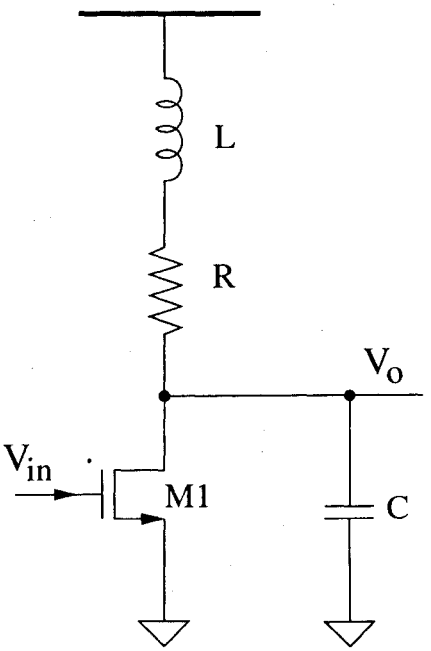

Figure 4.1: Inductive shunt-peaking technique

by

$$\frac{V_o(s)}{V_{in}(s)} = \frac{g_m(R + sL)}{1 + sRC - s^2LC}. \tag{4.2}$$

The zero is solely determined by the L/R time constant and is primarily responsible for the bandwidth enhancement. The frequency response of this shunt peaked amplifier is characterized by the ratio of the L/R and RC constants [33]. This technique, however, is not particularly applicable to current-mode circuits, mainly due to the existence of high-impedance biasing current sources between AC ground and the dominant pole, and it will create mismatch problems (see Section 5.3) if the inductor is placed in series with the current source.

The resistive-compensation technique was introduced in [32] [34] to enhance the bandwidth of current mirrors. The basic current mirror is a single-pole system. The resistive-compensation generates an additional pole and a compensating zero by inserting

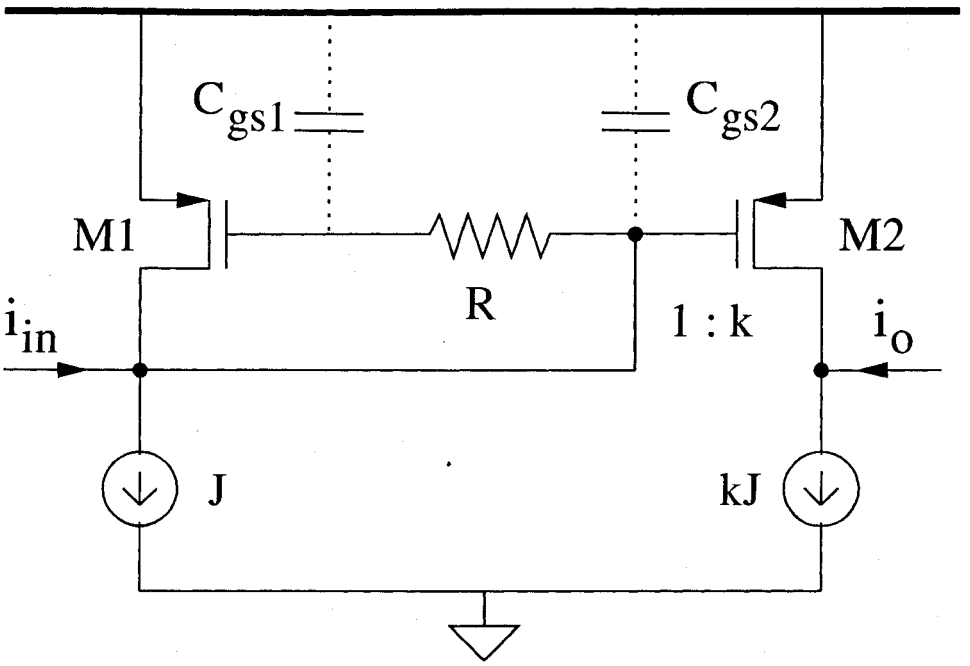

Figure 4.2: Resistive compensation technique

a passive resistor between the gates of the input and output transistors, as shown in Fig. 4.2. The transfer function is given by

$$\frac{I_o(s)}{I_{in}(s)} = \left(\frac{g_{m2}}{C_{gs2}}\right) \frac{s + \dfrac{1}{RC_{gs1}}}{s^2 + \dfrac{C_{gs1} + C_{gs2}}{RC_{gs1}C_{gs2}} + \dfrac{g_{m1}}{RC_{gs1}C_{gs2}}}. \tag{4.3}$$

For the compensated current mirror, the frequency response is characterized by the value of resistor R. The effectiveness of compensation is somewhat uncertain due to the inaccurate CMOS resistors. Additionally, as revealed in Section 3.4 that the thermal noise of the added resistor deteriorates the noise performance because its noise is directly referred to the input. For applications such as preamplifiers of data transceivers, noiseless elements that provides comparable bandwidth enhancement are preferred.

4.2 Inductor Series-Peaking

4.2.1 Current-Mirror Amplifiers

It is commonly said that the current-mode circuits possess large bandwidth [4] [3]. A main drawback of these circuits is their low current gain. To increase the current gain, the size of the transistor in the output branch of current-mirror amplifiers can be made large, however, at the expense of bandwidth.

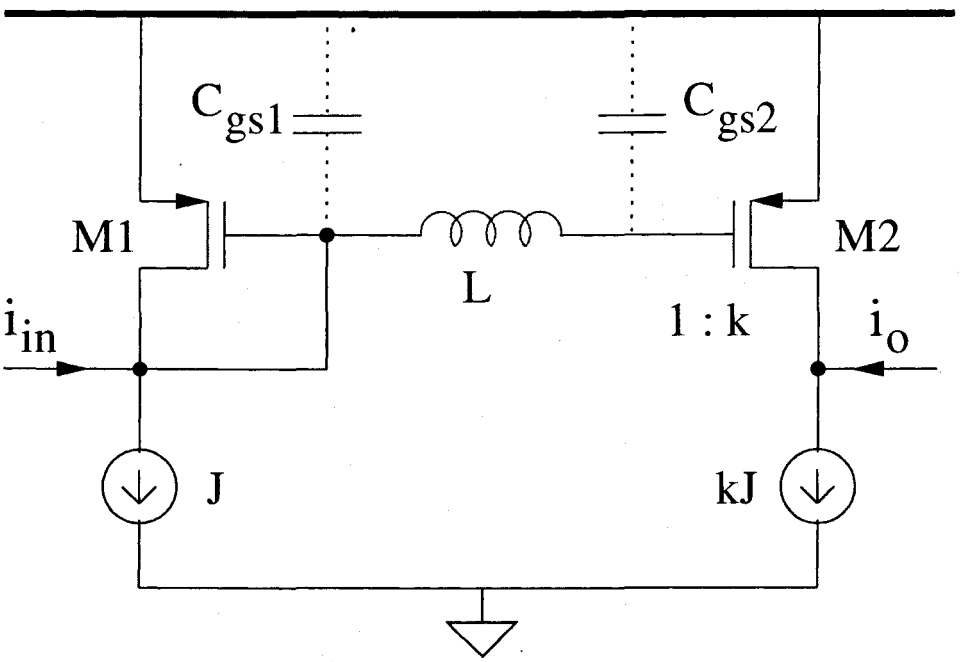

Figure 4.3: Current-mirror amplifier with series-peaking inductor
($J = 0.5$mA, $W_1 = 10\mu$m, $W_2 = 100\mu$m)

Neglecting the parasitic gate-drain capacitances, the basic current-mirror amplifier shown in Fig. 4.3 (with $L = 0$) has the first-order transfer function

$$\frac{I_o(s)}{I_{in}(s)} = \left(\frac{g_{m2}}{g_{m1}}\right) \frac{1}{s\dfrac{C_{gs1}+C_{gs2}}{g_{m1}} + 1}, \tag{4.4}$$

with bandwidth

$$\omega_o = \frac{g_{m1}}{C_{gs1} + C_{gs2}}, \tag{4.5}$$

where g_m is the transconductance and C_{gs} is the gate-source capacitance of transistors. Because the current gain $k = \frac{(W/L)_2}{(W/L)_1}$ is usually large, $C_{gs2} \gg C_{gs1}$ and dominates the frequency response. The bandwidth is therefore given by $\omega_o \approx \frac{g_{m1}}{C_{gs2}}$. To quantify the bandwidth, the amplifier is implemented in TSMC's 0.18μm 1.8V CMOS technology and analyzed using Spectre from Cadence Design Systems with BSIM3V3 device models. Simulation results with the circuit parameters given in Table 4.2 are shown in Fig. 4.11.

Because the dominant pole of CMOS current-mirror amplifiers is attributed to the gate-source capacitance of the output transistor, a compensation inductor L can therefore be placed between the gates of the input and output transistors and is in series with C_{gs2}, as shown in Fig.4.3. Note that the added inductor has no effect on the DC characteristics. The amplifier has a third-order transfer function

$$\frac{I_o(s)}{I_{in}(s)} = \left(\frac{g_{m2}}{g_{m1}}\right) \frac{1}{s^3 \frac{LC_{gs1}C_{gs2}}{g_{m1}} + s^2 LC_{gs2} + s\frac{C_{gs1} + C_{gs2}}{g_{m1}} + 1}. \tag{4.6}$$

With the assumption $C_{gs2} \gg C_{gs1}$, the transfer function is simplified to

$$\frac{I_o(s)}{I_{in}(s)} \approx \left(\frac{g_{m2}}{g_{m1}}\right) \frac{\frac{1}{LC_{gs2}}}{s^2 + s\frac{1}{g_{m1}L} + \frac{1}{LC_{gs2}}}, \tag{4.7}$$

with the poles given by

$$p_{1,2} = \frac{-1 \pm \sqrt{1 - \frac{4g_{m1}^2 L}{C_{gs2}}}}{2g_{m1}L}. \tag{4.8}$$

From the control theory, the transfer function of a stable, zeroless, second-order system can be expressed as

$$H(s) = \tilde{H}\frac{{\omega_n}^2}{s^2 + 2\xi\omega_n s + {\omega_n}^2}, \tag{4.9}$$

where $\tilde{H}$ is the DC gain, ω_0 is the undamped natural frequency, and ξ is the damping ratio. Three distinct cases are defined:

- the *under-damped* case, when $0 < \xi < 1$,
- the *critically damped* case, when $\xi = 1$, and
- the *over-damped* case, when $1 < \xi < \infty$.

Table 4.1: Damping characteristics

L	Poles	Damping characteristics	Response
$L < \frac{C_{gs2}}{4g_{m1}^2}$	Two distinct negative real poles	Over-damped	1) Small bandwidth 2) Large rise time 3) No ringing
$L = \frac{C_{gs2}}{4g_{m1}^2}$	Two identical negative real poles	Critically damped	1) Large bandwidth 2) Small rise time 3) No ringing
$L > \frac{C_{gs2}}{4g_{m1}^2}$	Complex conjugate poles with negative real part	Under-damped	1) Large bandwidth 2) Small rise time 3) Ringing

For the current-mirror amplifier, the damping ratio $\xi = \sqrt{\frac{C_{gs2}}{4g_{m1}^2 L}}$. It is seen that the characteristics of the current-mirror amplifier depend upon the value of the peaking

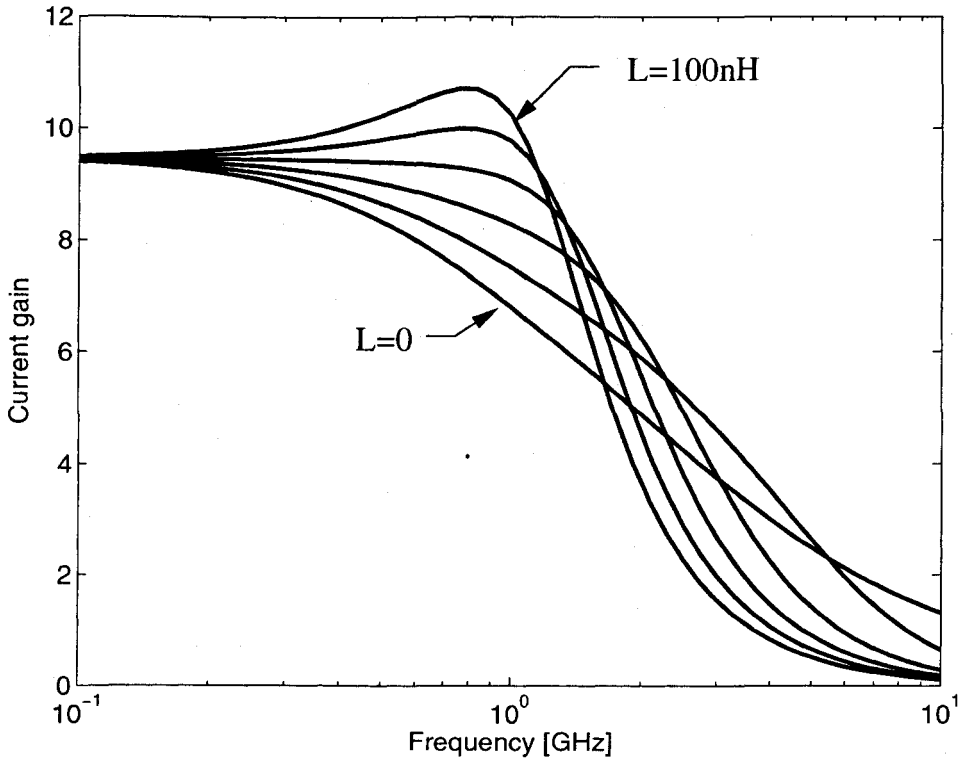

Figure 4.4: The effect of the peaking inductor on the bandwidth of current-mirror amplifier ($\beta = 0, L$ is varied from 0 to 100 nH with step 20 nH)

inductor, as detailed in Table 4.1. To maximize the bandwidth and avoid ringing in time-domain response, the peaking inductor is sized based on the criterion of the critical damping where

$$L = \frac{C_{gs2}}{4g^2{}_{m1}L}. \tag{4.10}$$

The amplifier in this case has the bandwidth of

$$\omega_o = \frac{2g_{m1}}{C_{gs2}}, \tag{4.11}$$

It is nearly twice that of the basic current-mirror amplifier. Simulation results with the circuit parameters given in Table 4.2 demonstrate that the inductor series-peaking

technique increases the bandwidth of the circuit from 1.6 GHz ($L = 0$) to 2.7 GHz ($L = 60nH$), as shown in Fig.4.11. Fig. 4.4 shows the effect of the value of the peaking inductor on the bandwidth of the amplifier. It is seen that the critical damping occurs at $L \approx 60$nH.

4.2.2 Optical Preamplifiers

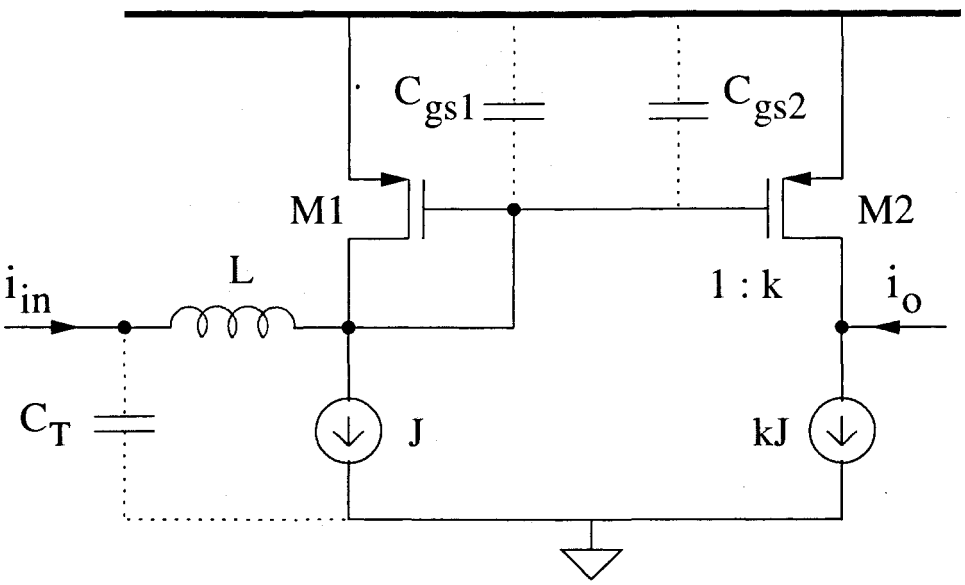

Figure 4.5: Optical preamplifier with series-peaking inductor
($J = 0.5$mA, $W_1 = 10\mu$m, $W_2 = 100\mu$m, $C_T = 0.5$pF)

In the preceding analysis, the parasitic input capacitance is neglected and the gate-source capacitance of the output transistor is assumed to constitute the dominant pole. However, in the design of preamplifiers for optical communications, due to the large parasitic capacitance of the photodiode and that of bonding pads of the chip, the input parasitic capacitance is usually much larger than the capacitance of the transistors. Fig. 4.5 shows a primitive current-mode preamplifier for optical communications ($L = 0$), where C_T equals the total parasitic capacitance of the photodiode and the packaging. The transfer function of the preamplifier is given by

$$\frac{I_o(s)}{I_{in}(s)} = \left(\frac{g_{m2}}{g_{m1}}\right) \frac{1}{s\dfrac{C_T + C_{gs}}{g_{m1}} + 1}, \tag{4.12}$$

with bandwidth

$$\omega_o = \frac{g_{m1}}{C_T + C_{gs}}, \tag{4.13}$$

where $C_{gs} = C_{gs1} + C_{gs2}$. Assuming $C_T \gg C_{gs}$, the bandwidth is given by $\omega_o \approx \dfrac{g_{m1}}{C_T}$. As shown in Fig. 4.12, the bandwidth of the preamplifier with $C_T = 0.5$ pF is only 0.45 GHz. To implement the series-peaking technique, the peaking inductor is placed at the input node of the preamplifier, as shown in Fig. 4.5. Both the bond wire inductance and on-chip spiral inductors can be used to realize this inductor. The preamplifier with the peaking inductor has a third-order transfer function

$$\frac{I_o(s)}{I_{in}(s)} = \left(\frac{g_{m2}}{g_{m1}}\right) \frac{1}{s^3\dfrac{LC_{gs}C_T}{g_{m1}} + s^2 LC_T + s\dfrac{C_{gs} + C_T}{g_{m1}} + 1}. \tag{4.14}$$

With the assumption $C_T \gg C_{gs}$, it can be simplified to a second-order function

$$\frac{I_o(s)}{I_{in}(s)} \approx \left(\frac{g_{m2}}{g_{m1}}\right) \frac{\dfrac{1}{LC_T}}{s^2 + s\dfrac{1}{g_{m1}L} + \dfrac{1}{LC_T}}, \tag{4.15}$$

with a pair of poles

$$p_{1,2} = \frac{-1 \pm \sqrt{1 - \dfrac{4g_{m1}^2 L}{C_T}}}{2g_{m1}L}, \tag{4.16}$$

These equations are similar to those of the current-mirror amplifier with a series peaking inductor. In the critically damped case where

$$L = \frac{C_T}{4g_{m1}^2}, \tag{4.17}$$

the circuit has the bandwidth of

$$\omega_o = \frac{2g_{m1}}{C_T}, \tag{4.18}$$

which is twice that of the basic preamplifier. Simulation results demonstrate that the inductor series-peaking technique increases the bandwidth of the preamplifier from 0.45 GHz ($L = 0$) to 1.0 GHz ($L = 100$ nH), as shown in Fig. 4.12. It should be noted that since the value of bond wire inductance is limited [33], a large on-chip spiral inductor is needed. On-chip inductors are very area consuming. Inductors greater than 100 nH are rarely used in practice [35].

4.3 Negative Current Feedback

It is well known that negative current-current feedback lowers the input impedance, improves the dynamic range, and boosts the bandwidth, however, at the expense of current gain.

Conventionally, current-current feedback is a series-shunt feedback which means that the feedback current is acquired in series with the output current [26]. As mentioned in Section 3.2, to sample the output current without affecting both the DC biasing condition and the supply voltage, we introduce a new current feedback mechanism shown in Fig. 4.6. In the basic current-mirror amplifier, the feedback transistor M_f is simply a diode-connected mirror of the input transistor M_1. It can be shown that the transfer function is given by

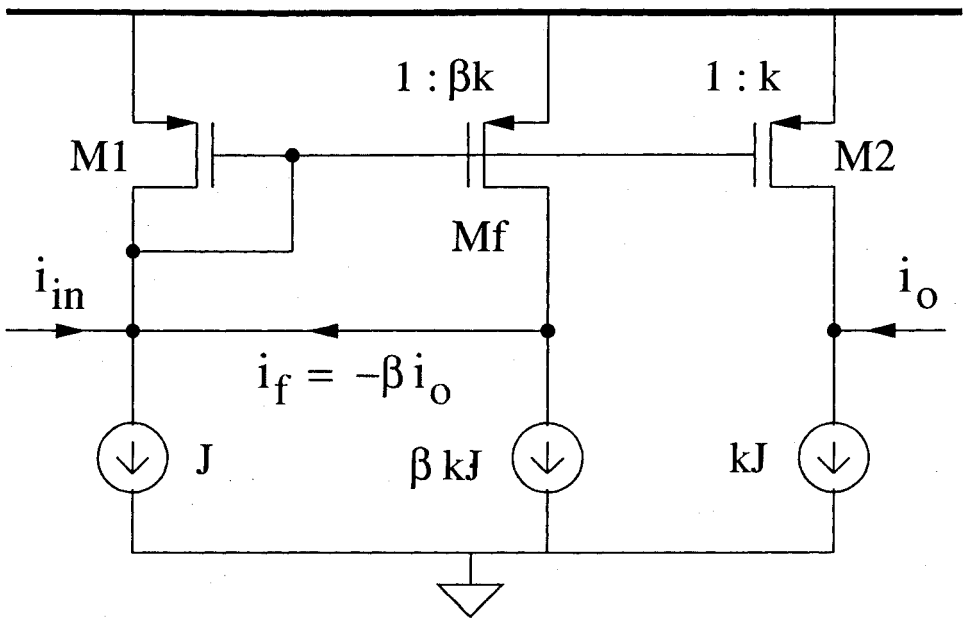

Figure 4.6: Current-mirror amplifier with current feedback
($J = 0.5$mA, $W_1 = 10\mu$m, $W_2 = 100\mu$m, $W_f = 10\mu$m)

$$\frac{I_o(s)}{I_{in}(s)} = \left[\frac{g_{m2}}{g_{m1}(1+k\beta)}\right] \frac{1}{s\frac{C_{gs1}+C_{gs2}+C_{gsf}}{g_{m1}(1+k\beta)}+1}, \tag{4.19}$$

with bandwidth

$$\begin{aligned} \omega_o &= \frac{g_{m1}}{C_{gs1}+C_{gs2}+C_{gsf}}(1+k\beta) \\ &\approx \frac{g_{m1}}{C_{gs2}}(1+k\beta) \end{aligned} \tag{4.20}$$

where $C_{gs2} \gg C_{gs1}, C_{gsf}$ was assumed. It is seen that the feedback increases the bandwidth by the factor $(1+k\beta)$. Two notable advantages of this configuration are (i) the feedback gain can be adjusted independent of that of the forward path, and (ii) no increase in the minimum supply voltage, which is given by $V_T + V_{sat}$, where $V_{T,n} = |V_{T,p}| = V_T$ is the threshold voltage and V_{sat} is the pinch-off voltage. Simulation results with $\beta = 0.1$ are shown in Fig. 4.11. It is seen that the feedback boosts the bandwidth from 1.6 GHz

to 2.8 GHz. It should be noted that the feedback also decreases the current gain by the same factor $(1 + k\beta)$, and the feedback has no effect on the output impedance because it sample the output current in different branch.

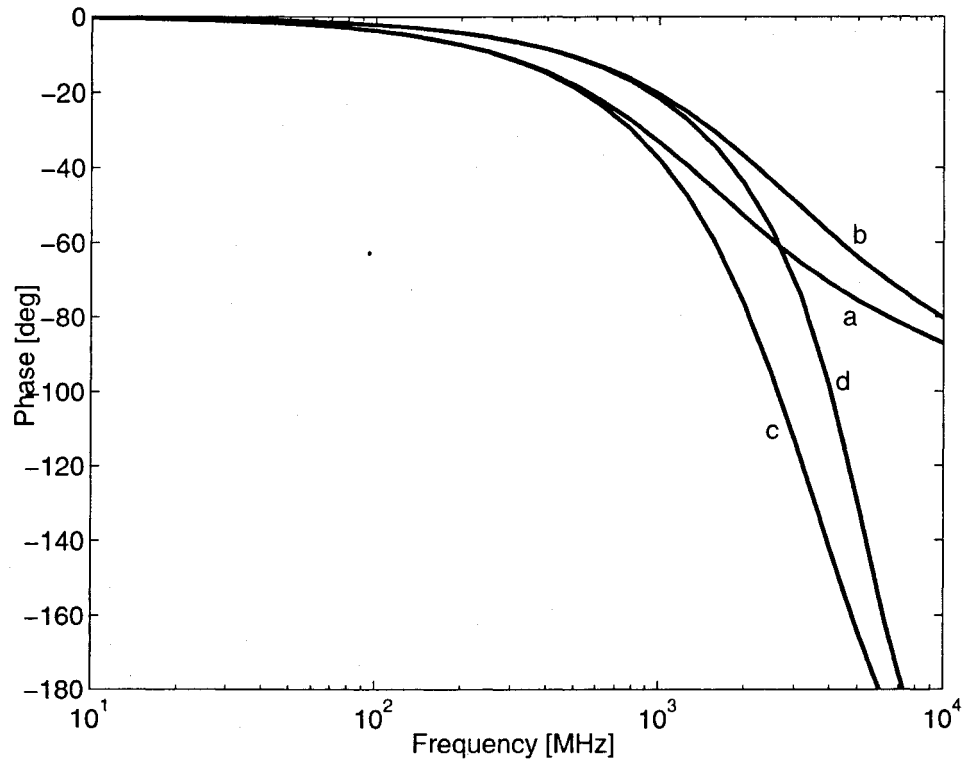

Figure 4.7: Phase response of current-mirror amplifier
(a) ($L = 0$, $\beta = 0$),
(b) ($L = 0$, $\beta = 0.1$),
(c) ($L = 60$nH, $\beta = 0$),
(d) ($L = 17$nH, $\beta = 0.1$)

It worth noting that the proposed current feedback does not create additional poles to the system. As shown in Eq.(4.19), the feedback moves the single pole further away from the original point. It not only does not create stability problems but also improves the phase response. Simulation results shown in Fig. 4.7 demonstrate that the circuits with feedback have a better phase response.

4.4 Inductor Series-Peaking with Current Feedback

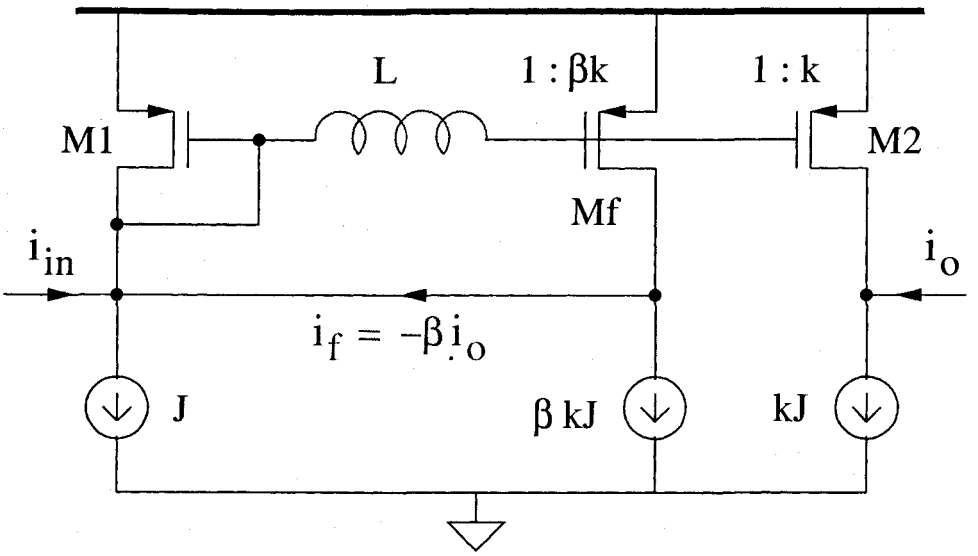

Figure 4.8: Current-mirror amplifier with series-peaking and current feedback ($J = 0.5$mA, $W_1 = 10\mu$m, $W_2 = 100\mu$m, $W_f = 10\mu$m)

It is evident from the preceding analysis that the bandwidth enhancement mechanisms of the inductor series-peaking and the current feedback differ fundamentally. This suggests that both techniques can be employed simultaneously to further improve the bandwidth. This is indeed true. Consider the current amplifier of Fig. 4.8 where both techniques are employed. To simplify the analysis, by assuming a large current gain k and a small feedback factor β, the effect of C_{gs1} and C_{gsf} can be neglected. Small signal analysis gives that the voltage at the input point

$$V_{in} = (I_{in} + I_f)\left[\frac{1}{g_{m1}} \| \left(sL + \frac{1}{sC_{gs2}}\right)\right]. \tag{4.21}$$

And the voltage at the gate of M_2 and M_f equals

$$V_{g2} = V_{in}\frac{1/sC}{sL + (1/sC)} \tag{4.22}$$

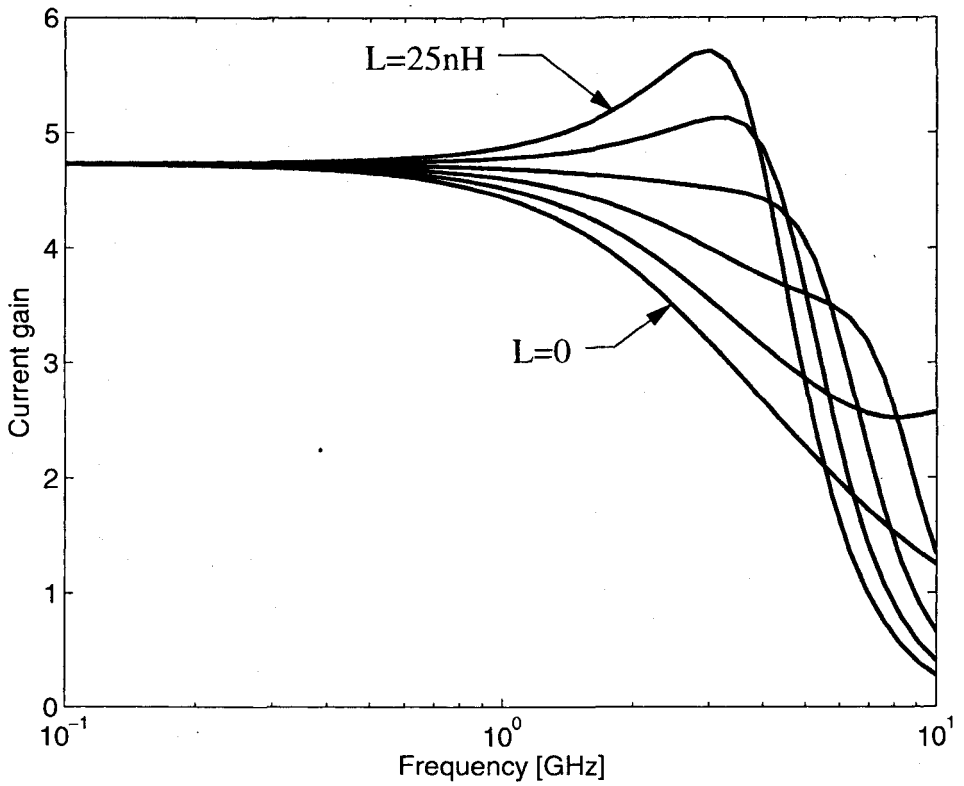

Figure 4.9: The effect of peaking inductor on the bandwidth of current-mirror amplifier with current feedback
($\beta = 0.1$, L is varied from 0 to 25 nH with step 5 nH)

Since $I_o = g_{m2}(V_{g2} - 0)$ and $I_f = -\beta I_o$, the transfer function of the amplifier with feedback is given by

$$\frac{I_o(s)}{I_{in}(s)} \approx \left[\frac{g_{m2}}{g_{m1}(1+k\beta)}\right] \frac{\frac{1+k\beta}{LC_{gs2}}}{s^2 + s\frac{1}{g_{m1}L} + \frac{1+k\beta}{LC_{gs2}}}, \tag{4.23}$$

with poles at

$$p_{1,2} = \frac{1}{2g_{m1}L}\left[-1 \pm \sqrt{1 - \frac{4g_{m1}^2 L(1+k\beta)}{C_{gs2}}}\right]. \tag{4.24}$$

The feedback changes the damping ratio of the current-mirror amplifier from $\xi =$

$\sqrt{\frac{C_{gs2}}{4g_{m1}^2 L}}$ to $\xi = \sqrt{\frac{C_{gs2}}{4g_{m1}^2 L(1+k\beta)}}$. In the critically damped case where

$$L = \frac{C_{gs2}}{4g_{m1}^2(1+k\beta)} \tag{4.25}$$

we have the bandwidth

$$\omega_o \approx \frac{2g_{m1}}{C_{gs2}}(1+k\beta) \tag{4.26}$$

Observed is that the bandwidth is $(1+k\beta)$ times that of the amplifier with series inductive peaking only, twice that of the amplifier with current feedback only, and $2(1+k\beta)$ times that of the basic current-mirror amplifier. Also seen is that the value of the peaking inductor in the critically damped case is reduced from $L \approx \frac{C_{gs2}}{4g_{m1}^2}$ with no feedback to $L \approx \frac{C_{gs2}}{4g_{m1}^2(1+k\beta)}$ with feedback. The reduction in the inductance using current feedback is very attractive because only a small inductor, subsequently, a small chip area and less parasitic effects, is required to achieve large bandwidth. Simulation results demonstrate that the bandwidth of the amplifier reaches 5.3 GHz with $L = 17nH$ and $\beta = 0.1$, as shown in Fig. 4.11. Fig. 4.9 plots the response of the amplifier for various values of the peaking inductor. It is seen that critical damping that occurs at $L \approx 17$nH provides the largest bandwidth.

Inductor series-peaking technique increases the bandwidth by introducing an additional pole-pair to the system. The drawback of this technique is that it deteriorates the phase response. As discussed in Section 5.3 and depicted in Fig. 4.7, the current feedback can improve the phase response of the amplifier with series-peaking inductor.

In a similar manner, one can show that for the optical preamplifier of Fig. 4.10, both inductor series-peaking technique and negative current-current feedback can be used for bandwidth enhancement. As shown in Fig. 4.12, with $L = 25$ nH and $\beta = 0.1$, the

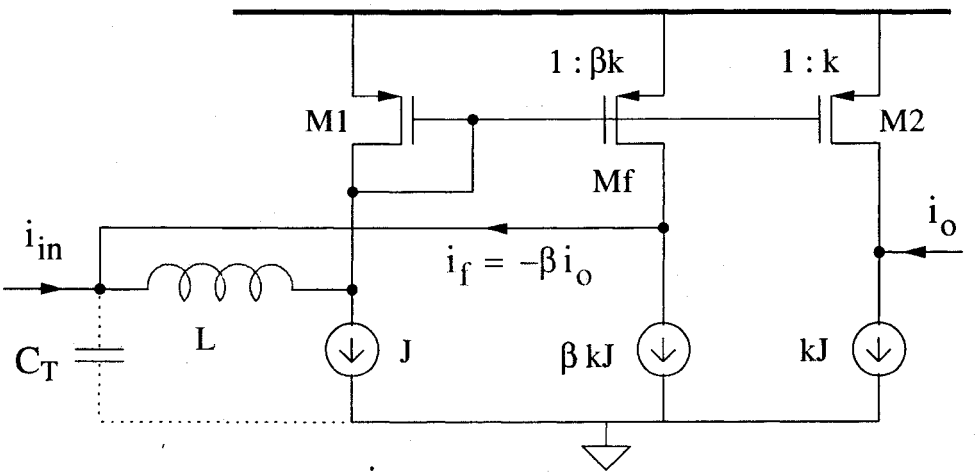

Figure 4.10: Optical preamplifier with series-peaking and current feedback ($J = 0.5$mA, $W_1 = 10\mu$m, $W_2 = 100\mu$m,$W_f = 10\mu$m, C_T=0.5pF)

bandwidth of the preamplifier is boosted to 2.0 GHz. Table 4.2 gives the comparable circuit parameters and simulation results.

Table 4.2: Circuit parameters and bandwidth ($L_{min} = 0.18\mu m$ is used for all transistors)

Amplifier	Dominant capacitor	Feedback	Peaking inductor	Bandwidth
Current-mirror amplifier	$C_{gs2} = C'_{ox}(WL)_2$	$\beta = 0$	$L = 0$	1.6 GHz
	$C_{gs2} = C'_{ox}(WL)_2$	$\beta = 0$	$L = 60$ nH	2.7 GHz
	$C_{gs2} = C'_{ox}(WL)_2$	$\beta = 0.1$	$L = 0$	2.8 GHz
	$C_{gs2} = C'_{ox}(WL)_2$	$\beta = 0.1$	$L = 17$ nH	5.3 GHz
Optical pre-amplifier	$C_T = 0.5$ pF	$\beta = 0$	$L = 0$	0.45 GHz
	$C_T = 0.5$ pF	$\beta = 0$	$L = 100$ nH	1.0 GHz
	$C_T = 0.5$ pF	$\beta = 0.1$	$L = 0$	0.88 GHz
	$C_T = 0.5$ pF	$\beta = 0.1$	$L = 25$ nH	2.0 GHz

4.5 Summary

A new inductor series-peaking technique for bandwidth enhancement of low-voltage CMOS current-mode circuits has been presented. For both current-mirror amplifiers and

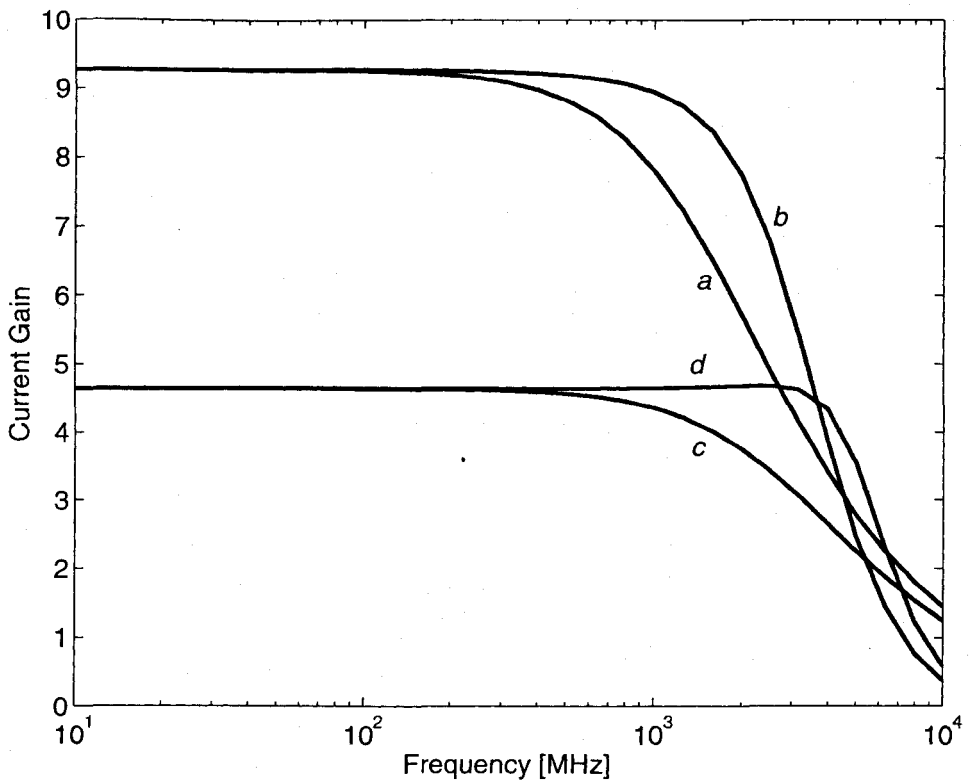

Figure 4.11: Frequency response of current-mirror amplifier
(a) $\omega_o = 1.6$ GHz, $(L = 0, \beta = 0)$,
(b) $\omega_o = 2.7$ GHz, $(L = 60nH, \beta = 0)$,
(c) $\omega_o = 2.8$ GHz, $(L = 0, \beta = 0.1)$,
(d) $\omega_o = 5.3$ GHz, $(L = 17nH, \beta = 0.1)$

optical preamplifiers, series inductive peaking boosts the bandwidth by 100% approximately with zero overshoot. The proposed novel current feedback technique increases the bandwidth by $(1 + k\beta)$. When both techniques are employed simultaneously, the bandwidth can be significantly improved by $2(1 + k\beta)$, and the current feedback also effectively reduces the value of the peaking inductor by $(1 + k\beta)$. Both inductor series-peaking and current feedback do not affect the DC biasing conditions and the minimum supply voltage. They are particularly attractive for low-voltage design.

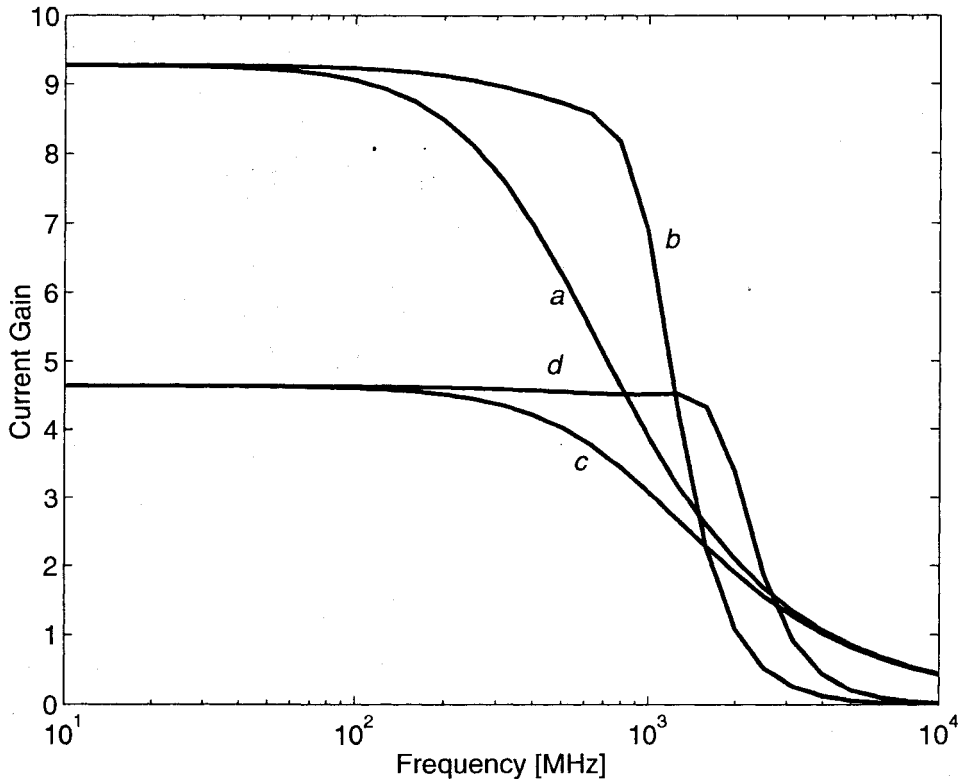

Figure 4.12: Frequency response of optical preamplifier with $C_T = 0.5$ pF
(a) $\omega_o = 0.45$ GHz, $(L = 0, \beta = 0)$,
(b) $\omega_o = 1.0$ GHz, $(L = 100\text{nH}, \beta = 0)$,
(c) $\omega_o = 0.88$ GHz, $(L = 0, \beta = 0.1)$,
(d) $\omega_o = 2.0$ GHz, $(L = 25\text{nH}, \beta = 0.1)$

Chapter 5

Topologies and Strategies of Current-Mode Amplifiers

This chapter presents new circuit topologies and design strategies for low-voltage current-mode amplifiers. It reveals that two-stage configurations have larger bandwidth compared with single-stage configurations. Fully balanced configuration can eliminate the effect of bias-induced mismatches. The noise performance of the current-mode circuits is analyzed. A current-branching mechanism is used to reduce the power consumption and increase the output impedance. It shows that differential configurations can minimize the effect of power and ground fluctuations. A new differential negative current feedback technique is introduced to boost the bandwidth and increase the dynamic range. A common-mode feedback topologies are proposed to increase the common-mode rejection ratio (CMRR) and to stabilize the DC biasing condition.

5.1 Gain and Bandwidth

The schematic of the basic single current-mirror amplifier is shown in Fig.5.1(a). Neglecting the effect of channel length modulation and load capacitance, it can be shown that the current gain is given by

$$\frac{I_o(s)}{I_{in}(s)} = \frac{k}{1 + sR_{in}C_{in}} \tag{5.1}$$

where $k = \frac{(W/L)_2}{(W/L)_1}$, $R_{in} \approx \frac{1}{g_{m1}}$, $C_{in} \approx C_{gs1} + C_{gs2} = (1+k)C_{gs1}$, and $C_{gs} >> C_{gd}$ is assumed. The bandwidth is therefore obtained from

$$\omega_{-3dB} = \frac{g_{m1}}{(1+k)C_{gs1}} \tag{5.2}$$

It can be seen that the current gain and bandwidth are conflicting design parameters. To achieve a large gain without sacrificing the bandwidth, a two-stage current amplifier shown in Fig.5.1(b) can be used. Note that a PMOS-pair is used at the first stage to achieve a better bandwidth and proper bias conditions [26].

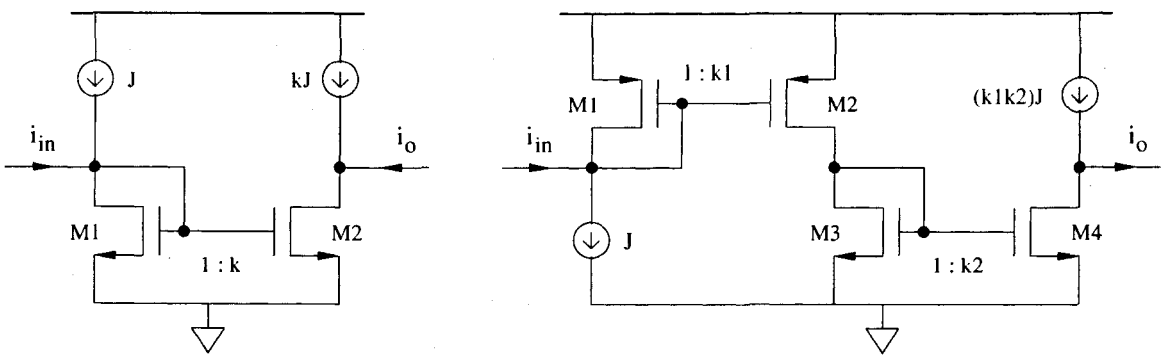

Figure 5.1: Current amplifiers (a)Single-stage; (b)Two-stage

$$\begin{aligned} \omega_{-3dB,1} &= \frac{g_{m1}}{(1+k_1)C_{gs1}}, \\ \omega_{-3dB,2} &= \frac{g_{m3}}{(1+k_2)C_{gs3}}. \end{aligned} \tag{5.3}$$

The current gain of the two-stage amplifier is given by

$$\frac{I_o(s)}{I_{in}(s)} = \frac{k_1 k_2}{(1 + sR_1C_1)(1 + sR_2C_2)} \tag{5.4}$$

Table 5.1: Circuit parameters of single- and two-stage amplifiers ($L_{min} = 0.18\mu m$ is used for all transistors)

Parameter	Single-stage	Two-stage
M_1	$W = 0.5\mu$m	$W = 0.5\mu$m
M_2	$W = 50\mu$m	$W = 3.5\mu$m
M_3	-	$W = 1.75\mu$m
M_4	-	$W = 25\mu$m
J	50 μA	50μA
Bandwidth	365 MHz	1.3 GHz

where $k_1 = \frac{(W/L)_2}{(W/L)_1}$, $k_2 = \frac{(W/L)_4}{(W/L)_3}$, $R_1 \approx \frac{1}{g_{m1}}$, $C_1 \approx (1+k_1)C_{gs1}$, $R_2 \approx \frac{1}{g_{m3}}$, and $C_2 \approx (1+k_2)C_{gs3}$. The frequencies corresponding to the two poles are

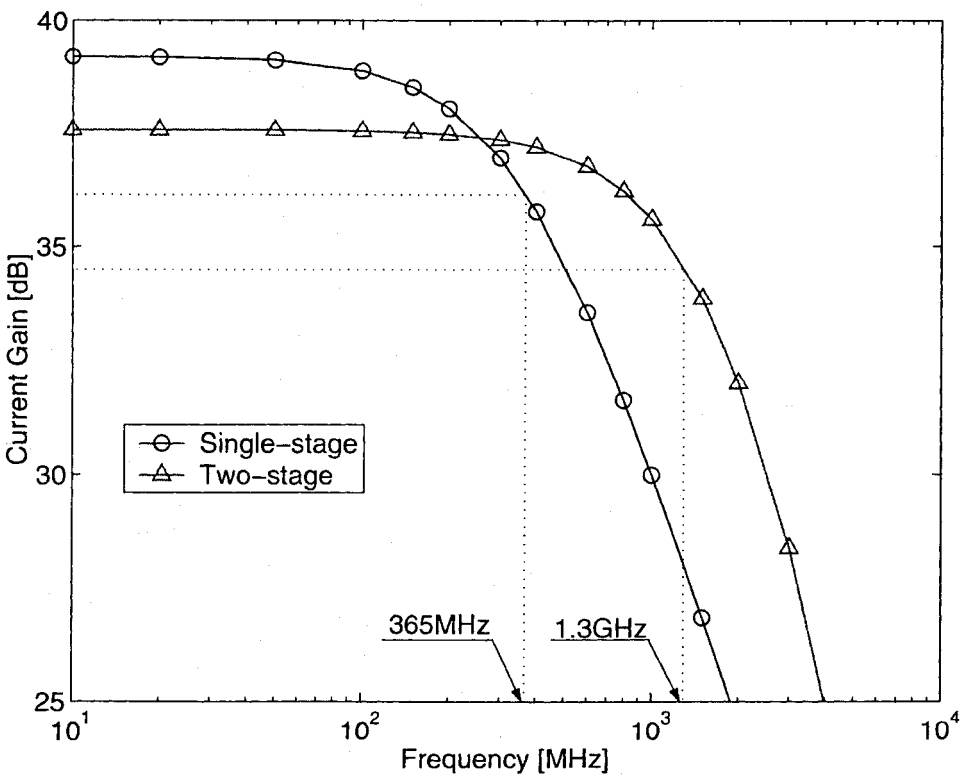

Figure 5.2: Frequency response of single- and two-stage current amplifiers

For a given current gain $k = k_1 k_2$, the bandwidth can be maximized if the two poles

are identical. It is known that $g_{m1} = \sqrt{2K_p(W/L)_1 I_{D1}}$ and $g_{m3} = \sqrt{2K_n(W/L)_3 I_{D3}}$, where $K_n = \mu_n C'_{ox}$ and $K_p = \mu_P C'_{ox}$. If we let $(W/L)_3 = \frac{1}{2}(W/L)_2 = \frac{1}{2}k_1(W/L)_1$, then $C_{gs3} = \frac{1}{2}k_1 C_{gs1}$ follows [36]. Since $I_{D3} = k_1 I_{D1}$, we arrive at

$$\frac{\sqrt{K_p}}{1+k_1} = \frac{\sqrt{2K_n}}{1+k_2} \tag{5.5}$$

Using this relation, if $K_n = 2K_p$, for $k_1 k_2 = 100$, we obtain $k_1 \approx 7$. Fig.5.2 shows the frequency response of the output current of the single-stage and two-stage amplifier that are implemented in TSMC 0.18μ, $1.8V$ CMOS process. The circuit parameter is listed in Table 5.1. It is seen that the bandwidth of the two-stage amplifier is 1.3GHz approximately whereas that of the single-stage is only 365MHz. Also seen is that the two-stage amplifier provides smaller current gain in DC steady state.

5.2 Noise

[11] reveals that the noise figure of the current-mirror amplifiers is determined by the power of the input-referred noise current generator. For the single-stage current amplifier in Fig. 5.1(a), the input referred noise current power density is given by

$$\overline{I^2_{n,in}} = \overline{I^2_{n,1}} + \frac{\overline{I^2_{n,2}}}{k^2}, \tag{5.6}$$

where $\overline{I^2_{n,1}}$ and $\overline{I^2_{n,2}}$ are the power density of the channel noise of M_1 and M_2. It is seen that for $k \gg 1$, the noise from M_2 can be neglected.

The input referred noise current power density of the two-stage amplifier in Fig. 5.1(b) is given by

$$\overline{I^2_{n,in}} = \overline{I^2_{n,1}} + \frac{\overline{I^2_{n,2}} + \overline{I^2_{n,3}}}{k_1^2} + \frac{\overline{I^2_{n,4}}}{(k_1 k_2)^2} \tag{5.7}$$

It is seen that the two-stage configuration increases the input referred noise. However, the dominant noise contributor is still the input transistor M_1 if we keep a large current gain k_1 at the first amplification stage.

5.3 Mismatches

The performance of the current amplifier in Fig.5.1(a) deteriorates when mismatches between the input and output branches exists. The mismatches generate an offset output current i_{os}.

(i) (W/L) **Mismatch** – Let $(W/L)_1 = (W/L)$ and $(W/L)_2 = k\big[(W/L) + \Delta(W/L)\big]$, it can be shown that the output current

$$\begin{aligned} i_o &= ki_{in} + i_{os1} \\ &= ki_{in} + k\frac{\Delta(W/L)}{(W/L)}(J + i_{in}) \\ &= ki_{in} + k\delta_{N,1}(J + i_{in}) \end{aligned} \tag{5.8}$$

(ii) V_T **Mismatch** – V_T mismatch is caused by process variation. Let $V_{TN1} = V_T$ and $V_{TN2} = V_T + \Delta V_T$, it can be shown that

$$\begin{aligned} i_o &= ki_{in} + i_{os2} \\ &= ki_{in} + k\left[\frac{(\Delta V_T)^2}{(V_{GS} - V_T)^2} - \frac{2\Delta V_T}{V_{GS} - V_{TN}}\right](J + i_{in}) \\ &= ki_{in} + k\delta_{N,2}(J + i_{in}) \end{aligned} \tag{5.9}$$

(iii) v_{GS} **Mismatch** – The mismatch of the gate voltage is mainly caused by an improper layout and the resistance of interconnection between gates of M_1 and M_2. Let $v_{GS1} = v_{GS}$ and $v_{GS2} = v_{GS} + \Delta v_{gs}$, it can be shown that

$$
\begin{aligned}
i_o &= ki_{in} + i_{os3} \\
&= ki_{in} + k\left[\frac{(\Delta v_{GS})^2}{(V_{GS}-V_T)^2} + \frac{2\Delta v_{GS}}{V_{GS}-V_{TN}}\right](J + i_{in}) \\
&= ki_{in} + k\delta_{N,3}(J + i_{in})
\end{aligned} \tag{5.10}
$$

(iv) v_{DS} **Mismatch** – The mismatch of v_{DS} is caused by the different output impedances of MOSFETs. Let $v_{DS1} = v_{DS}$ and $v_{DS2} = v_{DS} + \Delta v_{DS}$, it can be shown that

$$
\begin{aligned}
i_o &= ki_{in} + i_{os4} \\
&= ki_{in} + k\left[\frac{\lambda_N \Delta V_{DS}}{1 + \lambda_N \Delta V_{DS}}\right](J + i_{in}) \\
&= ki_{in} + k\delta_{N,4}(J + i_{in})
\end{aligned} \tag{5.11}
$$

Where λ_N is the channel length modulation of NMOS transistors.

When all mismatches are encountered, the output current of the basic current amplifier is obtained from

$$
i_o = ki_{in} + i_{os}. \tag{5.12}
$$

The offset output current i_{os} is given by

$$
i_{os} = k\delta_N(J + i_{in}), \tag{5.13}
$$

where δ_N is the total mismatch coefficient of the NMOS-pair. It equals

$$
\delta_N = \sum_{i=1}^{4} \delta_{N,i}. \tag{5.14}
$$

The above equations reveal that mismatches give rise to an output offset current that has both signal-dependent and bias-dependent parts. Because for class-A current ampli-

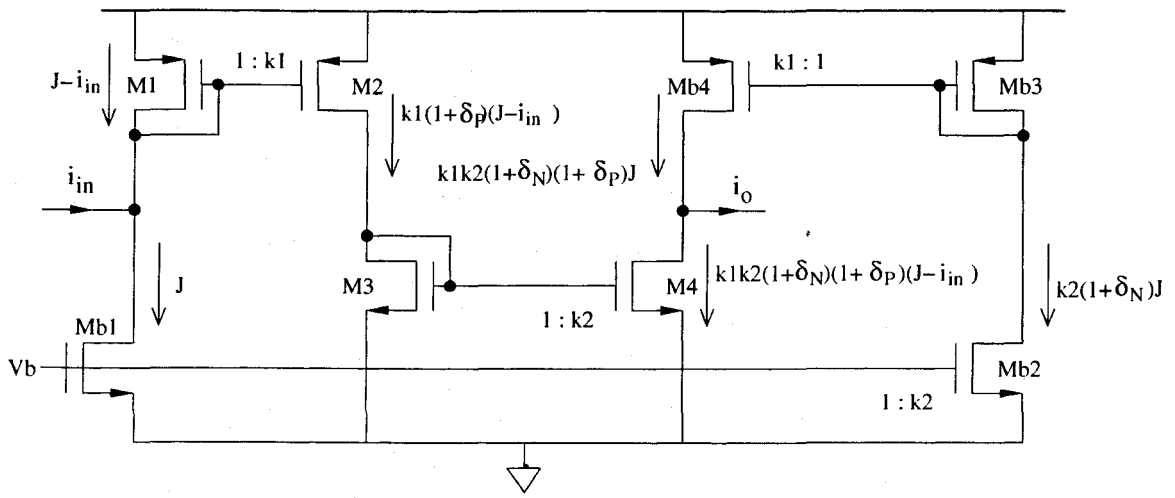

Figure 5.3: Fully balanced two-stage current current amplifier

fiers, signal is usually much smaller as compared with the biasing current, the biasing-dependent part dominates. Further, because the bias-dependent part is approximately time-invariant, its effect can be eliminated by using the fully balanced configuration, shown in Fig.5.3. The circuit is fully balanced such that the bias-induced output offset current in the signal path and that on the bias path are cancelled out. In saying so we have assumed that NMOS-pairs have the same mismatches and the same assumption holds for PMOS-pairs. Fig.5.3 shows the current flowing in the balanced amplifier. Thus, the output current can be given by

$$i_o = k_1 k_2 i_{in} + i_{os}. \tag{5.15}$$

The output offset current i_{os} is given by

$$i_{os} = k_1 k_2 (\delta_N + \delta_P + \delta_N \delta_P) i_{in}, \tag{5.16}$$

where δ_P is the total mismatch coefficient of the PMOS-pair which can be calculated in the same manner as δ_N. It is seen that the bias-dependent part is removed completely.

5.4 Power Consumption and Output Impedance

Current-mode amplifiers usually take high power consumption because the biasing current is amplified as well as the signal. As shown in Fig.5.4, the biasing current in the input branch is given by J. With current gain of $k = k_1 k_2$, the biasing current in the output branch reaches $k_1 k_2 J$. The DC power dissipation is given by

$$P_{diss} = V_{DD} \times (1 + k_1 + k_1 k_2) J. \tag{5.17}$$

The higher the current gain the higher the power dissipation.

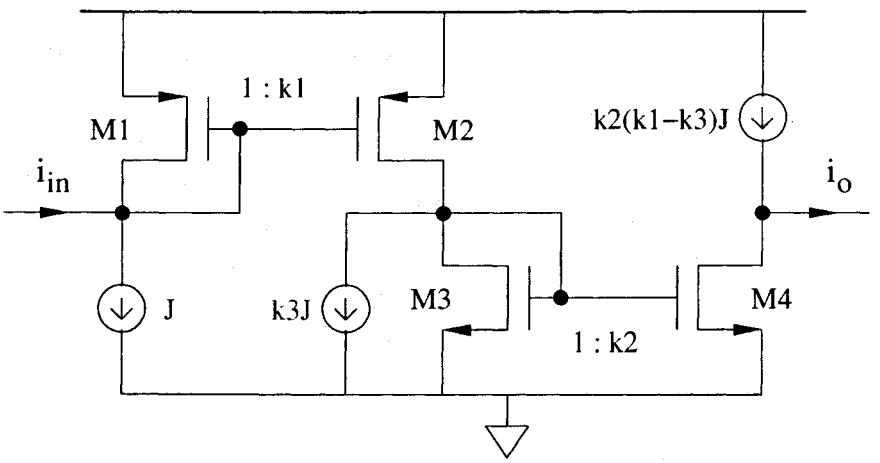

Figure 5.4: Two-stage current amplifier with current-branching

Another drawback of the current amplifiers is their low output impedance which is given by

$$R_{out} = \frac{1}{g_{ds2}} \approx \frac{1}{\lambda I_{D2}} = \frac{1}{\lambda k_1 k_2 J} \tag{5.18}$$

It is seen that the output impedance is reversely proportional to the current gain. To solve these two problems, we introduce a current-branching mechanism to the two-stage current amplifier as shown in Fig. 5.4. The branching current source $k_3 J$ is placed at

the second amplification stage. So the DC current flowing through M_3 is $(k_1 - k_3)J$ instead of $k_1 J$, and the output branch biasing current is $k_2(k_1 - k_3)J$. The DC power dissipation is given by

$$P_{diss} = V_{DD} \times [1 + k_1 + k_2(k_1 - k_3)]J. \tag{5.19}$$

And the output impedance is given by

$$R_{out} = \frac{1}{\lambda k_2(k_1 - k_3)J} \tag{5.20}$$

Because the transistors in this circuit always work at saturation region, k_3 can be set closely to k_1. Thus, both a significantly reduced power dissipation and a greatly increased output impedance are achieved.

The branching current source can be implemented by a NMOS transistor with a fixed gate-voltage. It should be noted that when k_3 is very close to k_1, the channel length modulation effect makes the g_{ds} of the branching transistor comparable to the g_m of M_3. Accountable part of the AC signal may flow through the branching transistor. Therefore, the AC current gain will be affected.

5.5 Differential Configuration

Simultaneously switching noise (SSN) is a considerable issue in mixed analog-digital circuit design. In optical receivers, the switching of clock and data recovery circuit causes power and ground fluctuations. To suppress this effect, a differential configuration shown in Fig. 5.5 is proposed.

To demonstrate the effectiveness of fully differential configuration, both the non-differential and differential amplifiers with 50Ω load are implemented in TSMC 0.18μ 1.8V CMOS process. A pulse voltage source of amplitude 150mV and frequency 200MHz

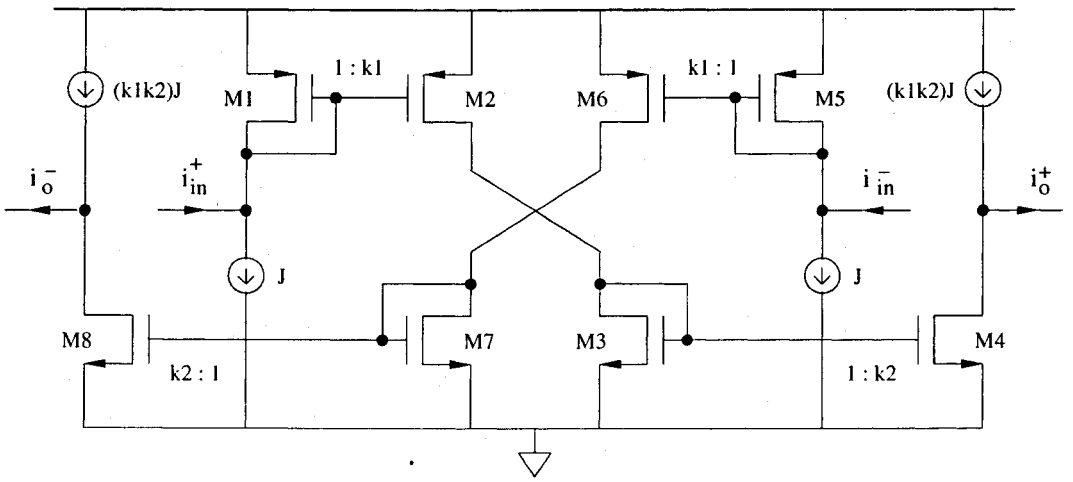

Figure 5.5: Differential current amplifier

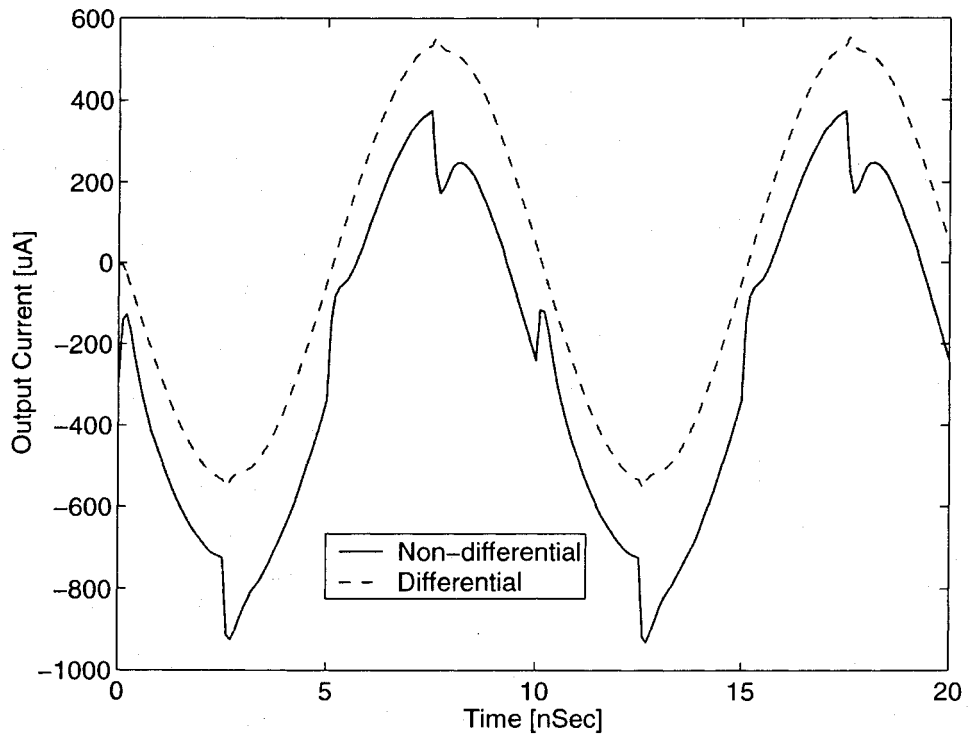

Figure 5.6: Output current of non-differential and differential amplifiers with a noisy supply voltage

is connected in series with the supply voltage as the source of power fluctuation. With a 100MHz sine-wave input signal, the output current is plotted in Fig. 5.6. It is seen that

the output current of the non-differential amplifier contains sparks at voltage switching point and there exists a DC offset component. whose value is proportional to the amplitude of the pulse voltage source, whereas that of the differential amplifier is insensitive to the power fluctuation.

5.6 Differential Current Feedback

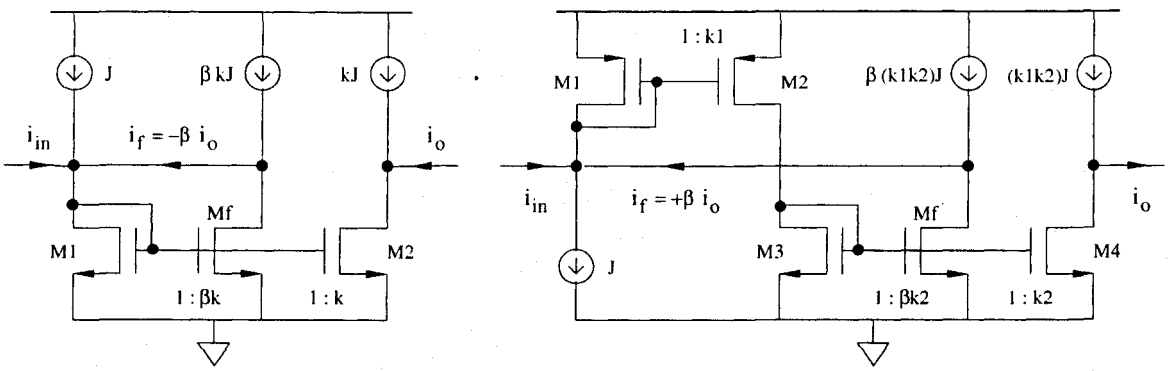

Figure 5.7: Current amplifiers with current feedback (a)Single-stage; (b)Two-Stage

Several differential current-mode circuits have been introduced in [31] [37] [38]. To our best knowledge, none of the existing differential current-mode configurations employ differential feedback. In those designs, the positive and negative input currents (i_{in}^{+} and i_{in}^{-}) are amplified in the separate branches, and the output current is obtained by $i_o = i_o^{+} - i_o^{-}$. Any changes in one branch do not affect the other one. As we know, negative current feedback is capable of boosting the bandwidth and increasing the dynamic range. Negative differential feedback is desirable in differential current-mode approaches.

As depicted in Section 4.2, the negative current feedback of the current-mirror amplifier as shown in Fig. 5.7(a) lowers the input impedance, increases the bandwidth. It is important to note that the feedback becomes positive when it is implemented in the two-stage (or even-stage) amplifier. As shown in Fig. 5.7(b), the feedback current is given by $i_f = +\beta i_o$. However, when this topology is employed in the differential con-

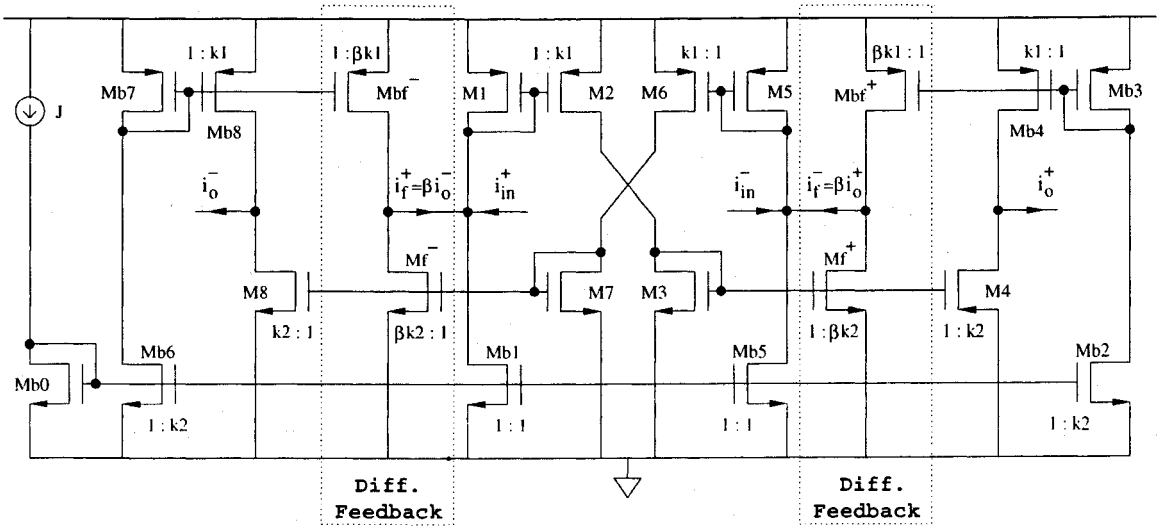

Figure 5.8: Differential current amplifier with negative differential current feedback

figuration, the feedback exhibits the desired negative characteristics. As shown in Fig. 5.8, the feedback current $i_f{}^+ = \beta i_o{}^-$ at the positive input point, and $i_f{}^- = \beta i_o{}^+$ at the negative input point.

Table 5.2: Circuit parameters of differential amplifier
($L_{min} = 0.18\mu m$ is used for all transistors)

Parameter	Value
M_1, M_5, M_{B0}	$W = 0.5\mu$
M_2, M_3, M_6, M_7	$(W/L)_3 = (W/L)_7 = \frac{1}{2}(W/L)_2 = \frac{1}{2}(W/L)_6$
M_{b2}, M_{b3}, M_{b6}, M_{b7}	$(W/L)_{b2} = (W/L)_{b3} = (W/L)_{b6} = (W/L)_{b7}$
J	$28\mu A$
k_1	7
k_2	100/7
β	0.02

It should be noted that the added differential feedback does not affect the output impedance of the amplifier because it acquires the feedback current in different branches. This structure remains the minimum supply voltage requirement. An advantage of this

Table 5.3: Key performance parameters of differential amplifier

—	Without Feedback	With Feedback
Current Gain (dB)	37.6	28.3
Bandwidth (GHz)	1.3	3.5
Input Impedance ($K\Omega$)	9.8	3.4
Power Dissipation (mW)	11.66	13.34

configuration is that the feedback factor β can be adjusted independent of the forward path. β should be keep small in order to achieve a large current gain. The dimension of the biasing transistors M_{bf}^{+} and M_{bf}^{-} in the feedback path can be carefully set so that the feedback will not affect the DC operating point of the circuit.

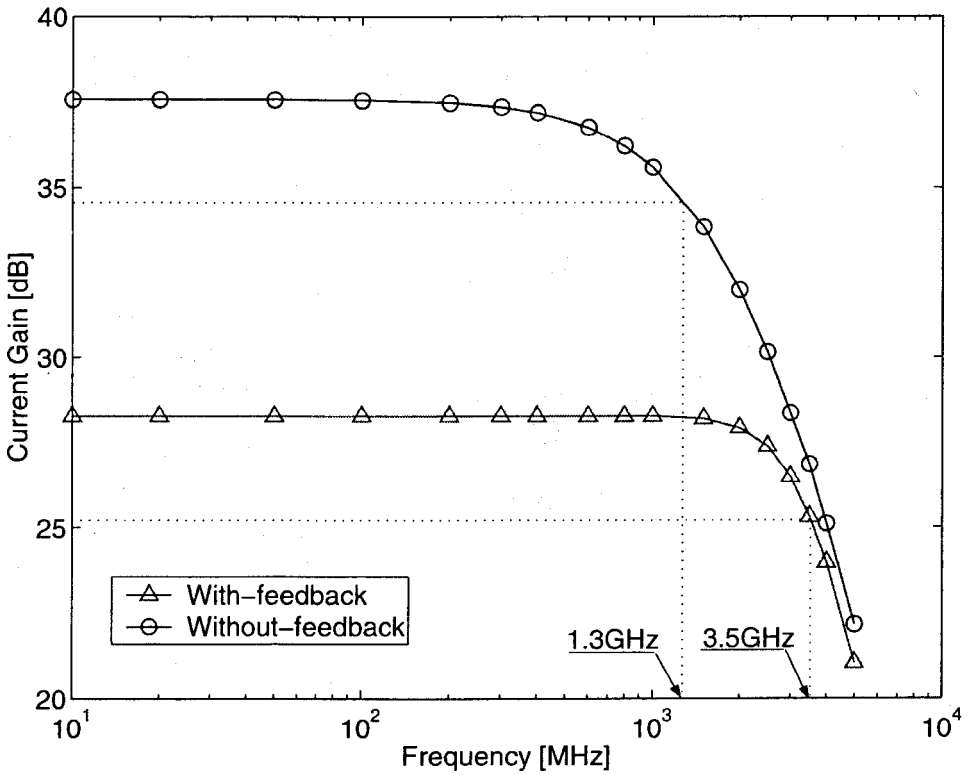

Figure 5.9: Frequency response of differential current amplifier with and without feedback

To illustrate the effectiveness of negative differential current feedback, we simulated

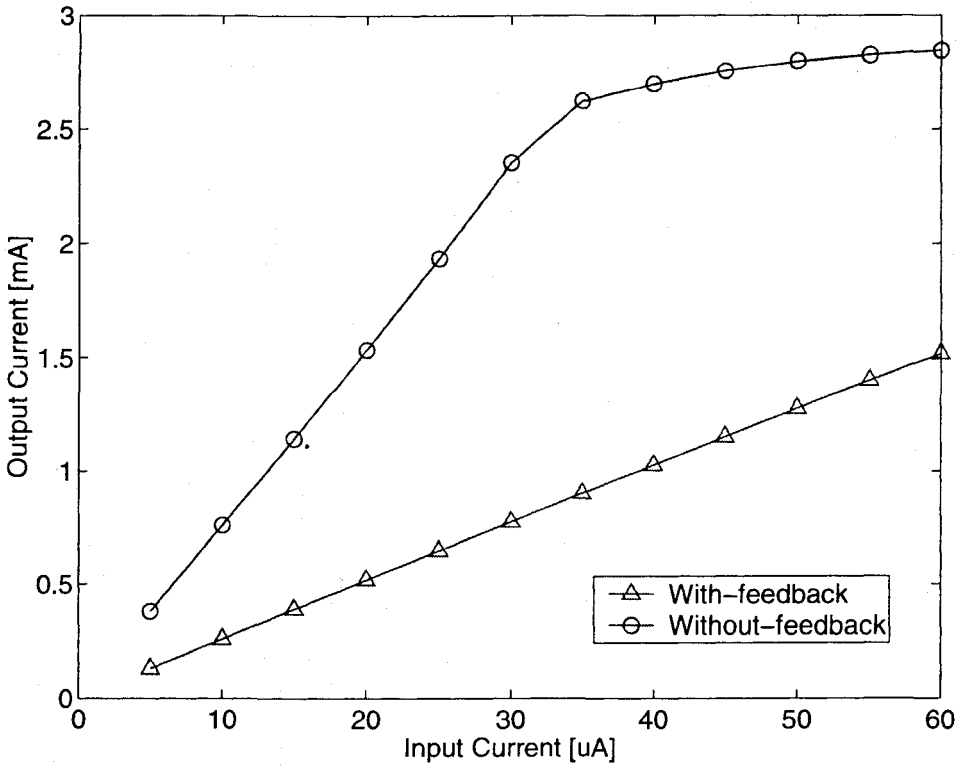

Figure 5.10: Dynamic range of differential current amplifier with and without feedback

the fully differential current amplifier with and without feedback. The circuit is implemented in TSMC 0.18μ 1.8V CMOS process, and the circuit parameters are given in Table 5.2.

With the open-loop gain $k = 100$ and the feedback factor $\beta = 0.02$, the loop gain is given by $(k\beta) = 2$. As depicted in Section 4.2, the feedback is expected to boost the bandwidth by $(1 + k\beta) = 3$. The simulated frequency response demonstrates the expectation. As shown in Fig.5.9, the differential feedback enlarges the circuit bandwidth from 1.3GHz to 3.5 GHz. Other key parameters are listed in Table 5.3. It is seen that both the input impedance and the current gain are reduced approximately by the same factor of $(1 + k\beta)$. The feedback only slightly increases the power dissipation of the circuit because the current flowing in the feedback are very small compared to that in

the output branches.

Another notable advantage of the negative differential current feedback is that it greatly boosts the dynamic range of the amplifier. The input current range is limited by the biasing current. In the given circuit, when the input current is larger than 28 μA, the output is distorted. As shown in Fig. 5.10, the dynamic range is significantly increased by the feedback. The input swing can be very large as long as the saturation current of the transistors is not reached.

5.7 Common-Mode Feedback

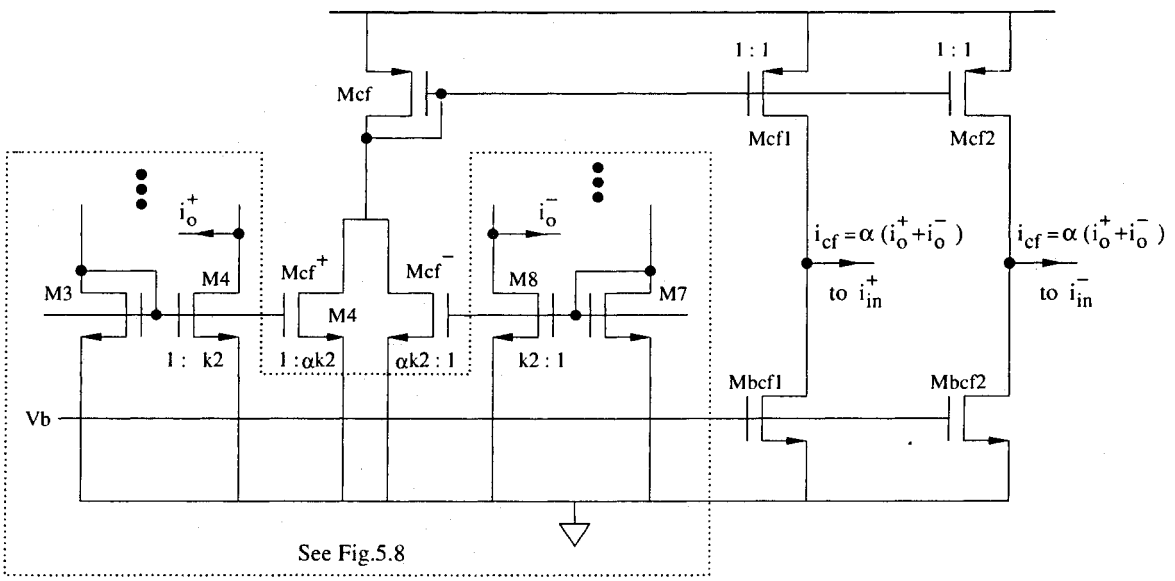

Figure 5.11: Common-mode feedback

Common-mode feedback (CMFB) is widely used in voltage-mode Op-Amp to increase the common-mode rejection ratio (CMRR) and to stabilize the DC operating point. Based on the previous analysis of the current feedback, we introduce a common-mode current feedback in this differential amplifier to increase the CMRR. As shown in Fig.5.11, the transistor M_{cf}^+ and M_{cf}^- add the output current $i_o{}^+$ and $i_o{}^-$ together.

The differential-mode signal will be eliminated and only the common-mode signal will be accumulated. The added common-mode signal is amplified by a current mirror pair, and then fed back to the input nodes separately. Since the signal has been amplified by three (odd) current mirrors, the feedback comes to be a negative common-mode current feedback. The common-mode gain is reduced by the negative feedback, thus the common-mode rejection ratio is increased.

5.8 Summary

Several circuit topologies and design strategies for low-voltage current-mode amplifiers have been analyzed. It shows that the fully-balanced two-stage current amplifiers are able to achieve wide bandwidth and minimize the bias-dependent mismatches. Analysis tells that the current gain is critical to the input referred noise. The proposed current-branching configuration significantly reduces the power consumption and increases the output impedance. It shows that the differential configuration is insensitive to the power and ground fluctuations. A new differential feedback has been introduced for differential current-mode circuits to boost the bandwidth and enlarge the dynamic range. A common-mode feedback topologies was proposed to improve the CMRR and to stabilize the biasing condition.

Chapter 6

New Low-Voltage Differential CMOS Current-Mode Optical Preamplifier

This chapter shows the complete design of a low-voltage differential CMOS current-mode preamplifier for optical communications. The circuit design and layout are based on TSMC 0.18 μm, 1.8 V, 6-metal layers, mixed-signal CMOS technology. Simulation analysis uses Spectre from Cadence Design Systems with BSIM3V3 device models. The designed chip is currently being fabricated by TSMC via CMC.

6.1 Circuit Schematic and Parameters

A differential optical front-end with a novel differential transimpedance amplifier was introduced in [24]. Fig. 6.1 shows the topology of the differential front-end. One input is connected to the photodiode, and the other one is connected to a capacitor C_d' who has the same capacitance as that of the photodiode.

In this thesis, we introduce a new differential current-mode amplifier for optical receivers. Fig. 6.2 shows the complete schematic of the preamplifier. M_{r1}, M_{r2}, M_{r3}, and M_{r4} constitute the so-called "self-biasing" circuit to provide a reference current. An important advantage of this self-biasing circuit is that the reference current is insensitive

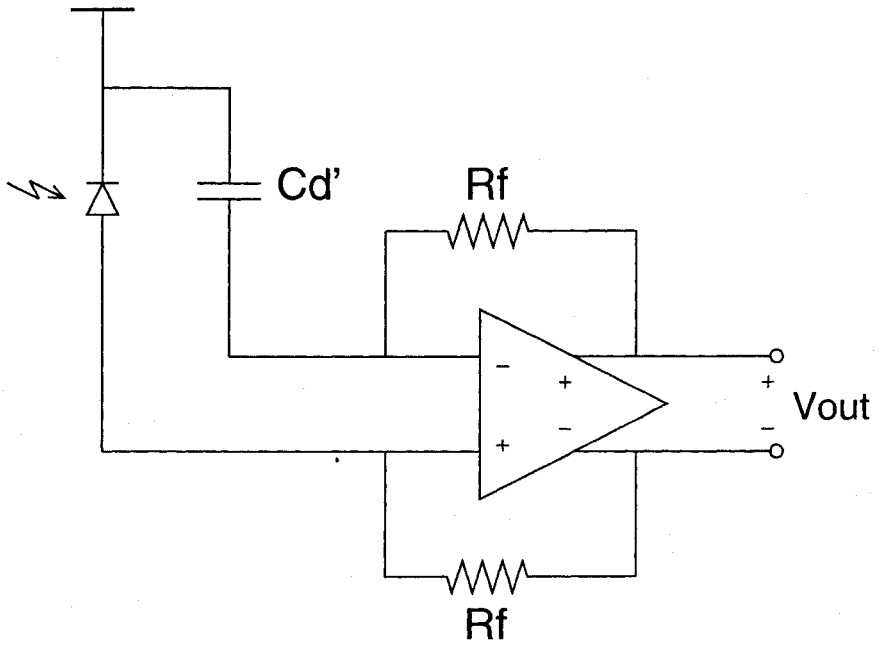

Figure 6.1: Differential optical front-end with differential transimpedance amplifier

to the fluctuation of the supply voltage [26]. The biasing current sources of the amplification and that of the feedback branches mirror from the reference current. Transistors M_1, M_3, M_5, and M_7 (M_2, M_4, M_6, and M_8) constitute the two-stage amplification path for i_{in}^{+} (i_{in}^{-}). M_{b1} and M_{b3} (M_{b2} and M_{b4}) provide the biasing current for the positive (negative) path. M_{f1} and M_{bf1} (M_{f2} and M_{bf2}) constitute the feedback path to generate the differential feedback current i_f^{-} (i_f^{+}). M_{s1} and M_{s2} are current-branching transistors used to reduce the biasing current at the second amplification stages. The parameters of all transistors are given in Table 6.1. The inductors $L_1 = L_2 = 8$ nH. The circuit is assumed to tolerate a 0.3 pF photodiode capacitance.

To simplify the description, we only analyze the positive amplification path. Because of the existence of a large photodiode capacitance, the input impedance has to be small enough to achieve large bandwidth. Therefore, a large biasing current at the input stage is needed. In our design the input biasing current mirrored from the reference is about

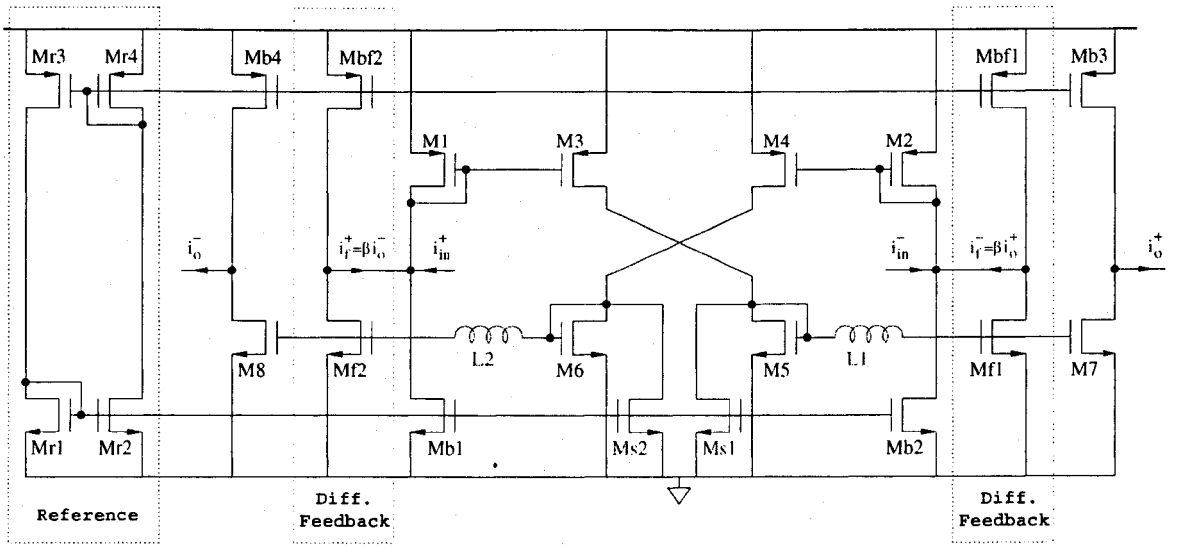

Figure 6.2: Differential current-mode amplifier

Table 6.1: Transistor sizes of the optical preamplifier ($L_{min} = 0.18\mu m$ is used for all transistors)

Transistor	Width (μm)
M_1, M_2	50
M_3, M_4	100
M_5, M_6	5
M_7, M_8	200
M_{b1}, M_{b2}	25
M_{b3}, M_{b4}	220
M_{f1}, M_{f2}	5
M_{bf1}, M_{bf2}	5
M_{s1}, M_{s2}	49
M_{r1}, M_{r2}	25
M_{r3}, M_{r4}	50

2.74 mA. Under this condition and with the given transistor size, the DC voltage at the input point is about $\frac{V_{DD}}{2}$.

The amplification gain at the first stage is set to be $k_1 = \frac{(W/L)_3}{(W/L)_1} = 2$. One reason to select such a small gain is to restrain the input gate-source parasitic capacitance that con-

tributes to the total input capacitance. Another reason is because of the implementation of the current-branching. With the given transistor parameters, the branching transistor M_{s1} greatly reduces the DC biasing current flowing through M_5 to 0.28 mA. The width of M_5 is small to reduce the size of the output transistor. Because of these, the channel length modulation causes $g_{ds,s1} \approx \lambda_n I_{D,s1}$ is comparable to $g_{m,5} = \sqrt{2\mu_n C'_{ox}(W/L)_5 I_{D,5}}$. It means that an accountable part of AC signal will flow through M_{s1}, resulting in a reduced signal gain. In our circuit, the simulated AC gain at the first stage is about 1, which means $g_{ds,s1} \approx g_{m,5}$. The channel length modulation effect can be reduced by using long-channel devices. The drawback is the long-channel devices have larger parasitic capacitances that will deteriorate the frequency response.

The major current gain is contributed by the second-stage. The open-loop gain of the second-stage is set to be $k_2 = \dfrac{(W/L)_7}{(W/L)_5} = 40$, which also approximately equals the total open-loop gain k. To keep a certain closed-loop current gain, a small feedback factor $\beta = (1/40)$ is selected making the loop gain $k\beta \approx 1$. As depicted in Section 4.3, the closed-loop gain is about half of the open-loop gain. The whole amplifier carries out a differential current gain of about 40. With 50Ω load resistance, a 2 KΩ transimpednace gain is achieved.

It should be noted that the two-stage current amplifier has two poles. Neglecting the gate-drain capacitances, one pole is at the input point with

$$s_1 = \frac{g_{m,1} + g_{ds,b1}}{C_d + C_{gs,1} + C_{gs,3}}, \tag{6.1}$$

where C_d is the capacitance of the photodiodes. Another pole is located at the input of the second-stage

$$s_2 = \frac{g_{m,5} + g_{ds,3} + g_{ds,s1}}{C_{gs,5} + C_{gs,7}} \tag{6.2}$$

Although the total capacitance of the 1st pole is still larger than that of the second pole. The reduction of both the biasing current and the size of M_5 dramatically lowers the value of $g_{m,5}$. Thus, the two pole may become comparable.

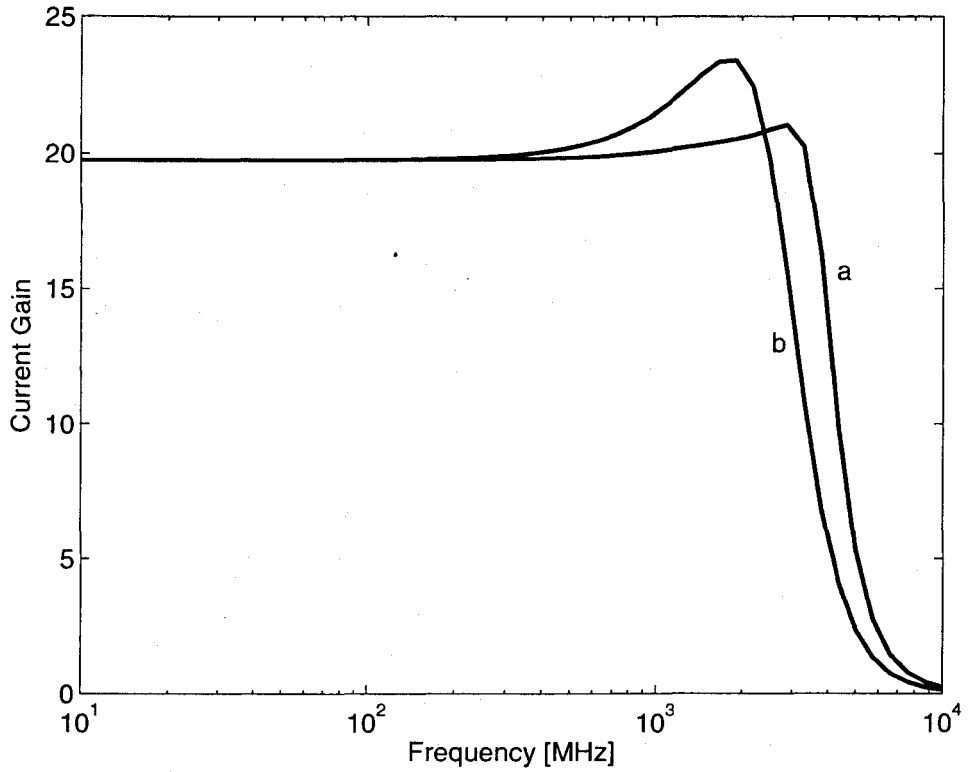

Figure 6.3: Simulation with L at the 1st-stage input node
[(a) C_d=0.3 pF; (b) C_d=0.5 pF]

The series-peaking technique supposes the peaking inductor to be placed in series with the capacitor constituting the dominant pole. For our circuit, we do the simulation by placing "ideal" inductors ($L_1 = L_2 = 8$ nH) at the first-stage input nodes and the second-stage input nodes, respectively. Simulation results are shown in Fig. 6.3 and Fig. 6.4. It is seen that:

(i) With C_d=0.3 pF: When L_1 and L_2 are placed at the 1st-stage input nodes, the frequency response is well-shaped, and the bandwidth f_{-3dB}=3.99 GHz. When L_1 and L_2 are placed at the 2nd-stage input nodes, the frequency response has a "drop-raise"

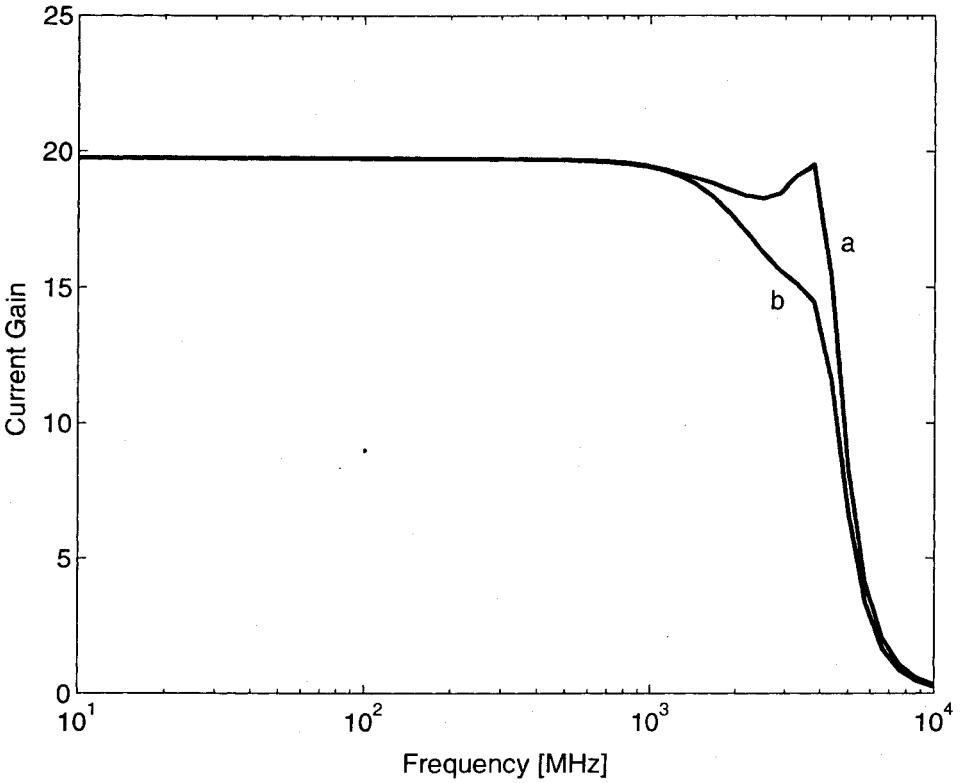

Figure 6.4: Simulation with L at the 2nd-stage input node
[(a) C_d=0.3 pF; (b) C_d=0.5 pF]

shape. This is because that, although the two poles are close to each other, the dominant pole is still at the 1st-stage. If the drop is tolerable, the bandwidth is about f_{-3dB}=4.49 GHz.

(ii) With C_d=0.5 pF: When L_1 and L_2 are placed at the 1st-stage input nodes, the response oscillates. When L_1 and L_2 are placed at the 2nd-stage input nodes, the frequency response still has a large bandwidth f_{-3dB}=3.89 GHz. So if the two poles are close to each other, the advantage to place the inductors at the second stage is the flexibility to tolerate variable input photodiode capacitance.

6.2 Circuit layout

6.2.1 Transistors

It is seen from the schematic that the differential amplifier is fully symmetric including the current reference circuits and the feedback circuits. For differential amplifiers, the matching requirement between the differential branches is very crucial. To overcome the mismatch problem, centroid multi-finger structures are used for all the symmetric transistors such as M_1 and M_2, or M_7 and M_8, etc. The multi-finger structure also helps to reduce the silicon area, and minimize the source-substrate and drain-substrate parasitic capacitance. To reduce the effect of the poly-resistance, the finger is restrained less than 5μm. The amplifying mirrors are derived from duplication. For example, M_3 and M_4 are duplicated from M_1 and M_2. This approach helps reduce mismatches of mirror pairs. The CMOS counterparts have the same number of fingers so that the routing distance between them can be minimized. To equally provide a stable reference current, the reference transistors are placed at the core of the circuit and guarded by guard rings.

6.2.2 Inductors

The lumped model of on-chip inductors shown in Fig. 6.5 is widely adopted in circuit design and simulation. The model parameters are:

- L_s – inductance,
- R_s – metal series resistance,
- C_s – overlap capacitance,
- C_{ox} – oxide capacitance,
- R_{sub} – silicon substrate resistance,
- C_{sub} – silicon substrate capacitance.

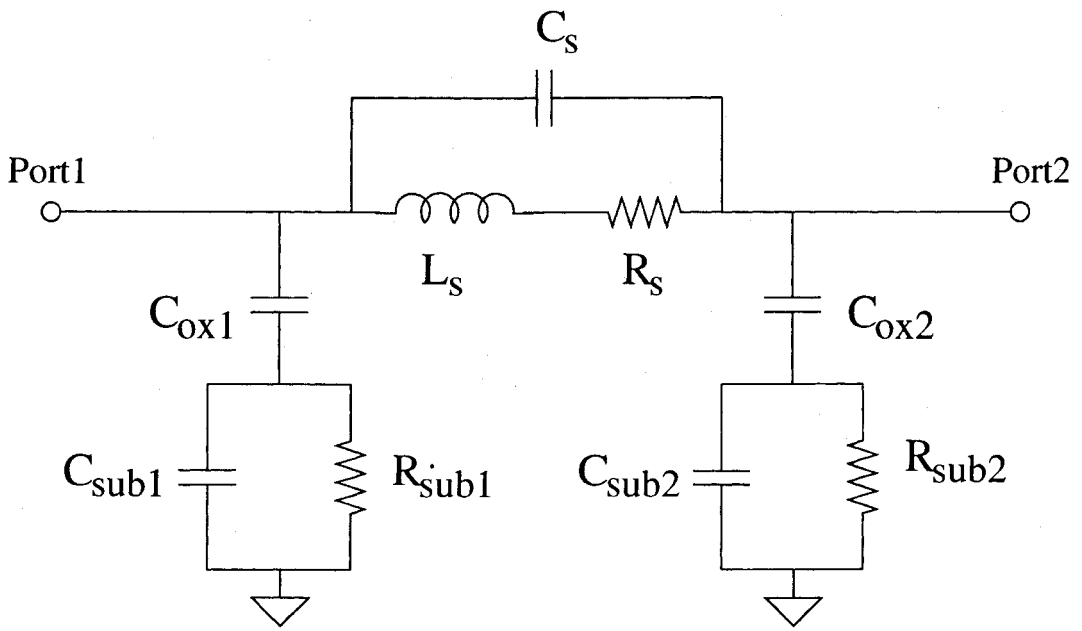

Figure 6.5: Lumped model of on-chip inductors

Usually, C_{ox} and C_{sub} are much larger than C_s. It is worth noting that for a series-peaking inductor, the C_{ox} and C_{sub} in both side are in parallel with the series-peaked capacitances. The series-peaking may also be effective on the C_{ox} and C_{sub}. So the on-chip inductor in very suitable to be employed in inductive series-peaking technique.

As shown in Fig. 6.6, the key layout parameters of the on-chip planar inductors are:

- n – turns,
- w – metal width,
- s – turn spacing,
- d_{in} – inner diameter.

The inductors are implemented using the top metal layer (Metal #6) to minimize the coupling effect on the substrate. In addition, to reduce their effect on other transistors, the two inductors are placed outside the rails of V_{DD} and GND, as shown in Fig. 6.7. The power and ground rails play a guarding role to the core transistors.

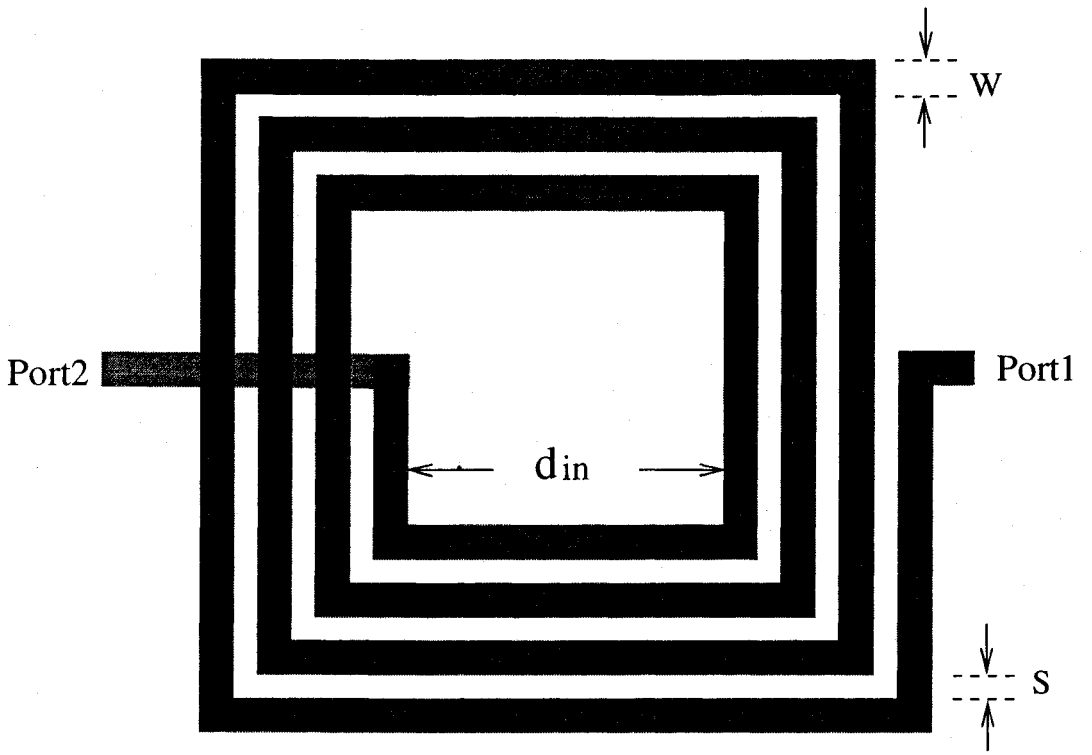

Figure 6.6: Layout of on-chip planar inductor

6.2.3 Routings

To reduce parasitic capacitances, only DC biasing routings and local interconnections use metal #1 and metal #2. The input and output signal go through metal #5. Avoiding long overlap between neighboring metal layers to reduce the coupling capacitances. Differential pair twisting is used to further reduce the signal coupling.

6.2.4 Pads and Power supply

For high-speed applications, the signal pads (for i_{in}^{+}, i_{in}^{-}, i_{o}^{+}, and i_{-}^{-}) are built by the top two metal layers (metal #5, 6) only to reduce the pad-to-substrate capacitance. They are placed at the middle of the die to reduce the signal routings and to minimize the interference from the inductors. The power pads (for V_{DD} and GND) are built by all metal layers. A balanced multi-power supply strategy is used to ensure equal voltage

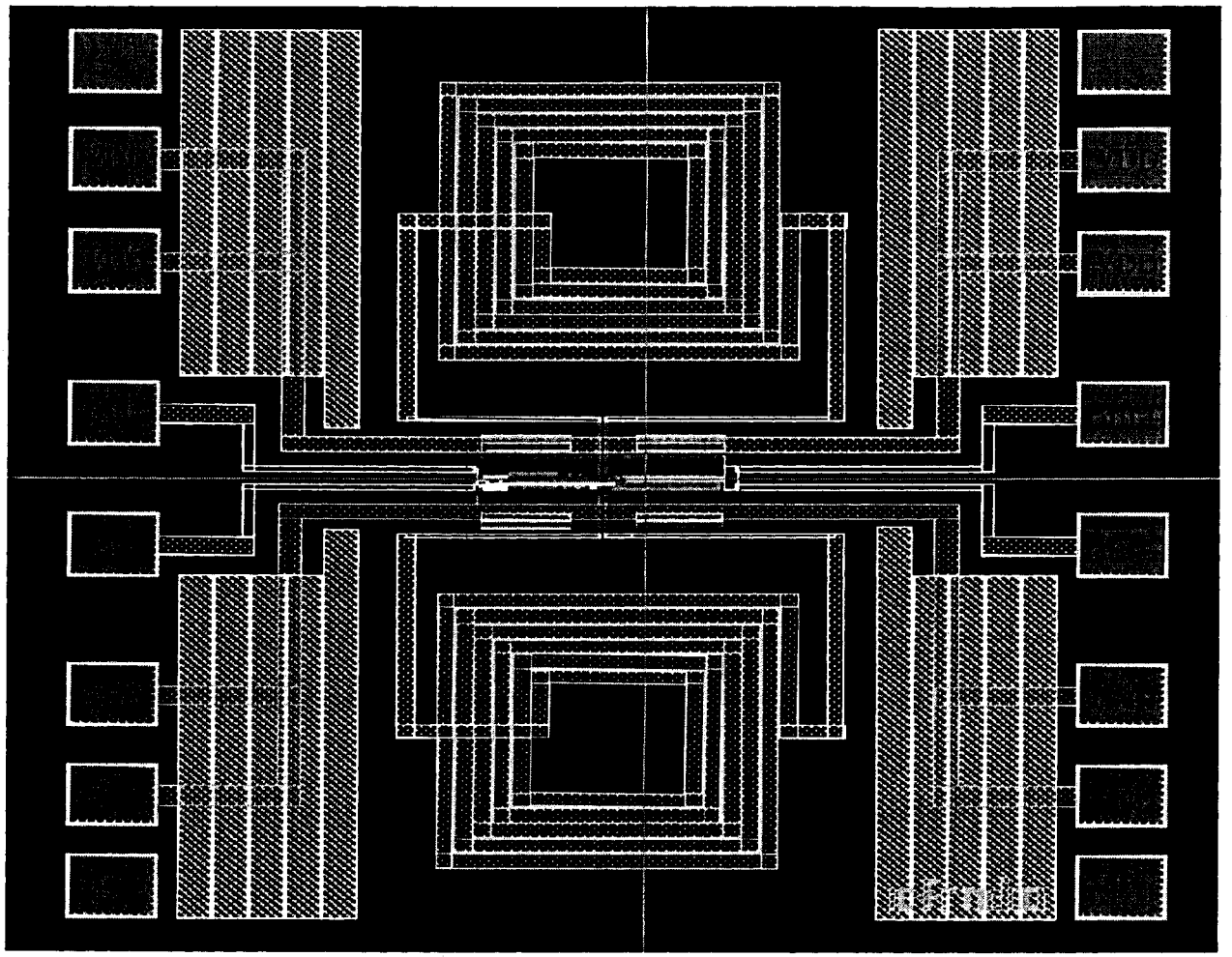

Figure 6.7: Layout of the differential current-mode preamplifier

supply.

Finally, dummy layers are added to satisfy the density requirement. The chip-area is about 1 mm $\times$ 1mm. It is seen that the inductors are very chip-area consumptive as compared with transistors.

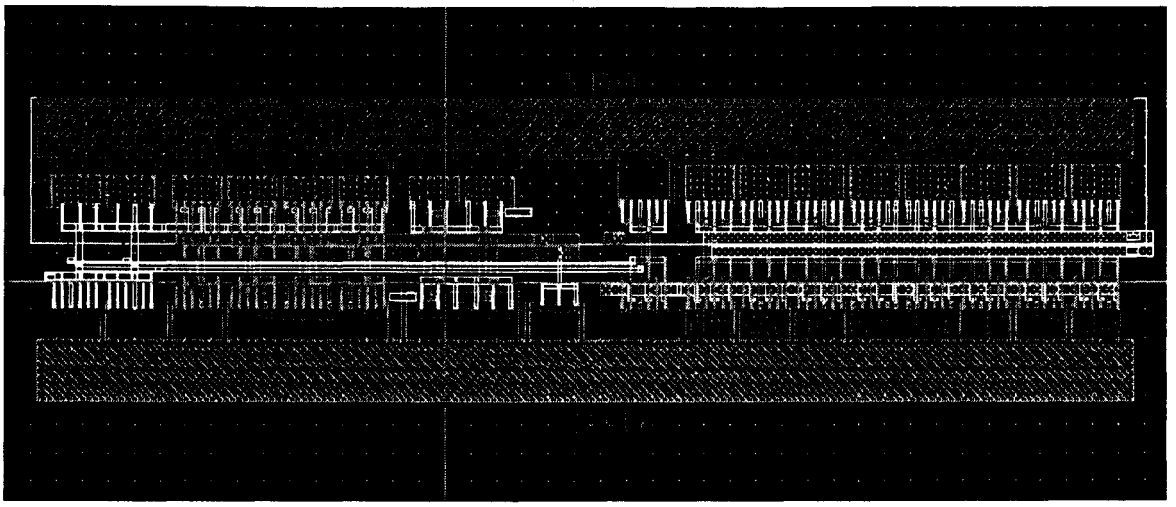

Figure 6.8: Layout of the core circuits

6.3 Simulation Results

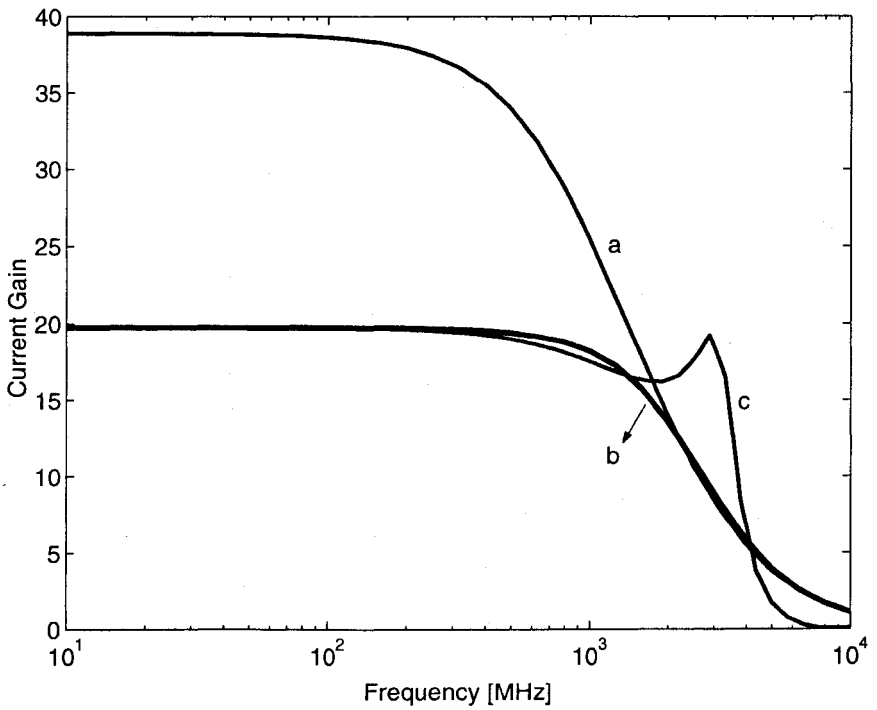

Figure 6.9: Frequency response of the differential preamplifier (with $C_d = 0.3$ pF)

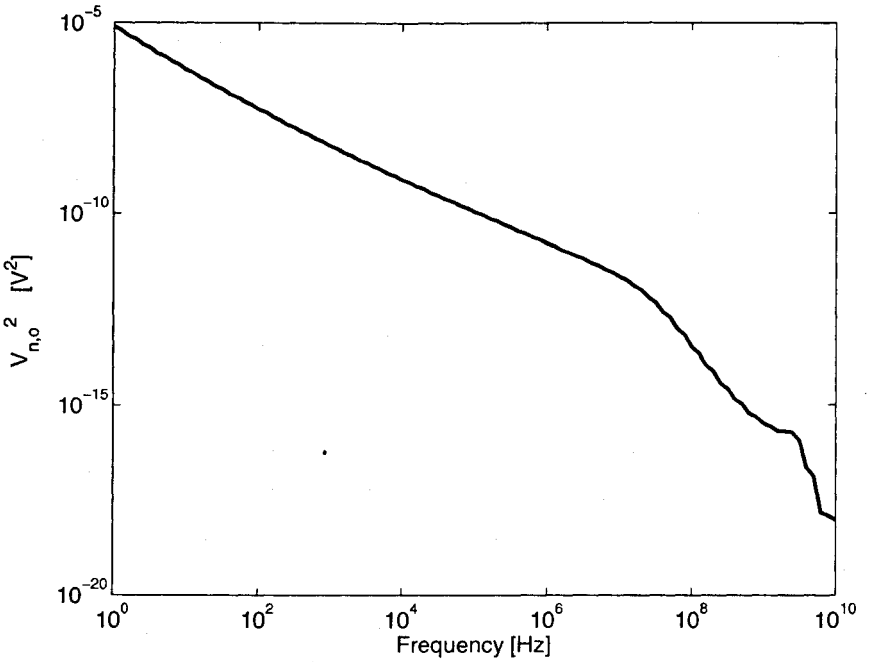

Figure 6.10: Output noise voltage power
(with 50 Ω loads)

As shown in Fig. 6.9, to demonstrate the effectiveness of the bandwidth enhancement techniques, we did the simulation in steps with the layout progress:

(a) The bandwidth of the basic amplifier without feedback and series-peaking is only about 0.87 GHz.

(b) The differential feedback boosts the bandwidth of the layout circuit to 1.9 GHz.

(c) When series-peaking inductors are built and implemented in the whole layout circuit, we get the "drop-raise" frequency response as depicted in Section 6.1. The bandwidth f_{-3dB}=3.5 GHz.

Fig. 6.10 shows the output noise voltage power with 50 Ω loads. The output noise voltage density is 0.14 $\mu V/\sqrt{Hz}$, and the input-referred noise current density is about 70 $pA/\sqrt{Hz}$. Fig. 6.11 shows the transient response of a 5 Gbps data rate input (±0.1 mA current pulse). Table 6.2 shows the key performance parameters of the designed

chip comparing with two recently published designs.

Table 6.2: Comparative performance of the preamplifiers

Design	[39]	[40]	Our design
Topology	Inverter Transimpedance	Common-source Transimpedance	Current-mode
Technology	0.18 μm	0.18 μm	0.18 μm
Supply voltage	2.0 V	1.8 V	1.8 V
Bandwidth	1.5 GHz	2.6 GHz	3.5 GHz
Transimpedance gain	47.9 $dB\Omega$	58.7 $dB\Omega$	66 $dB\Omega$ (with 50 Ω loads)
Input noise current density	9 $pA/\sqrt{Hz}$	13 $pA/\sqrt{Hz}$	70 $pA/\sqrt{Hz}$
Photodiode capacitance	0.275 pF	0.2 pF	0.3 pF
Power dissipation	76 mW	47 mW	85 mW
Maximum signal current	–	–	0.8 mA
Chip area	–	–	1mm × 1mm

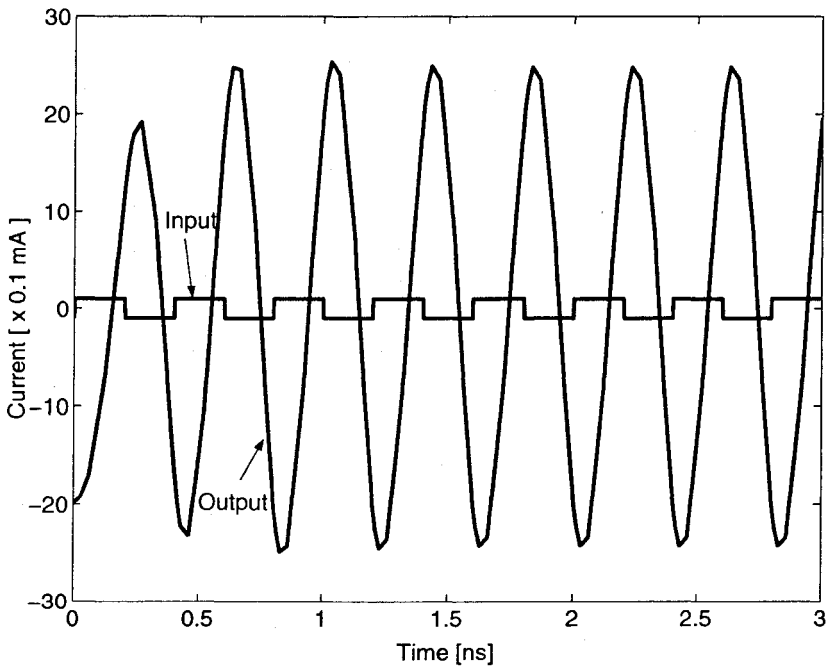

Figure 6.11: Transient response of the differential preamplifier (Date rate = 5 Gbps, C_d = 0.3 pF)

Chapter 7

Conclusions

7.1 Summary and Conclusions

We have discussed a CMOS current-mode approach for the optical front-end design. A new low-voltage fully-differential current-mode preamplifier for optical receivers has been designed and built using TSMC 0.18 μm 1.8 V mixed-signal CMOS technology.

An in-depth comparative analysis of the characteristics of various low-voltage CMOS current-mode circuits has been conducted. It is revealed that most configurations fail to function properly at high frequencies, and the current-mirror amplifier with current feedback offers the best performance.

Two new bandwidth enhancement techniques have been developed and implemented in the design. The inductor series-peaking technique boosts the bandwidth by utilizing the resonance characteristics of LC network formed by placing an inductor in series with the capacitor constituting the dominant pole. It is demonstrated that, in both of the current-mirror amplifier configuration and the optical preamplifier configuration, this technique boosts the bandwidth by about 100%. The current feedback technique increases the bandwidth by taking the advantage of negative feedback theory. A new sampling mechanism has been introduced to acquire the feedback current. It is shown that the feedback boosts the bandwidth by a factor of $(1 + k\beta)$. When both techniques

are employed, the bandwidth is significantly increased by $2(1 + k\beta)$. In addition, the current feedback greatly reduces the value of the peaking inductor. Both the inductor series-peaking and the current feedback techniques do not affect the supply voltage and DC biasing conditions.

In the design, several topologies and design strategies to improve the performance of current-mode circuits have been presented and implemented. It is shown that a two-stage amplifier configuration has a higher bandwidth than that of a single-stage one. The accuracy of current-mode circuits is severely affected by the errors caused by the mismatches of current mirrors. Analysis has shown that a fully balanced configuration can minimize the output offset current by cancelling out bias-dependent output offset current. A current branching mechanism has been adopted to reduce the power consumption of the circuit and increase the output impedance. The proposed preamplifier has a fully differential configuration to minimize the effect of power and ground fluctuations caused by the switching of digital portion of mixed signal circuits. A new negative differential current feedback has been employed to boost the bandwidth and improve the dynamic range of the amplifier.

Simulation results have demonstrated that the designed preamplifier achieves 66dBΩ differential transimpedance gain with standard 50 Ω loads. It operates at the bandwidth up to 3.5 GHz, which matches SONET OC-96 data rate (5Gbps). The designed chip has been granted for fabrication by CMC and is being fabricated by TSMC currently.

7.2 Future Work

Followings are some directions for the future research on optical front-end designs using CMOS current-mode approaches.

- Current-mode circuits usually suffer from high power consumption. Advanced low-

power current-mode techniques are greatly in demand for low-power applications.

- A high output impedance amplifier will significantly improve accuracy. The current-branching mechanism increases the output impedance with the drawback of creating channel length modulation problems. New configurations that have a high output impedance and in the mean time require a low supply voltage requirement are urgently needed.

- Current feedback improves the bandwidth and lowers the input impedance. It, however, also deteriorates noise performance. Low-noise wide-band current-mode circuits are desirable.

- It is seen that the on-chip passive inductors occupy a large chip area and have a strong interference with the substrate. Recently introduced active inductors provide a possible solution to this problem.

Appendix A

Brief SONET Specifications

Table A.1: Three broad application categories in SONET physical layers

Type	System Loss Budget	Distance
Long Distance (LR)	10 dB - 20 dB	> 40 km
Intermediate Distance (IR)	0 dB - 12 dB	> 15 km
Short Distance (SR)	0 dB - 7 dB	> 2 km

Table A.2: Maximum and minimum power requirement at different speeds

-	-	OC-1	OC-3	OC-12	OC-24	OC-48
LR	P_{Tmax} / P_{Rmax}	0 / -10	0 / -10	+2 / -8	0 / -10	0 / -10
	P_{Tmin} / P_{Rmin}	-5 / -34	-5 / -34	-3 / -28	-5 / -26	-5 / -26
IR	P_{Tmax} / P_{Rmax}	-8 / -8	-8 / -8	-8 / -8	0 / 0	0 / 0
	P_{Tmin} / P_{Rmin}	-15 / -28	-15 / -28	-15 / -28	-5 / -18	-5 / -18
SR	P_{Tmax} / P_{Rmax}	-14 / -14	-8 / -8	-8 / -8	-5 / -5	-3 / -3
	P_{Tmin} / P_{Rmin}	-23 / -31	-15 / -23	-15 / -23	-12 / -20	-10 / -18

(P_{Tmax} / P_{Rmax}: Maximum power for transmitters / receivers)
(P_{Tmin} / P_{Rmin}: Minimum power for transmitters / receivers)
(The unit of power level is dBm)

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