ARCHITECTURE AND CONTROL OF AN ELECTRIC VEHICLE CHARGING STATION USING A BIPOLAR DC BUS

By

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Knowing is not enough, we must apply.
Willing is not enough, we must do.

— Johann Wolfgang von Goethe

AUTHOR'S DECLARATION

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Architecture and Control of an Electric Vehicle Charging Station Using a Bipolar DC Bus

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ABSTRACT

DURING the last decade, Electric Vehicles (EVs) have become a reality, and several products that offer a cleaner alternative for transportation have become available on the market. However, despite the numerous advantages of EVs, drivers are still more inclined to use conventional vehicles because they do not see them as a real alternative to transportation. The main reasons for this are the long refueling process using conventional overnight charging and their limited mileage capacity.

Several options have been explored in order to address this reticent behaviour toward EVs. Among these alternatives, the high-power fast charging process of the battery packs holds the potential to facilitate large-scale adoption of EVs. However, to reduce the charging times and also meet all the chal-

lenges and requirements of this growing application, new high-performance architectures must be conceived and developed. Framed by this context, the main goal of this thesis is to contribute the development of fast-charging stations (FCS) configurations, control schemes and coordination methods to facilitate its grid integration.

The increased power levels and the amount of energy involved in transportation, make multilevel power converters as the most suitable topologies for enabling the station. Aiming in this direction, a novel architecture for FCS is proposed, based on the use of a bipolar dc bus enabled by a central Neutral Point Clamped Converter.

Given the selected dc configuration, the balancing of the dc voltages becomes more complex. This is related with the stochastic nature of the EV charging load, leading to unbalanced dc loads. To overcome this issue two balancing methods are proposed based on the use of a balancing circuit that enhances the central converter capabilities.

Moreover, the architecture enables the inclusion of energy storage and generation stages, allowing to extend its functionality. To fully explore the potential benefits of FCS, a third balancing mechanism is developed based on the use of an energy buffer. Without altering its main function, its power consumption can be managed toward aiding the balancing tasks.

Additionally, the inclusion of these optional stages requires a proper management of the energy available in the system. A novel generalized energy management strategy is proposed, that allows to evaluate the economical benefits of the different configurations.

Index Terms

- Electric Vehicles.
- Fast Charging Stations.
- Multilevel Converters.
- Grid Connection.
- Bipolar DC Bus.

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not been the same without your ubiquitous company. Thanks also to all my family members, specially my dear Nonna. This work is dedicated to her.

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LIST OF ACRONYMS

CC	Constant Current Mode
CHB	Cascaded H-Bridge
CV	Constant Voltage Mode
DG	Distributed Generator
DPC	Direct Power Control
DSP	Digital Signal Processor
DTC	Direct Torque Control
ESS	Energy Storage Stage
EV	Electric Vehicle
FCS	Fast Charging Station
FFT	Fast Fourier Transform
FOC	Flux Oriented Control
FPGA	Field Programmable Gate Array
GA	Global Adjustment Rate
HEV	Hybrid Electric Vehicle
HOEP	Hourly Ontario Energy Price
IESO	Independent Electricity System Operator
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
MV	Medium Voltage
NPC	Neutral Point Clamped
PAI	Plane of Array Irradiance
PHEV	Plug-in Hybrid Electric Vehicle
PV	Photovoltaic
PWM	Pulse-Width Modulation
SOC	State of Charge
SVM	Space Vector Modulation
TDD	Total Demand Distortion
THD	Total Harmonic Distortion

V2G	Vehicle to Grid
VOC	Voltage Oriented Control
VSC	Voltage Source Converter

CHAPTER I

INTRODUCTION

THE ADVENT of Electric Vehicles (EVs) is causing a profound transformation in the automotive industry. The differences in the manufacturing process, additional safety concerns, different requirements for the materials involved, and so on have changed the way the car industry operates. This changes are also reflected in different disciplines, such as energy conversion, because power electronics has a fundamental role in both EV traction and battery recharging processes. Several studies on traction have been conducted in order to provide lighter and smaller converters, smoother dynamic response, improve the efficiency and reliability of the equipment, which are not excessively distant from the conventional requirements in most motor drive applications. The fast charging process of the batteries, however, implies fundamental changes with conventional high-power applications because, aside from the vehicle, this process also involves the utility grid. In addition, the low-voltage levels of the battery packs increases the complexity, as typically these applications require medium voltage (MV) levels, hence impose a trade-off between the current stress of the switching devices and the step-down effort of the battery charger.

However, before delving deeper into details of this growing application, the following terminologies and standards definition must be considered to

fully understand the context of the dissertation.

1.1 EV Technology Definitions

The term EV is often used to designate different vehicle technologies, even though they have some substantial differences. To clarify the concepts used in this proposal the main types of EVs available today are defined as follows [1]:

Hybrid Electric Vehicles (HEV) This technology uses the electric power of batteries to improve the fuel efficiency of their internal combustion engine. The electric power to charge their batteries does not come from any external source.

Electric Vehicle (EV) These vehicles run on a purely electric motor which is powered by batteries. Refueling is done by plugging in the vehicle to the grid. The term *battery EV* is also used in the literature for this type.

Plug-in HEV (PHEV) As their name suggests, these vehicles can run on gasoline , similar to the HEVs, and recharge their batteries by plugging in the vehicle to the grid, similar to EVs. The result is increased driving range and reduced fuel usage and emissions.

This dissertation is mainly concerned with EV technology, although the same principles apply to PHEVs. For this reason, the remainder of this study exclusively considers the EV family.

1.2 Overview of the EV Charging Process and Existing Standards

A crucial part of the operation of the EVs is the recharging of their battery pack. This process can be carried out in two different ways: conductively

or inductively. The first charging method uses electrical contact between the charge port of the vehicle and the charger connector to transfer the energy into the battery pack. The second method uses wireless energy transfer through electromagnetic field coupling, eliminating the plug-in cord [2, 3]. This type of charger has been explored for Level I and II devices, and still under development and would not be discussed in detail here.

By contrast, conductive charging has already been adopted by the EV industry, including mainstream EV manufacturers. Depending on the rate at which the EV battery is charged, conductive chargers can be generally classified into slow chargers and fast chargers. The slow or conventional chargers are able to recharge the battery in 8 hours, while the fast chargers can do this process within 30 minutes. More specifications on the power levels, charging times for the available charging methods can be found in some of the existing charging standards.

To regulate and standardize the conductive chargers several organizations, such as the Institute of Electrical and Electronics Engineers (IEEE), the Society of Automotive Engineers (SAE), the International Electrotechnical Commission (IEC), are preparing standards to regulate the utility/customer interface.

1.2.1 SAE J1772 Standard

The SAE has published the standard SAE J1772^{TM} [4], which defines practices regarding the conductive charging architecture for electric vehicles. This standard defines three charging methods: ac Level I, ac Level II, and ac Level III, aside from the dc fast charging levels, which are still under development. The details of the charging levels included in SAE J1772 are presented in Table 1.1.

Levels I and II in general fall into the category of slow charging, except for Level II dc charging. A European standard IEC 62196 has also been developed promoting different charging levels (up to 690V ac and 1000V dc) that

Table 1.1. SAE charging configurations and ratings terminology (as in [4])

Charging Method	Input Voltage	Charger Location	Power Level	PHEV (EV) Charging Time
AC Level I	120 V	On-board	1.4 kW, 12 A 1.9 kW, 16 A	7 (17) hours
*DC Level I	200-450 V	Off-board	36 kW, 80 A	0.3 (1.2) hours
AC Level II	208-240 V	On-board	19.2 kW, 80 A	0.4-3 (1.2-7) hours
*DC Level II	200-450 V	Off-board	90 kW, 200 A	10 (20) min.
*AC Level III	208-240 V	On-board	96 kW, 400 A	(15) min.
*DC Level III	200-600 V	Off-board	240 kW, 400 A	(<10) min.

*Not finalized

1) EV (25 kWh usable pack size) charging always starts at 20% SOC, faster than a 1C rate will also stop at 80% SOC instead of 100%.

2) PHEV (10 kWh usable pack size) can start from 0% since the hybrid mode is available.

are analogous to those in SAE J1772. Additionally, there is an ongoing coordination between the two standards in order to develop a Combined Charging System (CCS) [5].

1.2.2 CHAdeMO Standard

Other than the SAE and IEC standards, an association named CHAdeMO proposed a quick charging method as a global industry standard. The name CHAdeMO is an abbreviation of *Charge de Move*, equivalent to *charge for moving* [6].

CHAdeMO was formed by Tokyo Electric Power Company (TEPCO), Nissan, Mitsubishi and Fuji Heavy Industries. Toyota later joined as its fifth executive member. TEPCO has developed a patented technology and a specification for high-voltage high-current automotive fast charging via a dc fast charge connector from the Japan Automotive Research Institute (JARI). The connector from JARI is apparently the basis for the CHAdeMO protocol. The connector is specified by the Japan Electric Vehicle Standard (JEVS) G105-

1993 from the JARI.

The maximum output compatible with CHAdeMO protocol is 500V/125A, with power reaching 62.5kW.

At present, this standard is gaining wide acceptance, and several leading industrial manufacturers are commercializing CHAdeMO standard dc fast chargers (*e.g.*, ABB-Terra 53CJ, Fuji Electric - FRCH50B-2-01, Siemens - CP300D3xB05-4xxx, and so on). According to [6], over 1,500 chargers and more than 57,000 compatible EVs are available on the road around the world.

1.3 Background of the Work

Both, EVs and PHEVs have emerged as the most likely successor to conventional internal combustion engine vehicles. In the past few years, the sales of these vehicles have been constantly increasing, as shown in Fig. 1.1, and this increasing trend is expected to continue in the coming years. Nevertheless, the shortcomings of these these vehicles must be solved before they can become a real alternative to transportation. The long refueling process of their

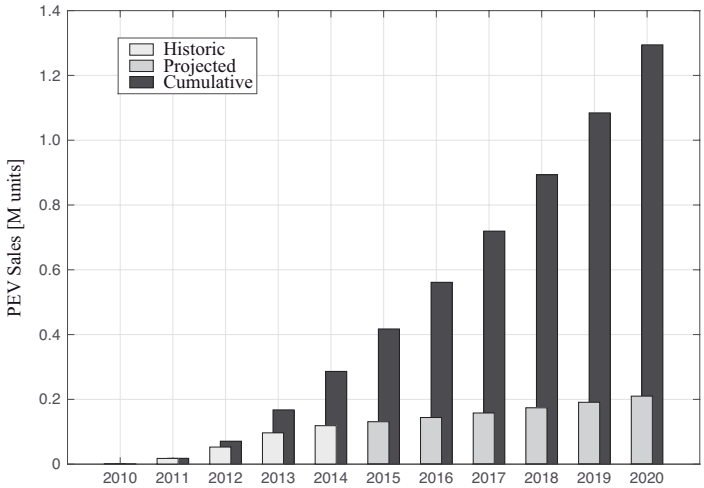


Figure 1.1. Cumulative and annual historical-projected EV and PHEV sales in the U.S. [7].

batteries, limited mileage capacity, lack of public fast-charging infrastructure are the main barriers to the widespread usage of EVs. However, changes are also required also from the grid side to allow a large-scale penetration of this technology, as electricity demand will grow accordingly. No real threat to the utility grid exists at present, because the automotive industry is still mainly sourced by the gasoline supply chain; however, a gradual shift to larger electricity consumption for transportation purposes will occur, and if this issue is not addressed properly, the electric system will be negatively affected (*e.g.*, demand and energy price increase, voltage stability decreased, power quality issues, and so on) [8, 9].

In order to address the effects of the large-scale adoption of these vehicles on utility systems, several studies have been conducted [10–14], most of them based on the conventional slow charging process of batteries. The focus in on conventional charging mainly because it is expected to be the preferred charging method [9]. Also, due to the fact that fast charging process of the EV batteries is still not a widespread practice among the owners, due to the lack of facilities and misconceptions regarding the impact of this process to the batteries. However, fast charging methods remain essential to the large-scale adoption of EVs, given that they will provide more flexibility to the drivers, particularly in terms of occasional longer trips, thereby addressing range anxiety [15–18].

An alternative that enables fast charging is in the form of fast charging stations (FCS), which are similar to conventional gas filling stations. The concept of FCS refers to high-power fast chargers that are installed off-board. The structure of these charging stations can either be with an ac-bus, where each charging unit is fed by its independent ac-dc stage, or each unit connected to a common dc bus enabled by a single ac-dc stage with higher power ratings [19, 20]. Currently, fast charging is only enabled by standalone units, each of which has its independent rectifier stage using the ac-bus concept.

However, considering the dc nature of the loads, the common dc bus configuration appears as the viable solution for utility scale adoption and also

presents advantages in terms of cost, efficiency and size, as fewer conversion stages are needed [19, 21, 22]. Moreover, this structure facilitates the integration of distributed generation or energy storage systems [19, 21].

The central converter ac-dc stage plays a fundamental role in this charging architecture, and is desirable to provide several features as low distortion operation, high power capability, and fully adjustable power factor. It can also simultaneously reduce the size of the input filters and the number in both active and passive components. This concept will be fully studied and developed during the succeeding chapters.

1.4 Dissertation Objectives

The connection to MV ac grids of EV FCS it is not a straightforward task because of the particularities involved. Unlike conventional multilevel converter applications, the loads in the system are volatile and present a stochastic behavior, therefore, the control scheme and the balancing techniques need careful designing. With the aim developing a neutral point clamped (NPC) fed FCS, the main objectives of this dissertation are as follows.

1. To develop a common bipolar dc bus fast charging architecture that allows the grid integration of several high-power fast charging units. This structure will be based on the NPC converter topology, with the aim of guaranteeing the proper balancing of the buses in the system under severe asymmetrical loads.

2. To establish a formal definition of the unbalanced operation limits provided by the central converter modulation stage and propose different balancing methods to guarantee the dc voltage balance regardless the load conditions.

3. To provide simulation results that verify the proposed architecture and control schemes. To complete the validation of the topics, the imple-

mentation of a low-voltage prototype of a NPC-based FCS will for the experimental validation.

To provide simulation results that verify the proposed architecture and control schemes and to complete the experimental validation of the topics through the implementation of a low-voltage prototype of an NPC-based FCS.

4. To propose a generalized energy management strategy that enables full exploration of the potential of the proposed architecture. The idea is to quantify the economic benefits of the inclusion of energy storage stages (ESS) or generation units in the FCS.

1.5 Dissertation Outline

The present dissertation consists of six chapters, which are organized as follows.

Chapter 1 covers the definitions related to EV technology, existing charging standards and provides the background of the study.

Chapter 2 describes in detail the FCS architectures, the most promising converter topologies applied as a central rectifier stage, and the state-of-the-art control schemes for grid-tied converters.

Chapter 3 proposes the bipolar dc bus concept for the fast charging application and introduces the 3L-NPC converter as the grid-tied converter. A formal definition of the balancing current of the NPC is provided because of the inherent circulation of currents through the neutral point of the converter. Finally, two dc voltage balancing approaches are proposed in order to enable the asymmetrical operation of the charging station, through the use of an additional balancing leg. Validation is performed in both simulation and experimental environments.

Chapter 4 presents a different balancing approach given that the system allows the straightforward inclusion of energy storage stages. Assuming that

the system considers an energy storage stage, its operation can be used toward the complimentary balancing tasks that the NPC requires. To do so, a three-level dc-dc stage is employed as the interface of the energy storage stage, as it requires access to both of the dc buses. This approach reduces the hardware requirements on the central converter, allowing the use of off-the-shelf equipment. Validation is also performed in simulation and experimental environments.

Chapter 5 introduces a generalized optimization method based on linear programming, which aims to reduce the operating costs of the system by the use of an energy buffer and, if available, distributed generators (DGs). Energy management is performed using a linear optimization method, which provides the optimal regulation based on the forecasted EV demand and the local electricity price. The optimization algorithm schedules the charging and discharging of the energy storage system depending on the actual electricity price. In order to study the effectiveness of the proposed strategy, sensitivity studies are performed.

Chapter 6 summarizes the main contributions and conclusions of the present work. Directions for future studies are also suggested.

CHAPTER II

OVERVIEW OF THE CHARGING STATION CONCEPT

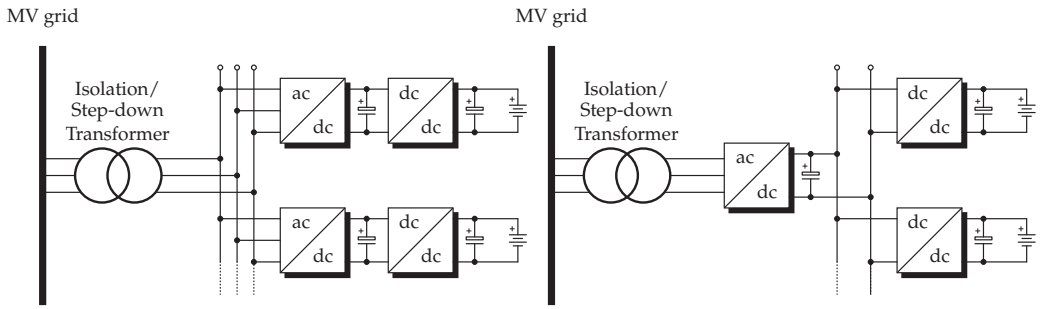
THE DEVELOPMENT of a vast fast charging infrastructure network has a fundamental role in the large-scale adoption of EVs as the main mean of transport, which in turn dramatically reduces the charging times of the batteries. Regardless fast charging becomes the main alternative for replenishing batteries or remains as a complimentary process to conventional overnight charging, the availability of quick-charge stations in different parts of the cities will provide drivers more flexibility in using their cars, address range anxiety, and allow occasional longer trips without the need of batteries with larger capacities.

Nevertheless, the fast charging process implies challenges not only to the vehicle itself but also to the utility system. To start with, the power rating involved in the fast charging process, which is expected to be higher than 50 kW, makes it unlikely to be adopted as an on-board solution because of the requirement for larger, heavier and costly additional equipment [3, 23]. Furthermore, studies show that conventional overnight charging (ac levels I and II) are expected to remain as the preferred charging method [9]; thus, installing an additional high power charger on-board is not needed.

On the other hand, quick charging is not suitable in residential applications for several reasons. First, dedicated equipment must be installed in the homes, as a result of the increase in the power consumed by the charger in order to reduce the charging time of the battery. In addition, this power consumption exceeds the typical power ratings of the conventional appliances. Moreover, a three-phase power connection is required because of the power levels involved. Furthermore, the electric system in these areas is not designed for high power levels; therefore, if fast chargers are installed in residential areas, then transformers and other distributions elements need to be replaced; otherwise they will be damaged [1]. This additional infrastructure makes the cost of the fast charging solution excessive, so that a different approach is required.

Finally, from the perspective of the utility grid, a large-scale penetration of EVs results in increased power demand, thereby leading to additional coordination methods of absorbing the EV charging load, and does not merely requires having sufficient generation capacity [12]. The reason for this is the stochastic behavior of the EV load, and if this issue is not addressed properly, the actual electric system will be unable to satisfy this demand. For example, an larger EV fleet will require additional operating reserves in order to cope with the increased power demand and the uncertainty associated with the EV charging [9]. This also affects the transformers and lines loading and the protection settings. In order to minimize these effects the addition of generation or energy storage units becomes necessary.

These reasons justify using the concept of the charging station as an enabling alternative for EV fast charging. These stations are similar to petrol stations, meaning that are commercial facilities composed by several off-board high-power chargers located in public places throughout the city (*e.g.*, parking lots, work, shopping locations or rest stops along highway). In this way, the load is concentrated in strategic points, which can be coordinated with the utility operator (*i.e.*, retrofit distribution and transmission equipment, discourage the demand in congested nodes, medium voltage (MV) connection, and so on). This concept allows the driver to choose its preferred



(a) Common ac bus concept (b) Common dc bus concept

Figure 2.1. Charging station architectures.

charging method for his vehicle. An additional charging possibility alleviates range anxiety, maximizes the use of EV batteries, and most importantly, provides the EV user a regimen equivalent to that of conventional cars.

2.1 Concept of Fast Charging Station

As established in the previous sections, the fast charging of plug-in vehicles might not be conceivable as an on-board solution, due to cost, size and weight constrains in the vehicle. Therefore, studying the concept of a public installation with installed off-board high power chargers that operates as a filling station is relevant. These stations will provide EVs the equivalent of a *fuel stop* by feeding their batteries with dc currents, which recharges the car in the shortest possible time [24]. This concept, along with emerging battery technologies that accept higher charging rates and several thousands of charging cycles [25], sets up fast charging as a realistic possibility [26, 27].

Two possibilities can be identified for the station architecture, as shown in Fig. 2.1. The first uses the secondary windings of the step-down/isolation transformer as an ac bus, where each load is connected to the bus via independent ac-dc stages. The second uses a single ac-dc stage in order to provide a common dc bus for all the loads of the system.

2.2 Common AC Bus Architecture

One alternative for the FCS architecture is the use of a common ac bus, as suggested in Fig. 2.1a. In this structure, each charging unit has its own rectifier stage that is connected to a common ac coupling point in the secondary windings of the step-down transformer. This architecture represent a simpler concept because it has been used for years, and well-developed standards and technologies are available. Furthermore, it needs lower power rating front end stages (which can be either passive or active).

However, the presence of several battery chargers, with independent rectifier stages and inherent low power-factor operation, may produce unwanted harmonic effects on the utility grid [11, 28], particularly for high power fast chargers. Moreover, the cost of several converter units with lower power ratings is higher than that of a single high-power converter unit, due the need of several filter sets, control stages and sensors.

In addition, in the case of having distributed generation units in the station, such as PV or fuel cells, or even the usage of energy storage systems, which generate energy at dc, will also require their independent ac-dc stage, thereby further increasing the number of the conversion stages in the system and, consequently, the cost and complexity of the system.

2.3 Common DC Bus Architecture

The alternative architecture described here is the use of a single ac-dc stage with a higher power rating to provide a common dc bus, as illustrated in Fig. 2.1b. This bus feeds several battery chargers and provides a more flexible structure, which can easily integrate distributed renewable energy conversion systems, or energy storage devices, since these systems are essentially dc, as depicted in Fig. 2.2. Moreover, no issues with synchronization nor reactive power exists. These features allow the charging station to act as an intelligent system that can mitigate the negative effects of a deeper EV pene-

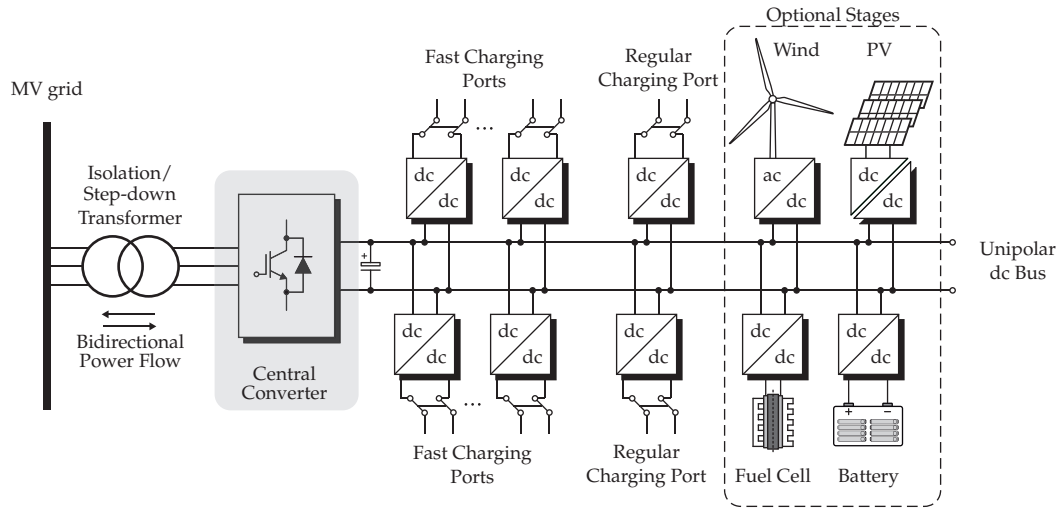


Figure 2.2. Charging station concept.

tration in the conventional utility grid, and also to be a part of a future smart grid.

The system in Fig. 2.2 is better in reducing device count and costs in comparison to the ac bus architecture, as a result of the fewer power conversion stages requirement, but at the expense of an increase in the power rating of the central converter. The lower number of power conversion stages also improves the overall efficiency of the charging station. However, the higher power ratings of the single rectifier unit lead to more stringent requirements by the grid code, in terms of harmonic components amplitude and total harmonic distortion (THD). Moreover, limits are imposed on the switching frequency on the devices because the switching losses become relevant when the power is in the megawatt range. Another issue with the dc grid concept is that it requires more complex protection devices than the ac grid, because no zero cross points of the voltage exists [29].

In general, a much lower number of converters is needed in comparison to the ac bus architecture, making the system simpler. Moreover, energy delivery at dc is characterized by reduced losses and voltage drops in lines [21]. Furthermore, assuming that the dc system has generation units,

in case of the abnormal operation of the utility grid, the dc system can be switched to stand-alone operation, and the loads are supplied with the generated power [22].

On the other hand, regarding to the application, the current development in dc charging standards [4, 6] also supports the idea of a centralized charging station serving as an active front end and providing dc power to several battery chargers, which can either be semi-fast or fast solutions. In addition, this allows to concentrate this potentially large loads in strategic places to minimize their impact on the grid, as opposed to the case of residential fast chargers that are randomly connected in different areas. For these reasons, the remainder of this dissertation focuses on the dc bus architecture and its feasibility in medium-voltage high-power ratings.

2.4 Central Converter Topologies

The central converter stage has a fundamental role in the dc charging architecture of Fig. 2.2, and is desirable to provide several features, such as distortion-free operation, fully adjustable power factor, reduced size of the input filters, while simultaneously featuring a reduced number in both active and passive components [23, 30].

2.4.1 Two-Level Voltage Source Converter

One of the most widely used topologies in the industry is the Two-Level Voltage Source Converter (2L-VSC), whose power circuit is presented in Fig. 2.3. As shown in the figure, the power circuit is composed by an array of six switching devices, typically insulated-gate bipolar transistors (IGBTs) and a capacitor as a dc link. The presence of these active switches, along with a proper control scheme, generates sinusoidal currents at the input side, a fully adjustable power factor, and a bidirectional power flow [31]. This converter also steps up the voltage to higher values than the input phase voltages. This

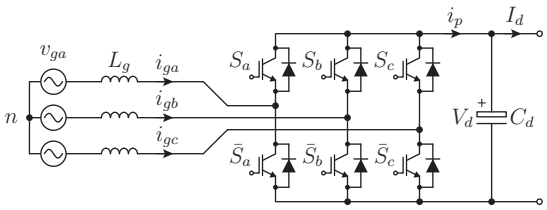


Figure 2.3. Grid-connected two-level voltage source converter.

features make this topology a valid alternative as the grid-tied converter for a high power off-board charger [30], or as the central converter of the charging station.

Both carrier-based pulse-width modulation (PWM) and space vector modulation (SVM) can be applied to generate the switching patterns for the 2L-VSC [32]. In addition, variable switching frequency methods, such as table or prediction-based methods, can also be used [33, 34]. As the names suggests, this converter generates a binary pulse train, which alternates between 0 and V_d whereas the line-to-line voltage presents a three-level waveform. This impacts the total harmonic distortion (THD) of the input current, as larger active/passive filters or higher switching frequencies are needed in order to meet the limits imposed by the grid code. This configuration typically operates at low ac voltage (690 V) allows a power rating of up to 0.7 MW, without paralleling switching devices or converters, limiting the number of chargers that the station is able to feed. To reduce the current stress on the devices, the converter can be connected to higher ac voltages; however, this also implies a larger dc voltage as well, thereby increasing the step down effort of the dc-dc stages of the chargers, which is not desirable.

Moreover, assuming the megawatt range for these stations is assumed to demand higher power ratings for the central grid-tied converter, and this topology will not be able to fulfill power ratings, power quality and efficiency requirements. Therefore, the use of several two-level converters is needed, which also means more power electronics, control systems, sensors, filters, larger size, and higher cost.

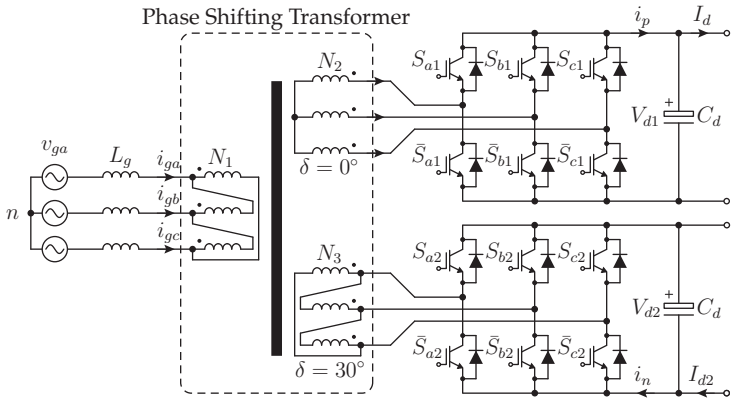


Figure 2.4. Grid-connected dual two-level voltage source converter.

In order to extend the power ratings of this converter topology, some alternative configurations can be used, which are based in the use of multi-winding transformers. A phase shifting transformer is included to share the power between two ac-dc stages, as presented in Fig. 2.4. Each 2L-VSC stage is connected to a different secondary winding of the transformer. The presence of this transformer, along with a symmetrical gating pattern of both converters, leads to the significant mitigation of certain harmonic components, in this case those with order $6n \pm 1$, with n odd, which is similar to that achieved when using a diode front end in the 12-pulse configuration [32]. The dc output of the converters, it can be either connected in parallel, to have a single dc bus; or in series to generate a split dc bus. The latter configuration is covered in depth in the remainder of the dissertation.

Although the phase-shifting transformer significantly improves the power quality at the grid side, the limited power that this topology is able to withstand without paralleling devices is still low for the application. The result is a higher cost of the grid interface assuming a 2 MW charging station, as the paralleling of devices or converters may be needed. In addition, the presence of the transformer is not optional because it is required for the harmonic improvement at the ac side, which results in the higher cost and size of the station even if the fast chargers provide isolation to the battery.

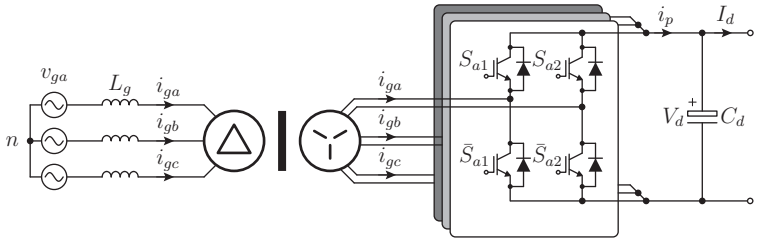


Figure 2.5. Grid-connected single dc-link H-bridge converter.

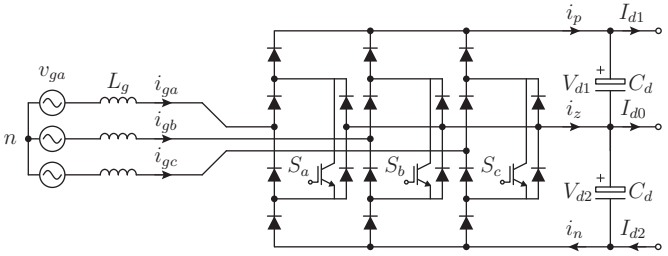


Figure 2.6. Grid-connected Vienna rectifier.

Finally, a different approach is presented in [35], where open-end secondary winding transformers are used, along with two 2L-VSC stages, in order to generate a single dc-link H-bridge converter, as presented in Fig. 2.5. This approach leads to a multilevel waveform generated at the ac-side, which improves the power quality while eliminating any possibilities of asymmetrical dc loads. However, its power handling capabilities are still limited for the intended power ratings of the FCS.

2.4.2 Vienna Rectifier

Some authors suggest that in the case of fast charging applications, the bidirectional operation is not mandatory, considering that its main functionality is to charge the batteries as quick as possible and also because vehicle-to-grid (V2G) operation is still not considered as a short term solution. Therefore, the bidirectional rectifier stage is replaced by a Vienna converter [23,30]. The power circuit of the converter is shown in Fig. 2.6.

This topology shares the operating principle of stepping up the voltage

with the 2L-VSC. It features a lower active switching devices count, at the expense of sacrificing the reverse operation characteristics. Moreover, this topology features a highly sinusoidal input currents, three-level voltage waveform, reduced voltage stress in the devices, and a high power factor operation. The input filter size is reduced because of the multilevel voltage waveform [36].

The control scheme is based on controlling the magnetization of the inductor by using high-frequency PWM [30]. One important advantage is that this topology offers operation without a neutral connection. Furthermore, the commutation of diodes takes place as soon as the switches are turned off, which removes any dead-time problems [36]. The disadvantages include the lack of regeneration and relatively high assembly effort exhibited by the circuit when a realization with discrete components is considered. In addition, the high switching frequency required limits its potential for high-power applications.

2.4.3 Multipulse Rectifier with DC Active Power Filter

Another approach is proposed in [19,37], where a non regenerative 12-pulse decoupled rectifier system provides the common dc bus for a 1.1 MW charging station. A dc active power filter (DC-APF) stage is also included to eliminate the harmonics at both dc and ac side. The circuit diagram is shown in Fig 2.7.

This harmonic cancellation is achieved through the triangular shaping of the currents i_p and i_n. The result is a grid-tied converter with reduced complexity and cost, which generates high-quality sinusoidal input currents. The resulting converter complies with the limits imposed by IEEE 519-1992 standard and produces a dc bus with reduced voltage ripple and improved dynamics.

This proposal also includes an ESS, in order to design the converter such that it withstand only the average demanded power, while this additional

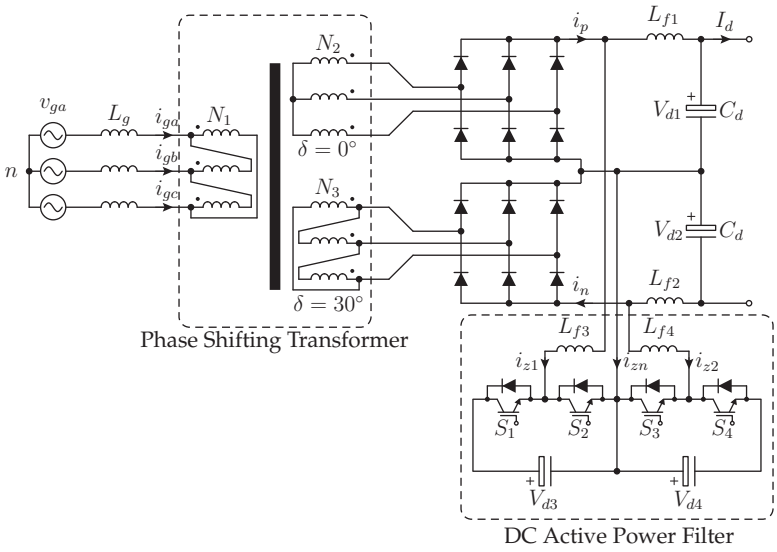


Figure 2.7. Grid-connected multipulse rectifier with dc active power filter.

stage provides the extra power during peak instants.

However, the inability to control the dc bus voltage and the lack of power factor adjustment and regeneration capabilities limit the potential of the charging station, given that it becomes unable to inject power into the utility grid or perform reactive power compensation.

2.5 Medium Voltage Converter Topologies

The remainder of this section gives an overview of the most relevant high-power converter topologies that are widely used in the industry. However, despite the potential benefits of these topologies, they have not been fully applied to produce fast charging solutions.

2.5.1 Cascaded H-Bridge Converter

Among the multilevel converters topologies, the Cascaded H-Bridge (CHB) is currently one of the most widely used topologies in MV applications. As

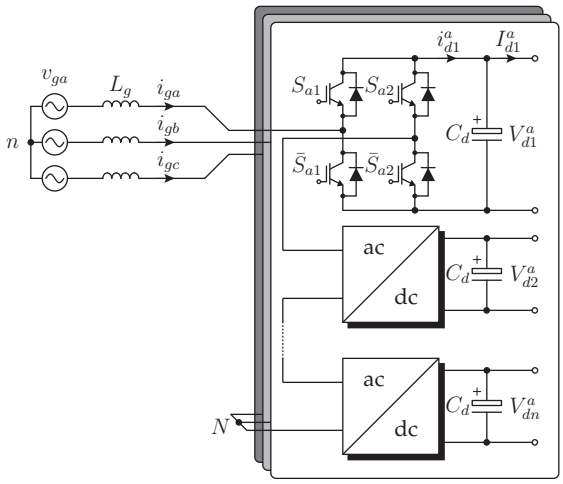


Figure 2.8. Grid-connected cascaded H-bridge converter.

its name indicates, the CHB is composed by the series connection of single-phase full-bridge converters (HBs). Each one of this cells enables an independent dc voltage, as displayed in Fig. 2.8. One of the main features of the CHB is its modularity; it can easily reach medium voltage by adding more power cells to each phase. This particular topology is commercially available to reach different voltage levels: 3.3 kV (three cells per phase), 6.6 kV (six cells per phase) and up to 11 kV (eleven cells per phase).

In [38], a CHB based architecture is proposed to enable the fast charging of several EVs. The architecture uses the CHB as the grid interface, which is directly connected to the MV ac-grid, intermediate ESSs as power buffers, and interleaved dual-half-bridge dc-dc converters as fast charging units. No issues with the asymmetrical operation have been found because of the connection of the dc-dc stages. This configuration makes the three-phases of the converter to always deliver the same power. However, to increase the number of charging units 3 additional cells, with their corresponding energy buffer and isolated dc-dc stages must be considered, which consequently limits the modularity offered by the CHB.

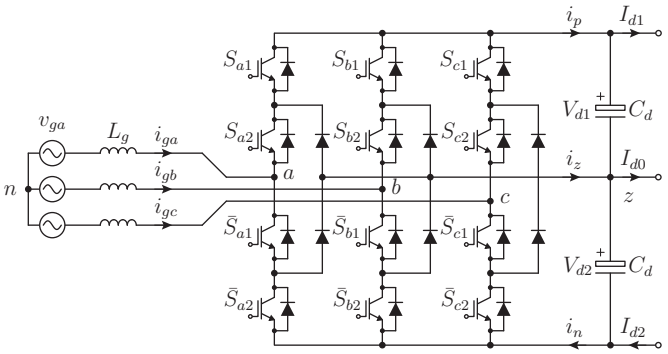


Figure 2.9. Grid-connected three-level neutral point clamped converter.

2.5.2 Neutral Point Clamped Converter

The three-level Neutral Point Clamped converter is currently one of the dominant topologies in newly developed MV drives. Its wide presence in the industry makes it a natural candidate for the selected architecture. Originally introduced at the beginning of the 1980s by Nabae *et al.* [39], the three-level NPC is considered to be the first multilevel converter to be used in MV applications. At present, commercial NPCs reach voltages in the range of 2.2-6.6 kV, within a wide power rating range (3-50 MW), and these NPCs can be found in several applications, which are used either as an inverter that feeds an ac load or as an active front-end converter that interfaces with the utility grid [40].

Regarding its structure, each phase of the NPC converter is composed of four hard commutation devices, which can either be IGBTs or integrated gate-commutated thyristors (IGCTs), and two diodes connected to the neutral point, as displayed in Fig. 2.9. The presence of these diodes, which are connected between the neutral point of the converter z and the middle point of the indirect series connection of the hard commutated devices, allows the connection of the phase with this neutral when the inner devices are turned on. The result is a third voltage level in the synthesized phase voltage; thus, the converter is able to generate $-V_{d2}$, 0 and V_{d1}. The phase voltage can be

modeled after the gating signals:

$$v_{kz} = V_{d1} S_{k1} S_{k2} - V_{d2} \bar{S}_{k1} \bar{S}_{k2}, \text{ where } k = a, b, c. \tag{2.5.1}$$

The three phases of the converter are able to generate 27 space vectors, only 19 of which are different. These redundancies are employed to balance the neutral-point voltage. The control of this voltage represents a critical aspect for the NPC. Otherwise, the generated voltage becomes distorted, thereby reducing the power quality and also potentially damaging the switching devices. For this reason, several balancing techniques are presented in the literature [41–44].

The selection of this topology as the central grid-tied converter of the charging station is due its higher grid power quality (three levels in the voltage waveform), superior harmonic performance (reduced THD), lower switching frequency, MV operation, lower transformer ratio and the possibility of having either a unipolar or bipolar dc bus [39, 41]. Besides, it offers the possibility of scaling up the power ratings for a larger charging station. Finally, if the charging units provide isolation, a bulky and costly isolation transformer at the grid side is not mandatory for MV operation. This is because the NPC structure reduces the voltage stress on the devices to half of the dc voltage, while the safety isolation of the battery pack is performed by the dc-dc stage.

As mentioned earlier, if the system is used as a unipolar dc bus, then the unbalancing problem is not too serious and can be solved by the modulation stage or by simple balancing mechanisms [41, 43, 44]. The reason for this is the fact that there are no excessive currents flowing through the neutral point, so the balancing efforts required are minimal. However, if the system is provides a bipolar dc bus, and each dc voltage feeds different loads, an unbalanced operation is inherent to the system due to the nature of the application, because of the random arrival of EVs to charge, therefore increasing the magnitude of the currents flowing through the neutral point. To minimize unbalanced condition, an alternated connection to the two dc buses can be

promoted. That being said, unbalanced operation still occurs, even worst-case scenarios in which all loads are connected exclusively to one of the dc buses. Therefore, even if the modulation scheme takes this into consideration, the unbalanced scenarios that the system can handle while keeping the midpoint voltage controlled are limited [45]. To date, no comprehensive studies have been made on the NPC application to enable fast charging solutions while providing a distributed bipolar dc bus. The volatile nature of the EV charging load make the balancing of the dc bus voltages imperative under any load condition. Therefore, this work primarily aims to propose cost-effective balancing techniques for the proper operation of the NPC as the grid-interface of a FCS.

2.6 Control Schemes for Grid-Tied Converters

The main function of a grid-tied power converter is to generate a regulated dc voltage, in order to properly control the input currents at the ac side. However, the requirements for these converters have increased through time because of more stringent grid codes and the increased use of generated electric energy to feed loads through rectifier stages, generally based on diodes and thyristors, thereby increasing the presence harmonic currents in the utility grid. Some of this additional requirements are as follows:

- The reduction of the harmonic content because of its negative effect on the electric system (*e.g.*, voltage distortion, electromagnetic interference, increased power ratings of power system equipment, and so on).
- Adjustable power factor.
- Bidirectional power flow.

The emergence of these requirements has resulted in new challenges for the control schemes and has prompted researchers to improve them to meet the control objectives and at the same time maintain high performance.

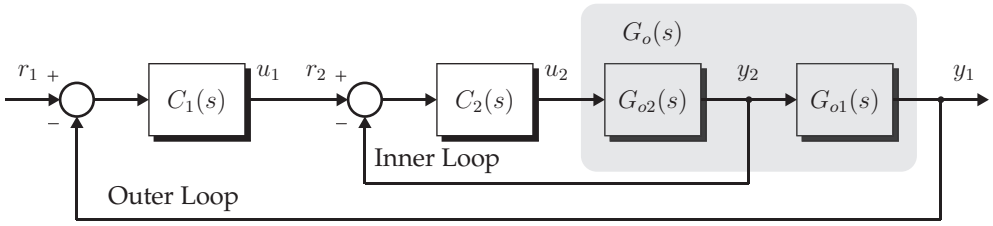


Figure 2.10. Cascade control structure.

On the other hand, the regulation of a grid-tied voltage source converter is similar to the generation of a controlled ac waveform from a dc source. In fact, a dual version for the rectifier side exists for all of the inverter control schemes [46]. However, two mainstreams schemes dominate the industry applications: Voltage-Oriented Control (VOC) and Direct Power Control (DPC).

2.6.1 Cascade Control

The control schemes that will be described in the following sections share the same control structure. This architecture corresponds to a two-degree-of-freedom architecture for dealing with disturbances, called *Cascade Control*. The main idea is based on the feedback of intermediate variables, which have a direct relation with the main output of the system, in order to improve the dynamic response of the loop.

Figure 2.10 shows the diagram of the cascade control structure. In the figure, two control loops are shown: the primary (or outer) loop with its controller $C_1(s)$, and a secondary loop with its controller $C_2(s)$. The design of the secondary loop is made in such a way that it mitigates the effects of disturbances before they significantly affect the plant output y_1 [47].

The main benefits of the cascaded control are obtained when when $G_{o2}(s)$ presents significant non-linearities that limit loop performance or when $G_{o1}(s)$ limits the bandwidth in a basic control loop (*i.e.*, the presence of non minimum phase zeros and/or pure time delays). The first benefit, is explained

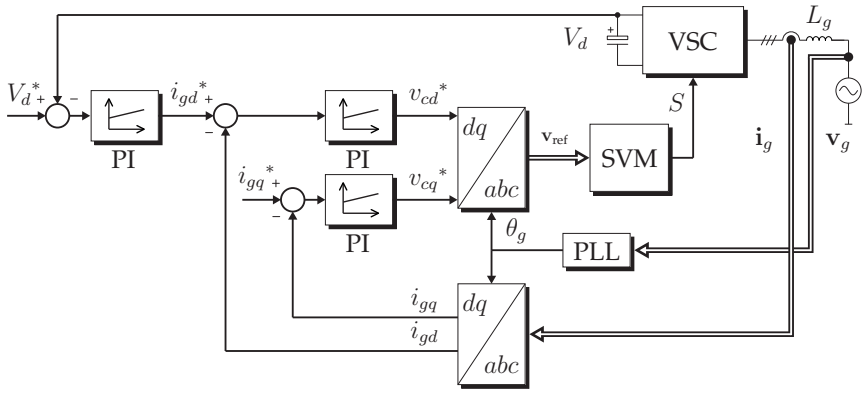


Figure 2.11. Voltage oriented control block diagram.

because the inclusion of $C_2(s)$ allows a high gain control, which tends to reduce the effect of nonlinearities. The latter one, is because this inner controller pre-compensates the effect of the disturbances that $C_1(s)$ has to deal with [47].

2.6.2 Voltage Oriented Control

Derived from the Flux-Oriented Control (FOC) of an induction motor [48], VOC is based on a cascade control structure and a coordinate transformation between the α-β stationary frame and the d-q synchronous frame. The result is fast transient response and high static performance, with no steady-state error, as a result of the dc nature of the controlled quantities [33].

The VOC block diagram is presented in Fig. 2.11. As displayed in the Figure, the measured signals are transformed to the synchronous frame, using a Phase-Locked Loop (PLL) for proper synchronization with the grid voltage vector $\mathbf{v}_g$. This synchronization leads to the decomposition of the current vector $\mathbf{i}_g$ into the orthogonal components i_{gd} and i_{gq}, which are related with the ac side active P_g and reactive power Q_g respectively. In addition, the outer dc voltage loop indirectly generates the active power reference, through i_{gd}^*, whereas i_{gq}^* can be set arbitrarily depending on the application requirements, usually set to zero for unity power factor operation.

Both, the d-q current components and the dc-link voltage V_d, are regulated using linear Proportional Integral (PI) controllers, as they are dc quantities, which lead to perfect tracking in steady state. Finally, the actuations of the currents PI are transformed back into a three-phase coordinate frame and then given to the modulation stage. This modulation stage can be either PWM or SVM, for the generation of the gating signals. For its application to multilevel converters, the basic structure of VOC is kept, and this latter stage is changed accordingly [49].

2.6.3 Direct Power Control

Given that the Direct Torque Control (DTC) regulates directly the torque and flux of an inverter fed induction machine using a switching table, it is possible to extend the same operating principle and control the active power and reactive power at the input of a grid-tied converter. This scheme is called Direct Power Control (DPC) [50]. The performance of this method can be improved by using the virtual flux concept [51], which results in the Virtual Flux Direct Power Control (VFDPC).

The control scheme is shown in Fig. 2.12. The scheme is also based on the cascade control structure, except that the inner loop controller is nonlinear. The dc-link voltage V_d is controlled by a linear PI controller, which provides

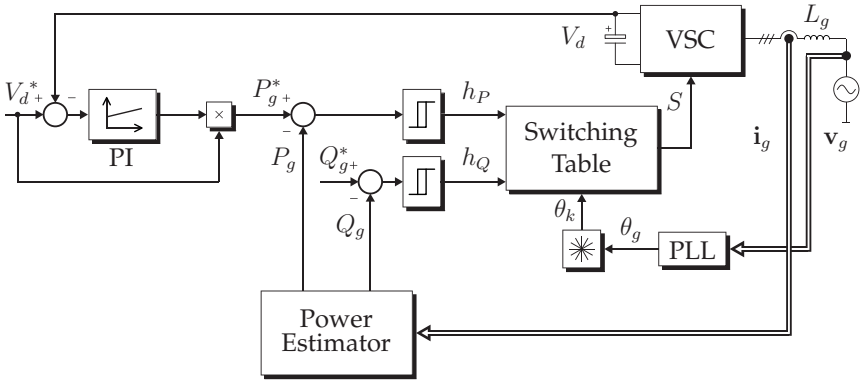


Figure 2.12. Direct power control block diagram.

the reference for the active power P_g^*, whereas the reactive power reference Q_g^* can be set arbitrarily. Both powers are estimated from measurements feedback and controlled with nonlinear hysteresis comparators. Its outputs h_P and h_Q along with θ_s, are used to access the voltage vector look-up table. Finally, the table delivers the gating signals to generate the selected voltage vector. Although this method is designed for the conventional 2L-VSC, some adaptations for the multilevel converters exists [52–55].

2.7 Summary

This chapter describes the different architectures for EV charging stations. Given the particularities of the application and its potential, the concept of the dc bus is adopted and analyzed in detail. The features of the selected configuration are a reduction on the power conversion stages, reduced losses and voltage drops, and simpler integration of additional charging units or optional stages (*e.g.*, DGs and ESSs). However, special attention is required for the grid-tied central converter, given that an increase in the power ratings imposes stringent limits in terms of switching frequency and harmonic distortion. The chapter then revises of the current grid-tied topologies used in the charging station application.

Finally, considering the grid integration of the FCS, the grid connection control requirements and dominant control schemes are discussed: VOC and DPC. Both methods are based on the cascaded control architecture to improve the overall performance of the main control loop. First, the VOC scheme is based on linear regulators, which offers a good dynamic response and an excellent harmonic performance. By contrast, the DPC scheme introduces nonlinear regulators to improve the dynamic response at the expense of a poorer harmonic performance.

CHAPTER III

CENTRAL CONVERTER FOR EV CHARGING STATIONS WITH A BALANCED BIPOLAR DC BUS

MOST OF high-power applications require an increase in the voltage levels in order to meet the current rating capacity of the switching devices. The majority of commercial energy conversion equipment in the range of 1-4 MW currently feature voltage ratings in the range of 3.3-6.6 kV [32]. Nevertheless, in this particular application the connection to MV grids it may not be straightforward because these voltages have a direct relation to the required dc voltage levels in order to properly connect the system to the distribution network. This increase in the dc voltages may reduce the efficiency of fast chargers, as the range of the battery voltage is typically within 350-600 V. Hence, an important step-down effort of the dc-dc stage may be needed.

In order to address this issue, an alternative dc bus structure is proposed. This alternative provides the battery chargers a suitable dc voltage level and at the same time features ac voltage in the MV range. To achieve these, the following sections explore a split dc bus or *bipolar* concept, which is based in the 3L-NPC given its inherent suitability. However, this structure causes challenges to the operation of the converter topology because it will naturally results in current flowing through the neutral point in the presence of asymmetrical loads. The converter limitation is studied, and correction methods

will be analyzed in both simulation and experimental platforms.

3.1 Bipolar DC Bus Architecture

The proposed charging station architecture is illustrated in Fig. 3.1, where a central high-power converter acts as a grid interface, providing dc power to several charging ports. These charging units can be either conventional or fast chargers, each with its own independent dc-dc stage. As it was mentioned in the previous chapter, the dc grid architecture features also the connection of distributed power systems, such as renewable energy generators (PV and wind) and also energy storage devices, as suggested in [19,20,56].

Regarding to the chosen dc structure, using a split dc bus provides more flexibility than the unipolar dc, due to the fact that the former allows the connection of the loads to two regulated voltages: between the neutral point and either the positive or negative bar; or between the positive and the negative bars [57]. Furthermore, this configuration also allows the connection of the station to higher ac voltages while maintaining the step down effort of the dc-dc stages. This bus structure also has an effect on the power handling capabilities, as the connection to higher ac voltages allows higher power without excessive currents and does not require parallel devices or converters. Given the adoption of the bipolar structure and the intended application, the balance control becomes essential [29], as there is no way to guarantee the requirement for fast charging of EVs will be identical in both of the buses of the system. This is because of the differences in terms of battery characteristic, charging powers levels, initial state of charge, and also random arrival to the station.

Furthermore, this charging station concept allows several opportunities to provide support to the grid, such as peak power shaving, frequency regulation, reactive power compensation and power fluctuation minimization. In addition, further developments of energy storage devices (batteries and supercaps), will make it possible to provide power back to the grid, enabling

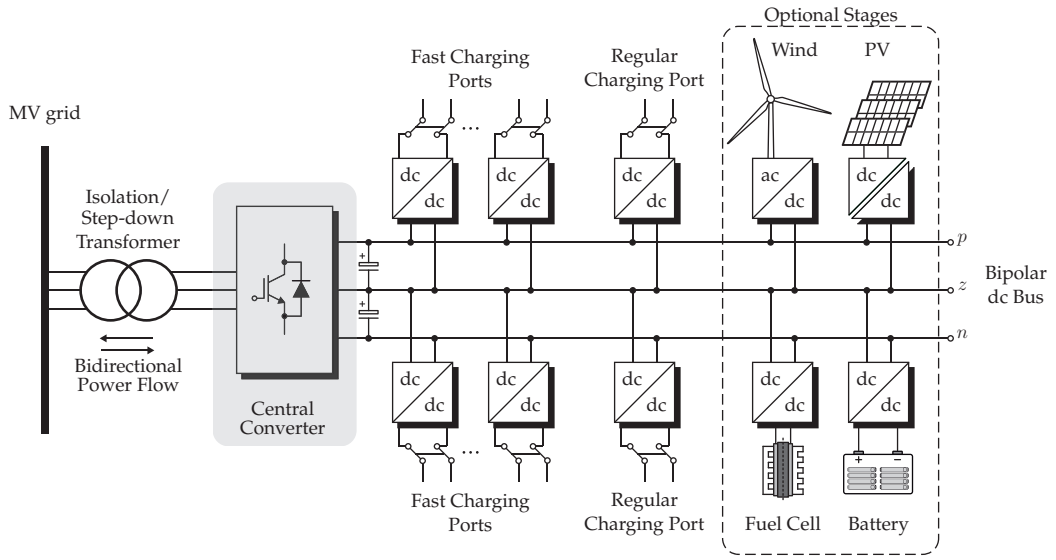


Figure 3.1. Proposed charging station architecture with bipolar dc bus

V2G operation.

3.2 Grid-Tied Central Converter

A four leg three-phase NPC converter that acts as the grid interface is selected, because it offers superior harmonic performance and higher power handling capabilities [40, 58, 59]. An additional leg is incorporated to act as a balancing circuit. The scaling of the system is thus made possible, which in turn allows the extension the power level if needed. The converter topology is illustrated in Fig. 3.2.

According to [58], the correct performance of the NPC is guaranteed only with the accurate control of its midpoint voltage. Hence, multiple solutions can be found in the literature [43, 60–63], which usually solve the problem in the modulation stage with the implementation of a simple balancing mechanism. It is important to note that these schemes are mostly designed considering that the system is being used as a unipolar dc bus, either as a rectifier or in back-to-back configuration. Consequently they are not able to keep this

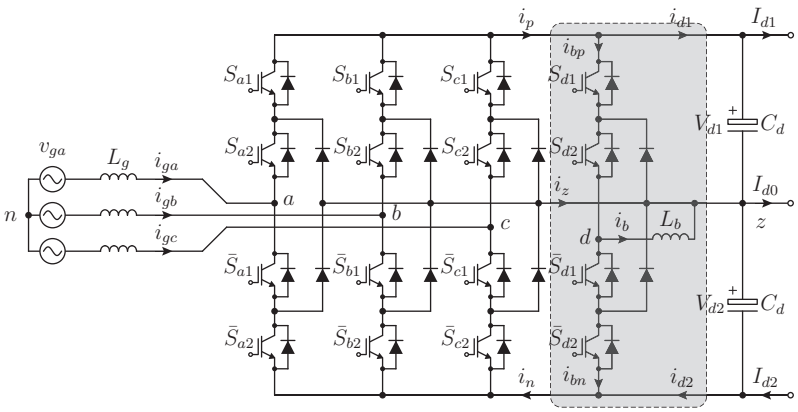


Figure 3.2. Grid-connected 3-phase NPC converter with balancing leg.

voltage controlled under the bipolar structure. Therefore, a balancing technique must be developed. Then, the system provides a bipolar dc bus, and each voltage feeds different loads. As such, unbalanced operation is inherent in the system, given the selected dc architecture and the nature of the intended application. This is explained as follows, as a result of the circulation of current through the neutral point of the converter the dc voltages may become unbalanced. Such circulation is imposed by the asymmetrical load of the dc buses. This effect can be mitigated by alternating the connection of the loads to the dc buses. Nevertheless, even if this connection is promoted, unbalance operation still occurs because of the random arrival of the vehicles to be charged, different battery characteristic, different charging powers, and so on. Therefore, despite the modulation stage performs the balancing corrections to keep the voltage controlled, the unbalanced scenarios that the system is able to overcome are limited [64]. This limitation is studied in detail in the succeeding section.

3.2.1 NPC Limitation of Unbalanced DC Load

To illustrate the balancing limitation provided by the central converter, the following analysis is considered. The system and its variables definition are presented in Fig. 3.2 on the facing page. The figure shows that the dc power

demanded by the load is defined as:

$$P_d = V_{d1} I_{d1} + V_{d2} I_{d2}. \tag{3.2.1}$$

Moreover, the NPC requires its dc voltages to be properly balanced for correct operation; thus, for the rest of the analysis, the condition is assumed to be met, which means that $V_{d1} = V_{d2} = V_d/2$ leads to

$$P_d = \frac{V_d}{2} \left(I_{d1} + I_{d2} \right). \tag{3.2.2}$$

The study of the unbalanced operation becomes relevant as explained in the earlier section. During balanced operation the current flowing through the neutral point I_{d0} is approximately zero, and the balancing of the midpoint is similar to the one needed in the unipolar architecture. However, the presence of differences in the loads results in current flowing through this point, thereby increasing the possibilities of drifts in the dc voltages. To illustrate the balancing capability of the modulation stage, the following scenario is proposed: assume that the power demand in the upper dc bus is P_{d1}, which is kept constant, whereas P_{d2} is reduced to only a fraction ϵ of it. As the dc voltages remain balanced, the demanded power becomes

$$P_d = \frac{V_d}{2} I_{d1} \left(1 + \epsilon \right). \tag{3.2.3}$$

On the other hand, the current in the positive bar can be assumed to be equal to the current demanded by the upper bus; thus, $i_p \approx I_{d1}$ without losing generality. According to [43], and under unity power factor, i_p is given by

$$i_p = \left(\sqrt{3} m_a + \frac{6\alpha}{\pi} \right) \frac{I_g}{2} \cos \delta, \tag{3.2.4}$$

where m_a stands for the amplitude modulation index, α is the dc drift of the converter voltage during the positive half cycle, I_g is the grid current amplitude and δ is the phase angle between the converter and the grid voltage vectors. Note that i_p is defined only by the demand on the upper bus and therefore does not change for variations in the lower one. Additionally, note that during normal balanced operation the dc drift α injected is virtually zero.

The balancing capability of the modulation stage is reflected by (3.2.4), which suggests that the midpoint can be controlled in a certain range through the injection of a dc bias in the generated voltage. Nevertheless, this capability is limited by the linear operation of the modulation stage and therefore varies depending on the modulation scheme and balancing technique. Moreover, this capability is a function of the amplitude modulation index m_a as well.

Going back to the previous case of asymmetry, when the demand at the lower bus is ϵP_{d1}, and assuming that ϵ is such that the system is at its limit, injecting the largest dc drift value $\hat{\alpha}$, and keeping the voltages balanced, the current in the positive bar is given by

$$i_p = \left(\sqrt{3}m_a + \frac{6\hat{\alpha}}{\pi}\right)\frac{I_g}{2}\frac{1+\epsilon}{2}\cos\delta. \tag{3.2.5}$$

However, this current must be equal to the one defined by (3.2.4), as the demand in the upper bus has not changed. Hence, using (3.2.4) and (3.2.5) to solve ϵ leads to

$$\hat{\epsilon} = \frac{2\sqrt{3}m_a}{\sqrt{3}m_a + \frac{6\hat{\alpha}}{\pi}} - 1, \tag{3.2.6}$$

where $\hat{\epsilon}$ is the lowest value for the ratio between P_{d1} and P_{d2} that the modulation stage is able to handle and keep the voltages from drifting.

The same analysis is repeated, but P_{d2} is kept fixed and P_{d1} is varied. In this case, the negative bar current is used, which is defined by

$$i_n = \left(\sqrt{3}m_a + \frac{6\beta}{\pi}\right)\frac{I_g}{2}\cos\delta, \tag{3.2.7}$$

where β is the dc voltage drift introduced to the modulating signal during the negative half cycle. Analogously, regardless the load condition of the upper dc bus, the limit for the balancing capability of the modulation stage is defined by

$$\hat{\epsilon} = \frac{2\sqrt{3}m_a}{\sqrt{3}m_a + \frac{6\hat{\beta}}{\pi}} - 1, \tag{3.2.8}$$

because i_n is defined only by the load connected at the lower dc bus.

The previous analysis states that, if the system is able to operate above the determined value for $\hat{\epsilon}$, the balancing mechanism provided by the modulation stage is sufficient to keep the voltages controlled. However, the system is very unlikely to have a continuous balanced operation, so an additional balancing technique must be included in order to guarantee the proper operation of the converter in any load scenario.

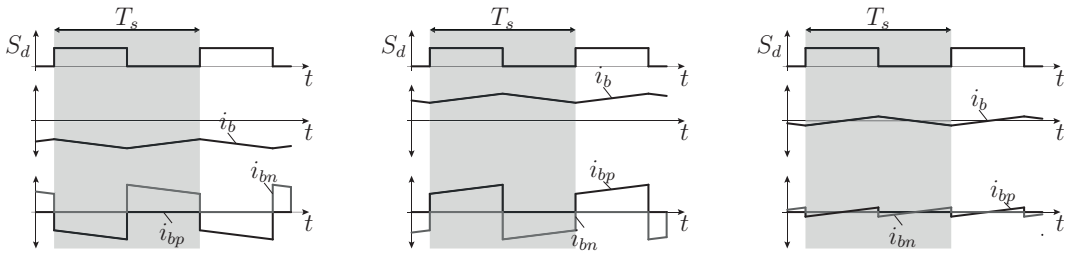
3.2.2 Voltage Balancing Circuit

The correct asymmetrical dc load operation of the charging station is limited by the modulation stage, as shown earlier. However, the system cannot be guaranteed to never be driven outside the valid operation zone because of several reasons (*e.g.*, random arrival of the EVs to the station, different battery packs, and so on.). Hence, a complimentary balancing circuit is needed in order to operate under any load condition.

The idea is to fully use the balancing capabilities of the modulation stage and, if this is not sufficient to keep the voltages balanced, a virtual impedance will be added in such a way that, when the system leaves the valid operation zone, it demands the minimal current in order to met the limit. In other words, for the modulation stage, the system keeps operating at the boundary condition.

As in grid connected systems, the amplitude modulation index m_a varies slightly because V_d is rarely changed, and it only responds to changes in the load demand, which do not reflect important changes on it. Then m_a can be assumed to be constant; hence, the minimal load condition is known *a priori*. In addition, the direction of I_{d0} will change depending on the location of the lighter load (imbalance), making mandatory the bidirectional characteristic of the balancing circuit, to control current in both directions.

As stated earlier, the modulator will provide a certain room to handle different loads through the injection of a dc bias in the converter voltage, and



(a) Lower bus current compensation (b) Upper bus current compensation (c) No current compensation

Figure 3.3. Different operating conditions of the balancing circuit.

is limited by the maximum current that can flow through the neutral point. If the unbalance ratio exceeds this operational zone, the voltages will drift regardless the corrections performed in the modulation stage. The presence of the balancing leg allows to emulate the minimal load condition. In other words, if the imbalance is present in the lower bus, the maximum current in the neutral point is $I_{d0} = (\hat{\epsilon} - 1)I_{d1}$, and the remanent current $\hat{\epsilon}I_{d1}$ must be conducted through the negative bar in order to maintain the voltages balanced. This principle can be further explained using the signals of Fig. 3.3. Consider that S_d is the switching function of the upper devices. In the studied case, the balancing circuit imposes a positive current i_{bn} such as the current in the negative bar is $\hat{\epsilon}I_{d1}$. To do so, the polarity of the current flowing through the inductor i_b should be reversed, as shown in Fig. 3.3a. The analogous scenario shown in Fig. 3.3b, occurs when the imbalance is present in the upper bus, thereby imposing a current i_{bp} with a positive average value. Finally, Fig. 3.3c presents the operation of the balancing leg during the balanced operation, when no current compensation is needed, making all the average currents in the circuit to be zero. Note how the duty cycle of remains fixed at 0.5 in all the scenarios, as the dc-dc stage is connected between the full dc voltage of the converter and its midpoint.

This balancing circuit can be implemented in several ways. In [65] a bidirectional boost converter is employed in a five level NPC. For the sake of simplicity, this proposal uses a fourth leg in the NPC, which is operated as a bidirectional dc-dc converter, as shown in Fig. 3.2. Using a leg identical to

the other phases of the circuit facilitates design and implementation through power electronic building blocks (PEBBs). This is a desirable characteristic in practical applications rather than hybrid converters.

3.3 Proposed Control Scheme

3.3.1 Voltage Oriented Control

The conventional VOC control scheme is used in regulating of the proposed grid-tied converter, which is displayed in Fig. 3.4. As established in the previous chapter, the modulation stage must be changed accordingly with the converter topology. In this case, the modulation is performed using the SVM algorithm for a three-level converter [32], and it is described in the following section. Additionally, a PI controller has been included in order to perform the partial balancing mechanism, which depends on the selected modulation strategy. This dissertation conducts partial balancing through the redistribution of the usage of positive and negative small vectors.

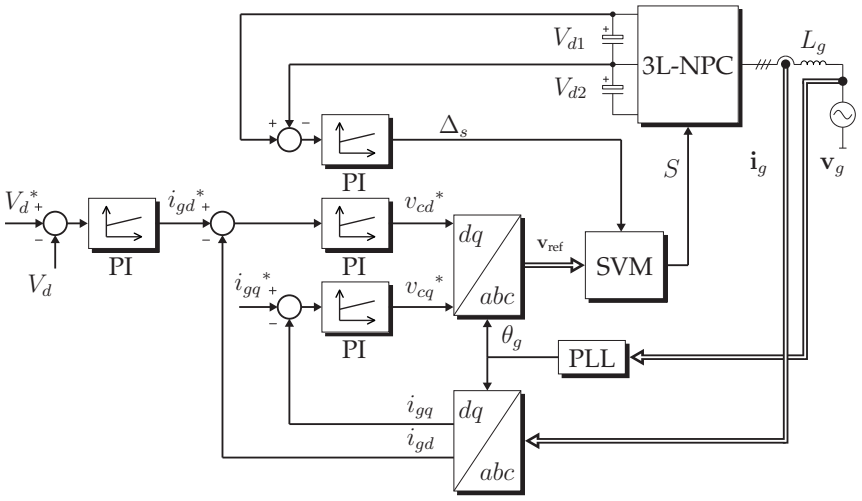
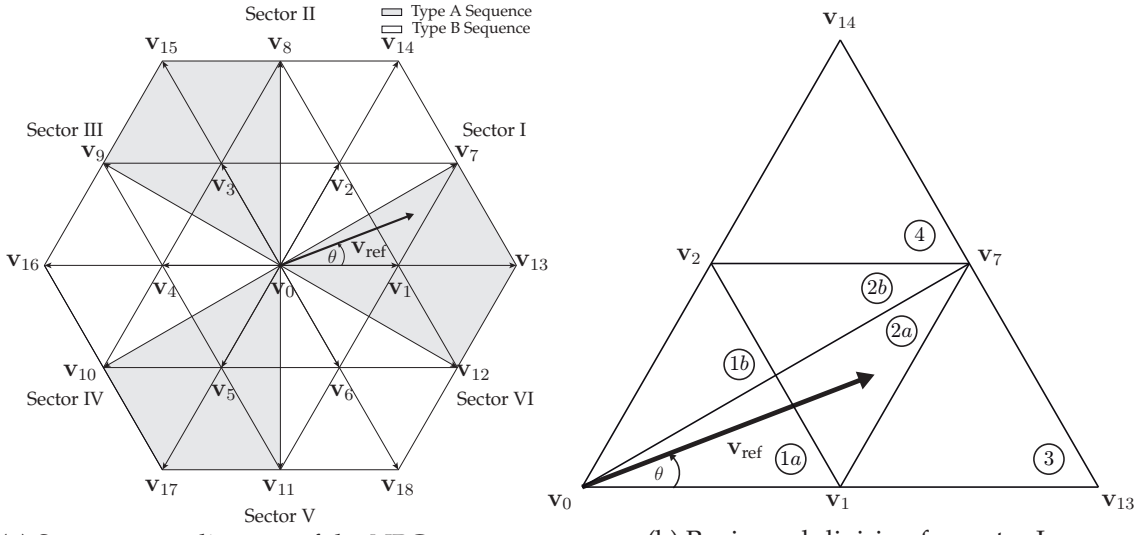


Figure 3.4. VOC block diagram for NPC.



(a) Space vector diagram of the NPC converter. (b) Region subdivision for sector I

Figure 3.5. SVM Scheme for the NPC converter.

3.3.2 Space Vector Modulation

The SVM scheme is a popular real-time digital PWM scheme that offers two degrees of freedom for advanced controller design. In comparison with conventional carrier-based sinusoidal PWM, the SVM extends the operation range by a 15% [32]. Considering the discrete nature of the switching devices and the valid combinations of the gating signals, the converter is able to connect each phase of the load to three voltage levels: $-V_d/2$, 0 and $V_d/2$. The converter voltage vector $\mathbf{v}_c$ is represented as a function of the phase switching state $S = (S_a, S_b, S_c)$ and the dc-link voltage V_d as

$$\mathbf{v}_c = \frac{V_d}{3}(S_a + \mathbf{a}S_b + \mathbf{a}^2 S_c), \text{ where } S_k \in \{\text{-1,0,1}\}, \text{ and } k = a, b, c. \quad (3.3.1)$$

Hence, the converter is able to generate 19 different voltage vectors (out of 27 different valid switching states), as it can be seen in Fig. 3.5a. The figure shows six small active vectors $\mathbf{v}_1$ - $\mathbf{v}_6$ (each one has a positive and negative redundancy), six medium vectors $\mathbf{v}_7$ - $\mathbf{v}_{12}$, six large vectors $\mathbf{v}_{13}$ - $\mathbf{v}_{18}$, and the zero vector $\mathbf{v}_0$ (which has three redundancies). Note that the previous analysis assumes that the dc voltages of the converter V_{d1} and V_{d2} are perfectly

Table 3.1. NPC voltage vectors and switching states

Vector	Switching State	Output Voltage	Vector	Switching State	Output Voltage
$\mathbf{v}_0$	[NNN][OOO][PPP]	0			
$\mathbf{v}_{1P}$	[POO]	$\frac{V_d}{3}$	$\mathbf{v}_7$	[PON]	$\frac{\sqrt{3}V_d}{3}e^{j\frac{\pi}{6}}$
$\mathbf{v}_{1N}$	[ONN]		$\mathbf{v}_8$	[OPN]	$\frac{\sqrt{3}V_d}{3}e^{j\frac{\pi}{2}}$
$\mathbf{v}_{2P}$	[PPO]	$\frac{V_d}{3}e^{j\frac{\pi}{3}}$	$\mathbf{v}_9$	[NPO]	$\frac{\sqrt{3}V_d}{3}e^{j\frac{5\pi}{6}}$
$\mathbf{v}_{2N}$	[OON]		$\mathbf{v}_{10}$	[NOP]	$\frac{\sqrt{3}V_d}{3}e^{j\frac{7\pi}{6}}$
$\mathbf{v}_{3P}$	[OPO]	$\frac{V_d}{3}e^{j\frac{2\pi}{3}}$	$\mathbf{v}_{11}$	[ONP]	$\frac{\sqrt{3}V_d}{3}e^{j\frac{3\pi}{2}}$
$\mathbf{v}_{3N}$	[NON]		$\mathbf{v}_{12}$	[PNO]	$\frac{\sqrt{3}V_d}{3}e^{j\frac{11\pi}{6}}$
$\mathbf{v}_{4P}$	[OPP]	$\frac{V_d}{3}e^{j\pi}$	$\mathbf{v}_{13}$	[PNN]	$\frac{2V_d}{3}$
$\mathbf{v}_{4N}$	[NOO]		$\mathbf{v}_{14}$	[PPN]	$\frac{2V_d}{3}e^{j\frac{\pi}{3}}$
$\mathbf{v}_{5P}$	[OOP]	$\frac{V_d}{3}e^{j\frac{4\pi}{3}}$	$\mathbf{v}_{15}$	[NPN]	$\frac{2V_d}{3}e^{j\frac{2\pi}{3}}$
$\mathbf{v}_{5N}$	[NNO]		$\mathbf{v}_{16}$	[NPP]	$\frac{2V_d}{3}e^{j\pi}$
$\mathbf{v}_{6P}$	[POP]	$\frac{V_d}{3}e^{j\frac{5\pi}{3}}$	$\mathbf{v}_{17}$	[NNP]	$\frac{2V_d}{3}e^{j\frac{4\pi}{3}}$
$\mathbf{v}_{6N}$	[ONO]		$\mathbf{v}_{18}$	[PNP]	$\frac{2V_d}{3}e^{j\frac{5\pi}{3}}$

balanced. Table 3.1 resumes the switching states for each available vector.

The SVM technique accounts for the available vectors of the system and provides an output with variable amplitude and variable frequency, which are defined by the rotating reference vector $\mathbf{v}_{\text{ref}}$. The operating principle is based on a discrete time control platform with a fixed sampling time T_s. During this sampling time, $\mathbf{v}_{\text{ref}}$ can be considered constant. This reference vector can be synthesized using the three closest vectors by applying them for a certain period of time, which is referred to as *dwell times*, essentially representing the duty cycle for the switches that generate these vectors.

In order to identify the closest stationary vectors, the α-β stationary plane must be discretized into six sectors, as presented in Fig. 3.5b. The angle of the reference vector θ must be obtained to perform this discretization. This

angle is defined as

$$\theta = \arctan\left(\frac{v_\beta}{v_\alpha}\right), \tag{3.3.2}$$

where v_α and v_β represent the real and imaginary parts of $\mathbf{v}_{\text{ref}}$, respectively. After obtaining θ, the discretization of the plane is defined as follows

$$(k-1)\frac{\pi}{3} \leq \theta_k < k\frac{\pi}{3}, \tag{3.3.3}$$

where θ_k stands for the k-th sector. In contrast with the conventional SVM scheme for the 2L-VSC, the sectors have to be subdivided into 6 regions, as shown in Fig. 3.5b, because of the larger vector availability of the NPC.

The sector information provided by θ_k, along with the proper detection of the region, can be used to calculate the dwell times. Using the example case provided in Fig. 3.5b, is possible to see that the $\mathbf{v}_{\text{ref}}$ is located in sector I region $2a$ (or region I-$2a$ for the rest of the dissertation). This voltage can then be synthesized as

$$\mathbf{v}_{\text{ref}} = \frac{1}{T_s}\left(t_a\mathbf{v}_1 + t_b\mathbf{v}_2 + t_c\mathbf{v}_7\right). \tag{3.3.4}$$

Separating (3.3.4) into its real and imaginary parts and using the stationary vector information provided by Table 3.1 lead to

$$v_{\text{ref}}\cos\theta = \frac{1}{T_s}\left(\frac{1}{3}t_aV_d + \frac{1}{6}t_bV_d + \frac{1}{2}t_cV_d\right) \tag{3.3.5}$$

$$v_{\text{ref}}\sin\theta = \frac{1}{T_s}\left(\frac{\sqrt{3}}{6}t_bV_d + \frac{\sqrt{3}}{6}t_cV_d\right). \tag{3.3.6}$$

Additionally, the dwell times must comply with

$$T_s = t_a + t_b + t_c. \tag{3.3.7}$$

Then, by clearing t_a, t_b and t_c, the dwell times for the example are given

Table 3.2. Dwell times calculation 3L-SVM for odd sectors

Region	t_a	t_b	t_c
$1a$	$2m_a \sin(\theta_1 - \theta)$	$2m_a \sin(\theta - \theta_2)$	$1 - 2m_a \sin(\theta - \theta_3)$
$1b$	$2m_a \sin(\theta - \theta_2)$	$1 - 2m_a \sin(\theta - \theta_3)$	$2m_a \sin(\theta_1 - \theta)$
$2a$	$1 - 2m_a \sin(\theta - \theta_2)$	$1 - 2m_a \sin(\theta_1 - \theta)$	$2m_a \sin(\theta - \theta_3) - 1$
$2b$	$1 - 2m_a \sin(\theta_1 - \theta)$	$2m_a \sin(\theta - \theta_3) - 1$	$1 - 2m_a \sin(\theta - \theta_2)$
3	$2 - 2m_a \sin(\theta - \theta_3)$	$2m_a \sin(\theta_1 - \theta) - 1$	$2m_a \sin(\theta - \theta_2)$
4	$2 - 2m_a \sin(\theta - \theta_3)$	$2m_a \sin(\theta_1 - \theta)$	$2m_a \sin(\theta - \theta_2) - 1$

where $\theta_1 = \frac{k\pi}{3}$, $\theta_2 = \frac{(k-1)\pi}{3}$, $\theta_3 = \frac{(k-2)\pi}{3}$ and k stands for the sector number.

Note: The dwell times are assigned in order, following the seven segment sequence used in [32]. For even sectors the expressions for t_b and t_c have to be swapped.

by the following expressions

$$t_a = T_s - 2T_s m_a \sin\theta \tag{3.3.8}$$

$$t_b = T_s - 2T_s m_a \sin\left(\frac{\pi}{3} - \theta\right) \tag{3.3.9}$$

$$t_c = 2T_s m_a \sin\left(\theta + \frac{\pi}{3}\right) - T_s, \tag{3.3.10}$$

where m_a is the amplitude modulation index, which is defined according to

$$m_a = \frac{\sqrt{3} v_{\text{ref}}}{V_d}. \tag{3.3.11}$$

Extending the same idea for the entire stationary plane and considering the seven-segment sequence provided in [32] the Table 3.2 is obtained for the calculation of the dwell times in the odd-numbered sectors. Note that the expressions for t_b and t_c must be swapped for the even-numbered sectors.

3.3.3 Switching Sequence

In the preceding section, the dwell-times calculation has been determined to synthesize the voltage reference. However, a proper sequence of the vectors must be defined, depending on the application requirements, such as

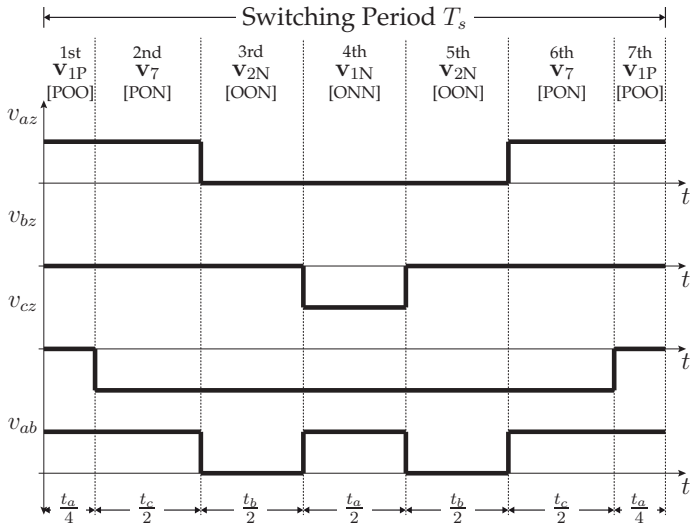
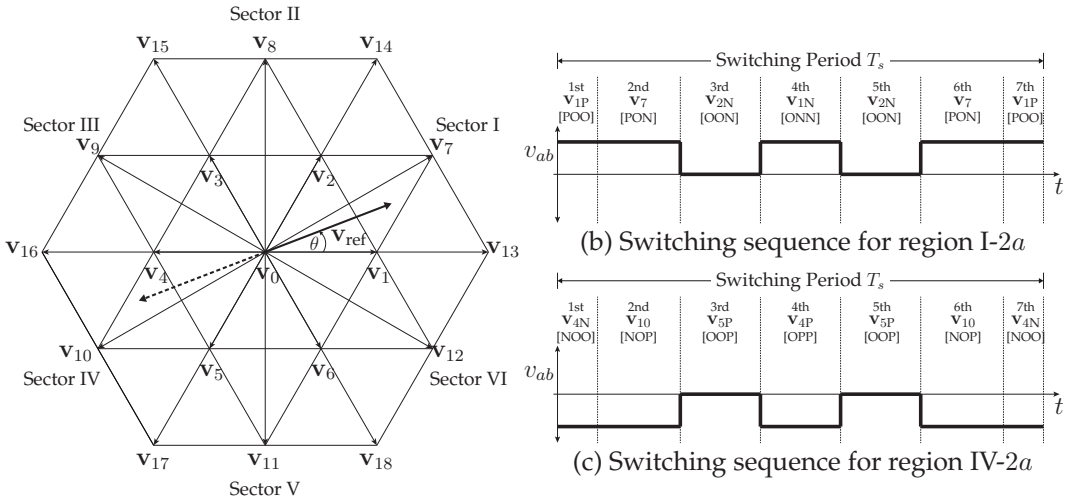


Figure 3.6. Seven segment switching sequence for SVM.

reduced switching frequency, symmetrical voltage generation, dc balancing capabilities, to name a few. The switching sequence used in this work is based in the seven segment proposed in [32]. This method basically consists in dividing one sampling time T_s in seven segments, as shown in Fig. 3.6, and performing transitions that involve only two switches at a time, resulting in a reduced switching frequency on the devices. In addition, the method alternates the use of type A and type B sequences sequences for the regions that lie 180º apart from each other. The type A sequences are characterized by starting with a positive redundancy of a small vector, as shown in Fig. 3.6. Type B sequences begin with a negative redundancy.

Alternating the use of different types of sequences allows to achieve half-wave symmetry in the generated voltages. This characteristic results in signals free of even order harmonics, which is an attractive feature for grid connected applications.

To illustrate the principle, Fig. 3.7 in the facing page shows a suggested case to be analyzed. The reference vector $\mathbf{v}_{\text{ref}}$ is in region I-$2a$ and then in IV-$2a$ (which are 180º apart). The sequences required to synthesize the reference



(a) Space vectors generated by the NPC

(b) Switching sequence for region I-2a

(c) Switching sequence for region IV-2a

Figure 3.7. SVM Operating principle for regions I-2a and IV-2a.

vector are, respectively

$$\mathbf{v}_{\text{ref}} = \frac{1}{T_s}(t_a\mathbf{v}_1 + t_b\mathbf{v}_2 + t_c\mathbf{v}_7) \tag{3.3.12}$$

$$\mathbf{v}_{\text{ref}} = \frac{1}{T_s}(t_a\mathbf{v}_4 + t_b\mathbf{v}_5 + t_c\mathbf{v}_{10}). \tag{3.3.13}$$

The required switching sequence and the resulting line-to-line voltages are shown in Figures 3.7b and 3.7c, respectively. The sequence used for region I-2a is type A because it starts with the positive redundancy of $\mathbf{v}_1$, whereas that for region IV-2a is type B because it begins with $\mathbf{v}_{4\text{N}}$. The result is a line-to-line voltage with a half-wave symmetrical waveform.

3.3.4 Unbalance Operation Limit for SVM

The usage of the small vectors is redistributed to control the midpoint voltage in the NPC and to restore the balance of the system. In this way, the tracking of the reference is not altered. To illustrate the principle, the example shown in Fig. 3.5b is revisited. The reference vector can be synthesized according to (3.3.4).

In order to determine the maximum injected dc drift $\hat{\alpha}$ that the modulation stage allows, the average usage time for the small vectors t_a is calculated over the positive half cycle (see Appendix III). During normal operation and using the example, t_a is equally divided in the redundancies of $\mathbf{v}_1$, $\mathbf{v}_{1\mathrm{N}}$ and $\mathbf{v}_{1\mathrm{P}}$, thus the maximum available time to redistribute is $t_a/2$, and, in extreme cases, it uses exclusively one of the redundancies of $\mathbf{v}_1$. This remaining time is equivalent to the maximum dc drift that can be injected within the linear zone of the modulation, and varies with m_a because, for different modulation indexes, the vector passes through different regions and also results in different dwell-times values. Hence, the dwell times in Table 3.2 for each small vector are averaged during their corresponding interval to obtain this remanent time. The resulting average expression for the maximum voltage drift is defined in (3.3.14).

$$\hat{\alpha} = \begin{cases} \dfrac{-3m_a + 6m_a \sin\left(\gamma + \frac{\pi}{6}\right)}{\pi}, & m_a \in \left[0, \frac{1}{2}\right[\\ \dfrac{\frac{\pi}{2} - 3\gamma + 3m_a\left(1 + 2\sin\left(\gamma - \frac{\pi}{6}\right) + \sqrt{3}\right)}{\pi}, & m_a \in \left[\frac{1}{2}, \frac{\sqrt{3}}{3}\right[\\ \dfrac{\frac{\pi}{2} + 3\gamma - 3m_a\left(1 + 2\sin\left(\gamma + \frac{\pi}{6}\right) - \sqrt{3}\right)}{\pi}, & m_a \in \left[\frac{\sqrt{3}}{3}, 1\right] \end{cases} \tag{3.3.14}$$

where γ is the angle at which the change of region occurs and is defined according to:

$$\gamma = \begin{cases} \dfrac{\pi}{6}, & m_a \in \left[0, \frac{1}{2}\right[\\ \arcsin\left(\frac{1}{2m_a}\right) - \dfrac{\pi}{3}, & m_a \in \left[\frac{1}{2}, \frac{\sqrt{3}}{3}\right[\\ \dfrac{\pi}{3} - \arcsin\left(\frac{1}{2m_a}\right), & m_a \in \left[\frac{\sqrt{3}}{3}, 1\right] \end{cases} . \tag{3.3.15}$$

As stated earlier, a linear PI controller is being used for the regulation for the midpoint voltage, as shown in Fig. 3.4. This controller modifies the usage of the small vectors as follows:

$$t_{a\mathrm{P}} = \frac{t_a}{2}(1 - \Delta_s) \ , \ t_{a\mathrm{N}} = \frac{t_a}{2}(1 + \Delta_s), \tag{3.3.16}$$

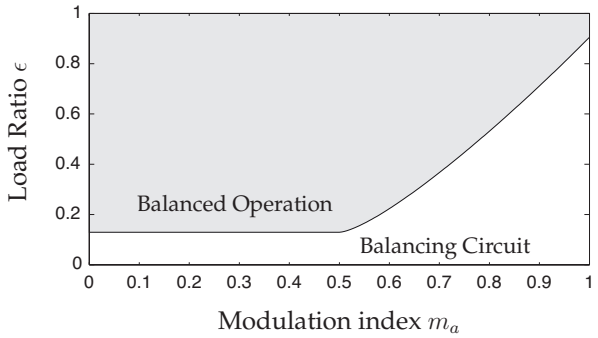


Figure 3.8. Critical load ratio for the NPC using SVM.

where Δ_s is the actuation of the PI. Note that these expressions hold when the loads are consume power from the grid. In the case of having active loads, the sign of Δ_s must be modified accordingly, given that the effect of the small vectors in the midpoint voltage is reversed.

Taking into account the balancing strategy and the maximum value of α allowed by the SVM algorithm, it is possible to determine a theoretical value for the critical load ratio $\hat{\epsilon}$ for the NPC, which depends on the modulation index as stated before. This limit operation is illustrated in Fig. 3.8.

3.4 Voltage Balancing Techniques

As previously established in the chapter, the balancing capabilities of the modulation stage are limited, and considering the nature of the application the presence of a balancing circuit is mandatory. The balancing circuit guarantees that the charging station continuously operates under any load condition. However, different approaches to regulating the balancing leg are available, as discussed in the following sections.

3.4.1 Method 1: Complimentary Balancing Circuit

The idea behind this approach is to extend the bipolar NPC operation through the entire load range, while using the maximum balancing capabilities of-

fered by the central converter modulator. To do so, the balancing leg must be able to act as a virtual impedance, such that the minimal load condition is met, and the modulator is able to keep the voltages balanced. This section explains the generation of the balancing current reference i_b^* in order to ensure the proper operation of the system. This current is related to Equations (3.2.6) and (3.3.14).

To illustrate the principle, let I_{d1} and I_{d2} denote the currents demanded by the dc loads at upper and lower buses, respectively. In addition, the critical load ratio $\hat{\epsilon}$ is known. First, assume an imbalance is present in the upper bus, such as the modulator is not able to keep the voltages controlled by itself even when the largest value of α is injected. The converter dc currents hold

$$i_p = \hat{\epsilon} i_n. \tag{3.4.1}$$

Furthermore, according to Fig. 3.2, these currents are related to the load currents as follows

$$i_p = I_{d1} + i_{bp} \tag{3.4.2}$$
$$i_n = I_{d2} + i_{bn}. \tag{3.4.3}$$

Moreover, the operation of the balancing leg is required, so the inductor current i_b is different from zero, which leads to

$$i_{bn} = -d_b i_b \tag{3.4.4}$$
$$i_{bp} = (1 - d_b) i_b. \tag{3.4.5}$$

However, given the implementation of the bidirectional dc-dc stage using an additional leg, its duty cycle d_b is fixed to 0.5. This is explained as the input voltage is the total dc-link voltage V_d, while its output is V_{d2}, which due the requirements of the proper operation of the NPC has to be equal to $V_d/2$; hence,

$$i_{bn} = -i_{bp} \tag{3.4.6}$$

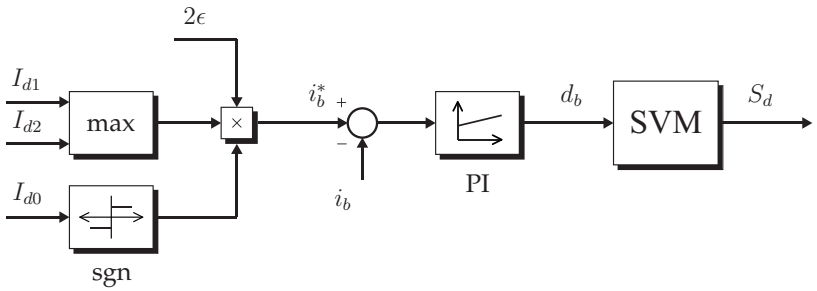


Figure 3.9. Voltage balancing circuit controller for the additional NPC leg.

Then, by replacing (3.4.2) and (3.4.3) in (3.4.1), and using the information provided by (3.4.4)–(3.4.6), an expression can be obtained for the required current circulating through the inductor that keeps the system balanced, which is defined as

$$i_b^* = \frac{2\hat{\epsilon} I_{d2}}{(1+\hat{\epsilon})}. \tag{3.4.7}$$

If the unbalance is at the lower bus, then the balancing circuit should demand a current such that $\hat{\epsilon} i_p$ is flowing through the negative terminal, making i_b negative. This leads to

$$i_b^* = -\frac{2\hat{\epsilon} I_{d1}}{(1+\hat{\epsilon})}. \tag{3.4.8}$$

It is important to mention that, this current value is the minimal in order to keep the system balanced, making the midpoint PI controller to operate saturated in the unbalanced scenarios. However, given the other reasons that can drive the system out of balance, such as differences in the capacitances of the dc links, a certain room is given to this PI by increasing the demanded current by the dc-dc stage to guarantee the proper operation of the station in any scenario. Therefore, the dc inductor current reference will be defined as follows

$$i_b^* = 2\hat{\epsilon} \max\{I_{d1}, I_{d2}\} \text{sgn}(I_{d2} - I_{d1}). \tag{3.4.9}$$

A PI controller is used to regulate the input current of the voltage balancing circuit, as presented in Fig. 3.9. It should be noted that this control

scheme only operates when the system is driven outside the gray area of balanced operation shown in Fig. 3.8. Therefore, an enabling signal is defined as follows.

$$e_{\mathrm{B}} = \begin{cases} 1 & \text{if } |I_{d1} - I_{d2}| > (1-\hat{\epsilon}) \max\{I_{d1}, I_{d2}\} \\ 0 & \text{if } |I_{d1} - I_{d2}| \leq (1-\hat{\epsilon}) \max\{I_{d1}, I_{d2}\} \end{cases} \tag{3.4.10}$$

3.4.2 Method 2: Virtual Disconnection of the Neutral Point

The disadvantage of the previous method is the appearance of even-order harmonics under the presence of imbalances. This appearance is because the dc bias injection leads to a non half-wave symmetrical waveform. A different approach can be utilized to prevent the dc voltages from drifting. The idea is as follows: given that the balancing circuit is already considered for the system, compensation is left exclusively to this stage, and the NPC converter controller exclusively regulates the grid-side currents, which improves the power quality at the expense of larger current ratings for the balancing leg.

In order to do so, the operation of the balancing leg is modified as follows. The mid point voltage PI will only regulate the small deviations, such as differences on the capacitances. Therefore, its actuation is always around zero. However, the dc loads are still connected to the mid point. Thus, the possibilities for voltage drifts are still present because the current will circulate through this node. To prevent this phenomena, the balancing circuit will provide the path for any difference in the dc loads currents, which is explained by the next equation. Using KCL in the z node leads to

$$i_z = i_{c2} - i_{c1} - I_{d0} - i_b. \tag{3.4.11}$$

Moreover, during balanced operation, I_{d0} is virtually zero, and no deviation is found in the dc voltages because i_z does not have a significant dc component. However, under asymmetrical operation, I_{d0} reflects the differences between the load consumptions in the dc buses and has a nonzero dc component, which is also present in i_z. Then, in order to avoid any alteration in the current flowing through the neutral point regardless of the dc load condition,

I_{d0} can be forced to be zero. This will eliminate the origin of the unbalances. To do so, the dc inductor current must be controlled to be

$$i_b^* = I_{d2} - I_{d1}. \tag{3.4.12}$$

The result is a virtual disconnection of the neutral point from the dc side of the system, as i_z always behaves similar to a normal balanced operation. Thus, the neutral point remains balanced under any load condition. Considering the previous balancing method, this approach is simpler and requires less effort from the computational perspective, the sequence is not altered during any scenario; therefore, the half-wave symmetry operation of the converter is unaltered. Nevertheless, the operation is achieved at the expense of an increased current rating for the balancing circuit. This is due the fact that the dc current that the inductor has to withstand is now the rated dc current. Please note that, this approach allows to use any modulation index, as the modulation stage is no longer used for balancing purposes.

3.5 Simulation Results for Method 1

After the proposal for the dc bus architecture and the balancing strategies for any load condition, the system is simulated using Matlab/Simulink® software. To do so, a 1.2 MW charging station is designed for the validation of the proposed strategy. The station is connected to the 4.16 kV grid through a step-down transformer and enables the operation of 12 charging ports, each one of them rated at 100 kW. Additionally, the voltage of each dc bus is set to 1 kV.

Considering the power ratings involved, the SVM algorithm is implemented to obtain an equivalent device switching frequency of 1080 Hz. The parameters of the system are described in Table 3.3. Both, the dynamic and steady-state operations are analyzed in detail in the following sections.

Table 3.3. Simulation and experimental parameters

Paramenter	Symbol	Value
Grid Voltage Amplitude	V_g	1 pu
Grid Frequency	f_g	1 pu
Input Filter Inductance	L_g	0.1 pu
Input Filter Resistance	R_g	0.02 pu
dc-Link Capacitance	C_d	4.5 pu
dc-Link Voltage	V_d	2.174 pu
Boost inductance	L_b	0.26 pu
Switching Frequency	f_s	36 pu
Amplitude Modulation Index	m_a	0.6408
Frequency Modulation Index	m_f	36
Critical Load Ratio	$\hat{\epsilon}$	0.2829
Simulation Base Voltage	V_{B}	$4160/960$ V
Simulation Base Power	P_{B}	1.2 MW
Experimental Base Voltage	V_{B}	208 V
Experimental Base Power	P_{B}	3.6 kW
Base Frequency	f_{B}	60 Hz

3.5.1 Dynamic Response

The first stage of the validation is the study of the dynamic performance under several load impacts, presented in Fig. 3.10, which is a situation that is possible during the sudden connections and disconnections of the EVs for charge because of their random arrival to the station. The following test is performed: the system is assumed to be in steady state with rated loads on both dc buses (balanced load). Then, at $t = 0.05$ s, the load connected to the lower bus is suddenly disconnected, whereas the load is kept at its rated value in the upper dc bus. Next, at $t = 0.1\bar{3}$ s the imbalance is reversed. Consequently, the rated load is connected to bus 2 and no load is connected to bus 1. Finally, at $t = 0.21\bar{6}$ s, both buses return to rated load condition. Note that, the grid voltage has been distorted by adding third- and fifth-order harmon-

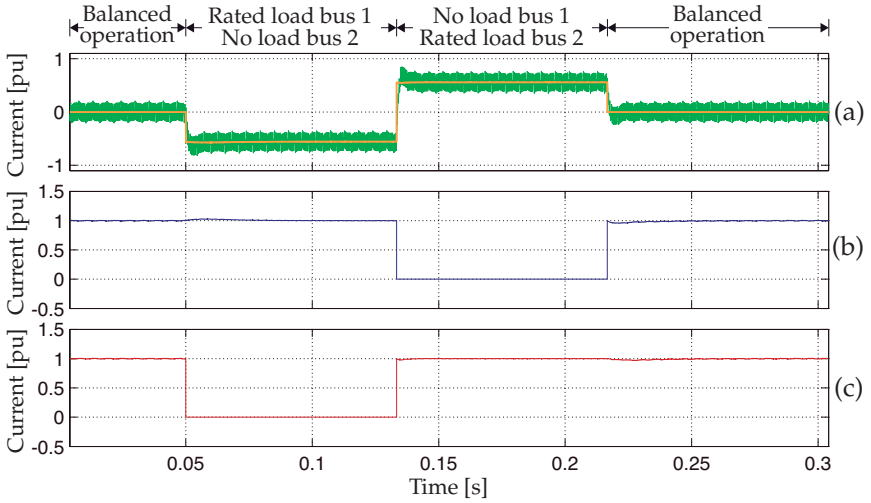


Figure 3.10. Simulated dynamic performance of the system with method 1. (a) Boost current i_b and its reference i_b^*. (b) Bus 1 current I_{d1}. (c) Bus 2 current I_{d2}.

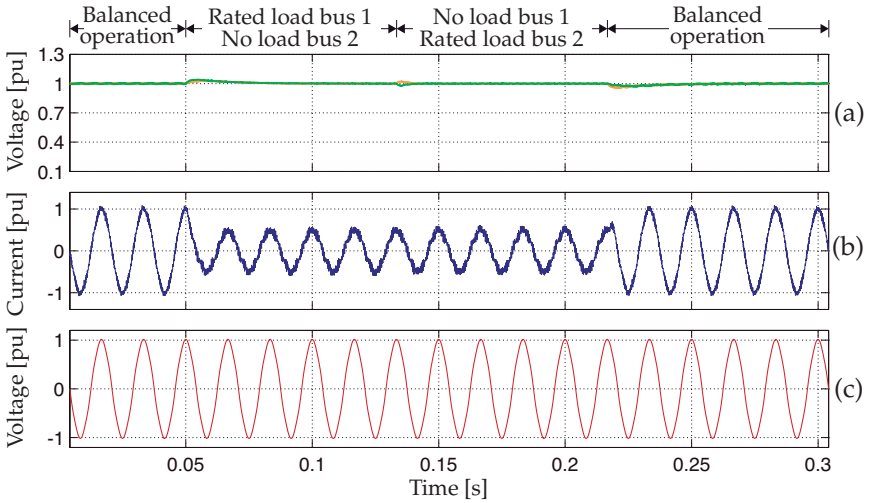


Figure 3.11. Simulated dynamic performance of the system with method 1. (a) DC voltages V_{d1} and V_{d2}. (b) Grid current i_{ga}. (c) Grid voltage v_{ga}.

ics, in order to emulate the voltage in the laboratory and keep the comparison fair, thereby making the scenario more realistic.

As shown, before $t = 0.05$ s the currents I_{d1} and I_{d2} are equal; therefore,

there is no need to generate a balancing action in the fourth leg. Consequently, inductor current i_b is set to zero. When the first load impact occurs, the current demanded by bus 2 becomes zero because there is no load connected and the modulation stage cannot keep the balance under such condition. As such, the dc-dc stage is commanded to generate a current equal to $-2\hat{\epsilon}I_{d1}$, whereas I_{d1} is kept constant at rated condition.

Later, after the second impact at $t = 0.1\bar{3}$ s, the direction of i_b is reversed to compensate the unbalanced condition. As the rated load is connected back to lower bus, the reference current becomes $2\hat{\epsilon}I_{d2}$.

Finally, the system is driven back to a state of balance after $t = 0.21\bar{6}$ s, and given that additional balancing capabilities are not required, the control scheme sets the inductor current to zero. Please note that the required current to be drawn by the dc-dc converter is only a fraction of the rated value; thus, the core losses and current stress on the dc choke are lower.

The proper regulation of the dc-dc stage current i_b leads to balanced capacitor voltages during the whole experiment, as can be seen in Fig. 3.11. The dc voltages are maintained at their references. The results confirm that the presence of the balancing leg overcomes the limitation of the conventional NPC, which is not capable of handling the no load condition in one of the buses while the other is still loaded.

The proper balance of the voltages leads to sinusoidal currents at the input side during the whole operating range, as shown in Fig. 3.11b which provides the waveform of i_{ga}. In addition, during the mentioned scenarios, the system remains in operation with unity power factor, as the current is kept in phase with v_{ga} shown in Fig. 3.11c.

3.5.2 Steady-State Analysis

In this section, steady-state waveforms of the converter voltage are presented in Fig. 3.12 to illustrate the balancing mechanism. Given that the differences between the upper and lower unbalances has already been covered in [64],

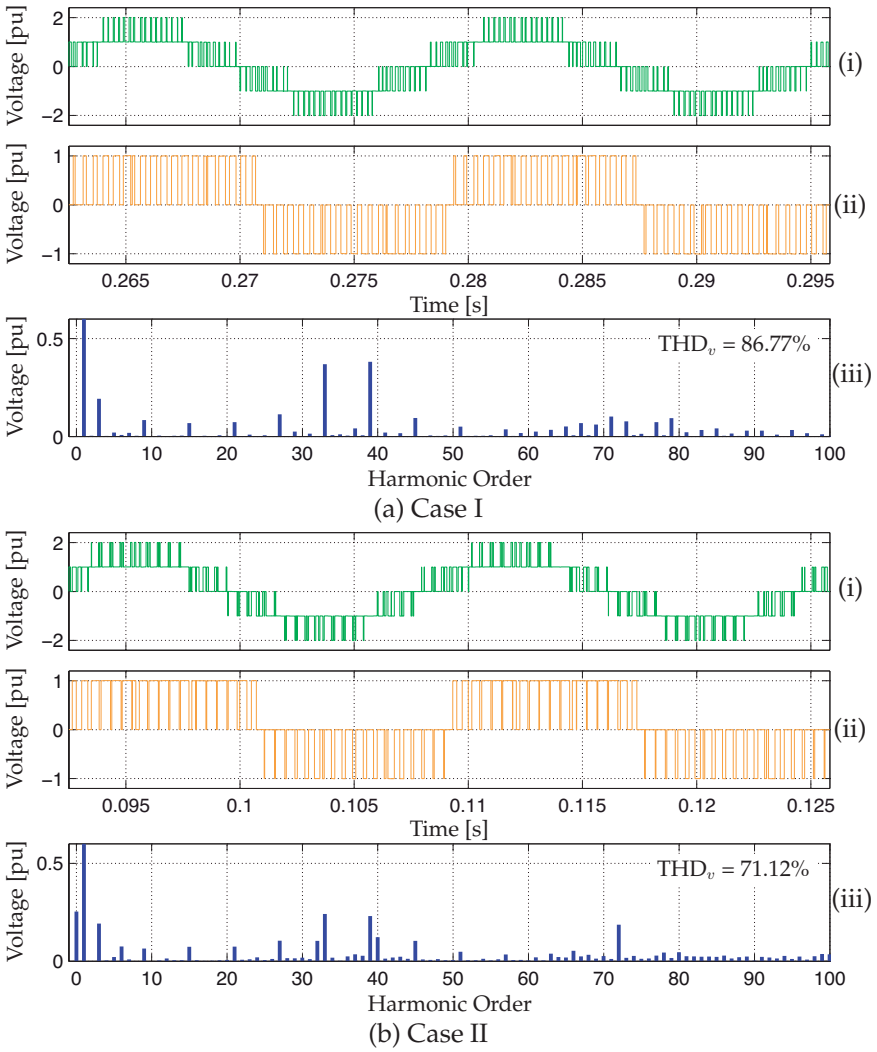


Figure 3.12. Simulated converter voltages with method 1. (i) Line-to-line voltage v_{ab}. (ii) Phase voltage v_{az}. (iii) Fast Fourier Transform (FFT) for v_{az}. (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2.

only one case will be described in detail.

The system behavior for balanced operation is presented in Fig. 3.12a. As shown, no dc drift is injected in either of the voltage signals, which leads to a symmetrical switching pattern during the positive and negative half cycles. This is confirmed by the lack of even-order harmonics in the spectral

components of v_{az}. However, the symmetry in the switching pattern is lost in the presence of load imbalances, because of the redistribution of the small vectors. This situation can be seen in Fig. 3.12bii, where the no load situation in the lower bus leads to the imposition of a positive dc drift to keep the voltages balanced. The dc drift becomes obvious by analyzing the voltage spectrum presented in Fig. 3.12biii. In addition, it is confirmed the balancing method misses the half-wave symmetry, because even-order harmonics appear under the presence of imbalances.

Despite the injection of a dc bias to v_{az} to prevent the drift of the bus voltages, it is confirmed that this effect is reflected neither by the line-to-line voltages nor the input currents. This phenomenon is attributable to the method, which identically modifies the three phases of the converter; therefore, the nonzero dc value is cancelled in the phase-to-phase voltages. The waveform for v_{ab} is presented in Fig. 3.12 for the two analyzed scenarios above, confirming that the balancing action does not introduce a nonzero dc value in the line-to-line voltages.

Finally, the input signals are shown in Fig. 3.13. Once again, the unity power factor operation of the station is confirmed during the whole test. The waveform for i_{ga} is kept sinusoidal in the three analyzed scenarios, with the corresponding increase in the ripple during the unbalanced operation. Moreover, under unbalance operation, these currents also show a lack of half-wave symmetry. This detail is confirmed by its harmonic content presented in Fig. 3.13biii, which contains even order harmonics. Nevertheless, cancellation of the triplen harmonics remains under the presence of unbalanced loads.

3.6 Simulation Results for Method 2

The second balancing strategy proposed is simulated under the same assumptions, for the sake of a fair comparison of the methods. Therefore, the same system in Table 3.3 is simulated using the method of virtual disconnection of the converter neutral.

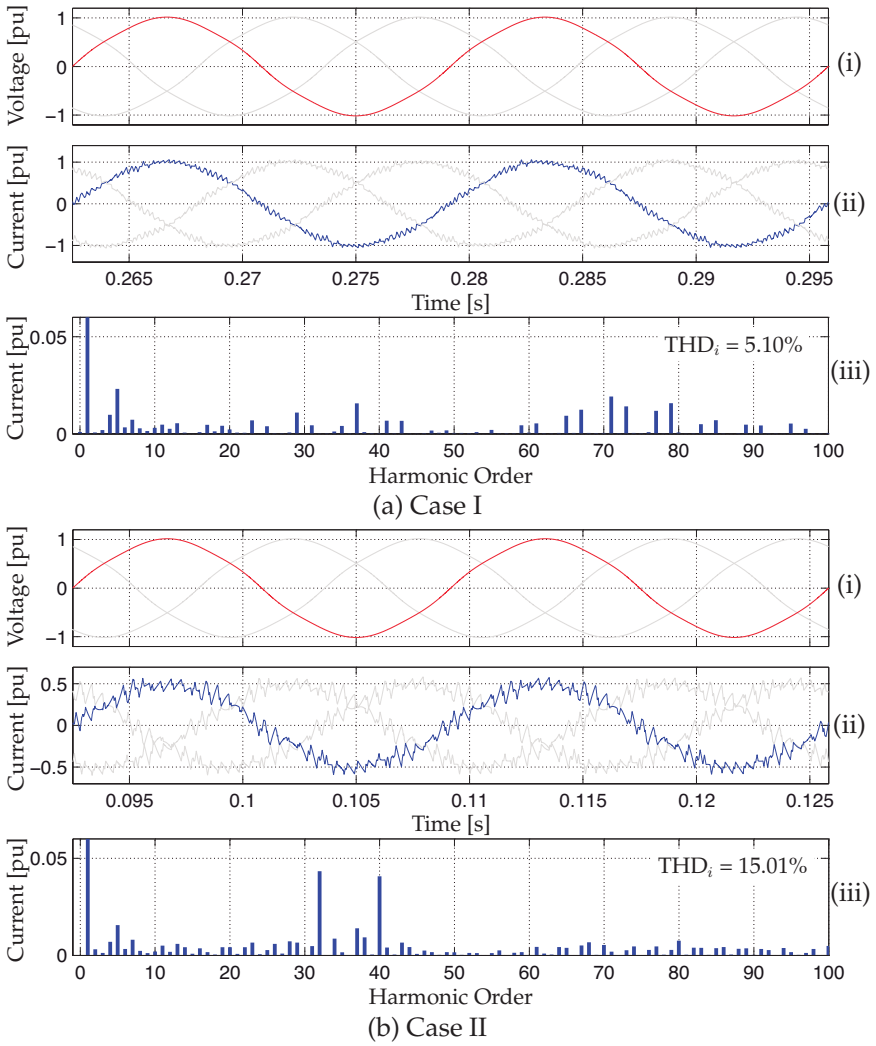


Figure 3.13. Simulated grid signals with method 1. (i) Grid voltage v_{ga}. (ii) Grid current i_{ga}. (iii) FFT for i_{ga}. (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2.

3.6.1 Dynamic Response

The simulated dynamic response of the dc currents is given by Fig. 3.14, which presents the resemblance with the previous case, as the methods share the same operation principle. During balanced operation, no current difference needs to be compensated; therefore, the inductor current is set to zero.

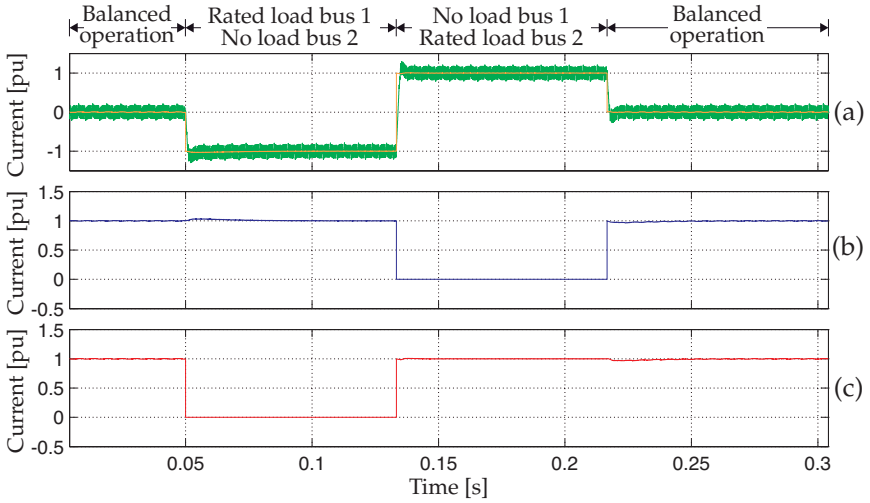


Figure 3.14. Simulated dynamic performance of the system with method 2. (a) Boost current i_b and its reference i_b^*. (b) Bus 1 current I_{d1}. (c) Bus 2 current I_{d2}.

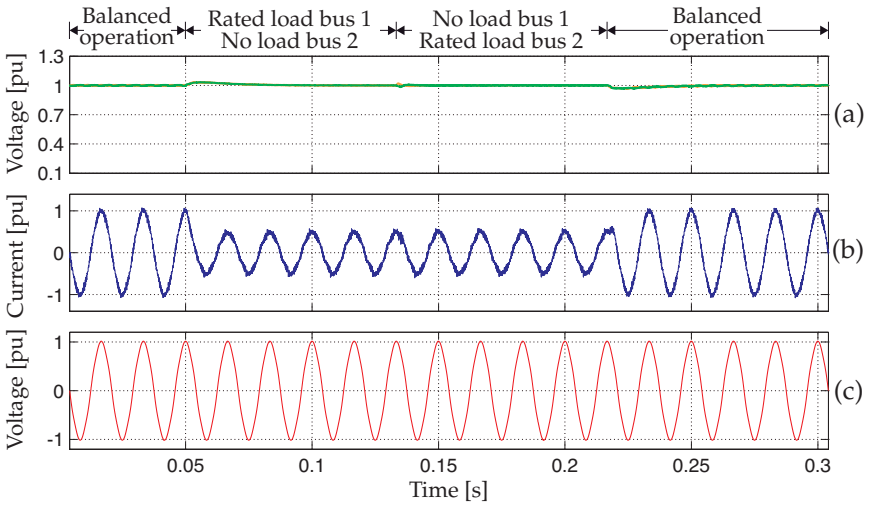


Figure 3.15. Simulated dynamic performance of the system with method 2. (a) DC voltages V_{d1} and V_{d2}. (b) Grid current i_{ga}. (c) Grid voltage v_{ga}.

Then, after the first load impact at $t = 0.05$s, i_b is set to a negative value, in order to provide a return path for the current demanded by the upper bus load. Later, at $t = 0.1\bar{3}$, this current polarity is reversed, as now the no load

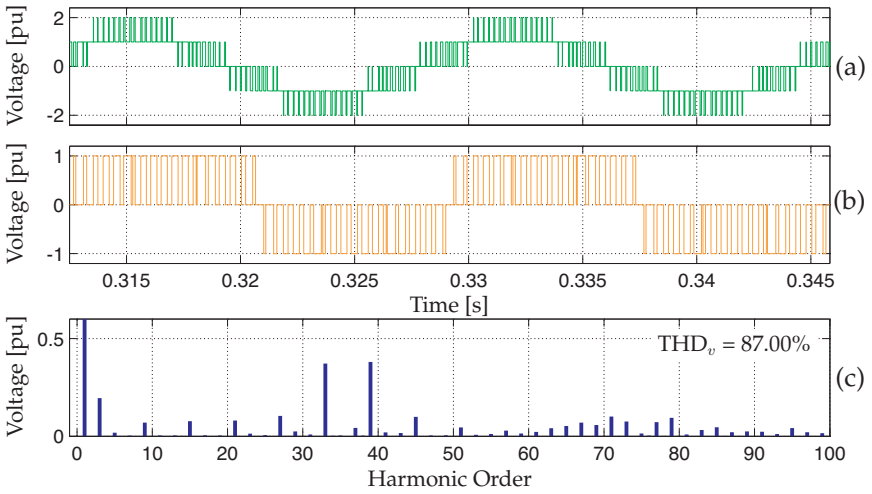


Figure 3.16. Simulated converter voltages with method 2. (a) Line-to-line voltage v_{ab}. (b) Phase voltage v_{az}. (c) FFT for v_{az}.

condition is in the upper bus as suggested by Fig. 3.14. However, in this case the inductor current average value reaches the rated dc current, as it is shown in Fig. 3.14a, given that the balancing leg now handles any current difference between the dc buses. Compared to the previous case the current stress in the dc choke is doubled. This situation exerts an impact on the losses associated to this component.

Subsequently, the proper compensation made at the dc stage allows to have high quality input signals, as it can be observed in Fig. 3.15. The dc voltages remain perfectly balanced during the complete test, resulting in a highly sinusoidal input current, which is shown in Fig. 3.15b. In this case, i_{ga} presents less harmonic distortion compared to the one in Fig. 3.11b, as the central converter is not performing any balancing task, leading to an unaltered switching pattern.

3.6.2 Steady-State Analysis

Considering that this method only presents differences in the unbalanced operation, only these cases will be discussed. First, as stated earlier, the grid-

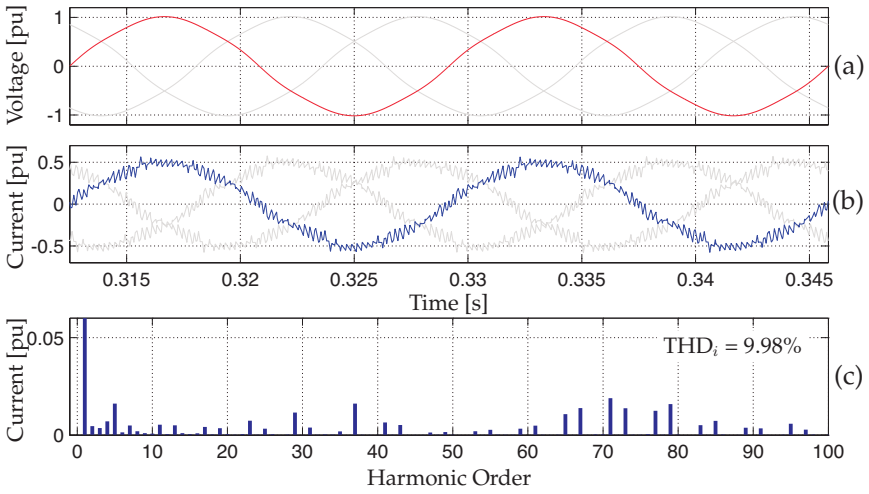


Figure 3.17. Simulated grid signals with method 2. (a) Grid voltage v_{ga}. (b) Grid current i_{ga}. (c) FFT for i_{ga}.

tied converter only performs the regulation of the input currents; hence, no significant dc drift is being injected into the generated voltages, as confirmed by Fig. 3.16, because the voltages v_{ab} and v_{az} do not undergo considerable changes relative to the balanced case, exhibited in Fig. 3.12a. Given that the NPC is not performing any balancing task, the harmonic content of the phase voltages remains unaltered, as it can be observed in Fig. 3.16c, and is therefore kept free of even order components during the whole test.

Finally, the grid voltage and current waveforms under the asymmetrical operation are displayed in Fig. 3.17. It is possible to observe that with this method, the currents under unbalanced operation remains highly sinusoidal as the ripple is kept constant. This yields to an increase in the THD which is only related with the reduction in the fundamental component. Hence, the total demand distortion (TDD) is kept constant. This is because there is no correction being performed by the modulator stage, therefore the switching pattern remains unaltered. In addition, as stated earlier, the modulation index does not vary significantly when the load is changed. Therefore, the high-order components in the current i_{ga} are kept constant, while its fundamental have dropped to half of its value. This can be corroborated with the

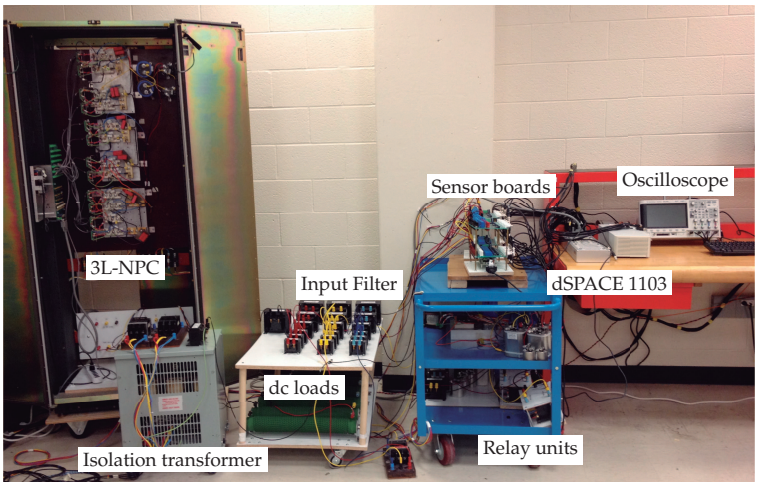


Figure 3.18. Photograph of the experimental setup.

spectral distribution for the input current in Fig. 3.17c.

3.7 Experimental Validation for Method 1

In order to complete the validation for the proposed architecture, experimental results are obtained using a 3.6 kW four leg three-phase NPC based charging station prototype, as shown in Fig. 3.18. The two balancing approaches are applied to verify their effectiveness and highlight their features and disadvantages.

The setup consists of an isolation transformer, an inductive filter, an IGBT-based four leg NPC converter, and a resistive load connected to each dc bus using a relay unit. The control platform used is a dSPACE (DS1103), which generates the gating pattern for the IGBTs. It is important to mention that the SVM algorithm is programmed to have an equivalent switching frequency of 1080 Hz per device. The control scheme is applied to the converter using the parameters presented in Table 3.3. A dynamic test is performed similar to the simulation study given in Fig. 3.10 to confirm the performance of the voltage balancing under any scenario.

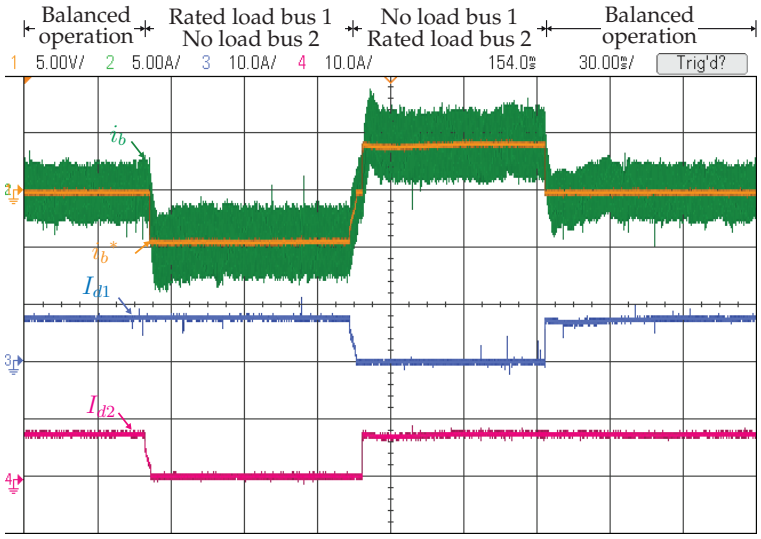


Figure 3.19. Experimental dynamic performance of the system with method 1. Ch1 boost current reference i_b^* (5 V/div). Ch2 boost current i_b (5 A/div). Ch3 bus 1 load current I_{d1} (10 A/div). Ch4 bus 2 load current I_{d2} (10 A/div). Time scale 30 ms/div.

3.7.1 Dynamic Response

The dynamic performance of the charging station is presented in Figures 3.19 and 3.20. It is possible to observe that the overall behavior of the system is close to the simulation results.

The dc currents are presented in Fig. 3.19. The control algorithm is able to extend the balanced operation of the NPC by adjusting the system currents through the bidirectional dc-dc stage. As shown in the previous section, the converter generates a negative current to compensate the no-load condition on the lower bus and positive for the no-load condition on the upper bus. The controller response allows reaching the steady state within two fundamental cycles. The main difference with the simulation results is the mechanical response of the relays, which present a 4 ms delay during the disconnection the loads.

It can be seen that the disconnection of the loads does not happen simul-

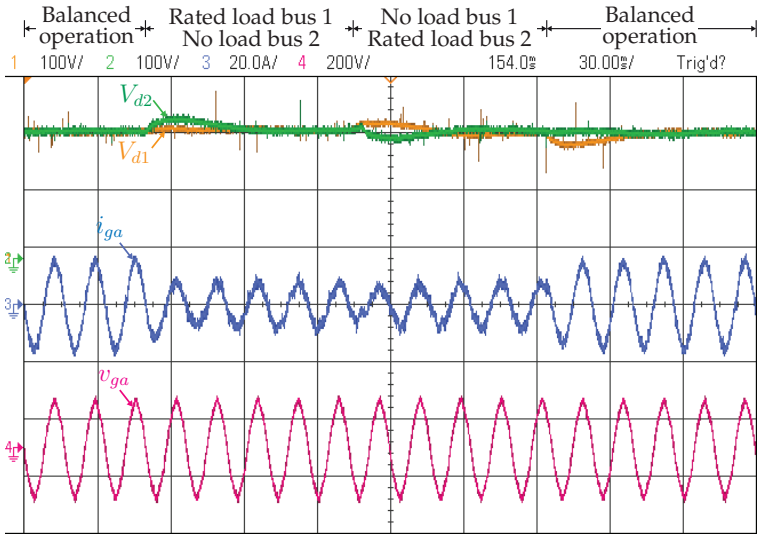
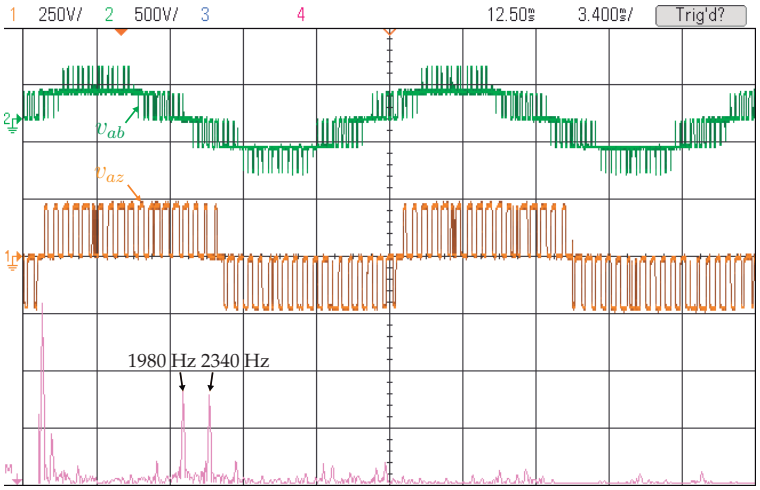


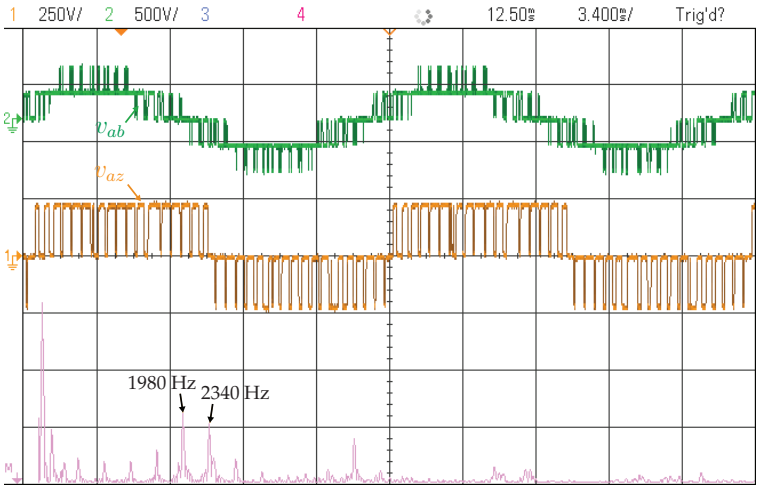
Figure 3.20. Experimental dynamic performance of the system with method 1. Ch1 dc bus 1 voltage V_{d1} (100 V/div). Ch2 dc bus 2 voltage V_{d2} (100 V/div). Ch3 grid current i_{ga} (20 A/div). Ch4 grid voltage v_{ga}(200 V/div). Time scale 30 ms/div.

taneously as in the simulated results, leading to a slight difference in the dynamic response. This is because the relay units have different disconnection responses.

The evolution of the main controlled variables in the VOC loop is presented in Fig. 3.20. The system can maintain the balance of the dc voltages during the entire test and presents minimal deviations from its reference in the transient periods. Additionally, it is confirmed that in steady state, the voltages V_{d1} and V_{d2} are perfectly balanced. This balance at the dc side allows to have a high input current quality, as exhibited in the evolution of i_{ga}. This current is kept highly sinusoidal during the rated-load condition, whereas its quality decreases accordingly during the unbalanced operation with the reduction on the fundamental amplitude and the changes in the switching pattern. The system also operates with unity power factor during the entire test, as the grid current is kept in phase with the grid voltage.



(a) Case I



(b) Case II

Figure 3.21. Experimental converter voltages with method 1. Ch1 phase voltage v_{az} (250 V/div). Ch2 line-to-line voltage v_{ab} (500 V/div). ChM FFT for v_{az} (20 V/div, Span 10 kHz, Center 4.8 kHz). (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2. Time scale 3.4 ms/div.

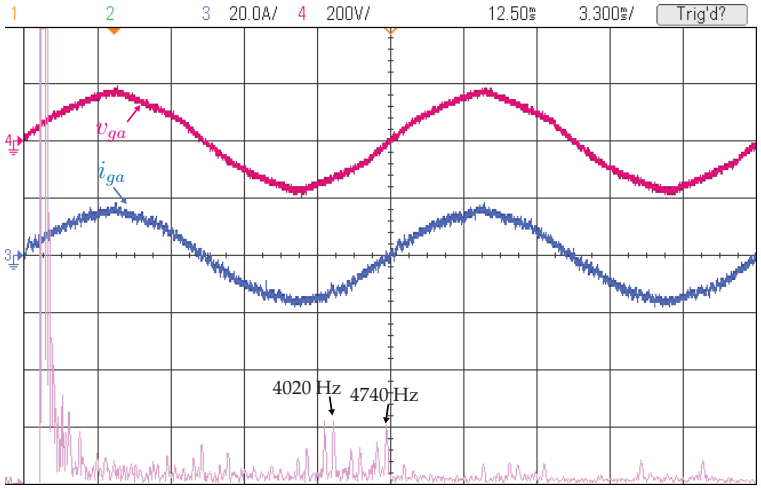
3.7.2 Steady-State Analysis

The waveforms for the voltages generated by the converter are presented in Figure 3.21 and show both the phase to neutral v_{az} and the line-to-line v_{ab} during steady-state operation. During the balanced operation, no dc bias

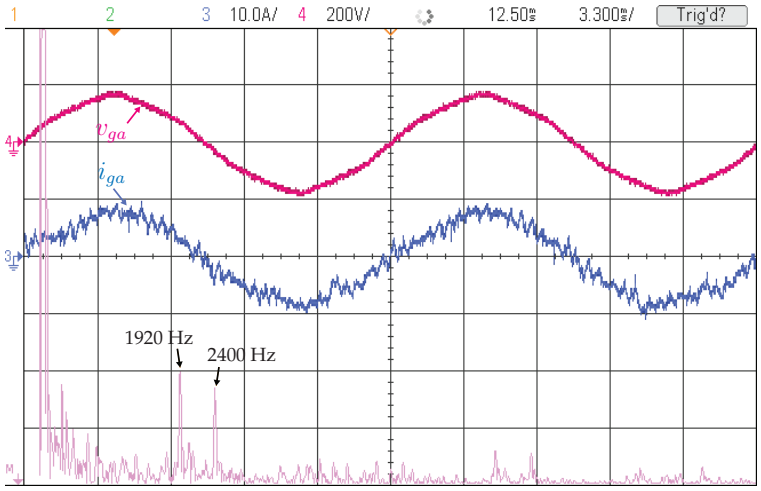
is injected to v_{az} because no current flows through the converter neutral point. The waveform presents half-wave symmetry, which is reflected in a harmonic content free of even-order components. The spectrum provided shows that the dominant harmonics are located in the sidebands around the component m_f. The resulting waveform for v_{ab} presents a steeped waveform with five levels, which are clearly defined due to the proper regulation of the midpoint voltage.

The dc drift injected by the midpoint controller becomes obvious in Fig. 3.21b. In case II, the system compensates for the no-load condition in the lower bus by injecting a positive dc value, thereby widening during the positive half cycle. Consequently, the symmetry in the generated voltage is missed, which leads to the appearance of even-order components in its spectrum. This appearance influences the demanded current distortion. Nevertheless, given that the compensation is injected equally to the three phases of the converter, the line-to-line voltages present a zero dc value in all the scenarios. The dominant harmonics of the current have shifted to lower frequencies, situation which can be explained by the partial balancing performed by the modulator, as the change in the width of the pulses results in a lower equivalent switching frequency, as exhibited in v_{ab}.

The ac side quantities are illustrated in Fig. 3.22 to complete the analysis in steady state. The experimental waveforms for the rated load condition of case I are presented in Fig. 3.22a. The results obtained confirm the correct performance of the proposed control scheme. The accuracy of the control of the mid point-voltage becomes clear, as the dc buses voltages are kept balanced, thereby leading to high-quality currents at the input side. The current i_{ga} exhibits a highly sinusoidal behavior with a fundamental of 15.35 A and reduced ripple, and is in phase with v_{ga}. A THD of 5.8% is obtained for the rated load condition. In the Figure, it also becomes evident the harmonic distortion present in the grid voltage. Then, in the case of unbalanced operation of Fig. 3.22b, proves that the system is able to operate properly even if one of the loads is disconnected at the dc side. The current is kept sinusoidal, but its ripple has increased, this is explained by the reduction of fundamental com-



(a) Case I



(b) Case II

Figure 3.22. Experimental grid signals with method 1. Ch3 grid current i_{ga} (20 A/div). Ch4 grid voltage v_{ga} (200 V/div). ChM FFT for i_{ga} (100 mA/div, Span 10 kHz, Center 4.8 kHz). (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2. Time scale 3.3 ms/div.

ponent of the current to 7.58 A. As established earlier, the modulation index in grid tied operation with unity power factor varies slightly under different load conditions. Therefore, the amplitude of the high frequency components is kept almost constant, thereby increasing its influence on the demanded current. This condition, along the lack of symmetry in the generated volt-

age, alters the distribution of the harmonics components, that is, shifting the dominant ones to lower orders. This result is confirmed by the input current spectrum shown in Figures 3.22a and 3.22b, showing that under balance operation, the dominant harmonics of i_{ga} are located in the sidebands around $2m_f$, but in the presence of unbalances, most of the energy is concentrated around m_f, thus are less mitigated by the action of the input filter.

The grid current THD under imbalance reaches a 14.9%, which corresponds to a TDD of 7.35%. This value is within the admissible limits of the grid code for the intended power levels ($20 < I_{\text{sc}}/I_{\text{L}} < 50$) [66]. Furthermore, if the unbalanced operation does not exceed 1 h in length, then it is considered as a unusual condition, and the system meets the grid code regardless of the $I_{\text{sc}}/I_{\text{L}}$ ratio.

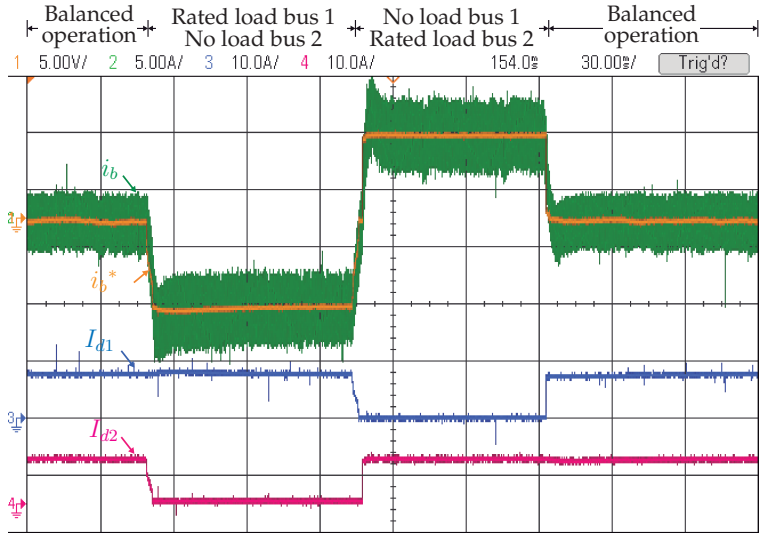
3.8 Experimental Validation for Method 2

Method 2 is applied to the setup displayed in Fig. 3.18 under the same dynamic scenario proposed for the first balancing method.

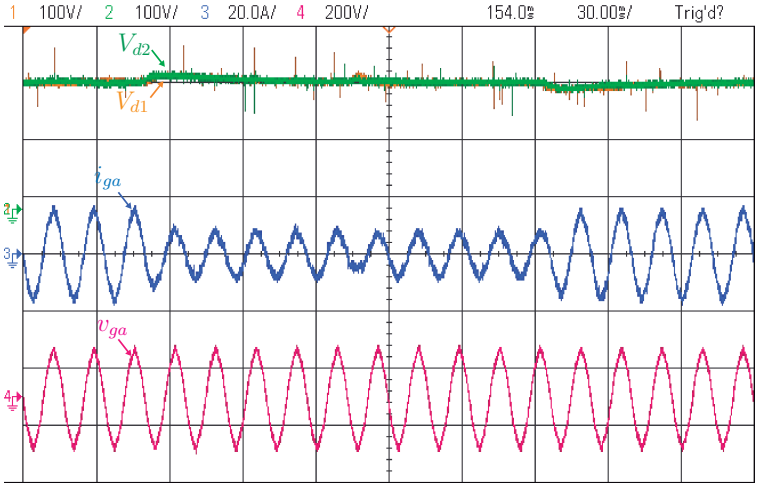
3.8.1 Dynamic Response

The analysis the acquired waveforms provided by Figures 3.23a and 3.23b, indicates a performance similar to that obtain with the previous method. As discussed in the simulation section, this approach results in a larger current stress in the dc inductor, as it handles the rated dc current in the worst-case scenario. This result is confirmed in Fig.3.23a, which shows that the average current driven by the balancing leg now reaches 7.5 A (doubling the previous case), thereby imposing larger requirements on the design and selection of this component.

This alternate compensation in the dc currents again leads to balanced voltages in the buses, as exhibited in Fig. 3.23b. On top of that, the virtual disconnection method has a faster response than the previous approach, be-



(a) dc currents



(b) VOC signals

Figure 3.23. Experimental dynamic performance of the system with method 2. (a) DC currents. Ch1 boost current reference i_b^* (5 V/div). Ch2 boost current i_b (5 A/div). Ch3 bus 1 load current I_{d1} (10 A/div). Ch4 bus 2 load current I_{d2} (10 A/div). (b) VOC signals. Ch1 dc bus 1 voltage V_{d1} (100 V/div). Ch2 dc bus 2 voltage V_{d2} (100 V/div). Ch3 grid current i_{ga} (20 A/div). Ch4 grid voltage v_{ga} (200 V/div). Time scale 30 ms/div.

cause the effect of the disturbances on the dc voltages under the load impacts are smoother than those observed in Fig. 3.19.

Accordingly, the input current remains as a sinusoid with minimal distortion during the test, as the balancing technique eliminates the influence of the disturbances immediately. Moreover, Fig. 3.23b shows that the system always operates with unity power factor, as i_{ga} and v_{ga} are kept in phase regardless of the load condition.

3.8.2 Steady-State Analysis

The steady-state operation is discussed to complete the validation of the method. The generated voltages are displayed in Fig. 3.24. Given that no dc voltage compensation occurs from the grid-tied converter, the waveforms do not exhibit major differences from the balanced case in Fig. 3.21a. For this reason, this approach results in converter voltages free from even order components under any load scenario. This result can be confirmed by the FFT for v_{az} provided by Fig. 3.24.

In consequence, the grid current shown in Fig. 3.25 presents higher quality because its distortion levels have remained unchanged from the balanced

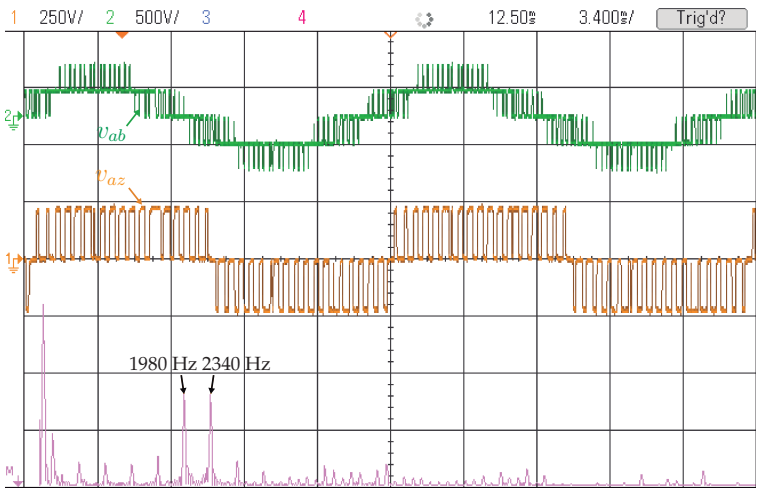


Figure 3.24. Experimental converter voltages with method 2. Ch1 phase voltage v_{az} (250 V/div). Ch2 line-to-line voltage v_{ab} (500 V/div). ChM FFT for v_{az} (20 V/div, Span 10 kHz, Center 4.8 kHz). Time scale 3.4 ms/div.

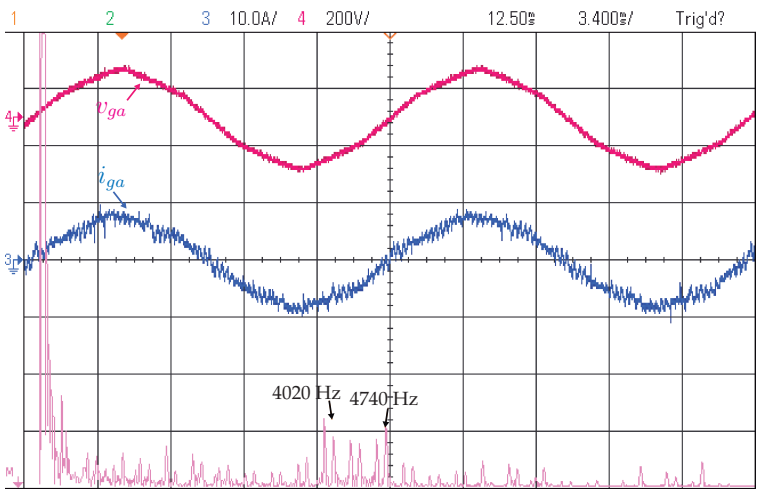


Figure 3.25. Experimental grid signals with method 2. Ch3 grid current i_{ga} (20 A/div). Ch4 grid voltage v_{ga} (200 V/div). ChM FFT for i_{ga} (100 mA/div, Span 10 kHz, Center 4.8 kHz). Time scale 3.4 ms/div.

condition of Fig. 3.22a. This result is confirmed as its harmonic content still concentrates most of its energy in the components around $2m_f$. The resulting THD for i_{ga} during unbalanced operation is 11.1%, and its increase is only related exclusively to the reduction in the fundamental amplitude, which is now 7.61 A. This means that the TDD has remained constant. Therefore, the system will meet the grid code requirements under any load condition regardless of the duration of the unbalanced operation.

3.9 Summary

A novel architecture for fast charging stations for EVs is proposed and validated. The architecture is based in the use of a single grid-tied NPC converter that enables a bipolar dc bus. Its main features are the megawatt range capability, a single ac-dc stage for powering several charging units, the sustained step down effort of the chargers, a balanced operation during any load scenario and the possibility to include additional storage or generating units into the system. The structure can be installed in different locations through-

out the city, which enables alternatives for refueling EVs in shorter times, in order to increase its acceptance.

The use of a multilevel converter enables the application in MV (lower currents, smaller ac chokes), and improved THD and power quality. Such a converter also enables a possible scale up in the power ratings, if necessary. The limited unbalanced operation of the converter is used to provide a complimentary solution and overcome its limits, which allows the operation in any load scenario.

Regarding the balancing techniques proposed, two methods are successfully validated through experiments, maintaining the balance in the system under severe unbalanced operation. The complimentary balancing concept reduces the dc current flowing in the balancing circuit, to only a fraction of the demanded current. This concept reduces the stress on the switches, the size of the inductor and also use higher switching frequencies. This is possible because the scheme exploits the balancing capabilities of the modulator and only uses the balancing circuit as a complement. In the case of the virtual disconnection of the neutral point, the balancing tasks are exclusively performed by the additional leg. Thus, the current stress in the dc choke is higher, altering the efficiency of the balancing dc-dc stage and the inductor design. However, this approach allows to keep the distortion of the input currents to be constant under any load scenario, thereby maximizing the the high power quality offered by the central NPC converter.

The distributed dc bus structure allows to reduce the power conversion stages in the system, thereby also reducing the costs and improving the overall efficiency. In addition, the structure facilitates the integration of PV generation and energy storage systems. Such an integration enables the opportunity to reduce the power demand of the chargers and provide support to the grid.

CHAPTER IV

EV CHARGING STATION WITH AN ENERGY STORAGE STAGE FOR DC BUS VOLTAGE BALANCING

IN THE PREVIOUS chapter, the bipolar dc bus architecture is validated for its continuous operation, even under severe load unbalances. This validation is conducted by adding an additional circuit to the system, which enhances the balancing capabilities of the grid-tied converter. The result leads to balanced dc voltages even under severe unbalanced load conditions.

Taking a different approach, this chapter provides the additional balancing capabilities using an energy buffer. As mentioned earlier, the selected charging station architecture allows the inclusion of optional ESSs, which are intended to be used in energy management tasks. However, it is possible to extend its operation, and the complimentary balancing capabilities required by the central converter can be provided. The presence of a stationary load in the system can be utilized to balance the dc voltages. This eliminates the additional NPC leg, thereby reducing the system cost. Moreover, the presence of this stage will allow the use of off-the-shelf products for both the central converter and the fast charging units. This use of such standardized components decreases hardware costs and improved system robustness, aside from

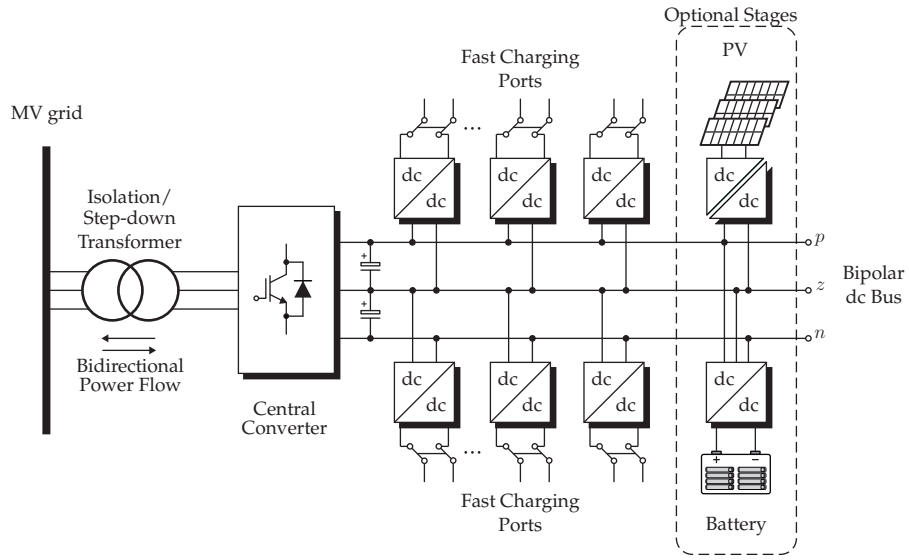


Figure 4.1. Proposed charging station architecture with balancing ESS

resulting in cost-effective implementation and maintenances [37].

In the following sections, the inclusion of a battery ESS in the system is discussed. This additional stage performs the energy buffer tasks and the complimentary balancing of the dc voltages. In order to do so, a dc-dc stage with access to both of the dc buses must be included, to avoid having two batteries in the system, as shown in Fig. 4.1. To meet this purpose, a three-level dc-dc stage is featured. A control scheme is developed and proposed, which covers the partial balancing tasks. A comparison with the balancing leg approach is also discussed.

The overall performance of the system is validated both in simulation and experiment.

4.1 Three-Level DC-DC Stage for ESS

As stated earlier, the ESS must have access to both dc buses in order to perform the balancing compliment to the grid-tied converter. Considering this requirement, a three-level dc-dc converter will be used as the dc-dc stage.

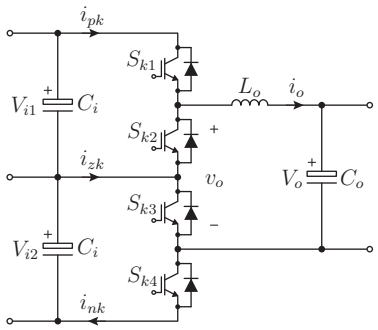


Figure 4.2. Circuit diagram for the three-level dc-dc stage for the ESS.

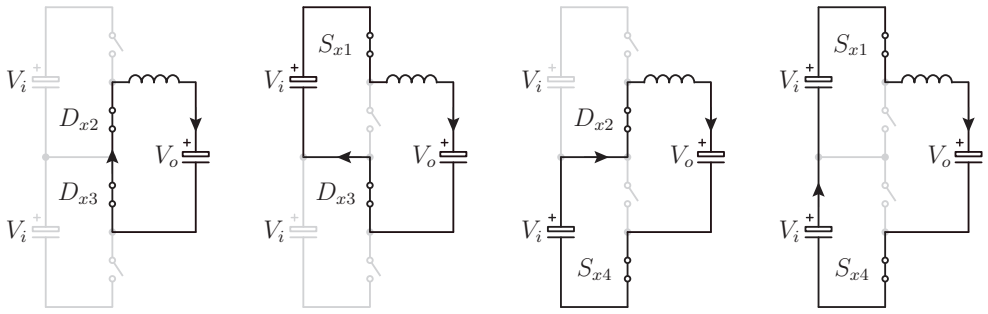
This selection is further justified by the reduced voltage stress on the switching devices, thereby allowing the use of conventional low-voltage-rated switches with improved output current waveform and improved efficiency in comparison to conventional two-level-based topologies [67]. This particular application requires including only a single ESS, as such converter is able to compensate currents in both of the dc buses.

The power circuit of the selected topology is presented in Fig. 4.2, which presents three input terminals that can be directly connected to the bipolar charging station. The converter is composed of four switching devices, along with their corresponding freewheeling diodes and output inductor L_o and capacitor C_o for filtering purposes.

Considering its structure, the basic requirement that $V_{i1} = V_{i2} = V_i$, and the valid combination of its switching signals, the converter generates four voltage states, which are resumed in Table 4.1, using the same nomenclature employed in the NPC to identify the switching states. Each state results in a different equivalent circuit, as presented in Fig. 4.3. These states are depicted as follows: When the inner switches S_{k2} and S_{k3} are turned on, the output voltage is equal to zero. When S_{k1} and S_{k3} are on, v_o becomes V_i. When the switches that are on are S_{k2} and S_{k4}, the same output voltage is generated. Finally, when the switches S_{k1} and S_{k4} are turned on, the output voltage v_o is equal to the total input voltage $2V_i$. Please note that the switching states $\mathbf{v}_{1\mathrm{P}}$ and $\mathbf{v}_{1\mathrm{N}}$ generate opposite neutral point currents, revealing the balancing

Table 4.1. 3L dc-dc converter switching states

States	Switching State	Output Voltage	Neutral Current
$\mathbf{v}_0$	[OO]	0	$i_{zk} = 0$
$\mathbf{v}_{1\mathrm{P}}$	[PO]	V_{i1}	$i_{zk} < 0$
$\mathbf{v}_{1\mathrm{N}}$	[ON]	V_{i2}	$i_{zk} > 0$
$\mathbf{v}_2$	[PN]	$2V_i$	$i_{zk} = 0$



(a) $\mathbf{v}_0$ (b) $\mathbf{v}_{1\mathrm{P}}$ (c) $\mathbf{v}_{1\mathrm{N}}$ (d) $\mathbf{v}_2$

Figure 4.3. Four switching states and their equivalent circuits.

capabilities of the converter. This state will be denominated mid-state for the rest of the chapter.

4.2 Operation Principle

According to the circuit diagram in Fig. 4.2, the operation of the outer switches S_{k1} and S_{k4} must be complimentary to the inner switches S_{k2} and S_{k3}, respectively, in order to avoid short-circuiting the input voltage sources. Therefore, the operation of the converter is regulated through two independent gating signals g_1 and g_4. These signals are usually generated using pulse-width modulators with phase-shifted carriers [67,68]. However, taking into account the generated switching sequence, it can also be synthesized by the a single phase SVM approach. The sequence will vary wether $d_o \leq 0.5$ and $d_o > 0.5$. This topic is discussed further in the succeeding sections.

4.2.1 Small Duty Cycle

To start the analysis, the average value of the output voltage is given by

$$V_o = \frac{1}{T_s}\int_0^{T_s} v_o(\tau)\mathrm{d}\tau, \tag{4.2.1}$$

This voltage is applied to the terminals of the ESS. By assuming that this voltage results in $d_o \leq 0.5$, the required reference that synthesizes it is defined as

$$V_o = \frac{1}{T_s}\left(t_a\mathbf{v}_{1\mathrm{P}} + t_b\mathbf{v}_{1\mathrm{N}} + t_c\mathbf{v}_0\right), \tag{4.2.2}$$

where t_a, t_b and t_o represent the dwell times of each state.

On the other hand, the duty cycle d_o is defined by the ratio between the output and input voltages, according to:

$$d_o = \frac{V_o}{2V_i}. \tag{4.2.3}$$

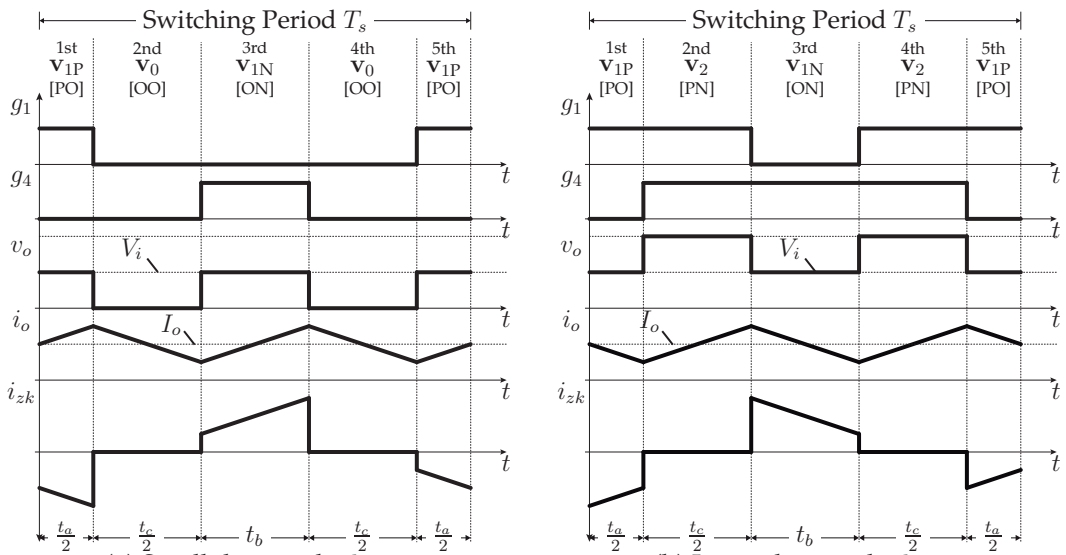
Considering the output voltages in Table 4.1 and replacing (4.2.2) into (4.2.3) the following expression are obtained:

$$d_o = \frac{d_aV_{i1} + d_bV_{i2}}{2V_i}, \tag{4.2.4}$$

$$d_k = \frac{t_k}{T_s}, \text{ where } k = (a, b, c). \tag{4.2.5}$$

Please note that the duty cycles d_a, d_b and d_c have been introduced.

The previous result reflects that, during normal balanced operation, the duty cycles for the outer switches are equal to d_o, as the voltages V_{i1} and V_{i2} are equal. In the presence of different dc voltages, the duty cycles d_a and d_b will be redistributed according to this voltage drift, in order to retrieve the balance condition. This results in the five segment sequence for the SVM principle shown in Fig. 4.4a.



(a) Small duty cycle $d_o \leq 0.5$ (b) Large duty cycle $d_o > 0.5$

Figure 4.4. Five segment switching sequence for SVM.

4.2.2 Large Duty Cycle

If the output voltage is larger than V_i, the sequence varies as follows. In this case, the output voltage is synthesized by

$$V_o = \frac{1}{T_s}\left(t_a \mathbf{v}_{1\mathrm{P}} + t_b \mathbf{v}_{1\mathrm{N}} + t_c \mathbf{v}_2\right). \tag{4.2.6}$$

Regardless the relationship between V_{i1} and V_{i2}, the duty cycle for $\mathbf{v}_2$ is equal to

$$d_c = 2d_o - 1. \tag{4.2.7}$$

Finally, replacing (4.2.7) into (4.2.6) and clearing the total duty cycle lead to

$$d_o = 1 - \frac{d_a V_{i1} + d_b V_{i2}}{2V_i} \tag{4.2.8}$$

The previous operation mode is illustrated in Fig. 4.4b. An important remark from the operating conditions displayed in Fig. 4.4, is the confirmation

that the redundancies of the state $\mathbf{v}_1$ generates opposite currents circulating through the neutral point i_{zk}. When the positive redundancy is employed, a negative average current flows through the neutral point, whereas a positive average value for i_{zk} is imposed when $\mathbf{v}_{1\mathrm{N}}$ is used. This concept will be used to develop the balancing scheme employed in this chapter.

4.3 Voltage Balancing Technique

As established in the previous chapter, the asymmetrical operation of the bipolar dc bus requires a minimal power ratio between the dc buses, which is determined by the grid-side modulation stage. The motivation of this chapter is to use the ESS to perform the balancing tasks when the system is driven out of its balanced zone. The fundamental difference with the previous technique is that the minimal load condition is no longer emulated, as the ESS remains permanently connected to the system. This approach redistributes the power consumption in order to satisfy the minimal power ratio allowed by the modulator, by concentrating it to the bus with lighter load. The complete analysis is given in the following sections.

4.3.1 Small Duty Cycle

For the first case, is necessary to revisit the example presented in Fig. 4.4a and assume there is no load connected to the upper bus, while the lower one is operating under rated condition. The last chapter demonstrated that, in order to keep the dc voltages from drifting, the following condition must be met under any scenario:

$$\min\{P_{d1}, P_{d2}\} \geq \epsilon \max\{P_{d1}, P_{d2}\}. \tag{4.3.1}$$

As stated earlier, the imbalances are compensated by redistributing the usage of the mid-states. This condition allows selecting which bus provides power to the ESS. Accordingly, the redistribution is conducted in such a way that the positive bar current i_{pk} must be equal to ϵI_{d2}. From Fig. 4.4a, it can be

deducted that this current is related with the output current i_o according to

$$i_{pk} = d_a i_o. \tag{4.3.2}$$

Additionally, assume that in order to meet the minimal load condition, the output current is such as it requires to exclusively use the positive redundancy of $\mathbf{v}_1$. This requirement leads to $d_a = 2d_o$. In consideration of the previous analysis, the minimal value for i_o that allows to meet the balancing condition is defined as

$$i_o = \frac{\epsilon I_{d2}}{2d_o}. \tag{4.3.3}$$

This is an interesting result, as it demonstrates that an ESS with a power equivalent to $\epsilon P_b/(2+\epsilon)$ is required in order to guarantee a balanced operation of a system rated at P_b. Moreover, it is worth mentioning that, despite the redistribution that the modulator is performing, the power delivered to the battery remains unaltered for this duty cycle range.

In the case the imbalance is located at the lower dc bus, the procedure is analogous because the battery requires to drain at least a current defined by

$$i_o = \frac{\epsilon I_{d1}}{2d_o}, \tag{4.3.4}$$

while employing exclusively the mid-state $\mathbf{v}_{1\mathrm{N}}$.

4.3.2 Large Duty Cycle

The balancing principle is the same for different modulation indexes, and the generated compensation current changes are demonstrated below. Using the example provided in Fig. 4.4b, and again assuming the unbalance location is the upper bus, the required value for i_{pk} to achieve the dc voltage balance is still set by (4.3.1), which must be equal to ϵI_{d2}. The relationship between this current and i_o is modeled by (4.3.2). Given that the positive redundancy is being exclusively used, the required output current is now defined as

$$i_o = \frac{\epsilon I_{d2}}{2(1-d_o)}. \tag{4.3.5}$$

This result demonstrates that, for large duty cycles, the minimal ESS power rating that can keep the system balanced under any load scenario is given by $\epsilon d_o P_b/(2-2d_o)$. In other words, in this duty cycle range, the ESS required to maintain the system balanced has higher power ratings. In case of having the imbalance located in the lower bus, the equations must change accordingly, assuming that only $\mathbf{v}_{1N}$ is being used.

4.4 Proposed Control Scheme

Considering that the ESS remains as a stationary load to in the system, which can drain power from any of the buses, its usage can be maximized. This is done by using its charging process to compensate for the imbalances in the system. For this reason, the overall structure of the grid-side controller that regulates the central NPC converter does not need to be modified. However, a change is introduced in the switching sequence employed in order to overcome the generation of even-order harmonics during the unbalanced operation.

4.4.1 Modified Sequence Under Unbalanced Operation

Considering the results obtained in the previous chapter, the main disadvantage of the control scheme was the presence of even-order harmonics in the line current during unbalanced load operation because the half-wave symmetry is missed. This is not desirable for grid-connected tasks because the grid code sets stringent limits for this particular components and must therefore be solved. The SVM switching sequence is modified during these instants in order to retrieve the half-wave symmetry and guarantee line currents without even-order harmonics.

As mentioned earlier, the dwell times for positive and negative small vectors are redistributed according the dc voltage deviations, using a PI controller to maintain the balance. To do so, the controller actuation Δ_s is fed to

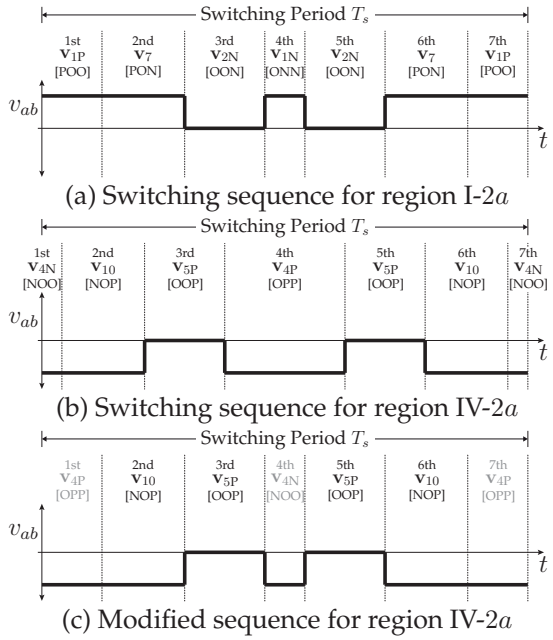


Figure 4.5. SVM switching sequences during unbalanced operation.

the SVM modulator to adjust the dwell times according to (3.3.16).

Considering the same voltage reference of the scenario in Fig. 3.5b, but in the presence of an unbalance at the dc side that results in $\Delta_s = -1/3$. This condition leads to $t_{a_P} = 2t_{a_N}$, and the resulting sequences are the ones shown in Fig. 4.5. It becomes clear how the balancing mechanism modifies the switching sequence, which leads to a lack of half-wave symmetry on the line to line voltages. This yields of even-order harmonics on the line currents.

Given that dwell times redistribution is necessary to balance on the dc voltages, a modification of the switching sequence is proposed to maintain the symmetry, and it will only be used when the dc loads are different. This modification is simply to swap the position of the negative and positive vectors in one of the the sequences, in order to retrieve the half wave symmetry. In the studied case, the type B sequence is modified by swapping $\mathbf{v}_{5\mathrm{P}}$ and $\mathbf{v}_{5\mathrm{N}}$. Is important to note that the condition of changing only two switches per segment is missed because of the swapping of the small vectors. This modification leads to the switching sequence presented in Fig. 4.5c for the

region IV-2a. Figure 4.5 shows that the symmetry in the line-to-line voltages is retrieved. However, the retrieval is achieved at the expense of increasing the number of switchings per sampling period.

4.4.2 ESS Controller

The following operation principle is proposed to regulate the ESS. First, the battery controller will not be modified in any way, generating the required duty cycle value d_o to regulate its voltage. Second, depending on the location of the imbalance, the dc-dc stage redistributes the usage of the mid-states $\mathbf{v}_{1\mathrm{P}}$ and $\mathbf{v}_{1\mathrm{N}}$ such that it drains the minimal current from the less congested bus. This redistribution is entirely related with the usage of the small vectors of the central stage controller. Thus, the same actuation Δ_s can be used for this purpose. In addition, in order to minimize the required battery power ratings, the ESS voltage is selected to be lower than V_i

The required controller for the ESS is presented in Fig. 4.6, which confirms that the controller for the battery is the conventional cascaded loop, that operates in constant current (CC) or constant voltage (CV) modes depending on its SOC. Additionally, it can be seen that the whole regulation of the ESS is governed by the battery management system (BMS), emphasizing that the main purpose of the ESS is to perform the energy management tasks. This structure generates the required d_o, and the modulator stage performs the redistribution of the states, using the information provided by the midpoint controller. This modification is done to the duty cycles d_a and d_b according to

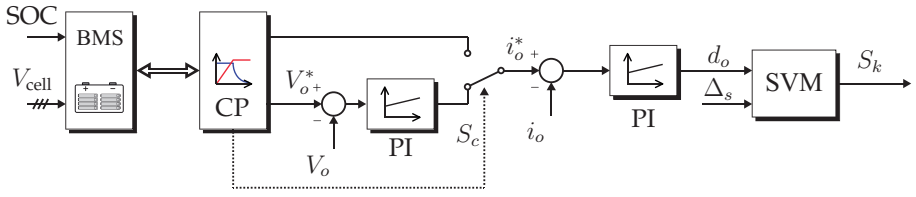


Figure 4.6. Proposed controller for the balancing ESS.

$$d_a = d_o(1 + \Delta_s) \tag{4.4.1}$$

$$d_b = d_o(1 - \Delta_s). \tag{4.4.2}$$

4.5 Simulation Results

Considering the proposed compensation technique to keep the dc-link voltages balanced, the system is simulated using the same dynamic scenarios forced in the previous chapter. In addition, the proposed switching sequence

Table 4.2. Simulation and experimental parameters for ESS system

Paramenter	Symbol	Value
Grid Voltage Amplitude	V_g	1 pu
Grid Frequency	f_g	1 pu
Input Filter Inductance	L_g	0.1 pu
Input Filter Resistance	R_g	0.02 pu
dc-Link Capacitance	C_d	4.5 pu
dc-Link Voltage	V_d	2.2117 pu
Output Filter Inductance	L_o	0.18 pu
Output Filter Capacitance	C_o	1.8 pu
ESS Rated Power	P_{ss}	0.1402 pu
Switching Frequency	f_s	36 pu
Amplitude Modulation Index	m_a	0.6433
Frequency Modulation Index	m_f	36
Critical Load Ratio	$\hat{\epsilon}$	0.2823
Simulation Base Voltage	V_{B}	4160/960 V
Simulation Base Power	P_{B}	1.38 MW
Experimental Base Voltage	V_{B}	208 V
Experimental Base Power	P_{B}	3 kW
Base Frequency	f_{B}	60 Hz

correction is performed in order to keep the ac side currents free of even-order harmonics. The simulation parameters are presented in Table 4.2. Only the power rating of the station has been increased in order to include the ESS. In this case, a 1.38 MW charging station is simulated using Matlab/Simulink®.

4.5.1 Dynamic Performance

The study of the dynamic performance in the presence of severe load impacts is the first stage of validation. As mentioned earlier, this validation is designed simulate the volatile loads that the EVs represent. Figure 4.7 exhibits the dynamic evolution of the dc currents in the system. It is possible to see that before $t = 0.05$ s, the system operates with symmetrical dc loads, as $I_{d1} = I_{d2}$. Hence, any current compensation does not need to be generated with the balancing ESS. Given that the usage of the mid-states does no need to be redistributed, the average value of i_{zk} is zero, while the ESS continues its charging process. Then, at the instant when the first load impact occurs, the current I_{d2} goes to zero, and in order to keep the voltages from drifting,

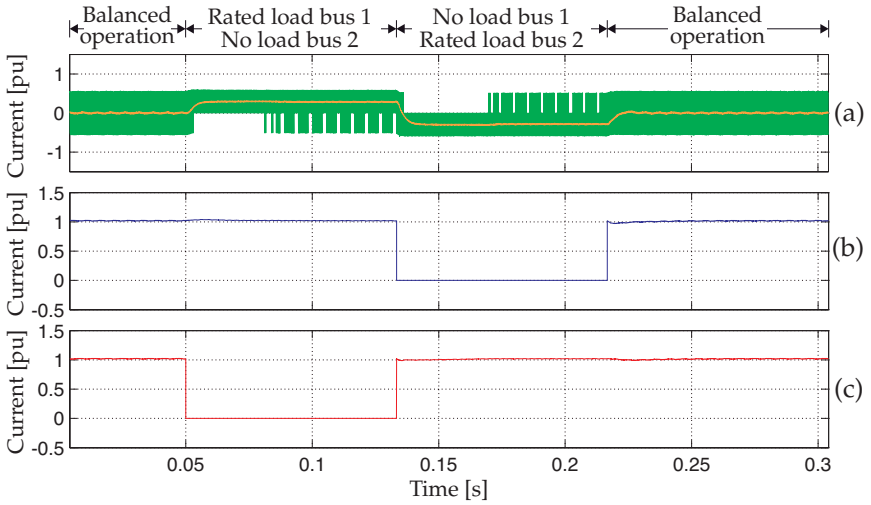


Figure 4.7. Simulated dynamic performance of the ESS system. (a) Neutral point current i_{zk} and its average value I_{zk}. (b) Bus 1 current I_{d1}. (c) Bus 2 current I_{d2}.

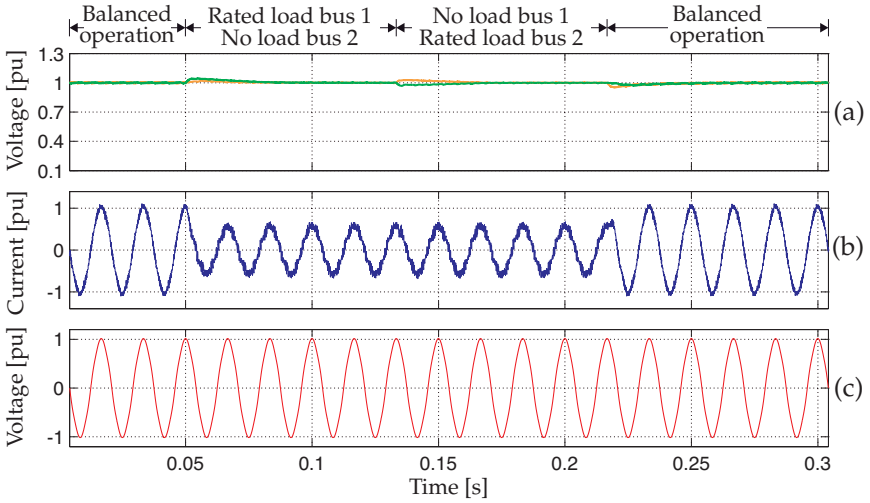


Figure 4.8. Simulated dynamic performance of the ESS system. (a) DC bus voltages V_{d1} and V_{d2}. (b) Grid current i_{ga}. (c) Grid voltage v_{ga}.

the system forces the power demand to be exclusively from the lower bus. This condition is confirmed by the positive average value of i_{zk}. Similar to that in previous chapter, I_{d1} remains unaltered, thereby demonstrating the independent operation of the dc buses.

Later on, the asymmetrical operation is reversed at $t = 0.1\bar{3}$ by disconnecting the load in bus 1 and reconnecting the rated load to bus 2. This reverse process demonstrates how the polarity of the current in the neutral point changes, as a result of the exclusive use of only the positive redundancy of the mid-state.

When the system returns to balanced operation at $t = 0.21\bar{6}$, no compensation actions from the ESS are necessary. Hence, the distribution of the mid-states is conducted equally, which results in zero average current flowing through the midpoint. A remarkable fact from the proposed method is the reduced current stress in the output dc choke, because the ESS power rating is merely 14% of the rated power of the station.

The proper regulation performed at the dc side keeps the voltages perfectly balanced throughout the entire simulation. This situation is confirmed

by Fig. 4.8a, which shows how the voltages of the dc capacitors remain tracking their reference. As in the previous method, the proposed balancing technique allows to overcome the limitations of the conventional NPC.

Given that the balancing technique keeps the dc voltage balance, the currents at the input side exhibit a sinusoidal waveform during any scenario, as shown in the waveform of i_{ga} in Fig. 4.8b. Finally, the unity power factor operation remains unaltered during the load impacts, as the currents are kept in phase with the grid voltage v_{ga} plotted in Fig. 4.8c.

4.5.2 Steady-State Analysis

Following with the validation of the proposed balancing scheme, the steady-state waveforms of the converter voltages are discussed. Figure 4.9 presents these waveforms for the balanced and unbalanced cases.

The behavior of the system for symmetrical operation can be seen in Fig. 4.9a, which displays that no corrections are applied to either of the voltage signals because no difference exists between the dc loads. The generated voltages presents half-wave symmetry which leads to an spectral content that has no even-order harmonics, as shown by the FFT of v_{az}. Then, in the presence of imbalances, a dc drift is injected to the phase voltage with balancing purposes, which results in a positive dc drift due the lack of load in the lower bus, as presented in Fig. 4.9bii. The modification of the switching sequence for the asymmetrical operation can also be observed, as v_{az} exhibits some extra switchings per fundamental cycle.

The presence of the dc injection is confirmed by the spectrum of v_{az} of Fig. 4.9biii. The dc voltage injection has led to a lack of symmetry between the positive and negative half cycles of the converter phase voltages, which is confirmed by the presence of even order components in Fig. 4.9biii.

As in the previous method, the dc bias injected to v_{az} is not reflected toward the line-to-line voltages because the three phases are modified equally. This result is confirmed by Figures 4.9ai and 4.9bi.

To complete the analysis, the input signals for steady-state regimen are presented in Fig. 4.10. The input current i_{ga} exhibits a sinusoidal nature for both balanced and unbalanced cases, with the corresponding increase in its ripple during the unbalanced operation. However, the effectiveness of the modified switching frequency is confirmed, as the currents have maintained

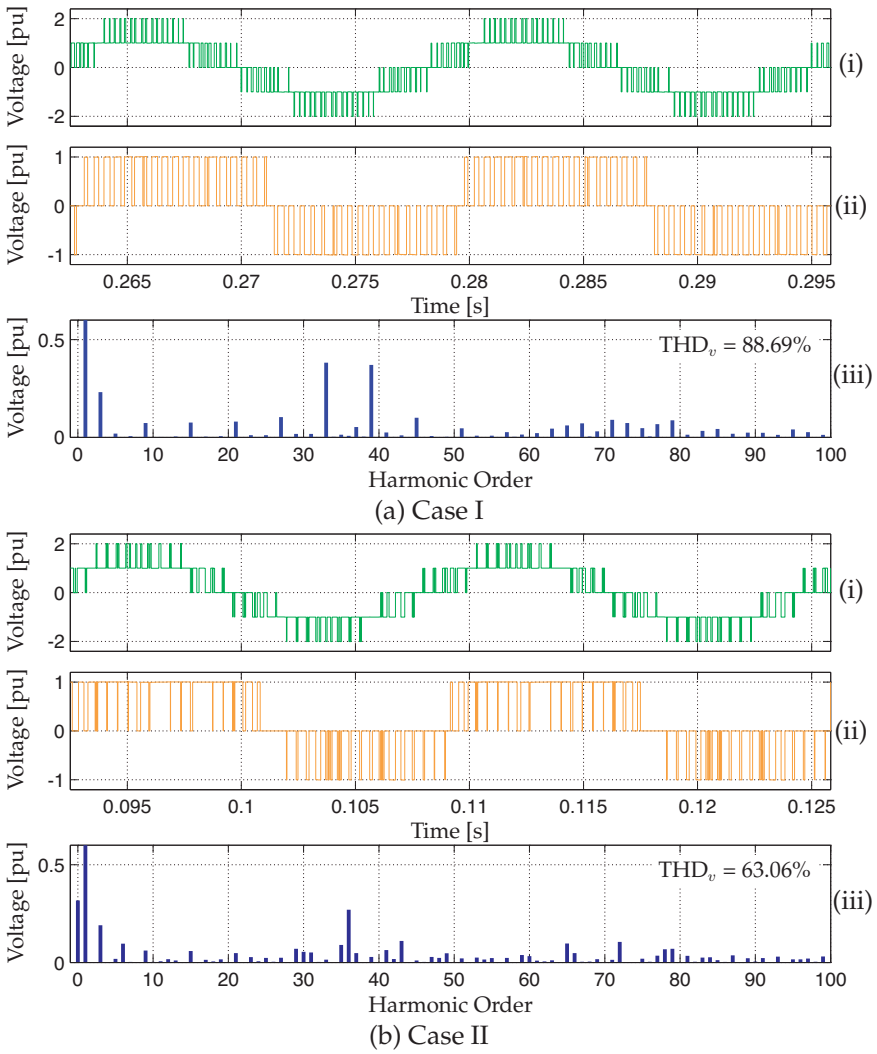


Figure 4.9. Simulated converter voltages of the ESS system. (i) Line-to-line voltage v_{ab}. (ii) Phase voltage v_{az}. (iii) FFT for v_{az}. (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2.

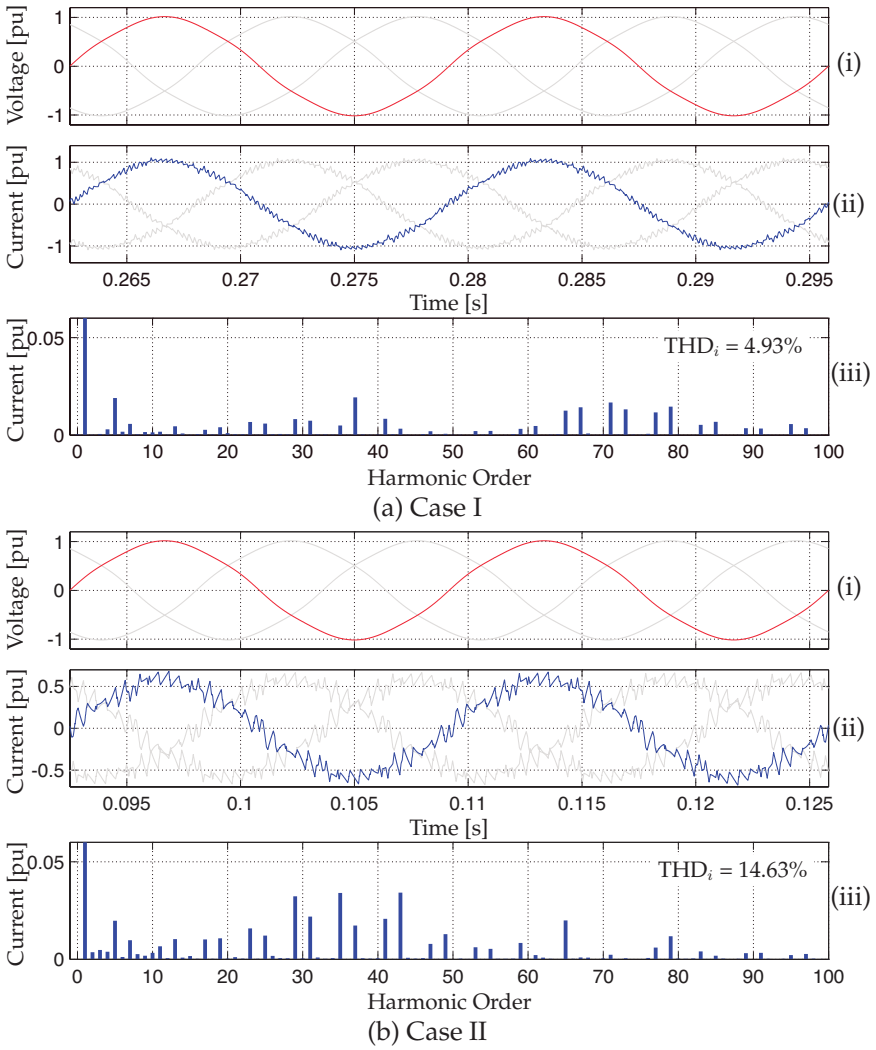


Figure 4.10. Simulated grid signals of the ESS system. (i) Grid voltage v_{ga}. (ii) Grid currenti_{ga}. (iii) FFT for i_{ga}. (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2.

the half-wave symmetry. This result is confirmed by its harmonic content, presented by Fig. 4.10biii, because no energy is concentrated in the even-order components.

4.6 Experimental Validation

The final step to demonstrating the effectiveness of the proposed balancing approach is through experimental verification. In order to do so, the 3 kW NPC prototype exhibited in Fig. 4.11 is employed. This experimental platform is composed of an isolation transformer, an inductive input filter and the central NPC converter (four leg three-phase) in the ac side, while the dc side has an IGBT based three-level dc-dc stage for the ESS interface and the resistive loads for each bus. Both of the loads are connected to the dc bus through a solid state relay to force the asymmetrical operation. The control platform used is an eZdsp (TMS320F28335) from Spectrum Digital, which is performing the main calculations and control actions, along with an Altera Cyclone FPGA (EP1C6T144C8) to manage the peripherals and protections, aside from generating the dead-times for the switching signals. In this case, the SVM algorithm is programmed to have an equivalent switching frequency of 1020 Hz per device. The control scheme is applied to the converter using the parameters presented in Table 4.2. The same dynamic test of the simulations is performed to validate the approach.

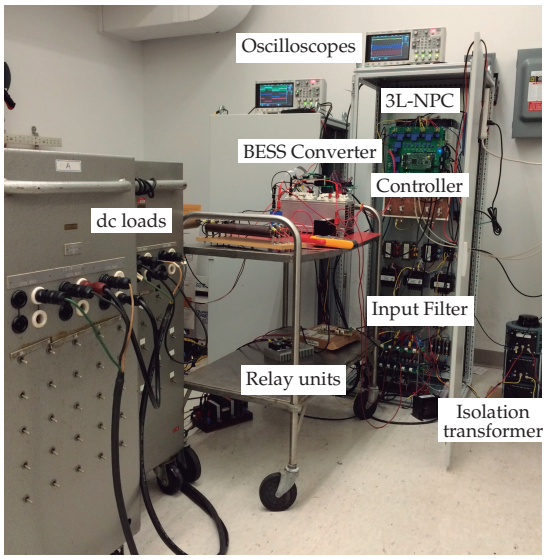


Figure 4.11. Photograph of the experimental setup.

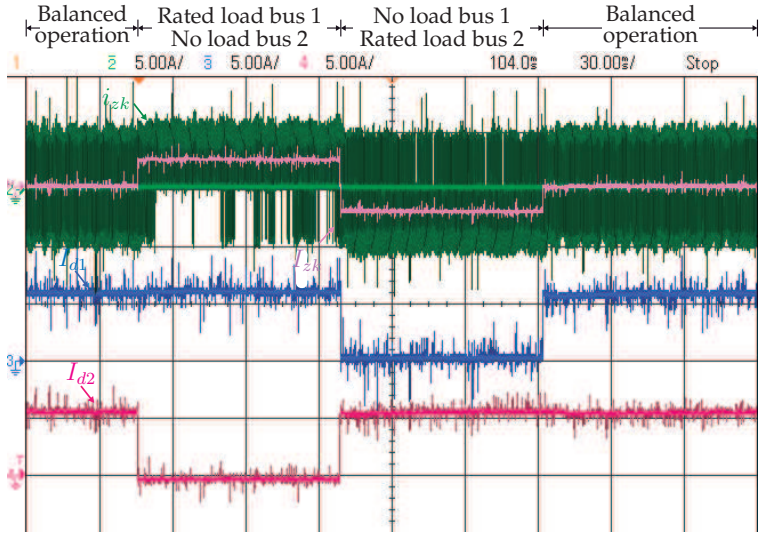
4.6.1 Dynamic Performance

The obtained results are displayed on Fig. 4.12. Once again it is possible to observe a close similarity with the simulation results obtained earlier.

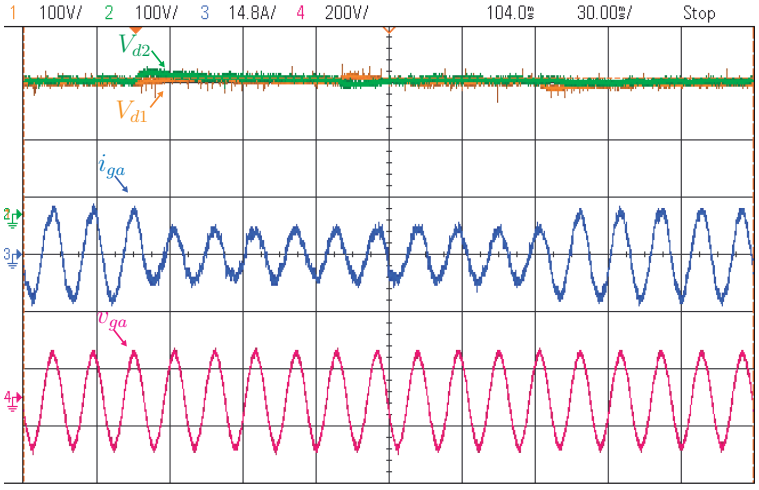
Figure 4.12a displays the behavior of the dc currents during the entire test. It is important to remind that the ESS is performing its charging tasks during the entire scenario. Considering that system starts in balanced operation, no current compensation is required from the ESS. Therefore, its draining power equally derives from both dc buses, as indicated by the average neutral point current I_{zk}, which is zero. Later on, when the lower dc bus is disconnected (*i.e.*, I_{d2} is set to zero), it immediately changes to a positive value to keep the dc voltages from drifting. Consequently, when the imbalance is reversed (*i.e.*, I_{d1} is now zero), it changes its direction in order to reach the minimal load condition. When the system returns to balanced regimen, the current compensation is no longer required and I_{zk} returns to zero.

As a continuation of the analysis, the evolution of the quantities related with the grid-tied regulation is presented in Fig. 4.12b. The figure shows how the severe asymmetrical operation is overcome by forcing the minimal load condition at the dc side. The dc bus voltages present an improved dynamic response by returning rapidly to their reference. This improved response leads to a balanced operation during the entire test. A proper regulation of the input current i_{ga} is achieved, which exhibits a highly sinusoidal waveform, and does not distort excessively. In addition, the current maintains its phase disposition with the grid voltage, hence keeping the unity power factor operation.

Although the ESS interface is able to redistribute its power consumption and provide the complimentary balancing capability, its main function is still charge or discharge the battery. In order to highlight this issue, Fig. 4.13 shows the evolution of the current injected to the battery i_o and the voltage generated by the dc-dc stage v_o. It becomes clear that these outputs remain almost unaltered during the entire dynamic test, with the exception of a slight



(a) dc currents



(b) VOC signals

Figure 4.12. Experimental dynamic performance of the ESS system. (a) DC currents. ChM Neutral point current average value I_{zk} (4 A/div). Ch2 Neutral point current i_{zk} (5 A/div). Ch3 bus 1 load current I_{d1} (5 A/div). Ch4 bus 2 load current I_{d2} (5 A/div). (b) VOC signals. Ch1 dc bus 1 voltage V_{d1} (100 V/div). Ch2 dc bus 2 voltage V_{d2} (100 V/div). Ch3 grid current i_{ga} (14.8 A/div). Ch4 grid voltage v_{ga}(200 V/div). Time scale 30 ms/div.

increase in the current ripple. The reason for this increase is the exclusive use of one of the redundancies of the mid-state, which leads to a reduction of the

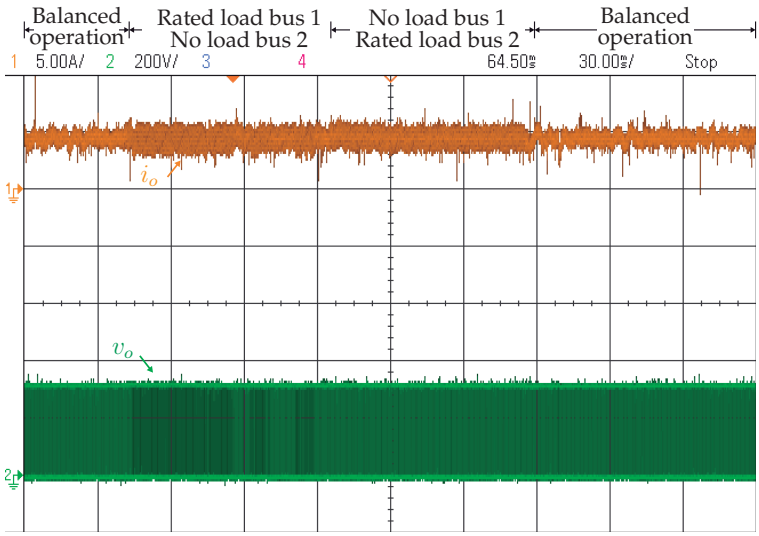


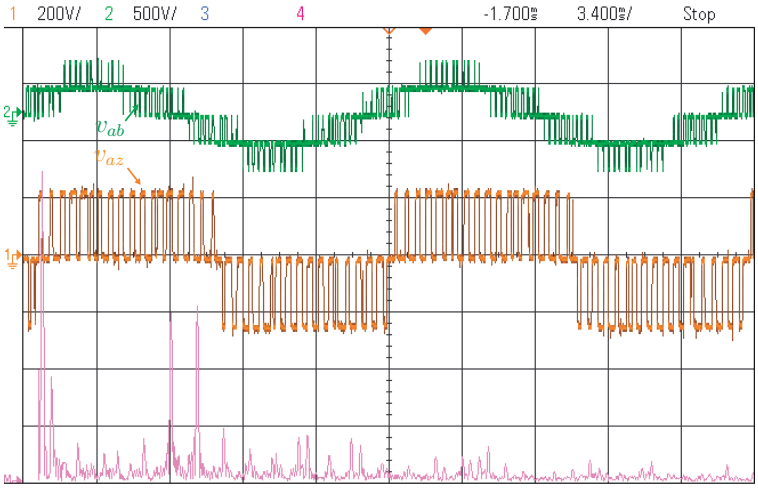
Figure 4.13. Experimental dynamic performance of the ESS system. Ch1 ESS input current i_o (5 A/div). Ch2 ESS input voltage v_o (200 V/div). Time scale 30 ms/div.

apparent switching frequency. This results demonstrate that the operation of the ESS can be integrated with the complimentary balancing required by the grid-tied converter.

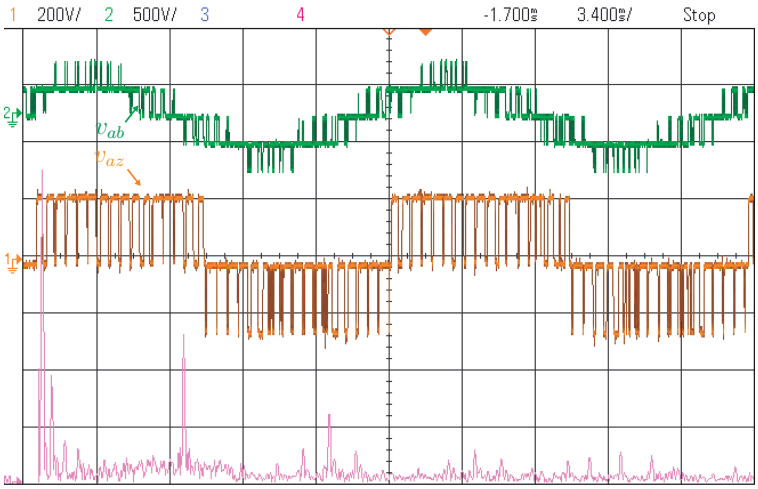
4.6.2 Steady-State Analysis

Finally, the results in steady state are analyzed in order to complete the validation of the balancing approach, which are displayed on Figures 4.14 and 4.15.

As it could be expected, the converter voltages during the symmetrical operation from Fig. 4.14a do not present major differences with those obtained in the earlier chapter because the modification of the switching sequence only takes place during the unbalanced operation. This result is confirmed by the waveforms in Fig.4.14b, in which the effort to maintain the symmetry of the line to line voltages is reflected in the additional switchings in the negative half cycle of v_{az}. The line-to-line voltage v_{ab} retrieves the



(a) Case I

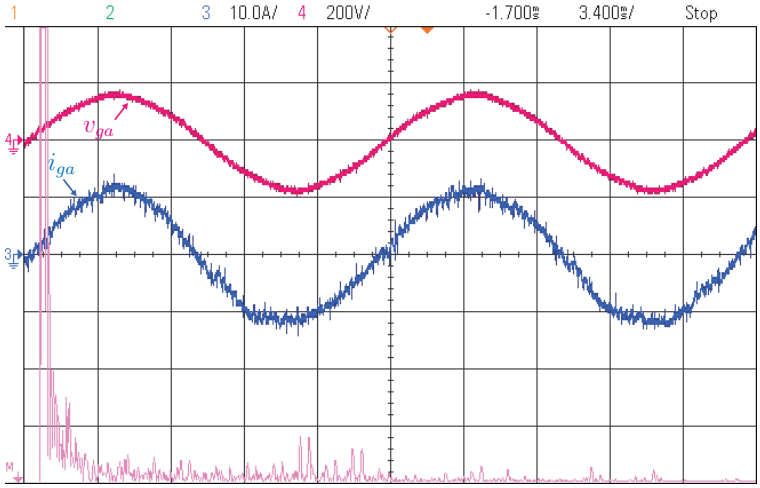


(b) Case II

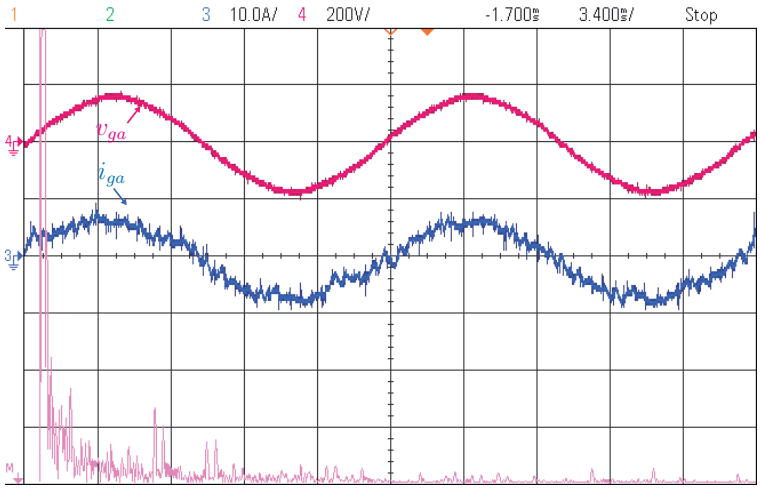
Figure 4.14. Experimental converter voltages with balancing ESS. Ch1 phase voltage v_{az} (200 V/div). Ch2 line-to-line voltage v_{ab} (500 V/div). ChM FFT for v_{az} (20 V/div, Span 10 kHz, Center 4.8 kHz). (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2. Time scale 3.4 ms/div.

half-wave symmetry as expected, leading to an input current with no energy concentrated in the even-order harmonics.

The effectiveness of the modified switching sequence can be observed in Fig. 4.15b. In the presence of asymmetrical dc loads, i_{ga} maintains its si-



(a) Case I



(b) Case II

Figure 4.15. Experimental grid signals with balancing ESS. Ch3 grid current i_{ga} (10 A/div). Ch4 grid voltage v_{ga} (200 V/div). ChM FFT for i_{ga} (100 mA/div, Span 10 kHz, Center 4.8 kHz). (a) Case I, balanced operation. (b) Case II, unbalanced operation in bus 2. Time scale 3.4 ms/div.

nusoidal behavior and retrieves its half-wave symmetry, which can be confirmed by the exclusive presence of odd-order harmonics in its spectrum. Is important to keep in account that the balancing actions performed by the central converter results in a reduction of the apparent switching frequency on the line-to-line voltages, as it can be appreciated in the cases of Fig. 4.14,

which explains the shift of input current dominant harmonics into lower frequencies.

4.7 Summary

A different complimentary balancing approach is developed and successfully validated. This approach utilizes from the optional stages allowed by the distributed dc bus architecture. In this case, the presence of an ESS, interfaced with a three-level dc-dc converter, eliminates of the balancing leg and provides the supplementary balancing capability required. These features reduce the overall cost of the charging architecture because as the requirements for the rectifier stage are reduced, allowing to use off-the-shelf equipment.

It is important to highlight that although the ESS converter is providing the additional balancing ability, its presence in the system is for energy management purposes and not exclusively for the dc voltages balance. It is demonstrated that this additional function does not dramatically alters its operation, which keeps its main function, that is, the charging and discharging of the battery toward the energy management strategy. Given the nature of the three-level dc-dc converter, the minimal load condition does not impose a significant restriction on the battery sizing, which means that the battery ratings are still set by the selected approach to energy management.

As the previous balancing methods, the current method provides a solution that maintains high quality input signals, despite the presence of severe imbalances. In addition, the alternate switching sequence performs the complimentary balancing while keeping the current symmetrical.

CHAPTER V

ENERGY MANAGEMENT STRATEGY

THE SELECTED configuration for the fast charging station features the direct inclusion of several optional stages into the system, such as energy storage units, renewable generators, fuel cell generators, and so on. The connection is made at the dc side; therefore additional synchronization mechanisms, control and sensor sets are not required, neither issues with reactive power are present. Nevertheless, this feature has implications on the management of the available energy because such stages provide an additional degree of freedom that enables the fast charging station to perform secondary services, such as energy arbitrage, standalone operation in case of grid faults, and other grid ancillary services (*e.g.*, load leveling, power pulsation minimization, frequency regulation, etc.), depending on its power ratings.

Accordingly, an energy management strategy is necessary to optimally use the available resources. The main objective of this chapter is to develop a generalized optimization model, which is intended for studying the economic effects of dedicated ESS and locally installed renewable generators on the overall operation costs of the station. This generalized structure provides flexibility in studying the different types of ESSs or DGs available for the station [69], without changing the formulation of the problem. The proposed method also provides an operation schedule for the storage stage in order

to maximize its life-span or to perform additional objectives, such as grid support.

The flexibility and effectiveness of the proposed method are evaluated in different scenarios, and its possible extension to a larger number of fast charging stations is proposed to perform the grid ancillary services.

5.1 Optimal Energy Management Based on Linear Programming

Before formulating the optimization problem, a discussion is required regarding the potential demand of the fast charging station. The number batteries to be fast charged has a direct impact on the sizing of the components of the charging station (*e.g.*, power rating, number of charging units, size of the ESS). Furthermore, it also has an impact on the coordination required from the distribution and transmission system. This information is also necessary for the optimization process, as it influences the operation of the ESS. However, as the fast charging process is still not a widespread practice, there is no data regarding the pattern of the charging or the energy levels involved. Considering this, the load profiles that are generated in this chapter will consider the traffic patterns and conventional drivers behavior as a starting point of the study.

On the other hand, the selected dc bus configuration allows the inclusion of DGs. This increased generation capacity can help alleviate the effect on the grid that these stations are likely to create in the coming years [15]. Considering the location and limited space of these installations, Photovoltaic (PV) energy conversion systems are typically used [15,18], assuming that the majority will be located in the urban areas of the cities. Therefore, the inclusion of the PV potential of the station in the optimization model is relevant to quantify the associated benefits in the design stage. To achieve this, real irradiance data of the city to be studied are considered accordingly in the optimization model. Another important aspect for this optimization is the elec-

tricity cost associated to the operation of the charging station. The electricity price varies depending on the yearly energy consumption of the station and the peak demanded value, as established by the Independent Electricity System Operator (IESO). Thus, an accurate estimation of the demand is needed to correctly estimate the operation costs. After formulating the corresponding demand, generation and price profiles, the design and operation of the fast charging infrastructure can be coordinated [18], allowing the system regulator to properly set the location of the station, selecting the adequate type of ESS or its capacity and power ratings. The optimization method will use these profiles in order to schedule the operation of the ESS, aiming to reduce the electricity costs of the station while extending the life-span of the selected energy buffer.

5.1.1 Demand, Generation and Price Profiles

As established in the previous chapters, the model assumes an EV FCS with dedicated installed charging ports for simultaneously recharging up to n_{ev} vehicles. In case no storage nor generator stages available in the station, all the electricity used for recharging the batteries of the EVs must be purchased from the grid at the corresponding price. However, this may not be beneficial for the customer because the current price may be higher than during other hours, but also represents a negative impact on the utility grid [9]. This negative effect is due the uncontrolled pattern of the charging [12], which is enhanced by the high-power levels. This issue becomes critical, as shown in the following sections; the busiest hours of the station may match the peak electricity consumption hours, so that the electric system cannot fulfill this demand [18].

The motivation behind this strategy is to redistribute of the energy consumed from the grid, with the use of DGs and ESS. This strategy reduces the FCS operation costs and also develops an intelligent system that considers the grid congestion and works toward the benefit of the electric system.

Table 5.1. Time leaving for work, Toronto from [70]

Hour range	Total	Percentage	Hour range	Total	Percentage
5:00-5:59	104,605	4.089%	8:00-8:59	446,515	12.454%
6:00-6:59	298,800	11.680%	9:00-11:59	217,650	8.508%
7:00-7:59	487,290	19.048%	12:00-4:59	204,960	8.012%

*Note: The percentage values are calculated with respect to the total of people commuting to work as a driver.

5.1.2 Traffic Demand Forecast

A model for estimating the EV fast charging demand is required to begin the formulation of the optimization strategy. The availability of such model facilitates the development of a suitable infrastructure and coordinates its integration in the utility system.

Several assumptions have to be considered to obtain the potential demand. First, the pattern for the refueling process of the EVs depends on several factors whose nature is entirely random, such as the initial state of charge of the batteries to be replenished, the beginning and ending of the charging process, battery chemistry and specific energy capacity. The general pattern is also strongly influenced by traffic habits and the electricity rates [12].

Second, if the fast charging process is assumed to complement the conventional overnight charging, then the process occurs most probably during daytime, and more specifically, when the EV drivers are commuting to work. Based on these assumptions, the National Household Survey (NHS) database [70] provides useful information on the time leaving to work, means of transportation used for commuting, the average commuting time, and so on, which can be used to estimate the behavior of the EVs to be recharged.

Following this, an initial estimation of the fast charging demand is then generated. The data related to car commuting in Toronto City, as presented in Table 5.1, are used. The information provided contains only the data cor-

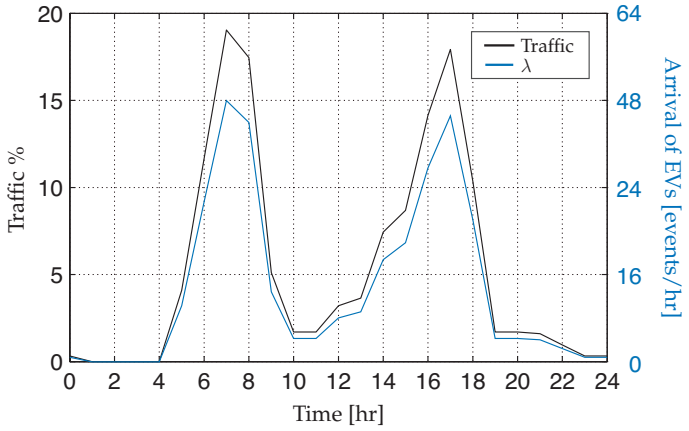


Figure 5.1. Traffic distribution for commuting trips and estimated EV rate of arrival to FCS in Toronto.

responding to commuters using a car, truck or van as a driver, regardless if driven alone or with passengers. The average work day is assumed to be 8 hours in length, in order to extrapolate the time leaving from work. This assumption facilitates a rough estimation of the traffic distribution throughout the day, which leads to the commuting pattern shown in Fig. 5.1. The resulting pattern is similar to the one in the United Kingdom presented in [12]. Please note how the resulting pattern presents two peaks during the day. One is during the morning (between 6:00 to 8:00), and the other during the evening (16:00 - 18:00). This evening peak might require some special attention, as it coincides with the peak consumption hours, as shown in the following sections.

Assuming that the EV driver exhibits similar habits to those of a regular driver, then the busiest hours in terms of traffic may also be the busiest hours of operation for the charging station. This is on the premise that, as it happens with conventional vehicles, the refueling process usually takes place when the car is being used. In other words, as fast charging is assumed as a complimentary method, drivers will stop in the charging station during the commuting. Hence, the number of EVs arriving for recharge to the station is accordingly assumed as a Poisson-distributed random variable with

parameter λ, due the discrete nature of the counting process. Therefore, the probability of having k EVs for recharge their batteries in a given period of time is given by the following probability mass function

$$f(k,\lambda) = \Pr(X = k) = \frac{e^{-\lambda}\lambda^{k}}{k!}, \tag{5.1.1}$$

where X is the poisson distributed variable representing the number of EVs to charge and λ is the mean value of EVs to arrive per hour. However, for this particular application, the rate of arrival of EVs will vary hourly depending on the usage of the vehicles. Hence, λ varies throughout the day according to the traffic pattern presented in Fig. 5.1. Using this approach, the following scenario is considered for the study: the transportation fleet has a heavy penetration of EVs, and the rate of arrival λ will be the one given by the blue line in Fig. 5.1. Note that, under these assumptions, the peak rate of arrival is such that the charging station expects to run at full capacity n_{ev} during its busiest hours.

This initial approach shows that it is possible to forecast the EV load, which is assumed as the expected value of EV arrivals in the corresponding time band. In addition, it is also assumed that the rated energy capacity for all the vehicle models is the same and equal to $E_{\text{ev}} = 24$ kWh (Nissan Leaf, Ford Focus battery pack). Is important to mention that the fast charging process is not intended to give a full recharge process, because this may be difficult for some Li-ion chemistries. For this reason, it is assumed that each car will stop its charging process when 80% of its rated capacity is reached [15]. In addition, it is also expected that the drivers charge their vehicles when the battery SOC drops to 20%. These assumptions lead to the following expression for the EV energy demand,

$$x_{\text{ev}_i} = 0.6E_{\text{ev}}\lambda_i, \tag{5.1.2}$$

where x_{ev} is the energy demanded from the EVs, E_{ev} is the rated capacity of the EV battery pack and λ_i is the rate of arrival of EVs to charge during the time band i. Please note that under this assumptions, the peak in the demand during the evening matches also the peak in the demand of the utility.

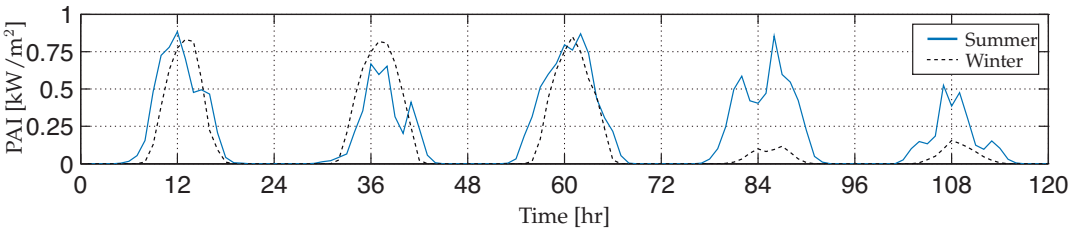


Figure 5.2. Sun irradiance hourly distribution in downtown Toronto.

Therefore, coordination may be required in the upcoming years to avoid any shortages issues in the system.

5.1.3 PV Generation Modeling

To mitigate the impact of integrating the charging station into the utility system, especially during peak consumption hours, the inclusion PV generation into the system is also studied from the economic point of view. Given that the charging station provides an ESS, it enables the shift of cheap electricity during the low-demand hours to high-demand hours (energy arbitrage), installation of PV modules in the station roof, and harvesting energy to further reduce the operating costs.

However, the benefits of having such feature vary from one geographical zone to another, as the sun irradiance, temperature and weather change from one place to another. For this reason, real irradiance measurements are used for a realistic estimation of the PV potential of the station. Another important factor in the irradiance values is its seasonality, as in some places the difference in terms of daylight hours and sun irradiance throughout the year varies considerably. In order to illustrate this, two sets of data are collected in the city of Toronto: one corresponding to five consecutive days in August during summer season and five days in February during winter season. The values of the sun irradiance are presented in Fig. 5.2. These values correspond to the Plane of Array Irradiance (PAI) measured in kilowatts per square meter (kW/m^2).

Table 5.2. Sunpower SPR-E20-327 module data

Parameter	Symbol	Value
Nominal Power	P_{nom}	327 W
Average Efficiency	η_{pv}	20.7%
Rated Voltage	V_{mpp}	54.7 V
Rated Current	I_{mpp}	5.98 A
Open-Circuit Voltage	V_{oc}	64.9 V
Short-Circuit Current	I_{sc}	6.46 A
Area	A_{pv}	1.559x1.064 m^2

Determining which kind of PV modules will be installed in the charging station is also necessary to estimate of the energy that will be generated under such conditions. Considering its high conversion efficiency and the power per square meter, the module used in this study corresponds to Sunpower SPR-E20-327, with a rated power of 327 W and an average conversion efficiency of 20.7%. The full specification of this module is presented in Table 5.2.

Now, it is possible to determine the generated power by each installed module, which is defined as follows

$$P_{\text{pv}_i} = A_{\text{pv}}\eta_{\text{pv}}\text{PAI}_i, \tag{5.1.3}$$

where A_{pv} is the area of each PV panel, η_{pv} is its conversion efficiency and PAI is the measured irradiance in the plane of the PV array.

The overall power generated in the station will depend on the area available for the installation of the PV arrays. Considering that the average area of a mid-sized gas station is about 400 m^2, it is assumed as the area for the charging station as well. Considering this, the number of panels n_{pv} installed in the station is approximated by

$$n_{\text{pv}} \approx \text{floor}(A_t/A_{\text{pv}}). \tag{5.1.4}$$

where A_t is the total area available in the station for the PV modules. An installed capacity of 80,115 W is consequently obtained. In other words, 245

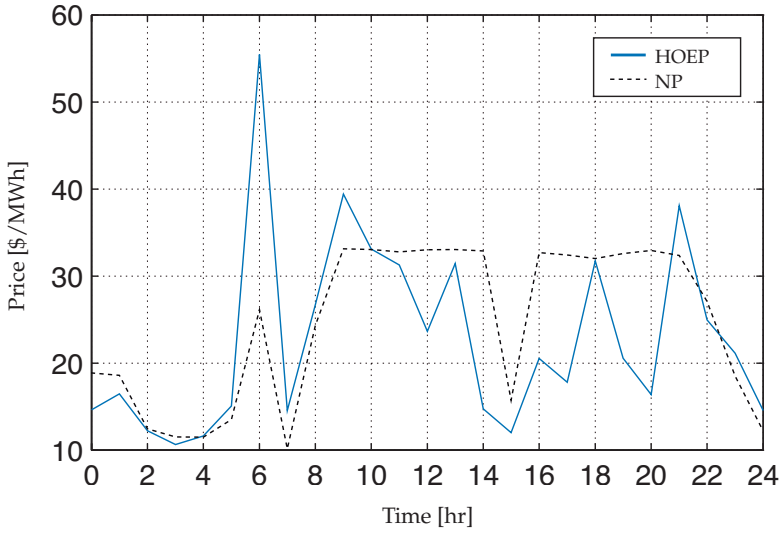


Figure 5.3. Nodal Price and HOEP fluctuations during a weekday in Toronto

PV modules are installed in the station. The average generated energy is then given by

$$x_{\mathrm{pv}_i} = n_{\mathrm{pv}} P_{\mathrm{pv}_i} \Delta t \tag{5.1.5}$$

5.1.4 Energy Price

Based on the assumptions made in the earlier sections and on the proposed power rating of the charging station [20], the projected energy usage will be comparable to the large electricity consumers in the system, in which the yearly consumption is over 250,000 kWh, as set by the IESO. In addition, the peak demand is in the range of 50 kW to 5 MW, which is considered in the category of a Class B customer. For these reasons, the electricity price that applies is the Hourly Ontario Energy Price (HOEP) plus the Global Adjustment (GA) rate. Although this rate applies for the entire province, it is not the only cost to account for. Depending on the point at which the system is connected into the grid, the economical effect of the location differs from node to node. The price to be considered in the optimization model therefore

corresponds to the nodal prices because they promote the efficiency of the system by discouraging the demand in the congested nodes of the transmission system, thereby reflecting the scarcity of transmission capacity at each point of the grid [71]. Is important to note that nodal pricing is currently not effective for customers in Ontario.

Figure 5.3 presents the variations in the HOEP, and the Nodal Prices of the Darlington node (Toronto) in Canadian dollars per megawatt hour ($/MWh) of a typical weekday to illustrate the difference between them. It can be seen that although both prices follow similar trends, the congestion existing in the Darlington node results in higher prices. This result is due to the more expensive transmission at congested points on the utility system. The idea is to incentive a decrease demand in these locations, which in turn alleviates congestion in the short term [71].

5.2 Problem Formulation

The analysis is conducted by discretizing the time in intervals of length Δt, assuming that during each interval the power demanded from the EV chargers is kept constant. Is important to mention that this study only considers the CC mode of the charging process because it is the operating mode for SOC under 80% of the battery capacity. All the vehicles are assumed to be capable to complete their charging processes during the corresponding time interval. To guarantee that, the rated power of the charging ports is selected in such a way that is able to fully recharge the batteries in a time shorter than Δt.

Having defined the forecasting model for the demand, the potential of PV generation in the system, and the cost of the energy purchased it is possible to formulate the optimization problem.

5.2.1 Constraints

The following constraints are required for the operation of the proposed system.

EVs Energy Demand

The main purpose of the charging station is to provide a fast way for EV drivers to replenish their batteries. Therefore, the mandatory and main requirement of the facility is to satisfy the energy demand from EVs at any instant, which leads to the following expression:

$$x_{g_i} + x_{\mathrm{pv}_i} + x^{-}_{\mathrm{ss}_i} - x^{+}_{\mathrm{ss}_i} \geq x_{\mathrm{ev}_i}, \forall i \tag{5.2.1}$$

where x_{ev_i}, x_{g_i}, x_{pv_i} $x^{+}_{\mathrm{ss}_i}$and $x^{-}_{\mathrm{ss}_i}$ stand for the energy demanded by the EV chargers, the energy purchased from the grid, the energy generated by the PV modules, the energy of the discharging and charging cycles of the storage unit during the i-th instant, respectively. Note that the energy used to charge and discharge the storage unit is separated into two different variables to facilitate the preservation of the linearity of the system, especially when measuring the energy throughput of the ESS.

Charging Rates and Energy Storage Level of the ESS

Another critical aspect is the physical limitation that the energy storage unit, more specifically in terms of the energy that can be effectively stored in it and the rate of change at which this energy is charged and discharged. Let SOC_i represent the state of charge of the ESS at the beginning of the i-th instant. Then, depending on the depth of discharge predefined for the ESS, the state of charge must be contained in a specific range, thereby leading to

$$\mathrm{SOC}_{\mathrm{min}} < \mathrm{SOC}_i < \mathrm{SOC}_{\mathrm{max}}, \forall i, \tag{5.2.2}$$

where $\mathrm{SOC}_{\mathrm{min}}$ and $\mathrm{SOC}_{\mathrm{max}}$ stand for the lower and upper boundaries for the state of charge, respectively. Assuming that the storage unit has a certain

efficiency η_{ss} in the charging/discharging process, then the SOC is related with the battery energy as follows [16]

$$\text{SOC}_{i+1} = \text{SOC}_i - \frac{\sigma_{\text{ss}}}{E_{\text{ss}}} + \frac{\eta_{\text{ss}}}{E_{\text{ss}}} x^{+}_{\text{ss}_i} - \frac{x^{-}_{\text{ss}_i}}{\eta_{\text{ss}} E_{\text{ss}}}, \forall i, \tag{5.2.3}$$

where σ_{ss} represents the self-discharge loss and E_{ss} is the specific energy of the ESS.

On the other hand, considering that the storage device has the same rating for the discharging and charging powers given by P_{ss}, then the energy that can be effectively transferred to/from it is limited in each time band to

$$\left| \eta_{\text{ss}} x^{+}_{\text{ss}_i} - \frac{x^{-}_{\text{ss}_i}}{\eta_{\text{ss}}} \right| \leq P_{\text{ss}} \Delta t, \forall i. \tag{5.2.4}$$

Grid-tied Converter Power Rating

Another constraint that restricts power is related with the rating of the grid-tied converter P_g to guarantee that the optimal solution is within the safe operating zone. The energy that can be consumed from the grid in each time band is accordingly limited by

$$x_{g_i} \leq P_g \Delta t, \forall i. \tag{5.2.5}$$

5.2.2 Objective Function

The final step in the optimization formulation is the selection of the cost function. The idea of this proposal is to study the impact of the station with an ESS and the inclusion of on-site PV generators on the operation cost. Therefore, one of the terms in the objective function is related with the cost of the energy involved in the charging of the EV batteries. The usage of the ESS must also be considered, in order to estimate the costs of its usage, to protect it, and to extend its life-span. Accordingly, the following objective function is chosen:

$$\min \sum_{i=1}^{N} c_{g_i} x_{g_i} + \frac{\text{LCOE}_{\text{ss}} E_{\text{ss}}}{\text{LET}(\alpha_d)} \sum_{i=1}^{N} (x^{+}_{\text{ss}_i} + x^{-}_{\text{ss}_i}) \tag{5.2.6}$$

where c_{g_i} represent the price per megawatt hour of the purchased energy from the grid during the i-th time band in \$/MWh, and corresponds to the Darlington nodal price plus GA, as established in the earlier sections. LCOE_{ss} is the levelized cost of energy in \$/MWh of the ESS, and LET is the ESS lifetime energy throughput, which is a function of the depth of discharge α_d. According to the previous formulation, the decision variables of the model will be the energy purchased from the grid x_{g_i} and the energy for charging and discharging the storage unit $x^+_{\text{ss}_i}$ and $x^-_{\text{ss}_i}$.

After selecting of the objective function, the constraints are rearranged to the canonical way, *i.e.*, with the decision variables on the left hand side of the equations. Given that the decision variables are the energy consumed from the grid and the charging and discharging energies of the ESS. In addition to the previously discussed constraints, the non-negativity of the decision variables is included to the model, thereby leading to

$$-x_{g_i} - x^-_{\text{ss}_i} + x^+_{\text{ss}_i} \leq -x_{\text{ev}_i}(\mu_{\text{ev}}, \sigma_{\text{ev}}) + x_{\text{pv}_i}(\mu_{\text{pv}}, \sigma_{\text{pv}}) \tag{5.2.7}$$

$$\sum_{j=1}^{i} \eta_{\text{ss}} x^+_{\text{ss}_j} - \frac{x^-_{\text{ss}_j}}{\eta_{\text{ss}}} \leq E_{\text{ss}}(\text{SOC}_{\text{max}} - \text{SOC}_1) + i\sigma_{\text{ss}} \tag{5.2.8}$$

$$\sum_{j=1}^{i} \frac{x^-_{\text{ss}_j}}{\eta_{\text{ss}}} - \eta_{\text{ss}} x^+_{\text{ss}_j} \leq E_{\text{ss}}(\text{SOC}_1 - \text{SOC}_{\text{min}}) - i\sigma_{\text{ss}} \tag{5.2.9}$$

$$\eta_{\text{ss}} x^+_{\text{ss}_i} - \frac{x^-_{\text{ss}_i}}{\eta_{\text{ss}}} \leq P_{\text{ss}} \Delta t \tag{5.2.10}$$

$$\frac{x^-_{\text{ss}_i}}{\eta_{\text{ss}}} - \eta_{\text{ss}} x^+_{\text{ss}_i} \leq P_{\text{ss}} \Delta t \tag{5.2.11}$$

$$x_{g_i} \leq P_g \Delta t \tag{5.2.12}$$

$$x_{g_i}, x^+_{\text{ss}_i}, x^-_{\text{ss}_i} \geq 0, \forall i, \tag{5.2.13}$$

where μ_{ev} and σ_{ev} correspond to the mean and standard deviation of the EV demand forecast error, respectively; μ_{pv} and σ_{pv} are the mean and standard deviation of the forecasted PV generation and SOC_1 is the initial state of charge of the ESS. It can be seen that the formulated model is linear with respect of the variable decisions. Hence, linear programming can be used

to find the optimal point if the problem is bounded. The model is also formulated such that it can include any additional stage in the charging station (*e.g.*, micro wind generation, fuel cell, etch) simply by modifying the right hand side of the constraints. Their effect can also be studied with the use of the corresponding shadow prices vector without the need to solve the entire problem again.

5.3 Optimization Results

Considering the formulated model, the following scenario is studied: assuming that the time is discretized in time-band of 15 min each, a typical business

Table 5.3. Simulation parameters for EMS

Paramenter	Symbol	Value
Grid-Tied Converter Rated Power	P_g	1.2 MW
Fast Charging Port Rated Power	P_{ev}	100 kW
Number of Charging Ports	n_{ev}	12
EV Battery Rated Capacity	E_{ev}	24 kWh
ESS Rated Capacity	E_{ss}	500 kWh
ESS Rated Power	P_{ss}	300 kW
ESS charging/discharging Efficiency	η_{ss}	0.95
ESS Maximum State of Charge	SOC_{max}	100%
ESS Minimum State of Charge	SOC_{min}	20%
ESS Depth of Discharge	α_d	80%
Time Band Length	Δt	0.25 hr
PV Module Rated Power	P_{pv}	327 W
PV Modules Installed	n_{pv}	245
PV Module Conversion Efficiency	η_{pv}	0.207
Li-ion Battery Self Discharge Loss	δ_{ss}	0.001% per day
Li-ion Battery Levelized Cost of Energy	LCOE_{ss}	350 $/MWh [69]
Li-ion Lifetime Energy Throughput	LET	2400 MWh

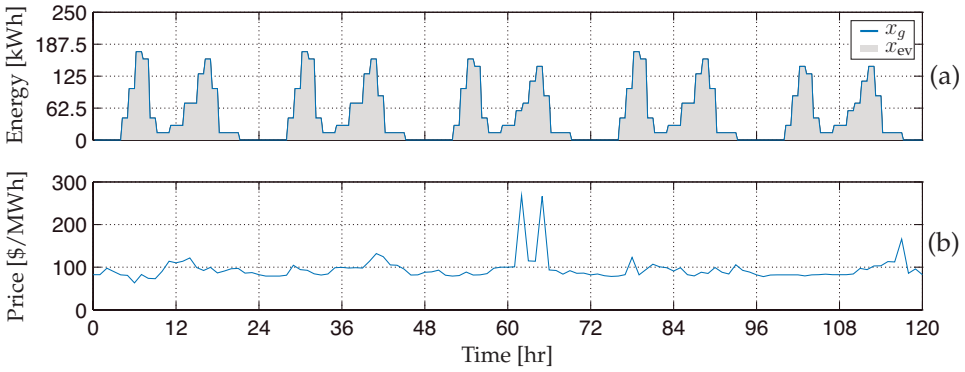


Figure 5.4. Simulated Case I, no ESS: (a) EV energy demand x_{ev} and grid energy consumption x_g. (b) Darlington Nodal Prices August 4th-8th 2014.

week window is analyzed (Monday to Friday). The following assumptions also hold: the behavior of the EV demand is as expected, and the sun irradiance is similar to the measured data. In each case, three scenarios are studied. The first scenario only considers the presence of the fast charging units in the system (Case I). The second scenario adds the presence of only the ESS (Case II). The third scenario studies the presence of both ESS and PV in the charging station (Case III). The system parameters are presented in Table 5.3. The obtained results were obtained considering a Lithium Ion Battery as the ESS. The optimization results are generated using MATLAB ®, with the *linprog* Optimization Toolbox.

Before analyzing the different scenarios, Fig. 5.4 presents the results from the base case with neither PV generators nor ESS installed in the system. The grid energy consumption follows exactly the shape of the EV demand, as it can be seen in Fig. 5.4a. In addition, Fig. 5.4b presents the variations for the Darlington nodal prices between August 4th to 8th during 2014, which will be used as the coefficients c_{g_i} in (5.2.6).

The results for case II, in which only the ESS is considered, are given in Fig. 5.5. It can be seen that the addition of the ESS allows to perform the energy arbitrage towards the minimization of the total electricity cost required to recharge the EV batteries. The optimal operation of the ESS leads to a dif-

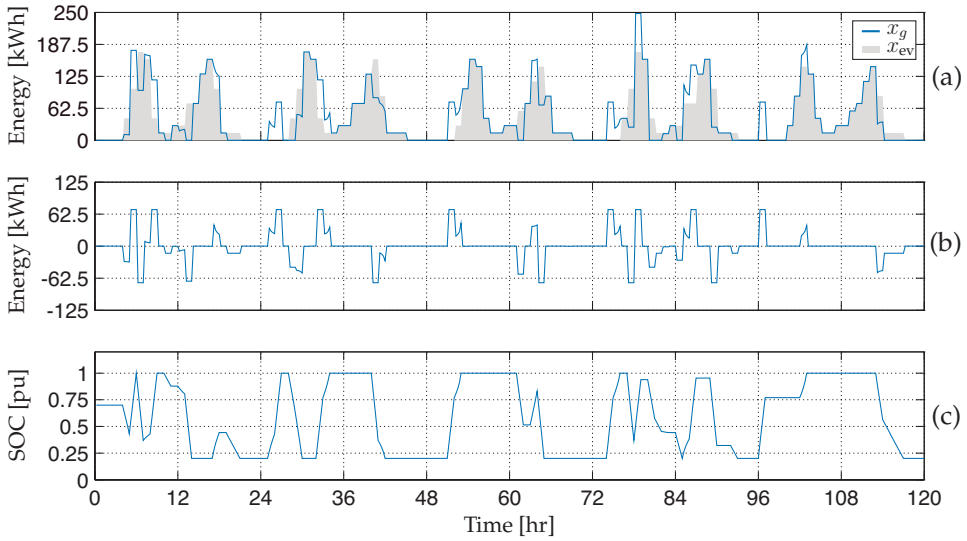


Figure 5.5. Simulated Case II, Li-ion ESS: (a) EV energy demand x_{ev} and grid energy consumption x_g. (b) ESS Energy x_{ss}. (c) ESS State of Charge.

ference between the grid consumption and the EV demand, which is dictated by the variation of the prices throughout the week. This result is confirmed in Figures 5.5a and 5.5b. The results from Fig. 5.5 confirm that the formulated problem is bounded because the optimization tool returns an optimal point, while none of the restrictions is voided.

Given that the secondary objective in the optimization scheme is to avoid a large number of charging/discharging cycles in the ESS, it can be seen in Fig. 5.5d, the average utilization of the energy storage system is controlled to be approximately 1.8 cycles per day. The presence of the ESS in the system reduces the operation costs of the charging station in 7.81%. The reduction of the operation costs directly affects the revenue of the charging station, as the same energy demand is covered.

To estimate the improvement on the profits consider that the price for fast charge is a flat rate 0.12 \$/kWh (*i.e.*, assuming that a larger penetration of EVs in the transportation fleet will reduce the price, current price in British Columbia is 0.35 \$/kWh [72]). Considering that the total amount paid by

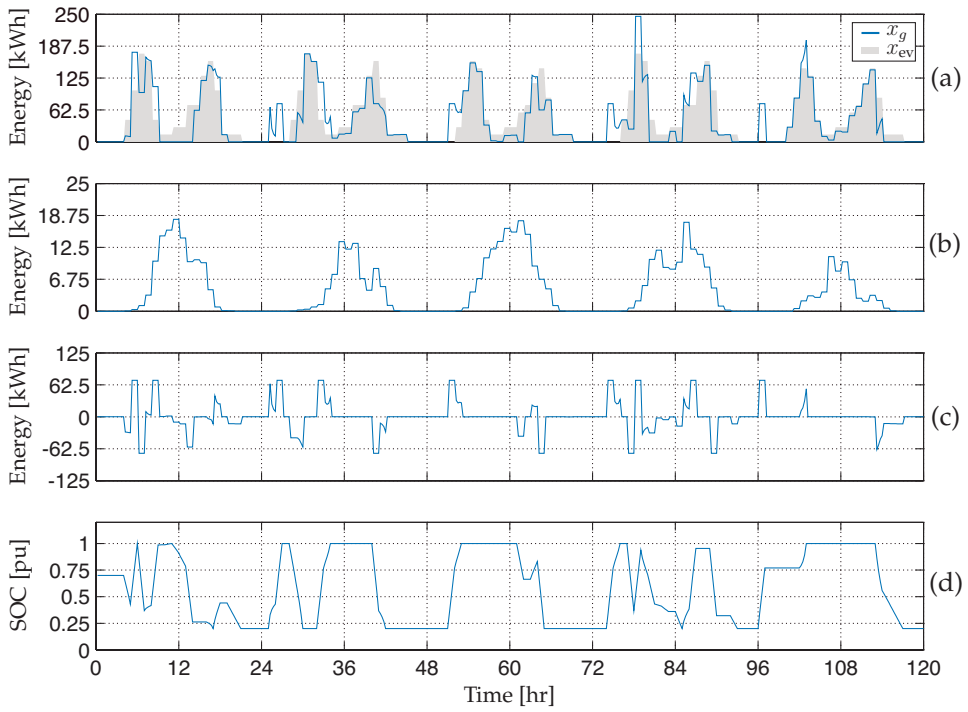


Figure 5.6. Simulated Case III, Li-ion ESS and PV Arrays: a) EV energy demand x_{ev} and grid energy consumption x_g. (b) PV Generated Energy x_{pv} (c) ESS Energy x_{ss}. (d) ESS State of Charge.

the customers is kept constant, the presence of the ESS in the system allows to improve the profit in 38.72%. Is important to mention that this is only to quantify the improvement on the daily profits of the charging station, without considering any installation or maintenance costs.

Following the analysis, the study the behavior of the system under the same demand scenario but using a combination of ESS and locally installed PV arrays that are sized according to the average area of a regular gas station. The ESS rated values are the same as those used in the previous case. The results are presented in Fig. 5.6. Despite the is a similar trend in the response of the variables, the inclusion of the PV generation allows to further decrease the energy requirements from the grid, thereby obtaining a reduction up to 16.47% in terms of the electricity costs. However, this result may

be misleading because only the data corresponding to the summer season are considered. This profit must be averaged with the results corresponding to the rest of the year, as the sun irradiance varies dramatically in certain places, especially in Toronto City. Repeating the analysis for the rest of the seasons (*i.e.*, corresponding prices and irradiance data are considered for each season) the average cost reduction of this configuration is 14.37%. In this case, a significant cost reduction improves profits at an average of 71.24%. Under this configuration, additional constraints can be included in the model, in order to evaluate wether is better to sell the PV generated energy back to the grid or use it locally to reduce the overall grid consumption. However, considering the available area for installing PV modules, the power generation capability of the station is much smaller than the expected demand, hence the reverse power flow operation is unlikely to happen. Additionally, even if there is a small surplus of power available during off peak periods, most of this power will be wasted in the form of energy conversion losses. Under this conditions, it is more economical to use this energy locally instead of selling to the grid.

An interesting result is that under this optimization scheme, given that the objective function uses the nodal prices to perform the minimization, the reduction in the overall operation costs benefits both the energy user (*i.e.*, the owner of the charging station or the EV driver) and the grid. This is explained as follows, the scheme reduces the electricity cost by prioritizing the purchases during the instants when the price is lower and discouraging them when the price is higher. However, the prices indirectly reflects the current status of the grid. A low price means that the system is more likely to provide energy, whereas a high price restricts the consumption during peak hours. If this scheme is extended through all the charging stations throughout the system, the fast charging infrastructure could be used as a support to the grid, performing tasks to regulate the frequency, reactive power compensation, peak power shaving, among others.

Table 5.4. Energy management strategy daily results for Toronto

Case	Total Cost $	Savings	Revenue	Daily Demand
Case I	450.07	-	-	4.516 MWh
Case II	415.74	7.81%	38.72%	4.541 MWh
Case III*	376.78	16.47%	81.65%	4.147 MWh

*Case III is only considering data corresponding to summer season.
Note: The prices are in Canadian Dollars.

5.4 Sensitivity Analysis

5.4.1 Uncertainty in the Forecasted Demand

One premise of the proposed energy management strategy is that the EV demand can be forecasted to schedule the operation of the ESS based on it. A relevant study then is how the profit is affected when the real demand takes different values compared to the mean forecasted demand. Assuming that the forecasted error is normally distributed, the uncertainty is represented using different values of its standard deviation σ_{ev}. In this analysis, five scenarios are considered, corresponding to percentage dispersions from the mean of 7.5%, 15%, 22.5%, 30% and 37.5%. Figure 5.7 illustrates how the profit of each case is affected when the error in the forecast has larger values of σ_{ev}. In the three studied cases, the profit shows a slight decreasing trend as the uncertainty in the forecast model increases. Despite of this trend, the obtained results confirm the robustness of the proposed model to the uncertainty in the EV demand model.

5.4.2 Sensitivity to the Market Price Bandwidth

The proposed method is based on the reduction of the operational costs by shifting the energy consumption from high to low priced periods. Thus, it is interesting to analyze the behavior under different bandwidths between the highest and the lowest price of the analyzed period. To do so, the revenues

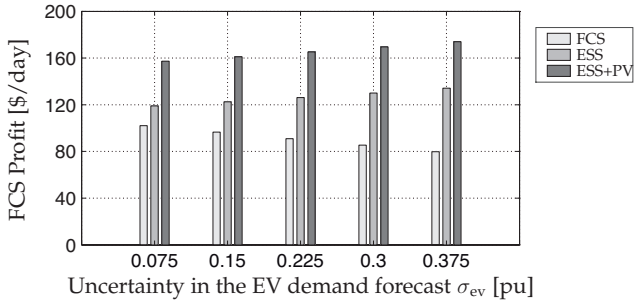


Figure 5.7. Revenue of the FCS for the studied cases for different EV charging demand forecast uncertainties.

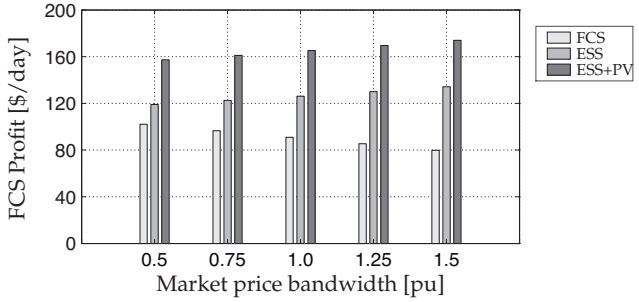


Figure 5.8. Daily revenue of the FCS for the studied cases for different bandwidths in the market price

for the three analyzed cases are studied in four sensitivity cases with different bandwidths for the electricity prices shown in Fig. 5.4b: 50%, 75%, 125% and 150% of the original price. It is important to mention that only the variation of the prices is modified, while maintaining the average price and its pattern.

From the obtained results presented in Fig. 5.8, it is possible to identify how the price bandwidth affects the FCS revenue. If the station does not includes an ESS, a slight decrease of the profits is observed for prices with large variations. However, in the presence of an energy buffer, the revenue is increased for larger bandwidths, as the effect of shifting the consumption to lower priced periods is enhanced.

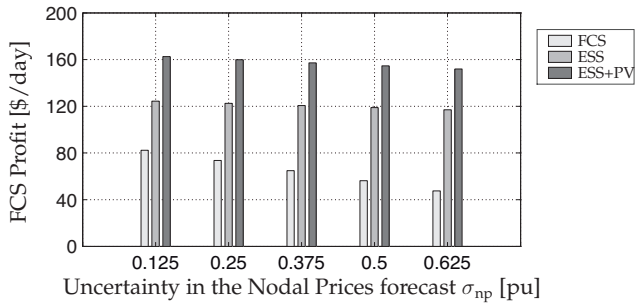


Figure 5.9. Daily revenue of the FCS for the studied cases under different nodal prices forecast uncertainties σ_{np}.

5.4.3 Uncertainty in the Nodal Prices

To complete the sensitivity analysis, the effectiveness of the proposed method is tested under the uncertainty of the representative nodal price. Is important to mention, that as occurs with the HOEP, the nodal price is known only after the corresponding period has passed, therefore the real values are not known and have to be forecasted. This study then uses five different measures of the nodal price forecast error, assuming that this error is normally distributed. The chosen values for the standard deviation σ_{np} are 12.5%, 25%, 37.5%, 50% and 62.5%, which are applied to the prices shown in Fig. 5.4b.

From the results in Fig. 5.9 it can be seen that the revenue under the proposed strategy exhibits a considerable sensitivity to the forecast error in the electricity prices. This sensitivity is explained as the optimization function considers the prices to redistribute the electricity throughout the scheduled period, in this case the week. Therefore, as the error in the forecast increases, the scheme shifts the energy consumptions to inconvenient periods. This results reflect that the forecasting of the nodal prices becomes a critical issue in the performance of the method.

5.5 Summary

A generalized linear programming optimization model is formulated for the optimal energy management of the optional ESS in a EV fast charging station. The proposed model offers flexibility in terms of the nature and type of storage and generators used, thereby making it suitable to study the effect of having different energy storage technologies connected to the system. The validation studies are carried out using a Li-ion battery as the ESS.

Although the estimation for the EV demand is rather simple because only a few factors are considered in forecasting it, the approach offers the possibility to include more sophisticated forecast methods to improve the estimation, including the probabilistic distribution of the initial state of charge, beginning of the charging time, and differences in the battery capacities. A more realistic EV demand forecast gives a better understanding regarding the real effects of EV fast charging into the utility system and therefore enables the coordination of measures that will alleviate or reduce this effects.

Using the proposed approach, the operation of the ESS is scheduled based on the forecasted quantities involved in the station to reduce the electricity costs and improve the daily revenues. The results show that, without considering the initial investment cost for this stage, the strategy always generates savings in terms of the energy purchased from the grid, thereby improving the profits. Furthermore, the inclusion of distributed generators enhances the effectiveness of the proposed scheme. Depending on the location of the fast charging station, different generation methods can also be considered. For example, highway-located stations may also include wind energy generators.

The proposed approach presents robustness toward the uncertainty of the estimated EV demand and is rather sensitive regarding the forecasted nodal prices. Thus, special attention must be given to the forecasting method chosen for the prices. Finally, the method shows and improved performance under prices that undergo larger variations because of the increased effect of

the energy arbitrage in the overall electricity cost.

CHAPTER VI

CONCLUSIONS

OVER THE last decade, significant attention and effort have been given to the EV technology. With the constantly increasing EV fleet, several challenges have arisen to prompt the current electric system to adapt to the requirements of this growing application. Assuming a large-scale adoption of EVs and PHEVs in the coming years, the development of a fast charging network infrastructure will be required. Therefore, considering the power ratings of these fast charging stations, multilevel-converter-based equipment emerges as the most suitable power converter technology. Modifications and newer coordination methods for the utility are also needed in order to absorb the EV charging load, and does not merely requires having sufficient generation capacity. The stochastic behavior of the EV load needs to be addressed properly for the actual electric system to satisfy this growing demand.

The main objective of this dissertation is the development a fast charging architecture based on the bipolar dc-bus concept. The idea is to provide a solution that enables the widespread of the fast charging process without affecting negatively the the utility grid.

6.1 Main Contributions and Conclusions

The main contributions of this work are as follows:

1. A bipolar common dc-bus architecture is developed for the grid integration of the charging ports. The use of a split dc-bus reduces the step-down effort of the fast charging units without sacrificing the MV capability of the system. The concept is based on the 3L-NPC converter. Therefore, its performance under asymmetrical loads is crucial because the intended application has a stochastic behavior, and the loads in the system are only temporarily. In order to guarantee the proper operation of the station regardless the load profile, the minimal load conditions are forced through additional circuits.

2. A formal definition of the unbalanced operation is given and two balancing methods are proposed to overcome this limitation. The results allow to understand that the inability of the 3L-NPC to handle any dc load asymmetries is related to its limited neutral point current handling capabilities. Considering this fundamental limitation, different balancing schemes are developed: emulating the minimal load condition at the dc side and simply avoiding the circulation of any current through this point.

   Both balancing techniques are proven to be effective. The system can keep its voltages from drifting during the worst-case scenario, when the rated-load condition is forced in one of the buses while the other remains idle.

3. Considering the possibility of including additional stages in the system, a third balancing mechanism is developed. Unlike the EVs to charge, these stages are stationary loads in the system. Therefore, they can be designed in such a way that they can force the minimal load condition in any of the buses. The proposed balancing technique uses a battery ESS with a three-level dc-dc converter as the interface. Moreover, it

does not alter the main function of the battery, which is to move the energy through time according to the energy management strategy of the charging station.

The power ratings requirements related to complimentary balancing are also rather low and do not result in excessive conditions in the sizing of the ESS.

4. A scaled-down fast charging station is designed and constructed to validate the architecture and the different balancing approaches. The prototype is based on four NPC leg modules and a laminated dc bus bar for the grid-tied converter. The ESS stage consists of two 2L-VSC modules, which can be used to study the performance interleaved three-level topology for further research. The system is regulated with a single control platform, which is based on the eZdsp (TMS320F28335) along with an Altera Cyclone FPGA (EP1C6T144C8).

5. A generalized linear programming optimization model is formulated for the optimal energy management of the optional storage stage the fast charging station. The proposed model offers flexibility in terms of the nature and type of storage and generators used, thereby making it suitable to study the impact of having different energy storage technologies connected to the system. The approach offers the possibility to include more sophisticated forecast methods to obtain a better estimation, including the probabilistic distribution of the initial state of charge, beginning of the charging time, differences in the battery capacities and chemistries.

   Using the proposed approach, the operation of the ESS is scheduled based on the forecasted quantities involved in the station, aiming to reduce the electricity costs and improve daily revenues. The results show that, without considering the initial investment cost for this stage, the strategy can generate savings in terms of the energy purchased from the grid, thereby improving the profits. Furthermore, the inclusion of DGs enhances the effectiveness of the proposed scheme. Depending on

the location of the FCS different generation methods can also be considered.

6.2 Suggested Future Work

1. The system performance should be evaluated using different modulations and control schemes. Non-linear control schemes such as direct power control or model predictive control, can offer enhanced performance. Nevertheless, a fixed switching pattern is required in order to meet the grid code requirements. Comparisons can also be conducted on switching frequency and semiconductor losses, aiming to determine the most suitable modulation strategy for fast charging applications.

2. The efficiency, reliability and availability differences between the ac bus concept and the proposed one should be demonstrated and evaluated.

3. The inclusion of second-order filters at the input side is relevant to further improve the performance of the charging station, especially considering the altered spectrum distribution using the balancing capabilities of the NPC. Suitable damping strategies must be considered to avoid any resonance issues.

4. Regarding the energy management strategy and the possibility of performing ancillary services to the utility, a cooperative generalization of the proposed strategy can be conducted. The overall power can augmented using several charging stations in a coordinated way. This coordination has a significant influence on the electric system, which leads to the possibility of performing power peak shaving, frequency regulation and reactive power compensation to name a few.

APPENDIX I

PER-UNIT SYSTEM CALCULATIONS

THE PRESENT thesis uses the per-unit system to present simulation and experimental results. The base values used for the calculations in the per-unit system are provided in Table A.1.

Table A.1. Definitions of base values for the per-unit system

Base Apparent Power	$S_{\mathrm{B}} = S_{\mathrm{R}}$ VA	S_{R} – Rated apparent power of the power converter.
Base Active Power	$P_{\mathrm{B}} = P_{\mathrm{R}}$ W	P_{R} – Rated active power of the power converter.
Base Voltage	$V_{\mathrm{B}} = V_g$ V	V_g – Grid rated voltage.
Base Frequency	$\omega_{\mathrm{B}} = 2\pi f_g$ rad/s	f_g – Grid rated frequency.
Base Current	$I_{\mathrm{B}} = \dfrac{P_{\mathrm{B}}}{3V_{\mathrm{B}}}$ A	I_g Rated current of the power converter.
Base Impedance	$Z_{\mathrm{B}} = \dfrac{V_{\mathrm{B}}}{I_{\mathrm{B}}}\,\Omega$	
Base Inductance	$L_{\mathrm{B}} = \dfrac{Z_{\mathrm{B}}}{\omega_{\mathrm{B}}}$ H	
Base Capacitance	$C_{\mathrm{B}} = \dfrac{1}{\omega_{\mathrm{B}} Z_{\mathrm{B}}}$ F	

APPENDIX II

INPUT CURRENT AMPLITUDE VARIATION IN UNBALANCED SCENARIOS

IN ORDER to determine the amplitude of the fundamental current in any load scenario, a power balance of the system is established:

$$\frac{3}{2}\text{Re}\left\{\mathbf{v}_g\mathbf{i}_g^*\right\} = \frac{3}{2}R_g\text{Re}\left\{\mathbf{i}_g\mathbf{i}_g^*\right\} + P_d, \tag{B.1.1}$$

assuming unity power factor operation, (B.1.1) can be rewritten in terms of the amplitudes of the ac signals V_g and I_g as

$$\frac{3}{2}V_gI_g = \frac{3}{2}R_gI_g^2 + \frac{V_d}{2}I_{d1}(1+\epsilon), \tag{B.1.2}$$

please note that the load on the upper bus is the rated value. On the other hand, V_d and I_{d1} can be written in terms of the input side quantities:

$$V_d = \frac{\sqrt{3}V_g}{m_a}\sqrt{(1-r_g)^2+l_g^2} \tag{B.1.3}$$

$$I_{d1} = \frac{\sqrt{3}}{2}m_aI_{g_{\text{Nom}}}\cos\delta, \tag{B.1.4}$$

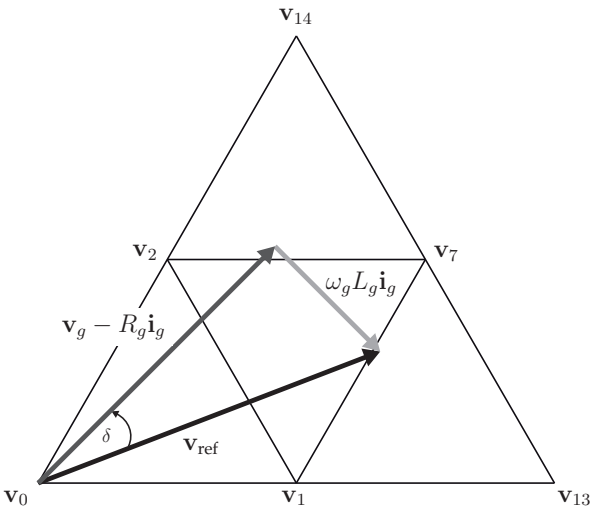


Figure B.1. Vector diagram of the system.

where r_g and l_g correspond to the per unit values of the input filter resistance and inductance, respectively. From the vector diagram shown in Fig. B.1, it can be stated that $\cos\delta$ is given by

$$\cos\delta \;=\; \frac{1 - r_g}{\sqrt{(1 - r_g)^2 + l_g^2}}. \tag{B.1.5}$$

Replacing (B.1.3), (B.1.4) and (B.1.5) and using the per unit value of the input filter resistance leads to

$$\frac{3}{2} V_g I_g \;=\; \frac{3}{2} r_g V_g I_g + \frac{3}{2} V_g I_{g_{\text{Nom}}} (1 - r_g)(1 + \epsilon). \tag{B.1.6}$$

Finally, clearing I_g leads to

$$I_g \;=\; \frac{I_{g_{\text{Nom}}}}{2}(1 + \epsilon). \tag{B.1.7}$$

This result can be generalized, and it models the input current amplitude between the balanced and unbalanced operation for a given fixed load at one

of the buses. Considering that δ varies slightly for different load conditions, the influence of these variations on the unbalanced current is neglected leading to

$$I_{g_{\text{un}}} \approx \frac{I_{g_{\text{bal}}}}{2}(1+\epsilon). \tag{B.1.8}$$

Remark B1

The previous analysis is conducted considering that SVM is used, thereby explaining the changes in the equations presented in [43]; however, the same final results are obtained for carrier-based PWM.

APPENDIX III

AVERAGE USAGE TIME OF THE SMALL VECTORS IN 3L-SVM

THE FOLLOWING approximation is established to estimate how much dc drift can be injected under the SVM scheme. Considering that the balance of the neutral point voltage in this scheme is related with the usage of the positive and negative small vectors and how its dwell times are distributed, the idea behind this work is to calculate an average value of the remaining time available for this vectors. In other words, under nominal conditions, these vectors are used each switching period half of the corresponding calculated dwell time for the small vector t_a. Therefore, $t_{a\mathrm{P}} = t_{a\mathrm{N}} = 0.5t_a$. Considering this idea, under a certain midpoint voltage drift, the maximum correction that the modulation scheme can perform is to use all the dwell time t_a exclusively for positive (or negative) small vectors. As the dwell times changes depending on the voltage reference angle and its amplitude, an average value is calculated in order to obtain an measure of the maximum dc drift that can be corrected.

C.1 Calculation of the Small Vectors Average Time

To determine the average time only the positive half cycle of phase a is considered. Given that the system is symmetrical, this result is extended for the remaining phases. The average time depends on the value of the amplitude modulation index m_a because the voltage reference crosses different regions of the sector depending on its value, as displayed in Fig. C.1. It can be seen that the value of m_a will result in three possible scenarios of redistribution.

The normalized mean value for the voltage in phase a during its positive half cycle is defined as:

$$\bar{S}_a = \frac{1}{\pi}\int_0^{\pi} S_a(x)\mathrm{d}x, \tag{C.1.1}$$

where S_a corresponds to the switching function of the devices in phase a. This switching function can be used to determine the additional dc drift that can be injected to this voltage, by calculating the average time that the small vectors are used, t_a. This time can be redistributed under the limit condition to the exclusive use of certain type of small vectors. Therefore, $t_a/2$ remains for balancing purposes. This remaining time is equivalent to the maximum

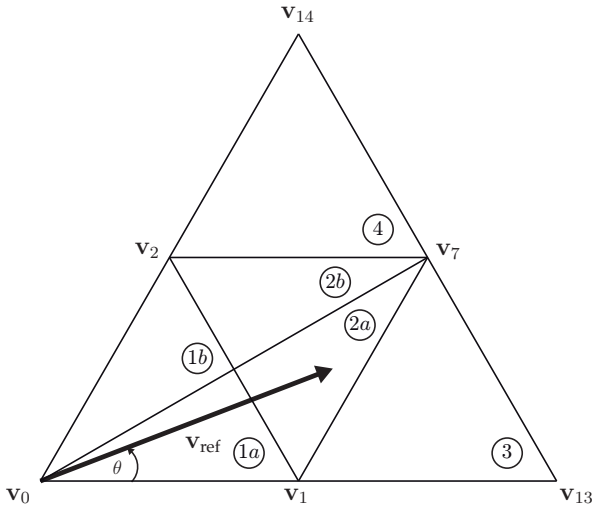


Figure C.1. Subdivision in six regions of sector I.

dc drift that can be added to the modulating signal.

C.1.1 Small Modulation Index

If $m_a \in [0, 0.5]$, then the reference vector passes only through regions $1a$ and $1b$ of each sector, as displayed in Fig. C.1. Then, the sectors associated with the usage of the phase a during the positive half cycle are I, II, V, and VI. The small vectors at the beginning of the switching sequence are used to determine the remaining average time. If the vector is located in the beginning (or center) of the switching sequence, then it is alternated with its corresponding negative (or positive) small vector in order to achieve one switch transition. This alternation does not occur if the vector occupies other positions in the switching sequence.

For region I-$1a$ the only small vector that use the phase a is $\mathbf{v}_1$, and its average dwell time is given by

$$t_{a_{\mathbf{v}_1}}^{\text{I-}1a} = \int_0^{\gamma} 2m_a \sin\left(\frac{\pi}{3} - x\right) \mathrm{d}x. \tag{C.1.2}$$

In region I-$1b$, the vectors are $\mathbf{v}_1$ and $\mathbf{v}_2$ and its corresponding average times need to be calculated. However, only $\mathbf{v}_2$ is in the beginning of the sequence ($\mathbf{v}_1$ has already been used the entire time, so there is no time left to use).

$$t_{a_{\mathbf{v}_2}}^{\text{I-}1b} = \int_{\frac{\pi}{3}-\gamma}^{\frac{\pi}{3}} 2m_a \sin\left(x - \frac{\pi}{3}\right) \mathrm{d}x. \tag{C.1.3}$$

For region II-$1a$

$$t_{a_{\mathbf{v}_2}}^{\text{II-}1a} = \int_{\frac{\pi}{3}}^{\frac{\pi}{3}+\gamma} 2m_a \sin\left(\frac{2\pi}{3} - x\right) \mathrm{d}x. \tag{C.1.4}$$

For region V-$1b$

$$t_{a_{\mathbf{v}_6}}^{\text{V-}1b} = \int_{\frac{5\pi}{3}-\gamma}^{\frac{5\pi}{3}} 2m_a \sin\left(x - \frac{4\pi}{3}\right) \mathrm{d}x. \tag{C.1.5}$$

For region VI-1a

$$t_{a_{\mathbf{v}_6}}^{\text{VI-1}a} = \int_{\frac{5\pi}{3}}^{\frac{5\pi}{3}+\gamma} 2m_a \sin\left(2\pi - x\right) \mathrm{d}x. \tag{C.1.6}$$

Finally for region VI-1b

$$t_{a_{\mathbf{v}_1}}^{\text{VI-1}b} = \int_{2\pi-\gamma}^{2\pi} 2m_a \sin\left(x - \frac{5\pi}{3}\right) \mathrm{d}x. \tag{C.1.7}$$

According to (C.1.1) and assuming that $\gamma = \pi/6$ in this range for m_a, the remaining time is given by

$$\frac{t_a}{2} = \frac{1}{2\pi}\left(t_{a_{\mathbf{v}_1}}^{\text{I-1}a} + t_{a_{\mathbf{v}_2}}^{\text{I-1}b} + t_{a_{\mathbf{v}_2}}^{\text{II-1}a} + t_{a_{\mathbf{v}_6}}^{\text{V-1}b} + t_{a_{\mathbf{v}_6}}^{\text{VI-1}a} + t_{a_{\mathbf{v}_1}}^{\text{VI-1}b}\right). \tag{C.1.8}$$

As established earlier, this time is equal to the normalized dc drift that can be added to the modulating signal in order to achieve balance. Therefore,

$$\hat{\alpha} = \frac{-3m_a + 3\sqrt{3}m_a}{\pi}. \tag{C.1.9}$$

C.1.2 Medium Modulation Index

If $m_a \in [0.5, 1/\sqrt{3}]$, then the reference vector passes through regions $1a$, $1b$, $2a$ and $2b$. In this case, γ is the angle at which the reference changes the triangle defined by the closest surrounding vectors, and it is defined as

$$\gamma = \arcsin\left(\frac{1}{2m_a}\right) - \frac{\pi}{3}. \tag{C.1.10}$$

The expressions for the dwell times in the regions $1a$ and $1b$ do not changed, (C.1.2) - (C.1.7) are still valid in this range, using the corresponding γ. The remaining dwell times are the following:

For region I-2a

$$t_{a_{\mathbf{v}_1}}^{\text{I-2}a} = \int_{\gamma}^{\frac{\pi}{6}} 1 - 2m_a \sin(x)\mathrm{d}x. \tag{C.1.11}$$

For region I-2b

$$t_{a_{\mathbf{v}_2}}^{\text{I-2}b} = \int_{\frac{\pi}{6}}^{\frac{\pi}{3}-\gamma} 1 - 2m_a \sin\left(\frac{\pi}{3} - x\right)\mathrm{d}x. \tag{C.1.12}$$

For region II-2a

$$t_{a_{\mathbf{v}_2}}^{\text{II-2}a} = \int_{\frac{\pi}{3}+\gamma}^{\frac{\pi}{2}} 1 - 2m_a \sin\left(x - \frac{\pi}{3}\right)\mathrm{d}x. \tag{C.1.13}$$

For region V-2b

$$t_{a_{\mathbf{v}_6}}^{\text{V-2}b} = \int_{\frac{3\pi}{2}}^{\frac{5\pi}{3}-\gamma} 1 - 2m_a \sin\left(\frac{5\pi}{3} - x\right)\mathrm{d}x. \tag{C.1.14}$$

In region VI-2a

$$t_{a_{\mathbf{v}_6}}^{\text{VI-2}a} = \int_{\frac{5\pi}{3}+\gamma}^{\frac{11\pi}{6}} 1 - 2m_a \sin\left(x - \frac{5\pi}{3}\right)\mathrm{d}x. \tag{C.1.15}$$

For region VI-2b

$$t_{a_{\mathbf{v}_6}}^{\text{VI-2}b} = \int_{\frac{11\pi}{6}}^{2\pi-\gamma} 1 - 2m_a \sin\left(2\pi - x\right)\mathrm{d}x. \tag{C.1.16}$$

By adding (C.1.2)-(C.1.16) and dividing by 2π, is possible to obtain the average remaining time of

$$\hat{\alpha} = \frac{\frac{\pi}{2} - 3\gamma + 3m_a\left(1 + 2\sin\left(\gamma - \frac{\pi}{6}\right) + \sqrt{3}\right)}{\pi}. \tag{C.1.17}$$

C.1.3 Large Modulation Index

The remaining modulation index range is $m_a \in [1/\sqrt{3}, 1]$, and the idea behind is the same as those of the previous ones. In this case, the regions that crosses the reference vector are $2a$, $2b$, 3 and 4. The results in (C.1.11) - (C.1.16) are still valid in this range, therefore the remaining average times are as follows

In the region I-3

$$t_{a_{\mathbf{v}_1}}^{\text{I-3}} = \int_0^{\gamma} 2 - 2m_a \sin\left(x + \frac{\pi}{3}\right) \mathrm{d}x. \tag{C.1.18}$$

following with region I-4

$$t_{a_{\mathbf{v}_2}}^{\text{I-4}} = \int_{\frac{\pi}{3}-\gamma}^{\frac{\pi}{3}} 2 - 2m_a \sin\left(x + \frac{\pi}{3}\right) \mathrm{d}x. \tag{C.1.19}$$

then, region II-3

$$t_{a_{\mathbf{v}_2}}^{\text{II-3}} = \int_{\frac{\pi}{3}}^{\frac{\pi}{3}+\gamma} 2 - 2m_a \sin(x) \mathrm{d}x. \tag{C.1.20}$$

Finally, region VI-4

$$t_{a_{\mathbf{v}_1}}^{\text{VI-4}} = \int_{2\pi-\gamma}^{2} \pi 2 - 2m_a \sin\left(x + \frac{4\pi}{3}\right) \mathrm{d}x. \tag{C.1.21}$$

Is important to note that in this range, the expression for γ changes into

$$\gamma = \frac{\pi}{3} - \arcsin\left(\frac{1}{2m_a}\right). \tag{C.1.22}$$

The average remaining time is the sum of (C.1.11)-(C.1.21) divided by π. Therefore, the maximum dc drift that can be injected is defined by

$$\hat{\alpha} = \frac{\frac{\pi}{2} + 3\gamma - 3m_a\left(1 + 2\sin\left(\gamma + \frac{\pi}{6}\right) - \sqrt{3}\right)}{\pi}. \tag{C.1.23}$$

To conclude, an analogous analysis can be conducted to determine maximum negative dc drift $\hat{\beta}$ that can injected by redistributing the small vectors time, because the generated waveform is half-wave symmetrical, thereby leading to

$$\hat{\beta} = \begin{cases} \dfrac{-3m_a + 6m_a \sin\left(\gamma + \frac{\pi}{6}\right)}{\pi}, & m_a \in \left[0, \frac{1}{2}\right[\\ \dfrac{\frac{\pi}{2} - 3\gamma + 3m_a\left(1 + 2\sin\left(\gamma - \frac{\pi}{6}\right) + \sqrt{3}\right)}{\pi}, & m_a \in \left[\frac{1}{2}, \frac{\sqrt{3}}{3}\right[\\ \dfrac{\frac{\pi}{2} + 3\gamma - 3m_a\left(1 + 2\sin\left(\gamma + \frac{\pi}{6}\right) - \sqrt{3}\right)}{\pi}, & m_a \in \left[\frac{\sqrt{3}}{3}, 1\right] \end{cases} \tag{C.1.24}$$

where γ is the angle at which the change of region occurs and is defined according to

$$\gamma = \begin{cases} \dfrac{\pi}{6}, & m_a \in \left[0, \frac{1}{2}\right[\\ \arcsin\left(\frac{1}{2m_a}\right) - \dfrac{\pi}{3}, & m_a \in \left[\frac{1}{2}, \frac{\sqrt{3}}{3}\right[\\ \dfrac{\pi}{3} - \arcsin\left(\frac{1}{2m_a}\right), & m_a \in \left[\frac{\sqrt{3}}{3}, 1\right] \end{cases} \tag{C.1.25}$$

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