

1-1-2011

A Comparative Analysis Of MEMS Parallel Plate Actuators

Boris Shapiro
Ryerson University

Follow this and additional works at: <http://digitalcommons.ryerson.ca/dissertations>



Part of the [Mechanical Engineering Commons](#)

Recommended Citation

Shapiro, Boris, "A Comparative Analysis Of MEMS Parallel Plate Actuators" (2011). *Theses and dissertations*. Paper 1627.

This Thesis is brought to you for free and open access by Digital Commons @ Ryerson. It has been accepted for inclusion in Theses and dissertations by an authorized administrator of Digital Commons @ Ryerson. For more information, please contact bcameron@ryerson.ca.

A Comparative Analysis of MEMS Parallel Plate Actuators

By

Boris Shapiro
Bachelor of Science, University of Toronto 2009

A report
presented to Ryerson University

in partial fulfillment of the
requirements for the degree of
Master of Engineering
in the Program of
Mechanical Engineering

Toronto, Ontario, Canada 2011
© Boris Shapiro, 2011

Author's Declaration

I hereby declare that I am the sole author of this thesis.

I authorize Ryerson University to lend this thesis to other institutions or individuals for the purpose of scholarly research.

I further authorize Ryerson University to reproduce this thesis by photocopying or by other means, in total or in part, at the request of other institutions or individuals for the purpose of scholar research.

A Comparative Analysis of MEMS Parallel Plate Actuators

Master of Engineering, 2011

Boris Shapiro

Mechanical Engineering

Ryerson University

Abstract

The purpose of this study is to compare the deformation of the moving top plate of five distinct parallel plate capacitor designs under applied voltage as well as compare the pull-in voltage of each design. The parallel plate designs are created using AutoCAD 2008 software and the simulations are performed using CoventorWare 2010. The control design is first validated with known results and then compared to the remaining four designs. Finally, pull-in voltages of all five designs is determined and compared to determine the advantages and disadvantages of each design.

Acknowledgements

I would like to thank Dr. Donatus Oguamanam for his guidance and support throughout the duration of this project. I would also like to thank my mother and girlfriend for their love and support.

Table of Contents

Author's Declaration	ii
Abstract	iii
Acknowledgements	iv
Table of Contents	v
List of Figures	vii
Chapter 1	1
1.1 Introduction	1
Chapter 2	3
2.1 Literature Review	3
2.1.1 Types of Parallel Plate Actuators/Capacitors	3
2.1.2 An Alternate Approach to Calculating Pull-In Voltage	4
Chapter 3	6
3.1 Theory	6
3.1.1 Traditional Pull-In Analysis	6
3.1.2 The Method of Zhang and Fang	7
3.2 Manufacturing Process	9
3.3 The Designs	13
3.4 Elements Used	18
Chapter 4	20
4.1 Analysis	20
4.1.1 Static Analysis	20
4.1.1.1 Design 1	20
4.1.1.2 Design 2	21
4.1.1.3 Design 3	22
4.1.1.4 Design 4	23
4.1.1.5 Design 5	23
4.1.2 Static Analysis Results	24
4.1.3 Pull-In Analysis	28
4.1.3.1 Design 1 Results	29

4.1.3.2 Design 2 Results	30
4.1.3.3 Design 3 Results	32
4.1.3.4 Design 4 Results	32
4.1.3.5 Design 5 Results	34
Chapter 5	35
5.1 Conclusions	35
5.2 Future Work	36
References	37

List of Figures

Fig 1. Parallel Plate Model With Translation and Deformation	4
Fig 2. Simplified Model of the Parallel Plate Capacitor	5
Fig 3. Traditional Model of the Parallel Plate Capacitor	5
Fig 4. Zhang and Fang's Parallel Plate Design	5
Fig 5. Schematic Illustration of Calculating the Capacitance of Two Plates with an Angle	9
Fig 6. Nitride, Poly0 and Photoresist layers deposited on the Silicon wafer substrate	10
Fig 7. The Photoresist Layer patterned using Photolithography	11
Fig 8. The exposed Poly0 sections are etched away and the Photoresist chemically peeled	11
Fig 9. First Oxide Layer, etched dimples and Anchor points	12
Fig 10. Poly1 and PSG mask are deposited	12
Fig 11. The completed MEMS device using PolyMUMPs process	13
Fig 12. Design 1: Modification of the design by Zhang and Fang for PolyMUMPS.....	15
Fig 13. Design 2: a modified version of Design 1 with displaced support beams.....	15
Fig 14. Design3: a modified version of Design 1 with displaced support beams.....	16
Fig 15. Design 4: Hexagonal plates and only 3 support beams	17
Fig 16. Design 5: a hybridization of Designs 1-4	18
Fig 17. An illustration of the mesh used in Design 1	21
Fig 18. An illustration of the mesh used in Design 2	21
Fig 19. An illustration of the mesh used in Design 3	22
Fig 20. An illustration of the mesh used in Design 4	23
Fig 21. An illustration of the mesh used in Design 5	24
Fig 22. Design 1 Static Analysis under 12.5V Load	25
Fig 23. Design 5 Static Analysis under 12.5V Load	25
Fig 24. Zhang and Fang's Static Analysis under 12-13V load	26
Fig 25. Design 2 Under 12.5V Load	27
Fig 26. Design 3 Under 12.5V Load	27
Fig 27. Design 4 Under 12.5V Load	28
Fig 28. Pull-In Simulation Results for Design 1	29
Fig 29. Design 1 Deformation at pull-in voltage	30

Fig 30. Pull-In Simulation Results for Design 2	31
Fig 31. Design 2 Deformation at Pull-In Voltage	31
Fig 32. Design 3 Pull-In Deformation	32
Fig 33. Pull-In Simulation Results for Design 4	33
Fig 34. Design 4 Pull-In Deformation	33
Fig 35. Pull-In Simulation Results for Design 5	34
Fig 36. Design 5 Pull-In Deformation	34

Chapter 1

1.1 Introduction

Variable parallel plate capacitors are widely used in various applications, such as Radio Frequency MEMS (RF MEMS). These MEMS devices can be microrelays[1], micromirrors[2], micro actuators[3], microswitches[4], micro position sensors[5], voltage controlled oscillators[6], resonators[7] and even pixels in display systems[8].

These capacitors consist of a single moving plate and a fixed plate (usually to the substrate). When voltage is applied to the capacitor the free plate is attracted to the fixed plate. If a high enough voltage is applied, the plates touch and the device is short circuited. The threshold distance apart after which the free plate cannot avoid touching the fixed plate is called the pull-in distance, and the voltage threshold is called the pull-in voltage.

In order to prevent the two plates from touching, designers must be aware of this pull-in distance and voltage and estimate them using two simple equations (which are expanded upon in the literature review and theory chapters). These two equations, however, ignore any deformation the moving plate may experience when voltage is applied. This report uses the work by Zhang and Fang[9] as a benchmark and compares five distinct parallel plate capacitors to determine the generality of their modified formulation for the pull-in voltage calculation.

This report also compares the deformations of the moving plate as well as the applied voltages of these five designs. Lastly, this report seeks to determine the generality of the

formulation by Zhang and Fang[9] and to determine any advantages or disadvantages of various parallel plate designs.

Chapter 2

2.1 Literature Review

2.1.1 Types of Parallel Plate Actuators/Capacitors

As mentioned before, variable plate capacitors are used in a myriad of applications. Digital micromirror devices, or DMDs, are used in digital light processing (DLP) projection technology invented by Texas Instruments in 1987[10]. The DMD is an array of micro square mirrors. Each of these mirrors can be turned on and off thousands of times a second. Each mirror represents a pixel in the projected image[10]. This allows for a brighter, sharper and more realistic images than using alternative technologies.

MEMS display technology is not limited to micrometers. Mirasol[8] has designed the MEMS Drive IMOD Reflective technology screen. This screen consists of millions of pixels, where each pixel is a parallel plate actuator with one moving plate (thin film) and one fixed plate. When voltage is applied, the moving film can achieve one of three states. When light hits a pixel and voltage is not applied, red, green or blue is reflected. When voltage is applied, the moving plate is moved towards the fixed plate and the pixel is then turned black[8]. By using ambient light and very small voltages, Mirasol was able to create displays that use very little power, in fact, Mirasol claims that when displaying static images their display has near zero power usage[8].

2.1.2 An Alternate Approach to Calculating Pull-In Voltage

Traditionally when it comes to parallel plate capacitors (or actuators) estimating the pull-in distance and voltage is relatively simple. The pull-in distance, $d_{\text{pull-in}}$ [14], is estimated to be one third of the initial gap, d_0 between the two plates:

$$d_{\text{pull-in}} = \frac{1}{3} d_0 \quad (2.1)$$

where d_0 is the initial gap between the two plates. The pull-in voltage, $V_{\text{pull-in}}$ [14], is estimated by

$$V_{\text{pull-in}} = \frac{2}{3} \sqrt{\frac{d_0}{3}} d_0 \frac{\sqrt{2A\epsilon_r\epsilon_0 k}}{A\epsilon_r\epsilon_0} \quad (2.2)$$

Where A is the overlapping area of the two plates, ϵ_r is the relative permittivity, ϵ_0 is the permittivity in vacuum and k is the stiffness of the support beams.

Zhang and Fang[9], however, argue that since the moving plate bends when voltage is applied, these estimates are not entirely accurate. They describe the top plate as having three sections (See Fig. 1 and Fig. 2) as opposed to the uniform change in displacement of the ideal model (Fig. 3), where under each section there is a variance in capacitance induced by the deformation of the top plate.

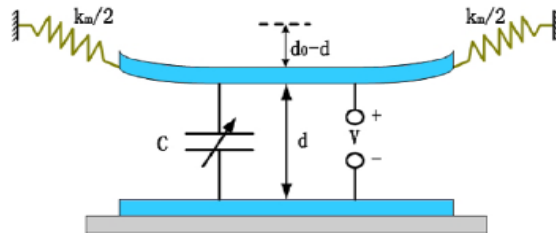


Figure 1. Parallel Plate Model With Translation and Deformation [9]

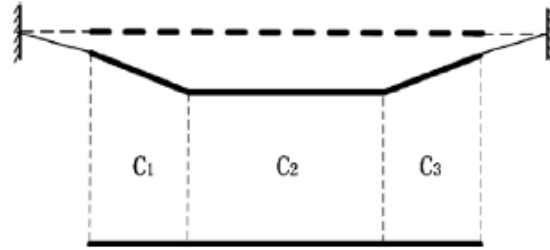


Figure 2. Simplified Model of the Parallel Plate Capacitor [9]

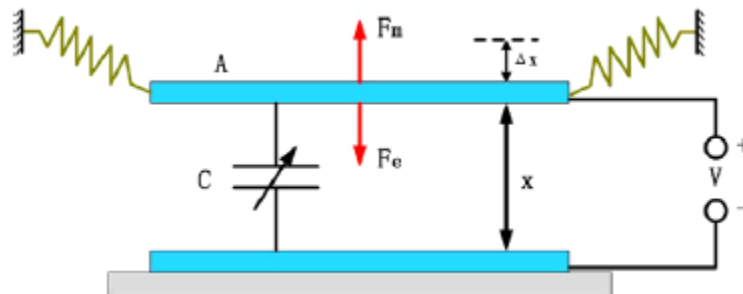


Figure 3. Traditional Model of the Parallel Plate Capacitor [9]

In their paper, Zhang and Fang[9] provide a formulation to compensate for the deformation of the top plate in order to obtain a more accurate pull-in voltage estimate. Their formulation is based on their own design of a parallel plate capacitor (and other similar designs), namely having the support beams on opposite edges (Fig. 4). This raises the question of just how generally applicable the formulation is and how the design of the capacitor affects the top plate deformation.

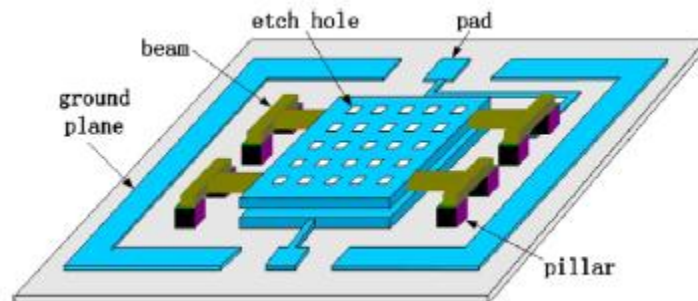


Figure 4. Zhang and Fang's Parallel Plate Design [9]

Chapter 3

3.1 Theory

3.1.1 Traditional Pull-In Analysis[14]

Consider the parallel plate actuator described in Fig. 3. The capacitance is expressed

$$C = \frac{A\epsilon_r\epsilon_0}{d_0} \quad (3.1)$$

where ϵ_r is the relative permittivity, ϵ_0 is vacuum permittivity, A is the overlapping area of the two plates and d_0 is the initial gap. The total electric energy stored, W_e , is expressed with

$$W_e = \frac{1}{2}CV^2 \quad (3.2)$$

where V^2 is the voltage applied squared. If there is a change in displacement, Eqn. (3.2) becomes

$$W_e = \frac{1}{2}CV^2 = \frac{1}{2} \frac{A\epsilon_r\epsilon_0}{d_0-d} V^2 \quad (3.3)$$

where d is the gap after applied voltage. According to the principle of virtual work[13], the electrostatic force, $|F_e|$, is equal to the gradient of stored energy with respect to the position (or displacement) of the moveable electrode (top moving plate). Thus

$$|F_e| = \left| \frac{\partial W_e}{\partial d} \right| \quad (3.4)$$

Combining Eqns. (3.3) and (3.4), the electrostatic force acting on the moving plate is

$$|F_e| = \left| \frac{1}{2} \frac{A\epsilon_r\epsilon_0}{(d_0-d)^2} \right| V^2 \quad (3.5)$$

The spring force, F_n , is acting in the opposite direction of F_e . This spring force is linear and is expressed as

$$F_n = k_e d \quad (3.6)$$

where k_e is the equivalent stiffness of the support beams. For the system to be in equilibrium,

$F_n = F_e$. Thus combining (3.5) and (3.6) it is possible to isolate V as

$$V = \sqrt{d}(d_0 - d) \frac{\sqrt{2A\epsilon_r\epsilon_0 k_e}}{A\epsilon_r\epsilon_0} \quad (3.7)$$

To determine the pull-in distance (maximum displacement) and voltage, the first derivative of Eqn. (3.7) with respect to d yields

$$\begin{aligned} \frac{dV}{dd} &= \frac{1}{2}d^{-\frac{1}{2}}(d_0 - d) \frac{\sqrt{2A\epsilon_r\epsilon_0 k_e}}{A\epsilon_r\epsilon_0} - d^{\frac{1}{2}} \frac{\sqrt{2A\epsilon_r\epsilon_0 k_e}}{A\epsilon_r\epsilon_0} = 0 \\ &\rightarrow d = \frac{1}{3}d_0 = d_{pull-in} \end{aligned} \quad (3.8)$$

Thus, Eqn. (9) shows that the pull-in distance is one third of the initial gap. Using eqn. (3.8) in Eqn. (3.7) it is straight forward to show that the pull-in voltage is

$$V_{pull-in} = \sqrt{d_{pull-in}}(d_0 - d_{pull-in}) \frac{\sqrt{2A\epsilon_r\epsilon_0 k_e}}{A\epsilon_r\epsilon_0} = \frac{2}{3} \frac{\sqrt{d_0}}{\sqrt{3}} \frac{\sqrt{2A\epsilon_r\epsilon_0 k_e}}{A\epsilon_r\epsilon_0} \quad (3.9)$$

3.1.2 The Method of Zhang and Fang[9]

Zhang and Fang[9] attempt to take into account the deformation of the moving plate. As such, they represent the capacitance of the system, C , in terms of the sum of the centre capacitance, C_2 , and the two border capacitances, C_3 , (Fig. 2). Thus

$$C = C_2 + 2C_3 \quad (3.10)$$

To calculate C_3 (Fig. 5), first suppose that the sloping length is δ , the sloping section and the horizontal section intersect at O and the angle between the two parts is θ . C_3 can be divided into many ideal narrow sections. The capacitance of each section is defined as

$$dC = \frac{\epsilon_0 b dr}{r \sin \theta} \quad (3.11)$$

where b is the width of the plate. Therefore, the capacitance C_3 is

$$C_3 = \int dC = \int_{R_1}^{R_2} \frac{\varepsilon_0 b dr}{r \cdot \sin \theta} = \frac{\varepsilon_0 b}{\sin \theta} \int_{R_1}^{R_2} \frac{dr}{r} = \frac{\varepsilon_0 b}{\sin \theta} \ln \frac{R_2}{R_1} \quad (3.12)$$

where

$$\frac{R_2}{R_1} = \frac{\Delta y + d}{d} = \frac{\Delta x \cdot \tan \theta + d}{d} = 1 + \frac{\Delta x \cdot \tan \theta}{d} \quad (3.13)$$

Thus

$$C_3 = \frac{\varepsilon_0 b}{\sin \theta} \ln \left(1 + \frac{\Delta x \cdot \tan \theta}{d} \right) \quad (3.14)$$

When $\theta \rightarrow 0$, $\Delta x \rightarrow \delta$

$$C_3 = \lim_{\theta \rightarrow 0} \left[\frac{\varepsilon_0 b}{\sin \theta} \ln \left(1 + \frac{\Delta x \cdot \tan \theta}{d} \right) \right] = \lim_{\theta \rightarrow 0} \varepsilon_0 b \frac{\frac{d \ln \left(1 + \frac{\delta \cdot \tan \theta}{d} \right)}{d \theta}}{\frac{d \sin \theta}{\theta}} = \frac{\varepsilon_0 b \delta}{d} \quad (3.15)$$

Equation (3.15) is the result of the nominal parallel plate capacitor. If θ is very small, suppose

$$\lambda = \frac{\Delta x}{a} \quad (3.16)$$

Then

$$C_3 = \frac{\varepsilon_0 b}{\sin \theta} \ln \left(1 + \frac{\lambda a \cdot \tan \theta}{d} \right) \quad (3.17)$$

The capacitance C_2 can be expressed as

$$C_2 = \frac{\varepsilon_0 (a - 2\Delta x)}{d} = \frac{\varepsilon_0 a (1 - 2\lambda)}{d} \quad (0 < \lambda < 0.5) \quad (3.18)$$

Since pull-in occurs at $d = \frac{1}{3}d_0$, Δy can be expressed as

$$\Delta y = \Delta x \cdot \tan \theta < \frac{1}{3}d_0 \quad (3.19)$$

That is

$$\lambda \cdot \tan \theta < \frac{1}{3}d_0 \quad (3.20)$$

Then the capacitance of the system can then be expressed as

$$C = C_2 + 2C_3 = \frac{\varepsilon_0 ab(1 - 2\lambda)}{d} + \frac{2\varepsilon_0 b}{\sin \theta} \cdot \ln \left(1 + \frac{\lambda a \cdot \tan \theta}{d} \right) \quad (3.21)$$

With this new expression for capacitance, the pull-in voltage can now be determined using Eqns. (3.1) to (3.9).

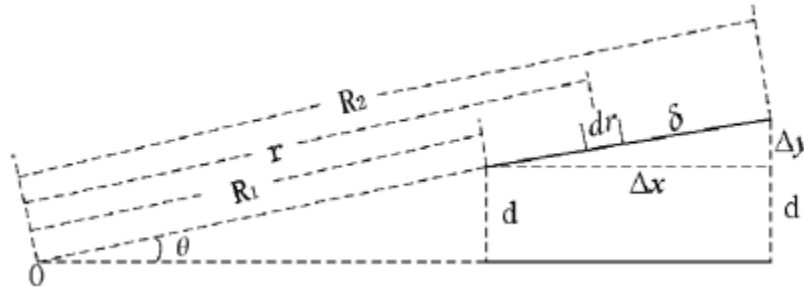


Figure 5. Schematic illustration of calculating the capacitance of two plates with an angle [9]

3.2 Manufacturing Process

Zhang and Fang[9] do not mention the manufacturing process of their actuator; they merely describe it as a "simple surface micromachining" and proceed to describe the steps taken to fabricate their capacitor. The material used in their design is nickel. Hence it can be speculated that the manufacturing process is MetalMUMPS: a process under the Multi User MEMS Process umbrella.

A different manufacturing process is used for this project. This process also falls under the MUMPS category, however instead of using Nickel the material of choice is Polysilicon. As such the name of this process is called PolyMUMPs. The familiarity of the author with PolyMUMPs influenced this decision. Additionally, since Zhang and Fang[9] indicate that their formulation is generalized, the actual manufacturing process and the materials used in fabrication should not affect its validity.

PolyMUMPs is a relatively simple process which consists of three layers. The process begins with a 150 mm silicon wafer, typically of 1-2 Ω resistivity[11]. The wafer is heavily

doped with phosphorus in a diffusion furnace using a phosphosilicate glass (PSG) sacrificial layer. This reduces (or prevents) the charge feeding through to the substrate from the devices on the surface. Then, after the removal of the PSG film, a silicon nitride layer is deposited as an insulation layer. This layer is 600 nm (0.6 μm) thick and deposited using a process called Low Pressure Chemical Vapour Deposition (LPCVD). Following that, the first polysilicon layer (Poly0) is deposited on top of the nitride layer. This polysilicon layer is 500 nm (0.5 μm) thick and is deposited using LPCVD. Poly0 is then patterned using photolithography (Fig. 6, 7 and 8). Photolithography is a process which involves the coating of the wafer with a photoresist material. The wafer is then covered with the appropriate mask (the design appropriate to the layer) and is exposed to UV light. After exposure, the poly0 layer is etched using a plasma etch system.



Figure 6. Nitride, Poly0 and Photoresist layers deposited on the Silicon wafer substrate [11]



Figure 7. The Photoresist Layer patterned using Photolithography [11]

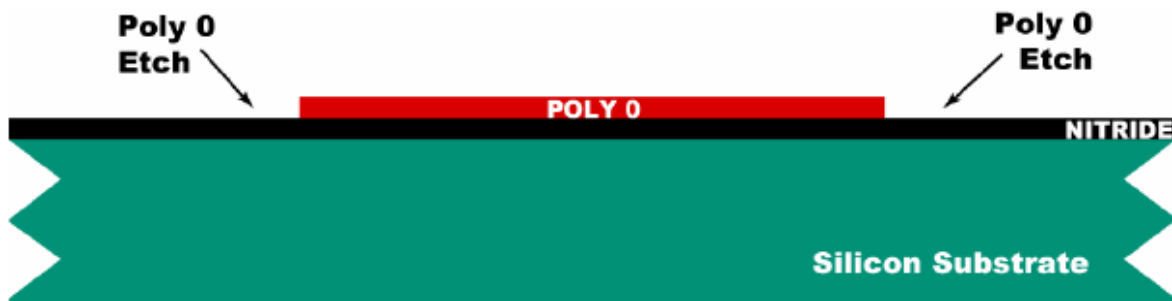


Figure 8. The exposed Poly0 sections are etched away and the Photoresist chemically peeled [11]

Following the etch of poly0, a 2.0 μm PSG sacrificial layer is deposited and annealed. This layer is known as first Oxide and it is removed at the end of the manufacturing process in order to free the first mechanical layer of polysilicon. This layer is lithographically patterned with dimples and etched using a Reactive Ion Etch (RIE) system. These dimples are generally 0.75 μm deep and are used to prevent sticking caused by the pull-in effect. After the dimples are etched the third mask layer, called Anchor1, is RIE etched into the PSG sacrificial layer. This provides anchor points for the Poly1 layer (Fig. 9).

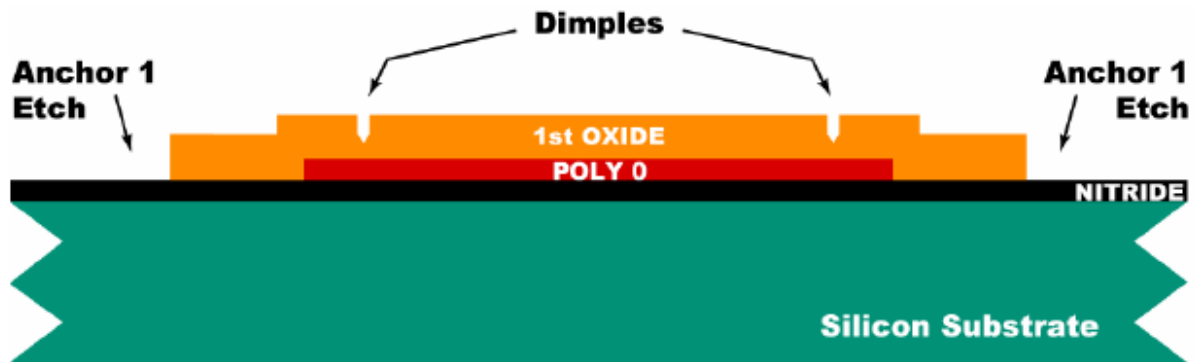


Figure 9. First Oxide Layer, etched dimples and Anchor points [11]

After Anchor1 is etched, the first structural layer of polysilicon (called Poly1) is deposited with thickness of $2.0\ \mu\text{m}$. A $0.2\ \mu\text{m}$ layer of PSG is then deposited on poly1 and annealed. This dopes poly1 with phosphorus from the PSG layer on both sides, significantly reducing the net stress in Poly1 (Fig. 10).

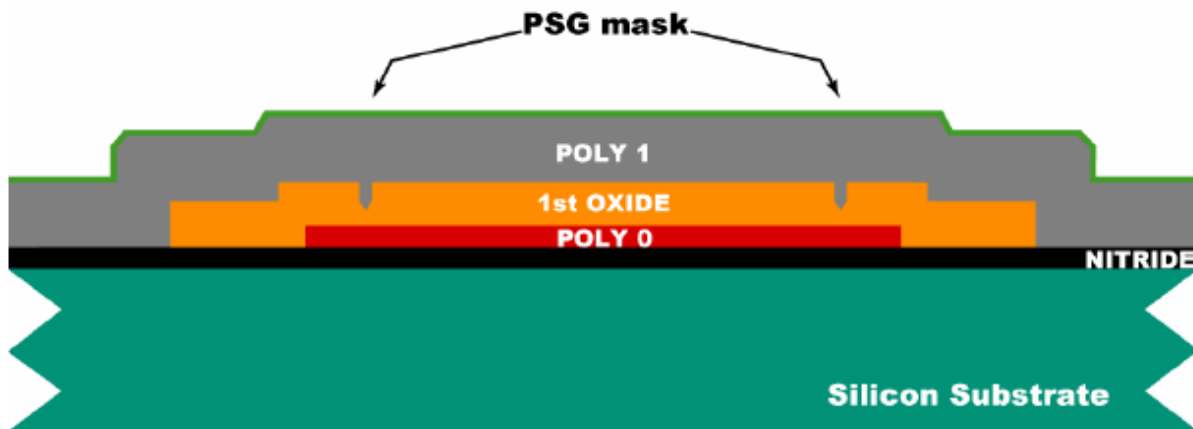


Figure 10. Poly1 and PSG mask are deposited [11]

PolyMUMPs machined MEMS devices can have a second structural layer of polysilicon (Poly2, $1.5\ \mu\text{m}$ thick) as well as a metal top layer ($0.5\ \mu\text{m}$). The metal layer provides for proving, bonding electrical routing and highly reflective mirror surfaces. However, the designs used in

this report do not use Poly2 or metal layers so the process and related steps – such as Anchor2 – are ignored.

At this point, the sacrificial layers are etched and Poly1 is supported entirely on its own (Fig. 11). In order to etch the sacrificial layer from under Poly1, holes are added (labelled Hole0 for poly1 and Hole1 for Poly2. Please note that Hole0 and Hole1 can only be seen from bird's eye view and as such are not mentioned in Figures 6 through 11. Hole0, however, is visible in Figures 12 through 16). These holes have no set size rules and are designed based on the engineer experience of the engineer; however there is a maximum distance between holes of 30 μm . Anything larger than that will result in the PSG layer under Poly1 to not be removed in its entirety. This 30 μm limit is due to limitations in the RIE process.

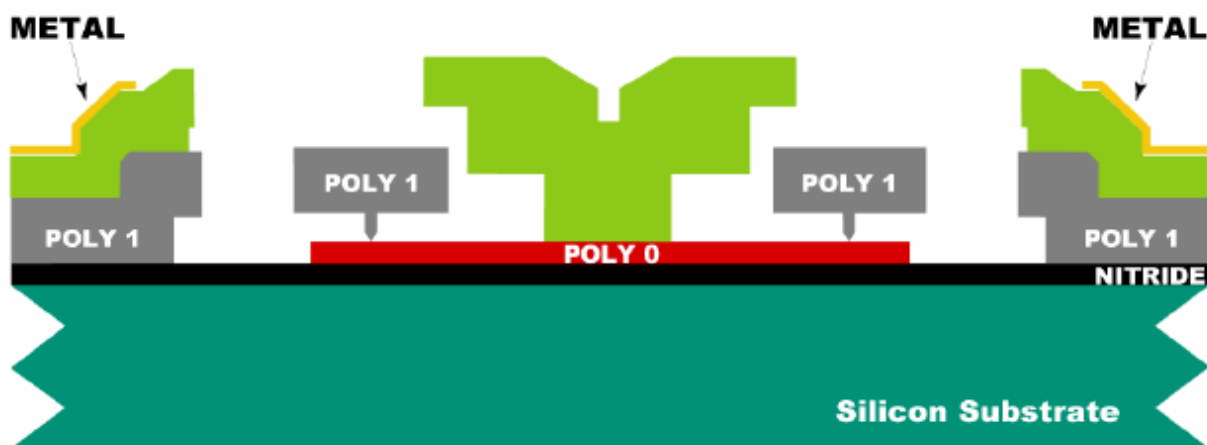


Figure 11. The completed MEMS device using PolyMUMPs process [11]

3.3 The Designs

Zhang and Fang's[9] design used two support beams on either side of the moving plate. This design played a part in their formulation. However, not all parallel plate actuators are designed in this manner and as such four additional designs are considered in this comparative

analysis. Zhang and Fang[9] provided some measurements of their device. It is known that the overlap area was 700 μm by 700 μm and that the air gap was 3 μm . Thus, all five designs used have an overlap area of 700 μm by 700 and the air gap, however, is only 2 μm as per PolyMUMPs design rules. The other dimensions in the design had to be estimated. As such, the connector pads were estimated to be 135 μm by 135 μm . The length of each support beam was estimated to be 248 μm and its width to be 68 μm . Since Zhang and Fang's design did not use MUMPs rule, Hole0 dimensions are adjusted to comply with MUMPs rules. For Designs 1, 2, 3 and 5 the holes are 25.83 μm by 25.83 μm .

Design 1 (Fig. 12) is identical to that of Zhang and Fang[9] with the exception of modifying the holes to conform with PolyMUMPs design rules. Design 2 (Fig. 13) and 3 (Fig. 14) contain slight modifications to Zhang and Fang's design. In Design 2 there are still four support beams, however they are connected at the halfway point of each side of the top plate: one beam per side. Design 2 again features a different location for the support beam. In this design, the support beams are located at the corners of the top plate and just like in Design 2, each corner has one support beam. In Designs 2 and 3 all dimensions are identical to Design 1.

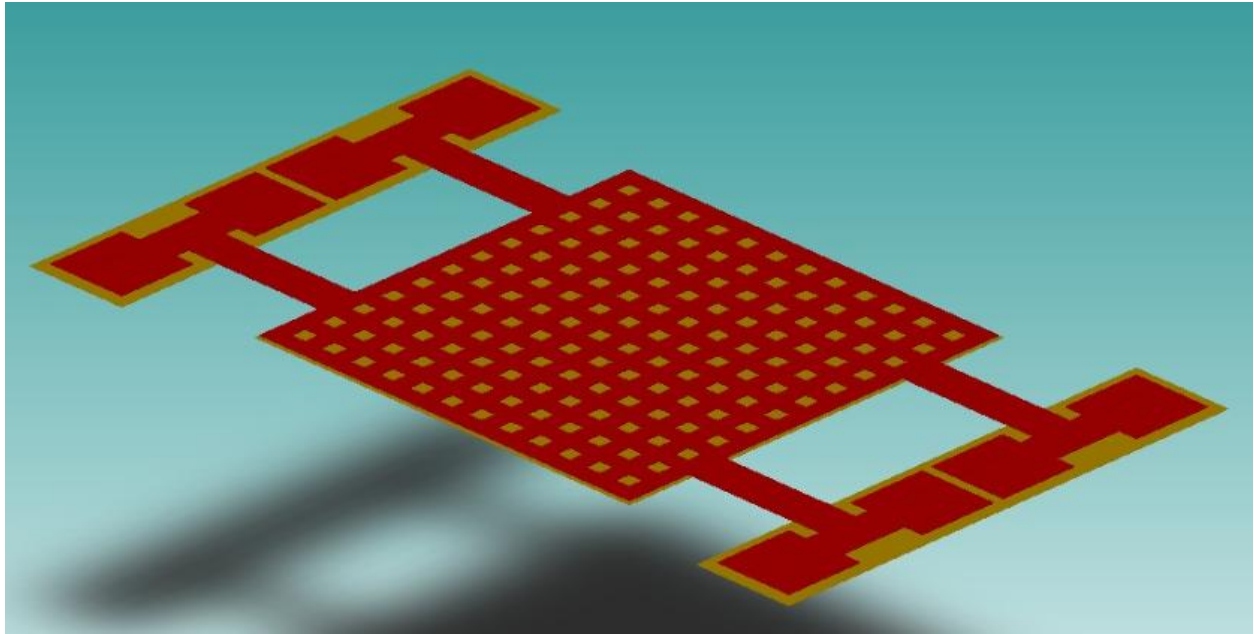


Figure 12. Design 1: Modification of the design by Zhang and Fang[9] for PolyMUMPs

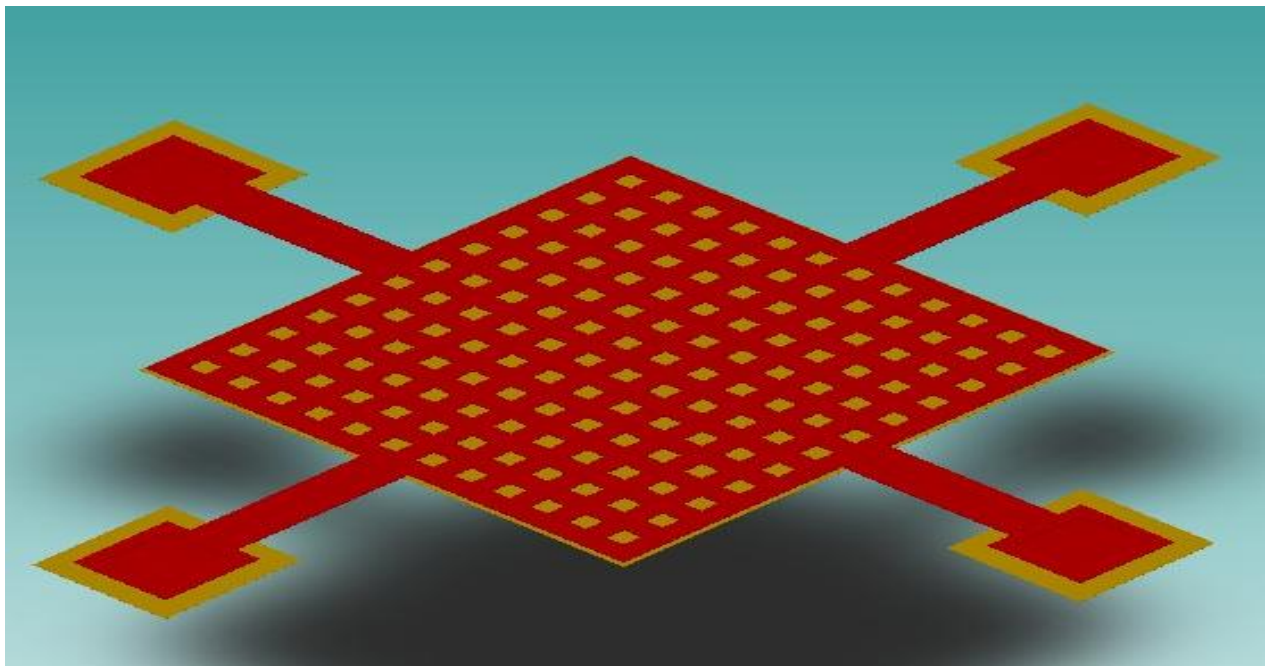


Figure 13. Design 2: a modified version of Design 1 with displaced support beams

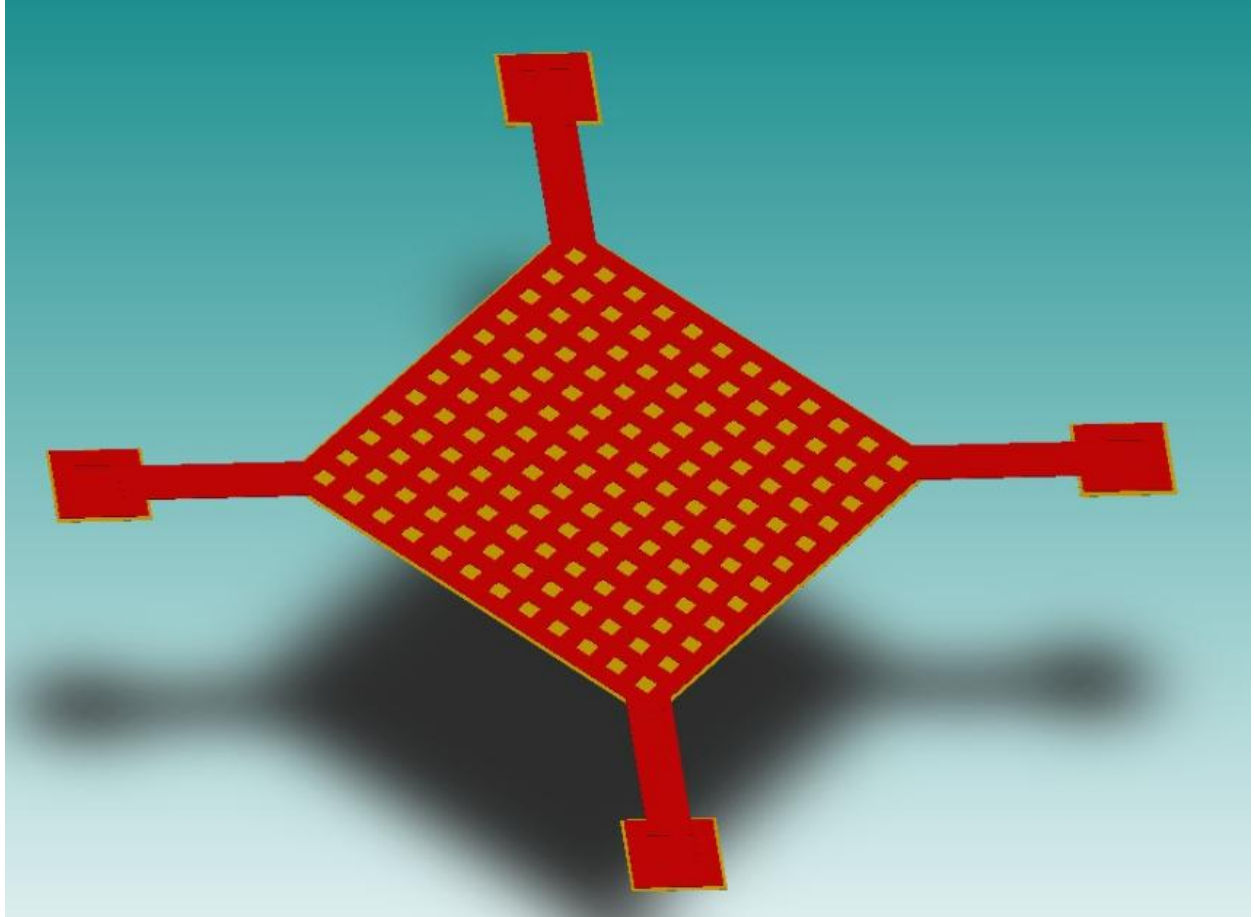


Figure 14. Design 3: a modified version of Design 1 with displaced support beams

Design 4 (Fig. 15) is not a simple square $700\text{ }\mu\text{m}$ by $700\text{ }\mu\text{m}$ actuator. As seen in Figure 15, it is of hexagonal shape with 3 support beams. To maintain consistency, the overlap area is remained as $700\text{ }\mu\text{m}$ by $700\text{ }\mu\text{m}$, however the dimensions are modified slightly. Each edge of the hexagon is $434.3\text{ }\mu\text{m}$. The support beams are $551.5\text{ }\mu\text{m}$ in length. The connector pads remain at $135\text{ }\mu\text{m}$ by $135\text{ }\mu\text{m}$. The holes are $25.56\text{ }\mu\text{m}$ by $25.56\text{ }\mu\text{m}$.

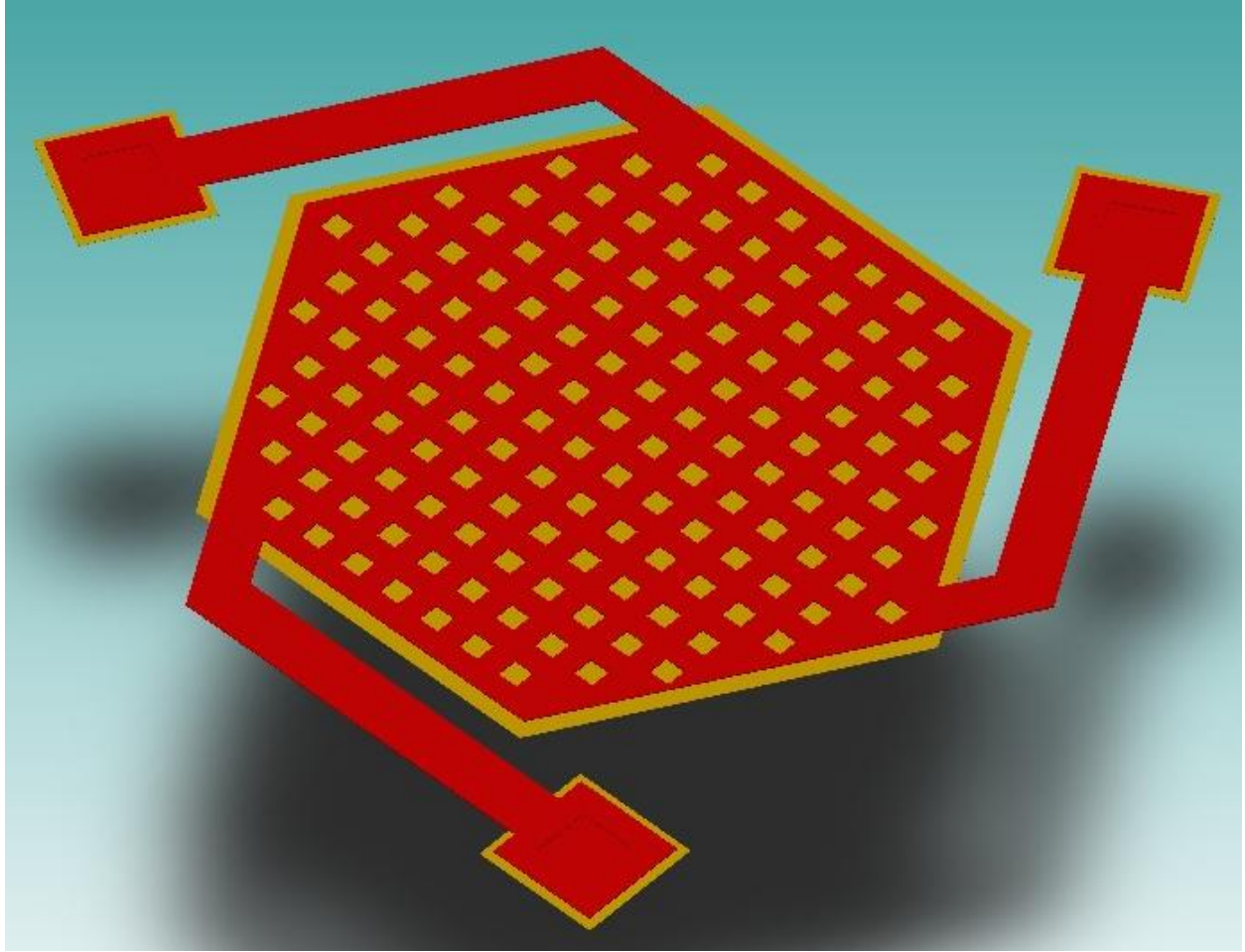


Figure 15. Design 4: Hexagonal plates and only 3 support beams

Design 5 (Fig. 16) is a combination of design 1 through 3 and 4 in the sense that it has a square top plate; however, the support beams are similar to that of design 4 in the sense that they form a 90 degree angle to each side of the plate and run parallel to the plate as opposed to perpendicular (or in the case of design 3, at a 45 degree angle). For Design 4, the length of the support beams is $620\text{ }\mu\text{m}$. The connector pads and holes have the same dimensions as Designs 1 through 4.

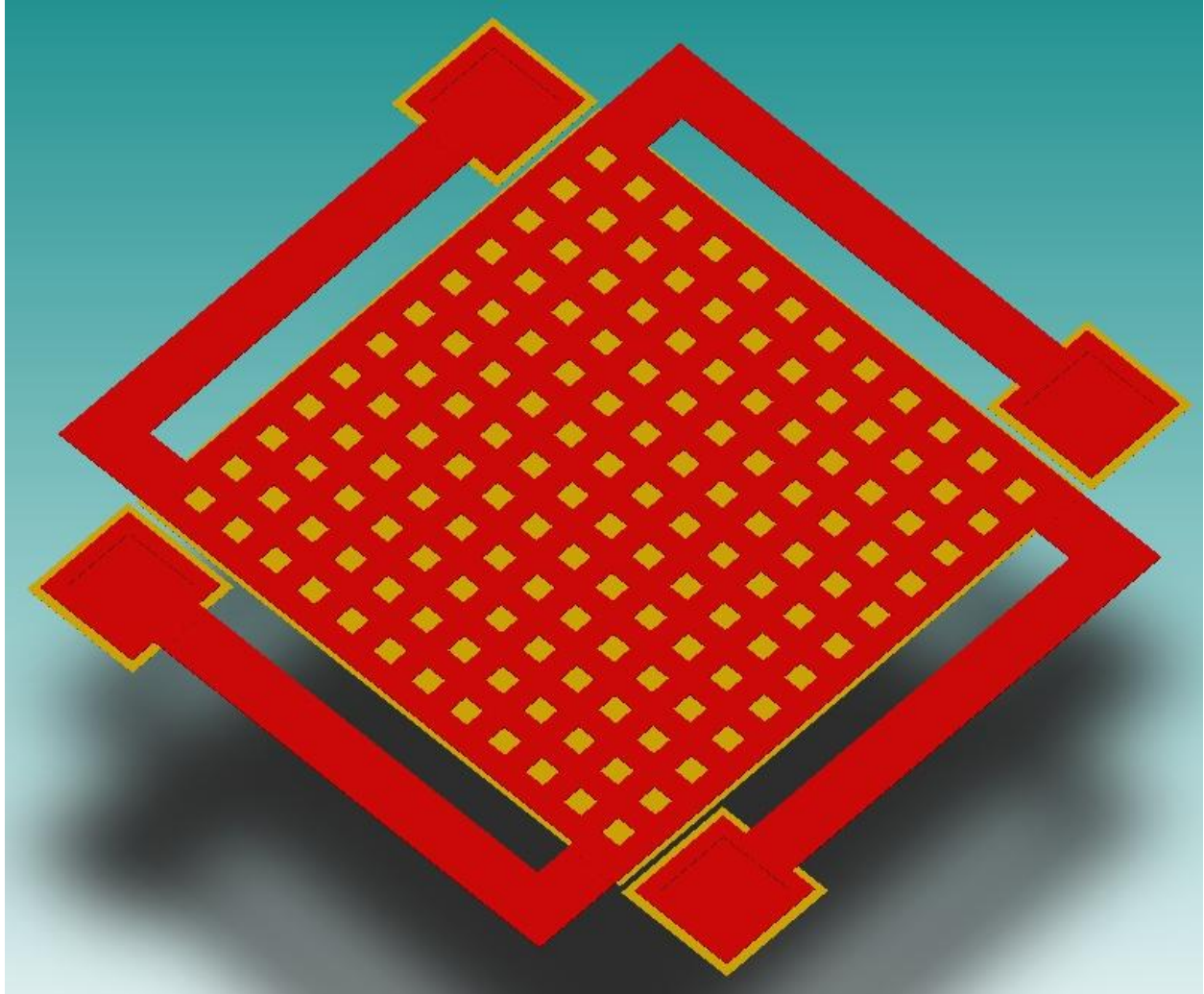


Figure 16. Design 5: A hybridization of Designs 1-4

3.4 Elements Used

For the Finite Element Analysis (FEA) two types of elements are used: Manhattan brick and tetrahedral elements. The Manhattan brick mesh option creates orthogonal or nearly orthogonal hexahedral, or brick, elements. The geometry is subdivided at concave intersections of faces and further subdivided using parallel planes or nearly parallel faces. These elements are best suited for orthogonal or near orthogonal geometry. Manhattan bricks can be linear or parabolic. Linear Manhattan bricks have two nodes along each edge, creating an 8-node

hexahedra (bricks). Parabolic Manhattan bricks have three nodes along each face, creating a 27 node hexahedra[12].

Tetrahedral elements are used when Manhattan brick meshing is impossible. The element order available is linear and parabolic. Linear tetrahedrons have two nodes along each edge, creating a four node tetrahedron. Parabolic tetrahedron elements have three nodes along each edge, creating a ten node tetrahedral element[12].

Chapter 4

4.1 Analysis

4.1.1 Static Analysis

For this section only the bending behaviour of the top plate of each design was examined. To remain consistent, 12.5V was used as the initial load; the same as Zhang and Fang[9] used in their Finite Element Analysis (FEA) of their design. However, instead of using ANSYS, a MEMS specific analyser, CoventorWare, was employed for all portions of the analysis with the exception of creating the 2D models. The models were created using AutoCAD 2008.

4.1.1.1 Design 1

As previously discussed, the first design is by Zhang and Fang[9]. The only exception is that PolyMUMPs process was used. For the mesh, Manhattan Brick elements were used with a size of 20 μm by 20 μm by 1 μm . This creates a relatively coarse mesh, however this was needed in order to reduce computational time during the simulation (Fig. 17).

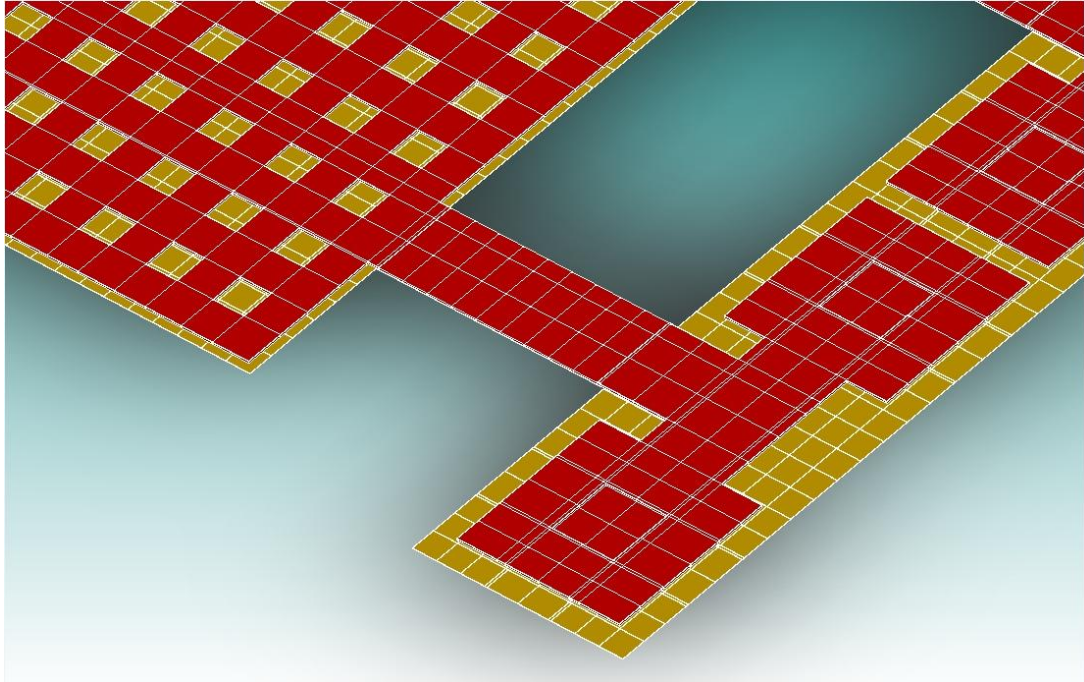


Figure 17. An illustration of the mesh used in Design 1

4.1.1.2 Design 2

Due to the similarities of Design 2 to Design 1, the same parameters are used for meshing (Fig. 18).

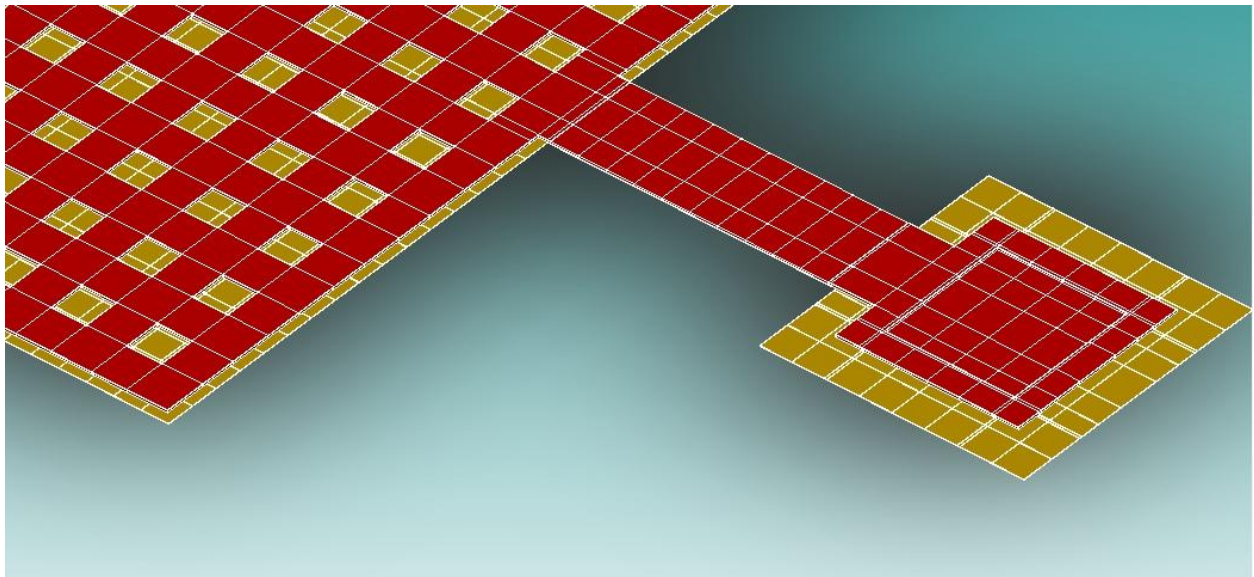


Figure 18. An illustration of the mesh used in Design 2

4.1.1.3 Design 3

Design 3 could not be meshed using Manhattan Brick elements due to the support beam placement, thus tetrahedral elements of size 20 were selected (Fig. 19). The same conductor boundary condition of 12.5V was used, the same as for Designs 1 and 2.

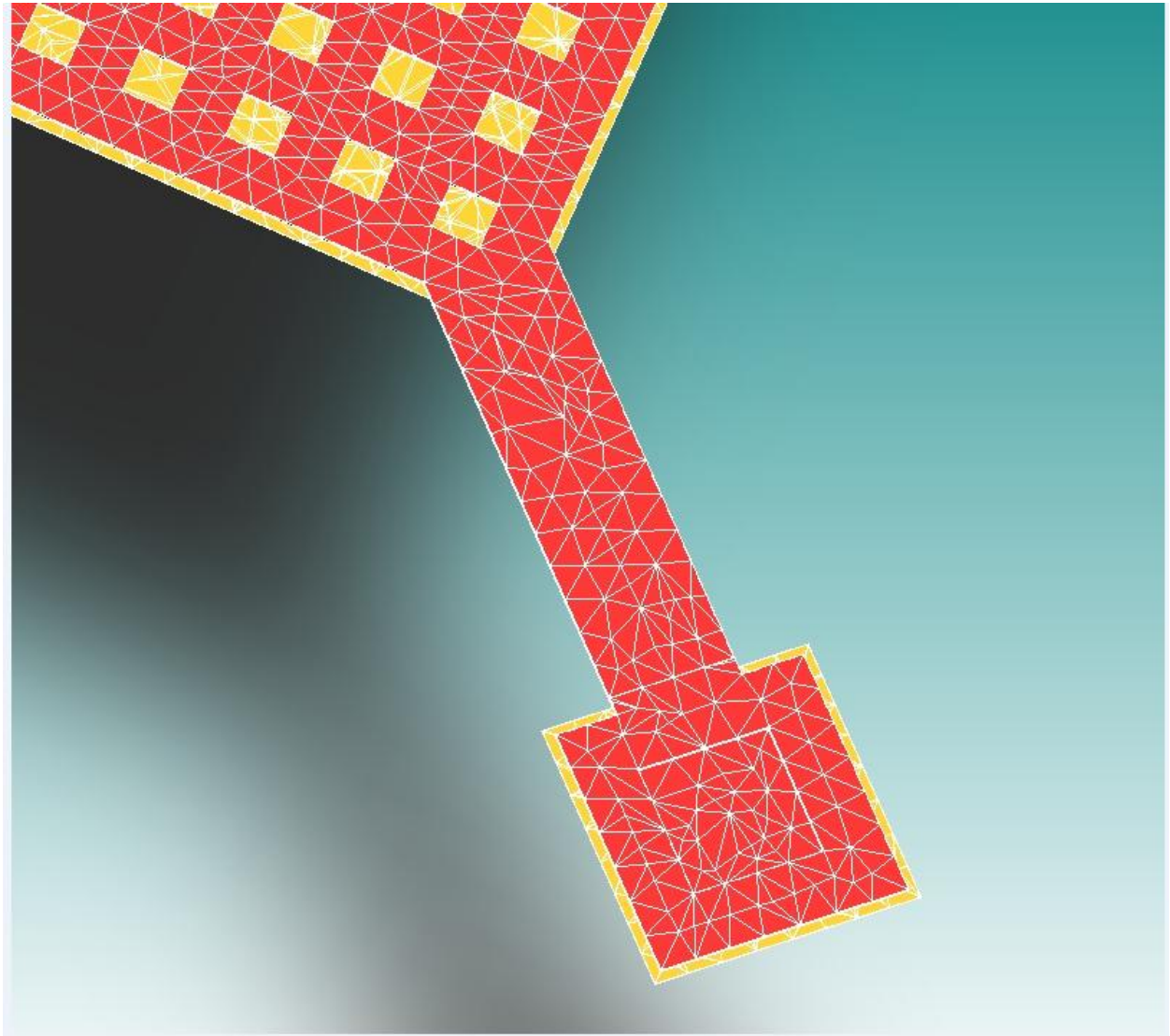


Figure 19. An illustration of the mesh used in Design 3

4.1.1.4 Design 4

Again, due to the unique geometry of this design, Manhattan Brick elements could not be used, and as a result the same parameters as Design 3 were chosen (Fig. 20).

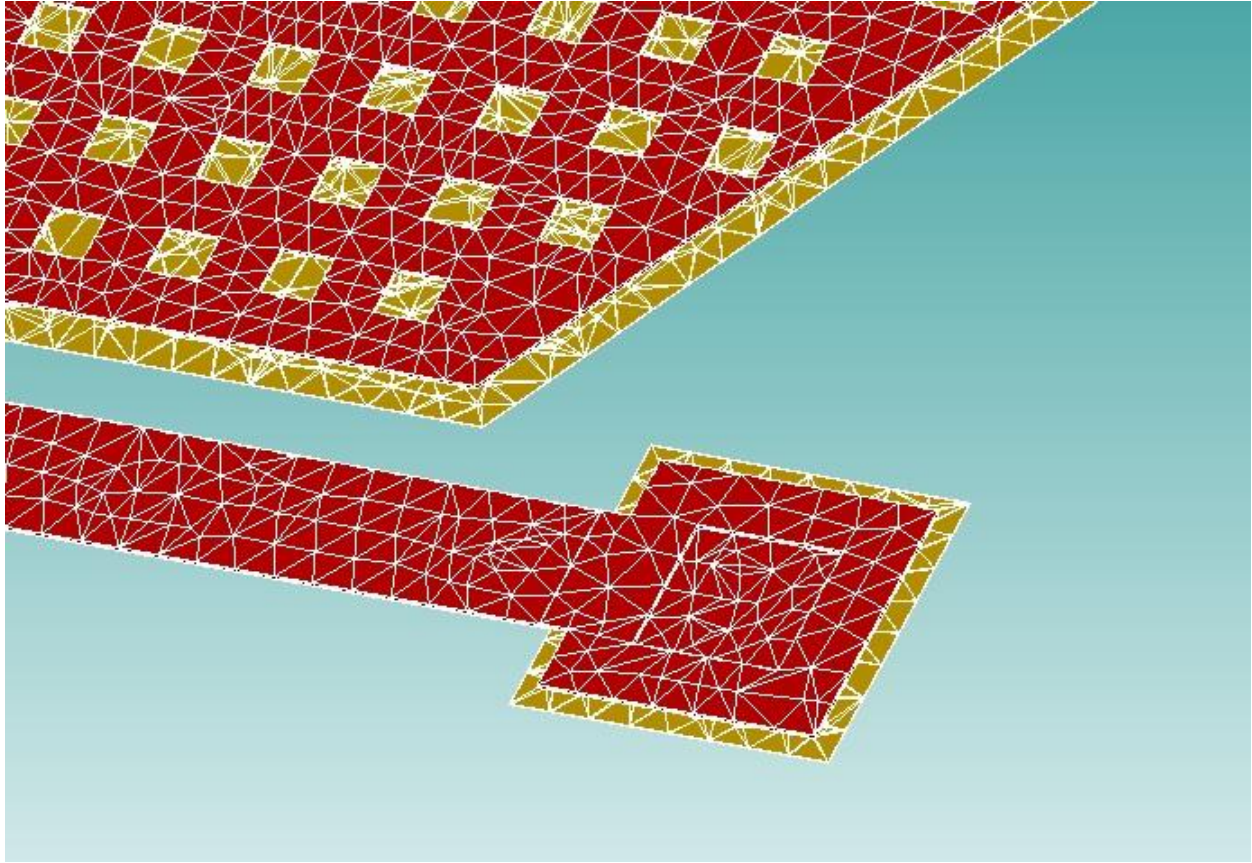


Figure 20. An illustration of the mesh used in Design 4

4.1.1.5 Design 5

The meshing for design 5 returns to Manhattan Bricks of size $20\text{ }\mu\text{m}$ by $20\text{ }\mu\text{m}$ by $1\text{ }\mu\text{m}$ (Fig. 21). Once again, the initial voltage boundary condition was set to 12.5V for consistency.

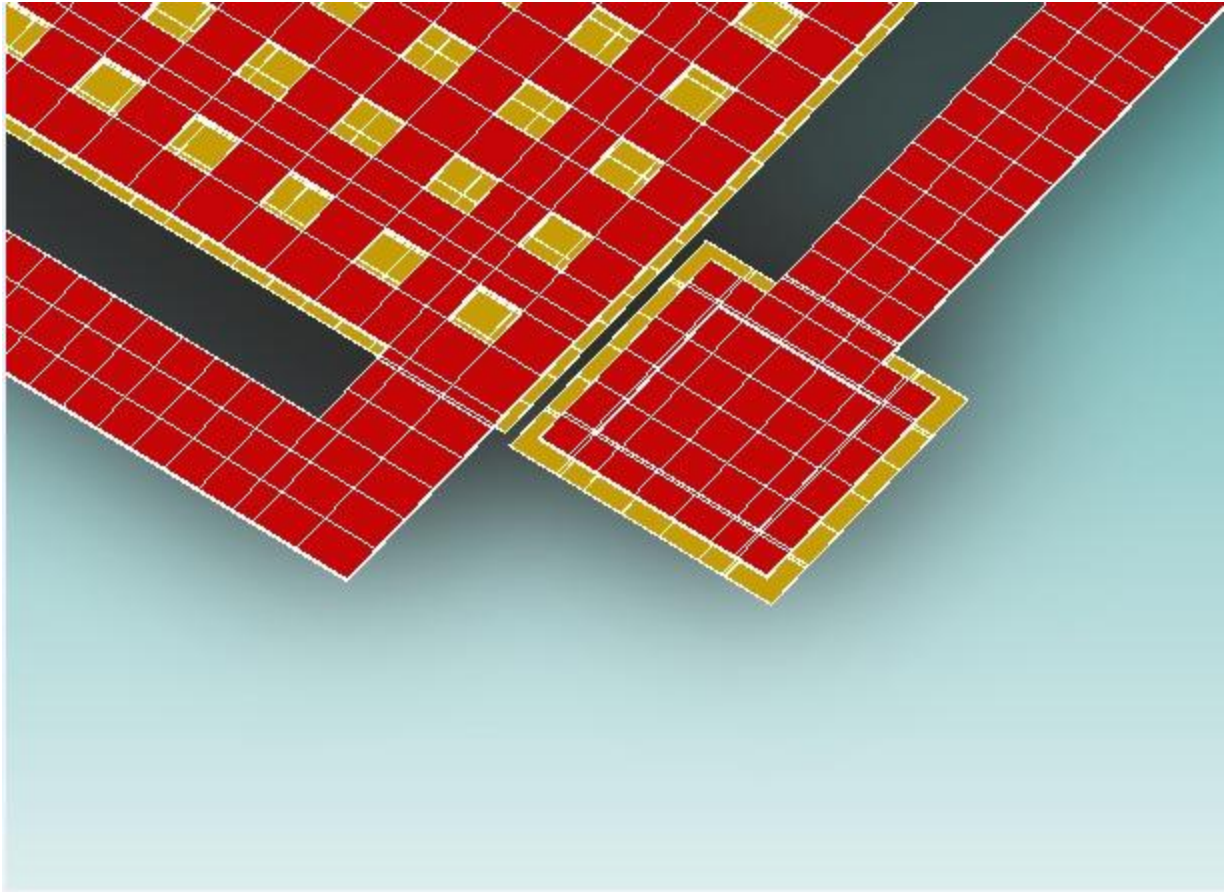


Figure 21. An illustration of the mesh used in Design 5

4.1.2 Static Analysis Results

It is immediately apparent that the voltage values used by Zhang and Fang[9] cannot be used for these designs when the manufacturing process is PolyMUMPs and the material is polysilicon; the maximum displacement of the moving plate is between $6.8\text{ }\mu\text{m}$ (Fig. 22) and $99\text{ }\mu\text{m}$ (Fig. 23). However, there is some consistency: Design 1 (Fig. 22) exhibits the same bending profile as shown in the simulations by Zhang and Fang[9] (Fig. 24). This allows Design 1 to be the control in this comparative analysis.

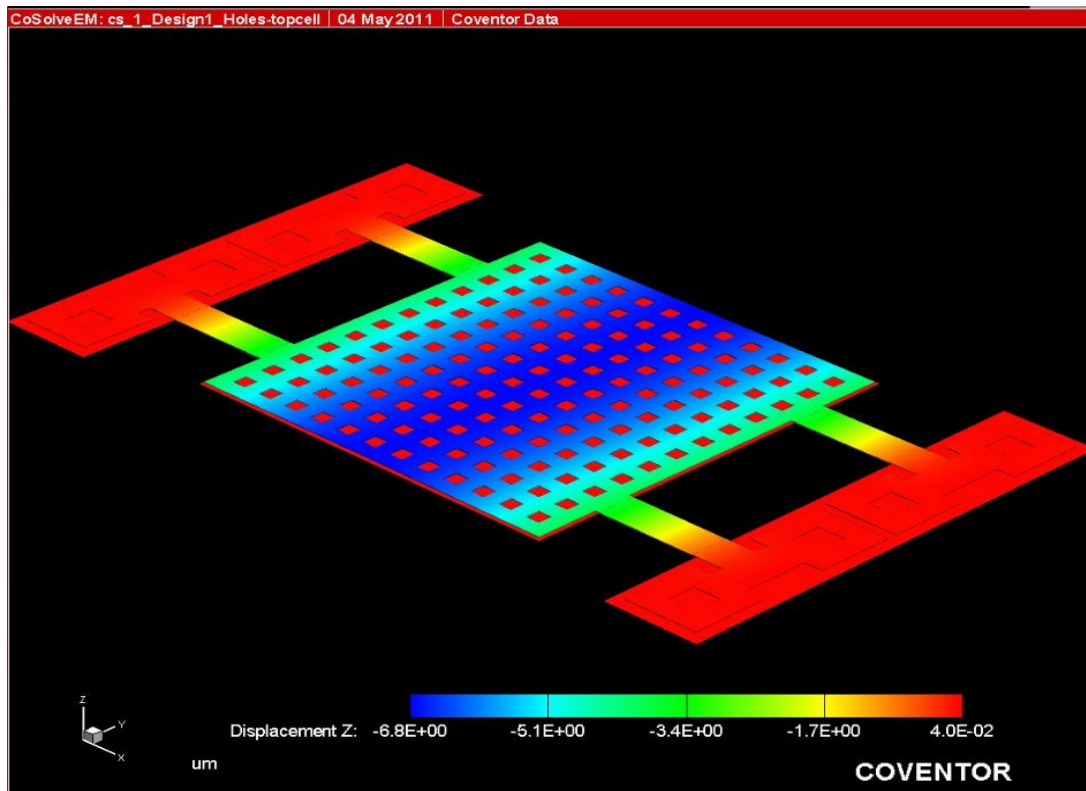


Figure 22. Design 1 Static Analysis under 12.5V Load

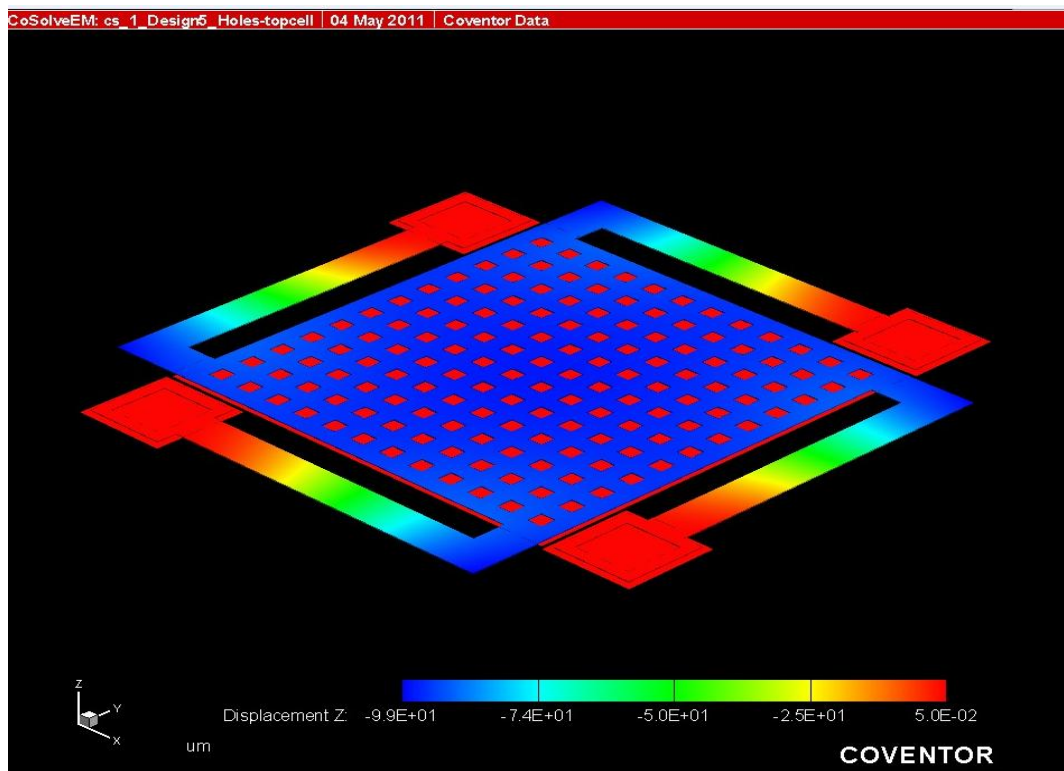


Figure 23. Design 5 Static Analysis under 12.5V Load

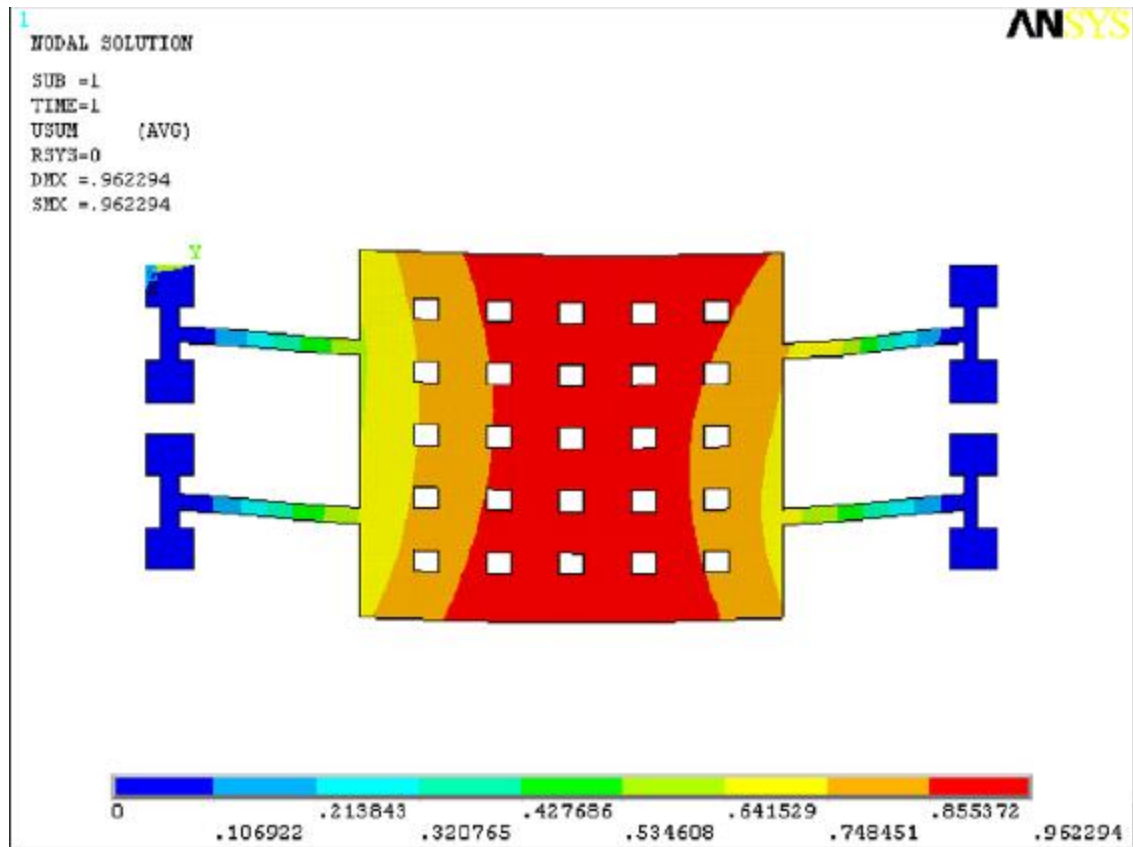


Figure 24. Zhang and Fang's Static Analysis under 12-13V load [9]

Based on the results of Design 1, the deformation shapes of the rest of the designs are expected to follow a similar pattern; greater deformation around the centre is due to the Designs having one support beam on each edge. This appears to hold true to Designs 2 (Fig. 25) and 3 (Fig. 26).

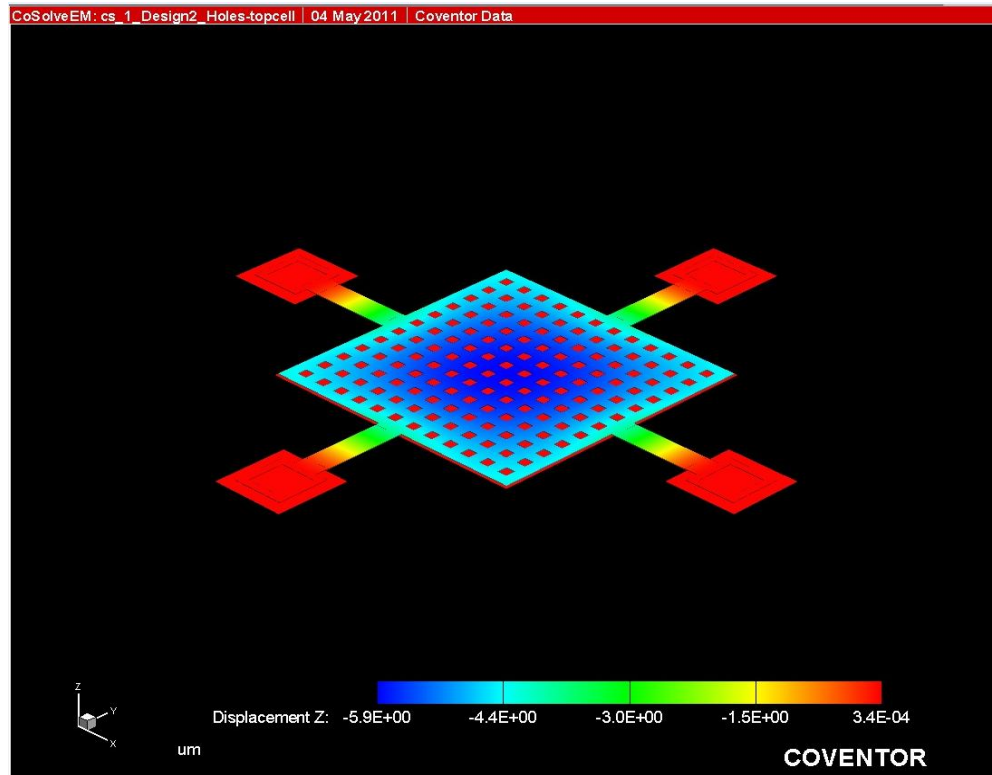


Figure 25. Design 2 Under 12.5V Load

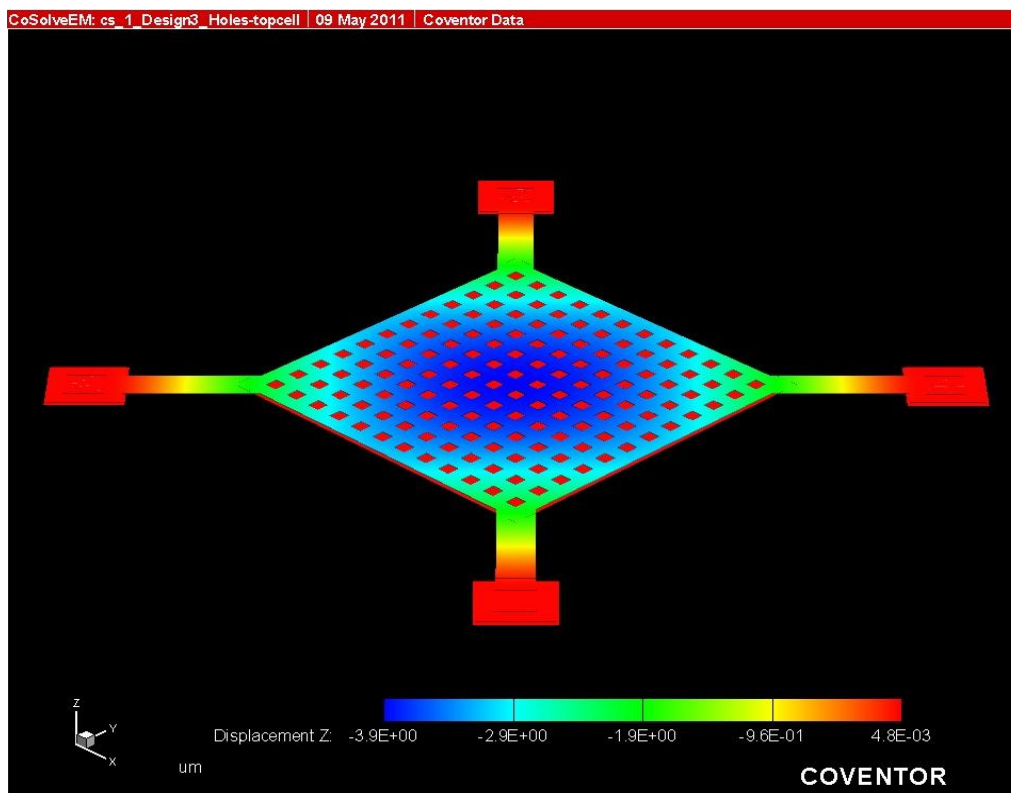


Figure 26. Design 3 Under 12.5V Load

Designs 4 and 5, however, do not follow this expected behaviour. Both Designs 4 (Fig. 27) and 5 (Fig. 23) have a uniform displacement about their moving plates with what appears to be little to no deformation under applied voltage. This is a very interesting result as it indicates that the placement and design of the support beam affect the way the moving plate deforms.

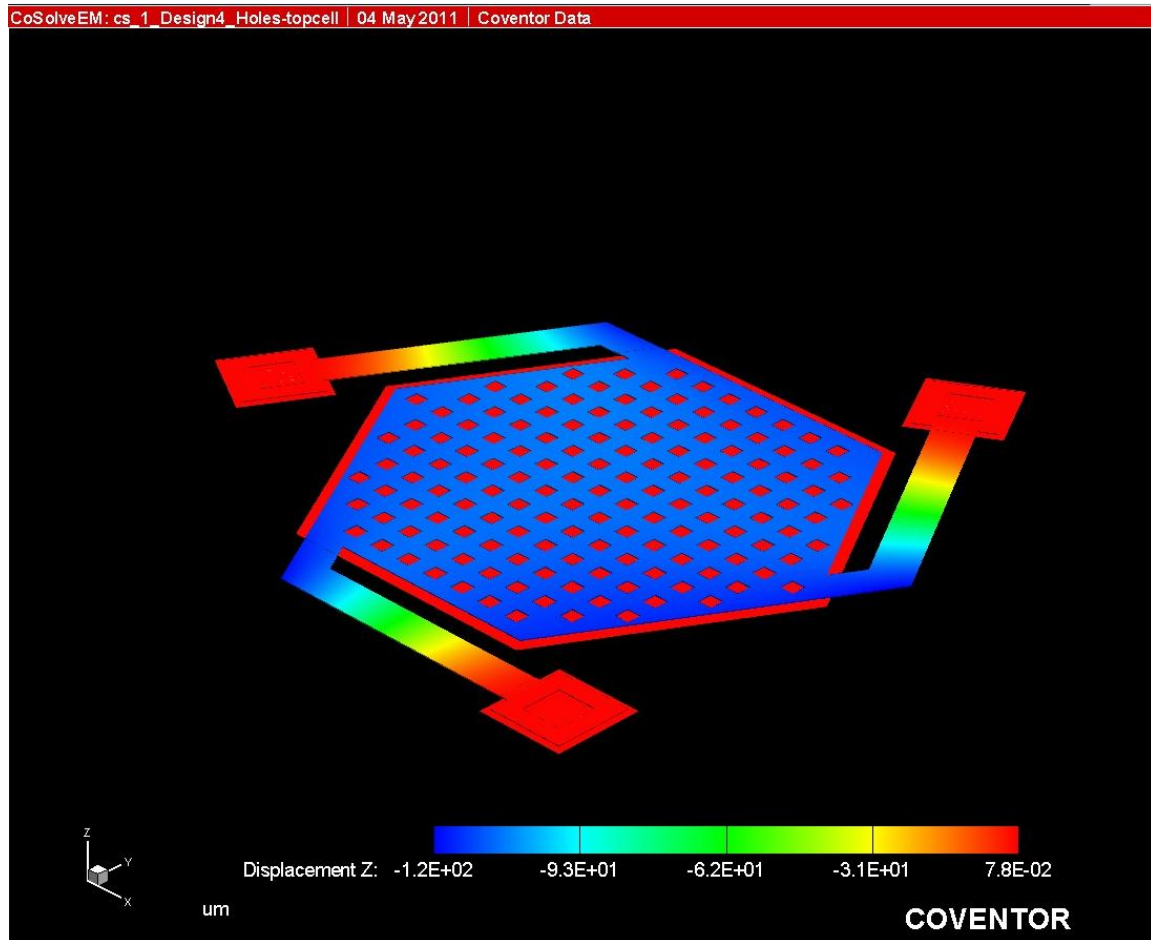


Figure 27. Design 4 Under 12.5V Load

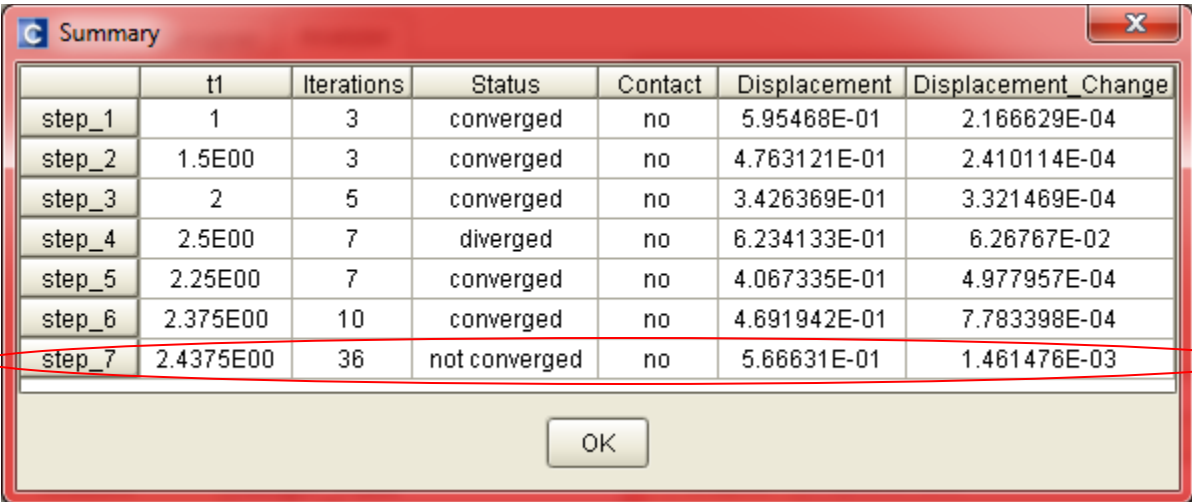
4.1.3 Pull-In Analysis

Using the static analysis it is possible to make a rough estimate for the pull-in voltages for each design. Given that under an applied voltage of 12.5V, the top plates maximum displacement was between 6.8 μm and 99 μm (far greater than the 2 μm air gap), it is safe to

assume that the voltage range is no more than 5V. Hence, the voltage range for the pull-in analysis was 1.0V to 5.0V with 0.5V increments. The pull-in tolerance – a setting required by the solver – is set to 0.1. The pull-in tolerance is used by the solver to determine when to stop the simulation; the simulation ends when the difference between the last convergent or non-convergent and divergent solutions is less than the pull-in tolerance.

4.1.3.1 Design 1 Results

The pull-in voltage for Design 1 predicted using CoventorWare is approximately 2.44V. The simulation neither converged nor diverged at this applied voltage (Fig. 28). CoventorWare treats "not converged" results the same as converged.



	t1	Iterations	Status	Contact	Displacement	Displacement_Change
step_1	1	3	converged	no	5.95468E-01	2.166629E-04
step_2	1.5E00	3	converged	no	4.763121E-01	2.410114E-04
step_3	2	5	converged	no	3.426369E-01	3.321469E-04
step_4	2.5E00	7	diverged	no	6.234133E-01	6.26767E-02
step_5	2.25E00	7	converged	no	4.067335E-01	4.977957E-04
step_6	2.375E00	10	converged	no	4.691942E-01	7.783398E-04
step_7	2.4375E00	36	not converged	no	5.66631E-01	1.461476E-03

Figure 28. Pull-In Simulation Results for Design 1

It is interesting to note that at pull-in voltage the moving plate of the capacitor is not deforming the way it deformed in the static analysis under voltages that exceeded the pull-in effect (Fig. 29). Only the edges where the support beams are attached to the moving plate approached the maximum displacement. At 2.44V, the top plate moved 0.57 μm (maximum displacement), or almost a third of the air gap between the two plates (approximately 0.67 μm), however the centre area of the moving plate displaced approximately 0.42 μm (Fig. 29).

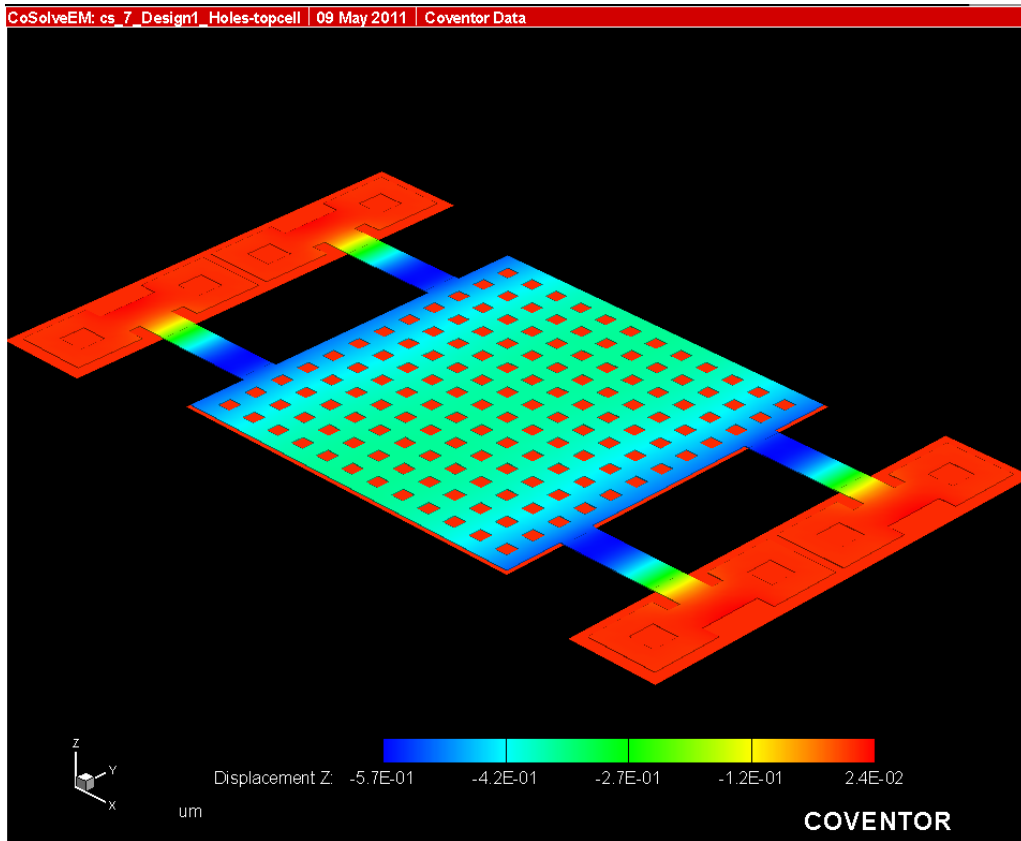


Figure 29. Design 1 Deformation at pull-in voltage

4.1.3.2 Design 2 Results

For this design, the pull-in voltage was determined to be 3.38V (Fig. 30) with, again, a maximum displacement of 0.57 μm (Fig. 31). For this applied voltage the simulation did converge, unlike Design 1. It is fascinating to note again, that the deformation is not as extreme as expected at the pull-in boundary, however there is slightly more deformation than in design 1. For design 2, only the corner edges of the moving plate deformed, as opposed to the beam placement edges. However, just like with design 1, the centre area of the moving plate does not reach the $1/3^{\text{rd}}$ distance. For 3.38V, the maximum displacement is calculated to be 0.57 μm , same as in Design 1, but the majority of the plate only reaches a displacement of approximately 0.24 μm (Fig. 31).

Summary						
	t1	Iterations	Status	Contact	Displacement	Displacement_Change
step_1	1	3	converged	no	7.740214E-01	2.962351E-05
step_2	1.5E00	2	converged	no	7.1648E-01	2.12431E-04
step_3	2	3	converged	no	6.27606E-01	1.393557E-04
step_4	2.5E00	4	converged	no	4.931849E-01	2.282858E-04
step_5	3	6	converged	no	3.048092E-01	4.74751E-04
step_6	3.5E00	5	diverged	no	6.97798E-01	7.960171E-02
step_7	3.25E00	9	converged	no	4.296033E-01	6.409734E-04
step_8	3.375E00	21	converged	no	5.751399E-01	9.984374E-04
step_9	3.4375E00	3	diverged	no	6.629873E-01	3.624025E-02

OK

Figure 30. Pull-In Simulation Results for Design 2

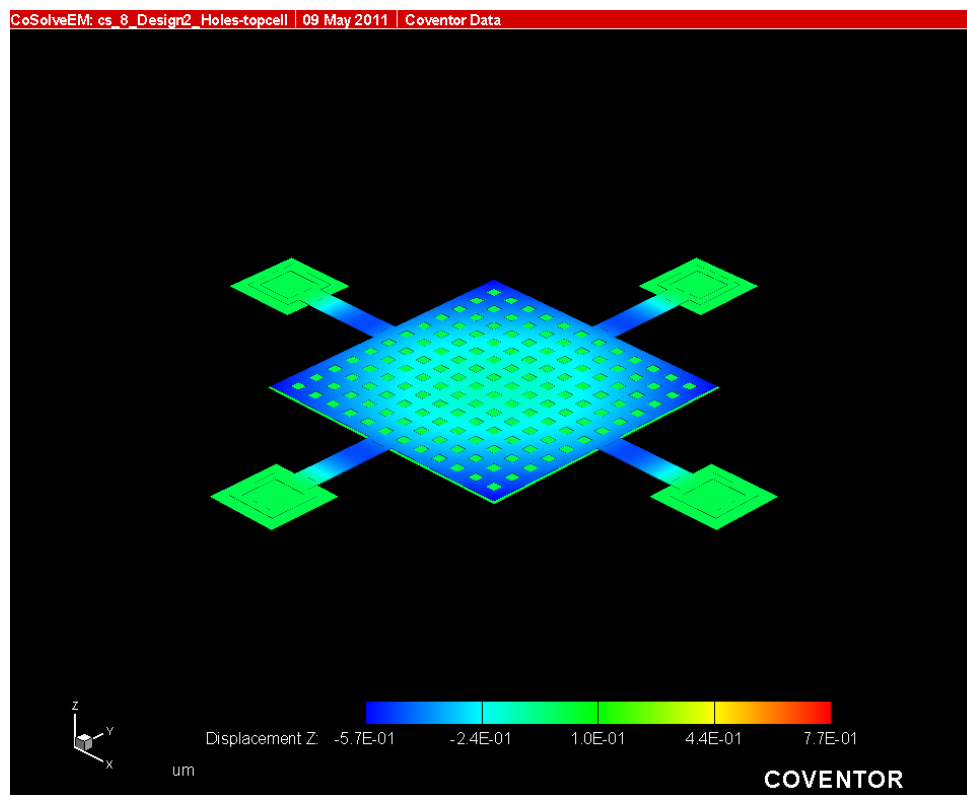


Figure 31. Design 2 Deformation at Pull-In Voltage

4.1.3.3 Design 3 Results

Unfortunately, the results for Design 3 do not appear to be correct. The top plate is being repelled from the bottom plate as opposed to being attracted. Several voltage ranges were used, however each time the results remained the same (Fig. 32). Hence, Design 3 will be ignored in the overall conclusion.

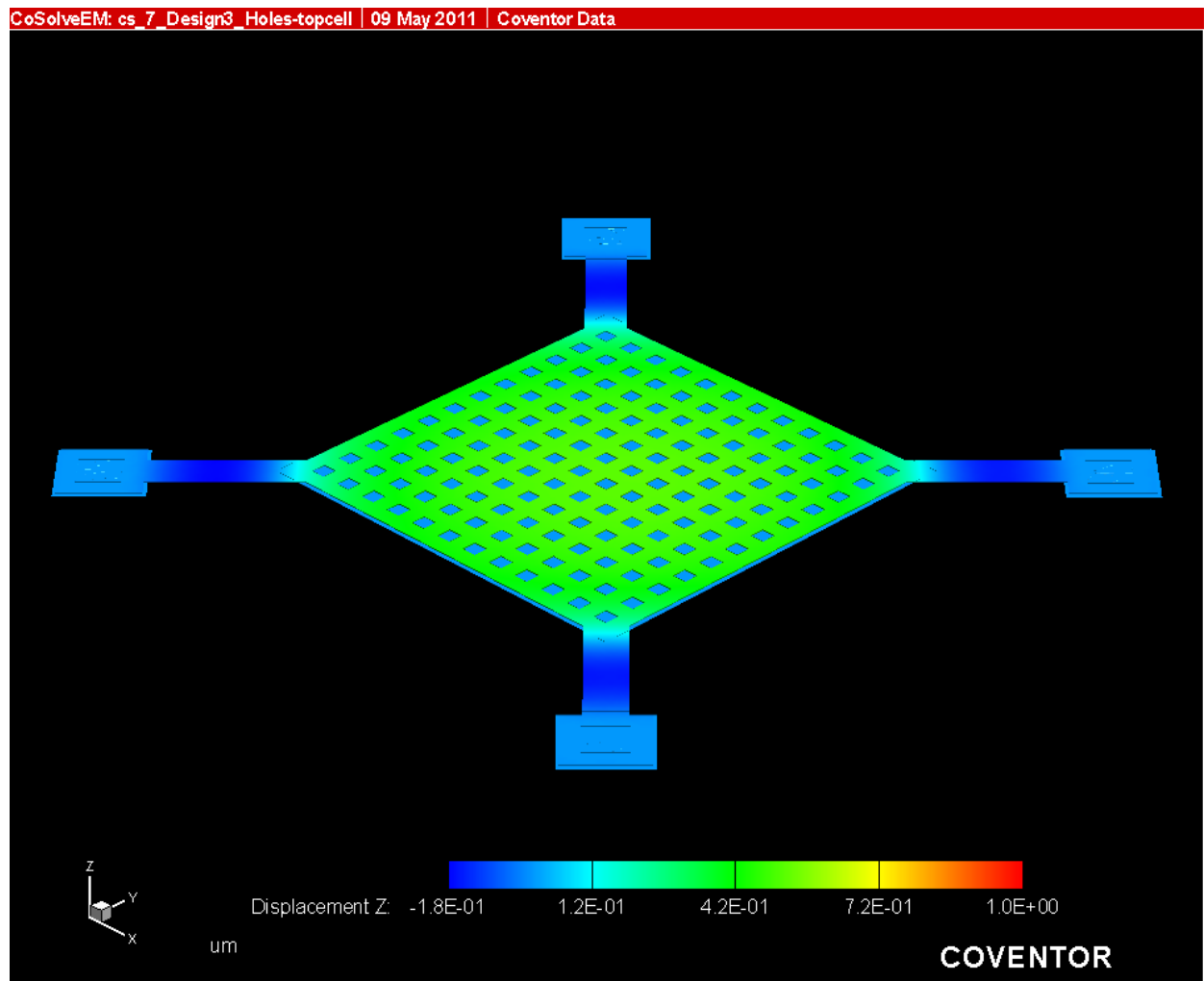
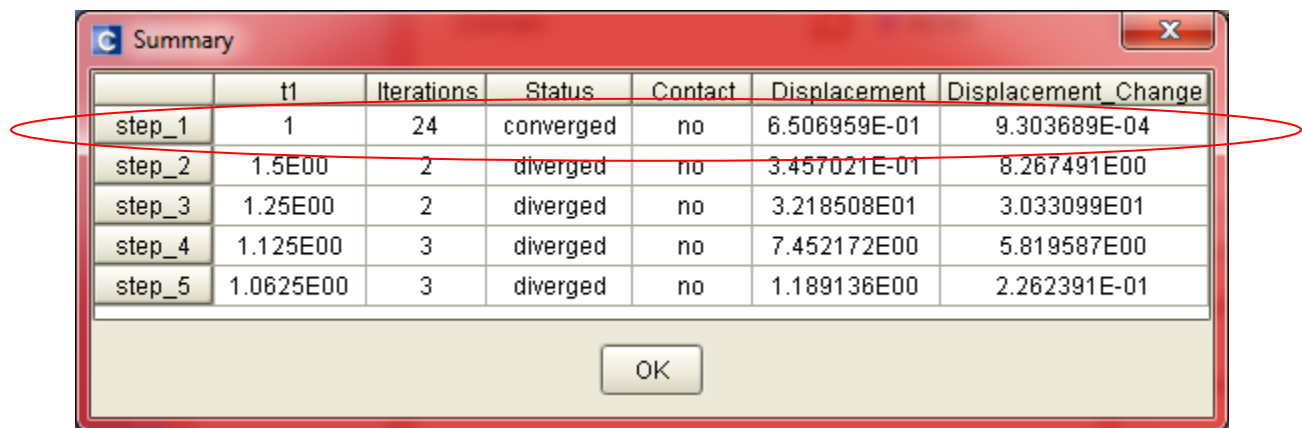


Figure 32. Design 3 Pull-In Deformation

4.1.3.4 Design 4 Results

For this design, the pull-in voltage was determined to be 1.0V (Fig. 33) with a maximum displacement of 0.65 μm (Fig. 34). Interestingly enough, just like the static analysis, the

deformation of the top plate is uniform throughout. It is an indication that the design of the plate, the design of the support beams, or the combination of the two affects how the moving plate deforms. In addition, this is the first example of the top plate approaching the estimated pull-in distance of $1/3^{\text{rd}}$ of the gap throughout. Finally, this result shows that by altering the design of the capacitor, greater displacement can be achieved at lower voltages.



	t1	Iterations	Status	Contact	Displacement	Displacement_Change
step_1	1	24	converged	no	6.506959E-01	9.303689E-04
step_2	1.5E00	2	diverged	no	3.457021E-01	8.267491E00
step_3	1.25E00	2	diverged	no	3.218508E01	3.033099E01
step_4	1.125E00	3	diverged	no	7.452172E00	5.819587E00
step_5	1.0625E00	3	diverged	no	1.189136E00	2.262391E-01

Figure 33. Pull-In Simulation Results for Design 4

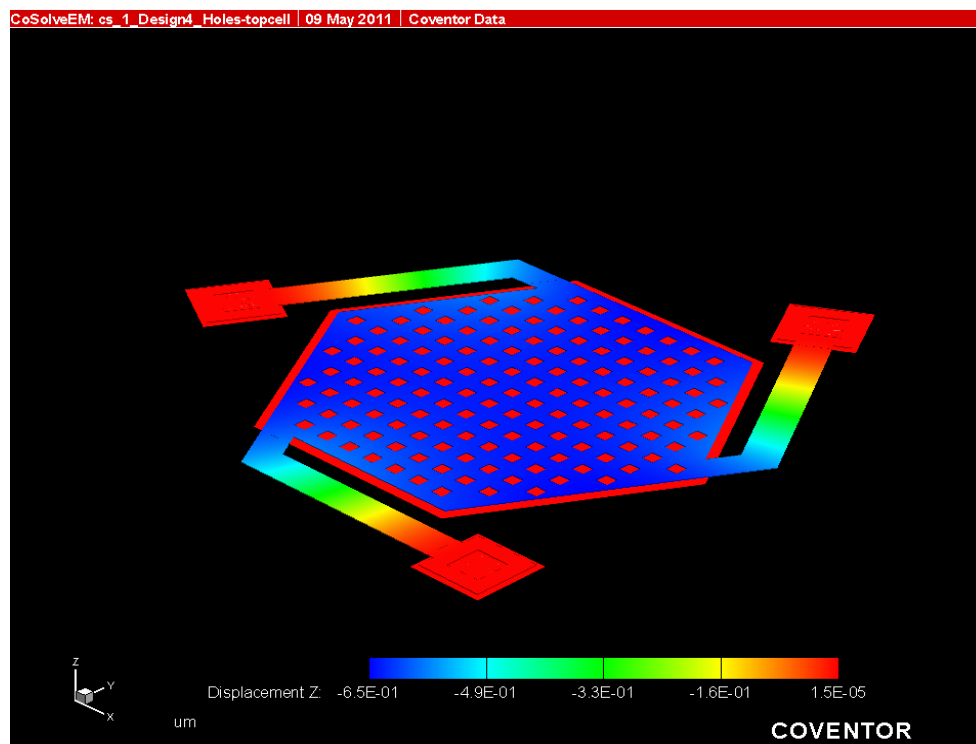
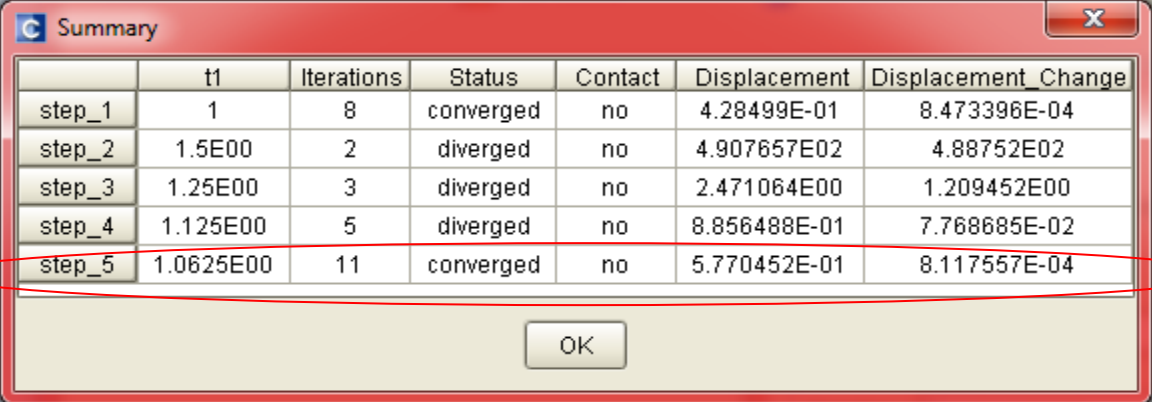


Figure 34. Design 4 Pull-In Deformation

4.1.3.5 Design 5 Results

For this design the pull-in voltage was determined to be 1.06V (Fig. 35) with a maximum displacement of 0.58 μm (Fig. 36). Just like for design 4, the top plate deformation is uniform throughout, which confirms the importance of the design of the support beams as conjectured in section 4.1.3.4.



	t1	Iterations	Status	Contact	Displacement	Displacement_Change
step_1	1	8	converged	no	4.28499E-01	8.473396E-04
step_2	1.5E00	2	diverged	no	4.907657E02	4.88752E02
step_3	1.25E00	3	diverged	no	2.471064E00	1.209452E00
step_4	1.125E00	5	diverged	no	8.856488E-01	7.768685E-02
step_5	1.0625E00	11	converged	no	5.770452E-01	8.117557E-04

Figure 35. Pull-In Simulation Results for Design 5

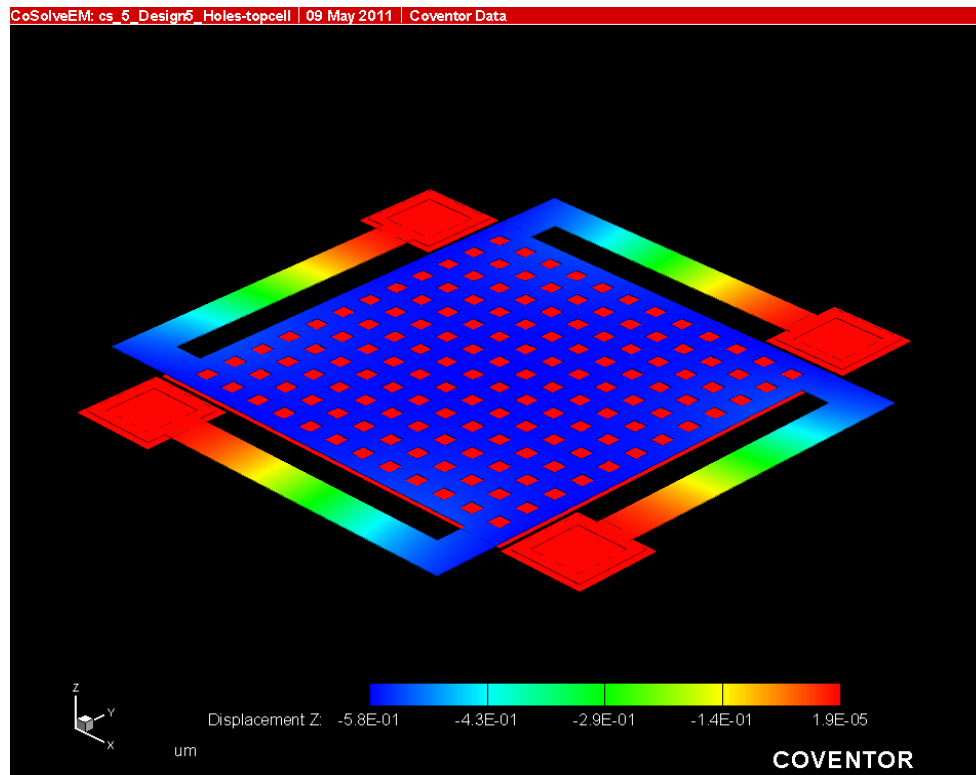


Figure 36. Design 5 Pull-In Deformation

Chapter 5

5.1 Conclusions

It is evident from Designs 1 and 2 and to a lesser extent Design 3, that deformation when voltage is applied can be a serious concern and that pull-in voltage and distance estimates cannot always be as accurate as desired. However, Designs 4 and 5 show that the effect can be ameliorated. For example, Changing the shape and length, not the position, of the support beam provides a more uniform motion of the moving plate and very little deformation, thus allowing for the relatively simplistic approximation to be very effective. This however, adds additional stress onto the support beams and makes the overall structure less stiff.

Designs 4 and 5 offer other advantages as well. Firstly, Designs 4 and 5 generate the same displacement as Designs 1 and 2, but with a significantly smaller applied voltage; an average voltage of 1.03V for Designs 3 and 4 versus 2.91V for Designs 1 and 2. Given the applications involving parallel plate, energy consumption is always an issue.

Secondly, Designs 4 and 5 are relatively more compact than Designs 1, 2 and 3. Design 1 is 1399 μm across. Design 2 is 1466 μm across. Design 3 is 1687.9 μm diagonally. While Design 4 is 1193.07 μm (distance between two furthest points) and design 5 is 1013 μm across. This not only uses less material but speeds up the manufacturing process and allows for more devices to be micro-machined on the same wafer.

Finally, as previously mentioned, Designs 4 and 5 do not require any modification to the pull-in distance and voltage equations. This allows for easy computation of these properties

without using any significant amount of computational power which is an ever important resource.

5.2 Future Work

Further work can be done on this topic. Firstly, the 5 designs can be made more consistent with each other; the support beams for Designs 4 and 5 are significantly longer than those of Designs 1, 2 and 3 as well as Design 4 having only three beams. As such the end results of this paper are skewed.

Secondly, stresses can be investigated and the advantages and disadvantages of applying more stress on the support beams as opposed to the moving plate. This investigation may provide insight on long term or heavy use effects of these actuators.

References:

- [1] R. Sattler, P. Voigt, H. Pradel, G. Wachutka, Innovative design and modelling of a micromechanical relay with electrostatic actuation, *J. Mciromech. Microeng.* 11 (2001) 428–433.
- [2] J.-M. Huang, A.Q. Liu, Z.L. Deng, Q.X. Zhang, J. Ahna, A. Asundi, An approach to the coupling effect between torsion and bending for electrostatic torsional micromirrors, *Sens. Actuat. A* 115 (2004) 159–167.
- [3] J.Q. Mou, Y. Lu, J.P. Yang, Q.H. Li, G.X. Guo, Design fabrication and characterization of single crystal silicon microactuator for hard disk drives, *J. Mciromech. Microeng.* 14 (2004) 1608–1613.
- [4] X. Rottenberg, S. Brebels, W. DeRaedt, B. Nauwelaers, H.A.C. Tilmans, RF-power: driver for electrostatic RF-MEMS devices, *J. Mciromech. Microeng.* 14 (2004) S43–S48.
- [5] A.P. Lee, C.F. McConaghy, G. Sommargren, P. Krulevitch, E.W. Campbell, Vertical-actuated electrostatic comb drive with in situ capacitive position correction for application in phase shifting diffraction interferometry, *J. Microelectromech. Syst.* 12 (2003) 960–971.
- [6] A. Dec, K. Suyama, Microwave MEMS-based voltage-controlled oscillators, *IEEE Trans. Microwave Theory Technol.* 48 (2000) 1943–1949.
- [7] Y. Ahn, H. Guckel, J.D. Zook, Capacitive microbeam resonator design, *J. Mciromech. Microeng.* 11 (2001) 70–80.
- [8] Mirasol: <http://www.mirasoldisplays.com/how-it-works> (May, 2011)
- [9] B. Zhang, D. Fang, Modeling and modification of the parallel plate variable MEMS capacitors considering deformation issues, *Mechanism and Machine Theory* (2008) 647–655
- [10] Why is the Texas Instruments Digital Micromirror Device™ (DMD™) so reliable?, http://clifton.mech.northwestern.edu/~me381/papers/intro/ti_micromirror3.pdf (May, 2011)
- [11] J. Carter, A. Cowen, B. Hardy, R. Mahadevan, M. Stonefield, S. Wilcenski. *PolyMUMPs Design Handbook*, MEMSCAP Inc. (2005).
- [12] CoventorWare 2010 Master Help File.
- [13] F. P. Beer, E. R. Johnston Jr., *Method of Virtual Work, Vector Mechanics for Engineers* (1998) 536–543.
- [14] S. He, ME8146 - Microelectromechanical Systems lecture notes, Ryerson University (2010)