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Abstract

This dissertation is dedicated to the development of reliable, practical and cost-effective solutions to the issues caused by CMVs in power converter systems. A novel integrated ac choke which incorporates the differential-mode (DM) filtering and common-mode (CM) suppression functions, and new modulation techniques for current-source converters (CSCs) are presented.

The CMVs are divided into three frequency ranges: 1) the low frequency range with triplen harmonics, 2) the medium frequency range referring to the switching frequency and sidebands of its integral multiples, and 3) the high EMI frequency range. In voltage-source converters (VSCs), CMVs are mainly distributed in the medium frequency range, and no low-frequency CMV component is produced by sinusoidal pulse-width modulation (SPWM). This is favorable for the passive filter and CM choke design. The CMVs in CSC-based drives are dominant in the low

frequency range. Under normal operating conditions, space vector modulation (SVM) generates a larger CMV magnitude than other modulation schemes in CSCs.

A three-phase integrated choke is proposed to suppress the CMV in the medium frequency range in VSC systems. Different magnetic paths for the CM and DM fluxes generate the required high CM-to-DM inductance ratio. The magnetic integration brings great benefits in savings of iron and copper materials, reduction of weight and cost, and improvement in efficiency. The finite element analysis and experiment of a prototype are carried out for verification.

Transformerless photovoltaic inverters and neutral-connected motor drives are identified as applications of the integrated choke. Appropriate system grounding and filter components, e.g. CM capacitors and damping resistors, are employed for coordination. The CM behaviors are explained by circuit modeling. With evaluated parameters, simulations of the VSC systems using the proposed choke are conducted, verifying the analysis of the CM voltage/current mitigation effect.

Modified SVM techniques that avoid zero states are adapted for use in CSCs to decrease the CMV magnitude. The nearest-three-state methods present superior harmonic performances with a high modulation index and no increase in the switching frequency. For a lower modulation index, the combined active-zero-state technique can be implemented as compensation. The proposed modulation schemes are supported by both simulation and experimental results.

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a	Width of the ring core
A_b	Cross-sectional area of the bridge legs
A_c	Cross-sectional area of the circular core
A_t	Total surface area of the choke
A_w	Cross-sectional area of the wire
b	Width of the bridge legs
B_{cm,c_peak}	Peak value of the common-mode flux density in the circular core
B_{dm,c_peak}	Peak value of the differential-mode flux density in the circular core
B_{sat}	Flux density saturation
C_{ag}, C_{bg}, C_{cg}	Stray capacitances between the inverter output terminals and the ground
$C_{b\text{-}DE}$, $C_{b\text{-}NDE}$	Parasitic capacitances of the lubricant grease films at the drive- and nondrive-end bearings
C_{cm}	Common-mode capacitor
$C_{cm\text{-}lf}$	Line-side filter common-mode capacitor
$C_{cm\text{-}mf}$	Motor-side filter common-mode capacitor
$C_{cm\text{-}n}$	common-mode capacitor on the neutral line
C_d	DC-link capacitor
C_{Df}	Differential-mode filter capacitor
C_E	Parasitic capacitance of PV panels to the ground
C_f	Filter capacitor
$C_{f\text{-}EMI}$	EMI filter capacitor

$C_{gf\text{-}Y}$	Y-connected filter capacitor on the generator side of a drive system on More-Electric Aircrafts
C_{lf}	Line-side harmonic filter capacitor
C_{mf}	Motor-side filter capacitor
$C_{mf\text{-}Y}$	Y-connected filter capacitor on the motor side of a drive system on More-Electric Aircrafts
C_{mg}	Lumped stray capacitor of the motor model with respect to the ground
C_{rg}	Parasitic capacitance between the rotor and the grounded frame
C_{sg}	Parasitic capacitance between the stator windings and the grounded frame
C_{sr}	Parasitic capacitance between the stator windings and the rotor
C_{tg}	Intrinsic winding-to-ground capacitance of the transformer
dv/dt	Rate of voltage change
e_{ug}, e_{vg}, e_{wg}	Three-phase voltages of the supply
f_1	Line-side fundamental frequency
f_m	Inverter output frequency
f_{sp}	Sampling frequency
f_{sw}	Switching frequency
i_1, i_2	Each-line current of a two-wire cable
i_a, i_b, i_c	Three-phase currents flowing out from the inverter
$I_{ac,peak}$	AC peak current
$i_{b\text{-}DE}$, $i_{b\text{-}NDE}$	Bearing currents at the drive and nondrive end
i_c	Capacitor current
i_{cm}	Common-mode current
$i_{cm\text{-}grid}$	Common-mode current flowing into the grid
i_d	DC current (without consideration of the common-mode current)

I_{dc}	DC source current
$i_{dc\text{-}p}$, $i_{dc\text{-}n}$	DC-link currents on the positive and negative rails
i_{dm}	Differential-mode current
i_E	Currents leaking from the PV parasitic capacitance
i_g	Total ground leakage current of a motor
I_{ref}	Current reference in SVM synthesis
i_{rg}	Ground leakage current from the rotor
i_{sa}	Load current (phase *a*) of a current-source inverter
i_{sg}	Ground leakage current from the stator
i_u, i_v, i_w	Three-phase currents flowing in the rectifier
I_w	RMS value of PWM current in a current-source inverter
i_{wa}, i_{wb}, i_{wc}	Three-phase PWM currents of a current-source inverter
J	Current density
l_b	Length of the bridge legs
l_c	Mean circumference of the circular core
$L_{cm,ep}$	Each-phase common-mode inductance
$L_{cm,w}$	Whole common-mode inductance
L_d	DC-link inductor
L_{Df}	Differential-mode filter inductor
L_{dm}	Differential-mode inductance
L_{dp}, L_{dn}	DC-link inductors on the positive and negative rails
L_f	Filter inductor
$L_{f\text{-}EMI}$	EMI filter inductor
l_g	Air-gap length

L_g	CM inductance between the ground connections of the PV inverter and the ground
L_L	Three-phase load inductor
L_{lf}	Line-side harmonic filter inductor
L_{mf}	Motor-side filter inductor
m_a	Amplitude modulation index
m_f	Frequency modulation index
MLT	Mean length per turn
N	Number of turns
Ni_A, Ni_B, Ni_C	Three-phase magnetomotive forces
P_{cu}	Copper loss
$P_{fe,cm}$	Common-mode core loss
$P_{fe,dm}$	Differential-mode core loss
$P_{fe,total}$	Total core loss
r	Inner radius of the ring core
R_c	Equivalent parallel resistance caused by the core loss of the integrated choke
R_d	DC load resistance
$R_{d\text{-}mf}$	Damping resistor in the motor-side filter
R_L	Three-phase load resistance
s_a, s_b, s_c	Binary-logic switching function of the inverter
SF	Stacking factor of laminations
s_u, s_v, s_w	Binary-logic switching function of the rectifier
SW_1, SW_2	Switches to interpret the occurrence of the dielectric breakdown of lubricant films

T_0, T_1, T_2,…	Dwell times for the current vectors
T_r	Temperature rising
T_s	Sampling period of SVM
v_{1G}, v_{2G}	Voltages of two power lines with respect to the common ground
v_{1g}, v_{2g}	Voltages of positive and negative dc points 1 and 2 on the rectifier side to the ground
v_{31}, v_{42}	Voltage drops on the positive and negative dc reactors
v_{3o}, v_{4o}	Voltages of positive and negative dc points 3 and 4 on the inverter side to the three-phase load neutral point
v_{ab}	Phase-to-phase voltage (between phase *a* and phase *b*)
v_{ag}	Phase-to-ground voltage (phase *a*)
v_{ao}	Phase-to-neutral voltage (phase *a*)
v_{az}, v_{bz}, v_{cz}	Output voltages of the inverter with respect to its dc-link midpoint
v_b	Shaft-to-frame voltage of a motor or bearing voltage
v_{cm}	Common-mode voltage
$v_{cm\text{-}drive}$	Common-mode voltage generated by the drive
$v_{cm\text{-}inv}$	Common-mode voltage of the inverter
$v_{cm\text{-}L}$	Common-mode voltage drop on the integrated choke
$v_{cm\text{-}m}$	Common-mode voltage imposed on motor terminals
$v_{cm\text{-}rec}$	Common-mode voltage of the rectifier
$v_{cm\text{-}sys}$	System common-mode voltage
v_{dc}	DC-link voltage
v_{dm}	Differential-mode voltage
v_g	Phase voltage of the power supply
V_g	RMS value of the power supply phase voltage

v_{og}	Voltage between the load neutral point and the ground
v_{oz}	Voltage between the load neutral point and the dc-link midpoint
v_s	Output voltage of a current-source inverter
V_s	RMS value of the output voltage of a current-source inverter
v_{uz}, v_{vz}, v_{wz}	AC voltages of the rectifier with respect to the dc-link midpoint
v_{zg}	Voltage between the dc-link midpoint and the ground
w	Thickness of the core
W_a	Window area of the core
WF	Window filling factor
W_{tc}	Total weight of the choke
W_{tcu}	Weight of the copper
W_{tfe}	Weight of the core
Z_1, Z_2	Impedances on each line of a two-wire cable
Z_{b1}, Z_{b2}	Impedances of the motor bearing and rotor shaft
Z_{cm}	Common-mode impedance
Z_d	Fictitious dc impedance to obtain the dc-link midpoint
Z_{dm}	Differential-mode impedance
Z_g	Grounded impedance of the grid
$Z_{g\text{-}lf}$	Grounding impedance of the line-side filter
Z_{lf}	Line-side filter impedance
Z_{mf}	Motor-side filter impedance
$\mathfrak{R}_b$	Reluctance of the bridge legs
$\mathfrak{R}_c$	Reluctance of the circular core
$\mathfrak{R}_g$	Reluctance of the air gaps

μ_0	Absolute permeability of free space
μ_r	Relative permeability of the core material
ρ_{cu}	Copper density
ρ_{fe}	Iron density
Φ	Flux in the integrated choke
Φ_{cm}	Common-mode flux
Φ_{dm}	Differential-mode flux
φ_m	Angle between the output phase voltage and load current in a CSI
φ_w	Angle between the output phase voltage and PWM current in a CSI
ω	Supply angular frequency

Chapter 1

Introduction

For the past several decades, power electronic converters have been widely employed in power systems, renewable energy generation, manufacturing, transportation and other industries. The application of power converters has brought revolutionary advancements in cost savings for energy production, productivity increases and power quality improvement [1, 2]. On the other hand, great efforts should be made to solve the attendant undesirable issues and challenges, such as harmonic distortion and dv/dt, etc., among which the problems caused by common-mode voltages (CMVs) have drawn special attention since the 1990s [3-12].

In 1995, it was reported from industry that motor failures due to bearing damage were detected only within a period of six months after installing a pulse-width modulated (PWM) insulated-gate bipolar transistor (IGBT) inverter drive system, while the motor was not retrofitted. This new system was a substitute for an original 1970-vintage six-step bulk inverter system on a synthetic fiber spinning machine. The bearing unreliability was attributed to more frequent occurrences of the steep change in CMVs of the PWM IGBT inverter drive [13].

The CMVs are generated by the switching action of solid-state devices in power converters. They may not only damage the insulation system in motor drives [14-16], but also induce shaft voltage, ground leakage and bearing currents. The shaft voltage and bearing currents are considered as reasons for the previously mentioned bearing failure [5-10, 17-20]. In other

converter systems, similar issues are also caused by CMVs, e.g., the large leakage current in photovoltaic (PV) inverters without galvanic isolation, which is not allowed by the standard [21-23]. The problems caused by CMVs and their mitigation are normally associated with the grounding of power converter systems that conforms to the standard.

An isolation transformer provides a simple and reliable solution to the machine insulation failure and leakage current in PV panels, but it is heavy, costly and decreases the system efficiency [24]. Moreover, the motor issues of shaft voltage, ground and bearing currents are not completely addressed by the transformer. Electromagnetic interference (EMI) filters are normally required on both sides of voltage-source inverter-(VSI) fed drives [25].

Another solution to these problems is to modify the motor and/or converter configurations, such as insulated and ceramic bearings, grounding the rotor shaft, the dual-bridge inverter for double-winding motors, four- or six-leg inverter topologies and common-mode (CM) active cancellation. All these methods employ extra hardware, and may increase the control complexity [13, 16, 19, 26-35].

Many PWM schemes and synchronization between the rectifier and inverter were proposed to mitigate the CMV magnitude [36-47]. Whereas it is possible to reduce or eliminate CMVs in multilevel voltage-source converters (VSCs) by using their modulation redundancy [40-44], there is a huge cost in two-level VSCs, including the deterioration of harmonic distortion and shrunken linear modulation regions [36-39, 48]. In addition, the CMV can hardly be eliminated in a three-leg, two-level VSC by nature.

The CMV issues can also be solved from the spectrum point of view, rather than from that of magnitude. Passive filters and CM chokes are regarded as this type of techniques [11, 49-59]. The incorporation of the CM suppression function into a differential-mode (DM) inductor

reduces the size and cost of the system. Most research on magnetic integration was conducted on single-phase or dc reactors [60-64]. The integrated dc-link choke in transformerless, current-source inverter (CSI)-based drives was a special example for high-power medium-voltage (MV: 2.3 kV–13.8 kV) systems [65-67]. Few configurations of the multi-phase integrated choke have been invented or optimized for CMV suppression in VSC systems [68-70].

Based on the CMV investigation in typical power converters, this dissertation proposes a novel three-phase integrated choke that mitigates CMVs from the perspective of spectrum. In VSCs, the proposed choke suppresses the CMV in its dominant distribution of the medium frequency range. The VSC systems using the integrated choke, in coordination with appropriate system grounding and other CM filter components, are analyzed. New space-vector modulation (SVM) techniques are also developed for CSI-fed drives to reduce the CMV magnitude and maintain the size of the integrated dc-link choke as small as using selective harmonic elimination (SHE) modulation. The research work surrounds two integrated chokes, involving 1) the three-phase ac choke design, optimization and analysis of its effect in VSC systems, and 2) the development of new SVM techniques to keep the compact design of the dc-link choke in CSI-fed drives.

In this chapter, the definition and generation of CMVs will be first discussed. Various issues caused by CMVs and their mechanisms are then explained, followed by an overview of the general grounding of power converter systems and CMV analysis. After reviewing the state-of-the-art solutions, the objectives and organization of the dissertation are presented at the end of the chapter.

1.1 Definition and Generation of CMVs

The CMV in power converter systems is defined in the same way as in electronics: the average of the voltage of each line with respect to the local common or ground. In a two-wire cable, a CMV appears on both lines, in-phase and with equal amplitudes. A simple case with two power lines is shown in Fig. 1-1, where v_{1G} and v_{2G} are the voltages of power lines 1 and 2 to the common ground; Z_1 and Z_2 are the impedances on the lines; Z_{dm} and Z_{cm} are the DM and CM impedances respectively. The voltages can be decoupled into DM and CM components:

$$\begin{cases} v_{dm} = v_{1G} - v_{2G} \\ v_{cm} = \left(v_{1G} + v_{2G}\right)/2 \end{cases}, \tag{1-1}$$

and the currents are expressed by

$$\begin{cases} i_1 = i_{dm} + i_{cm}/2 \\ i_2 = i_{dm} - i_{cm}/2 \end{cases}. \tag{1-2}$$

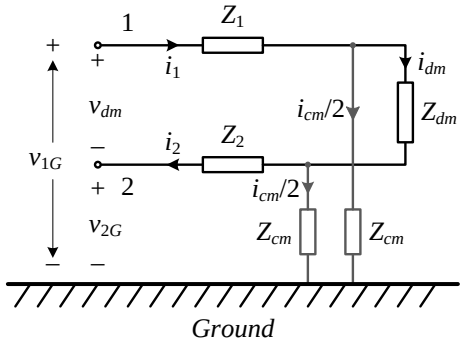


Fig. 1-1 CM and DM definitions in a circuit with two power lines.

In Fig. 1-1, even though the voltage sources v_{1G} and v_{2G} do not contain any CM component, the impedance asymmetries can generate CM currents, equivalently adding a CMV [71, 72]. For example, the CMV produced by $Z_1 \neq Z_2$ is

$$v_{cm} = v_{dm} \cdot \frac{Z_1 - Z_2}{2\left(Z_1 + Z_2\right)}. \tag{1-3}$$

In power converter systems, the switching action of solid-state devices is a main source of CMVs. Take an example of a single-phase full-bridge converter shown in Fig. 1-2. The CMV is defined with respect to the dc-link midpoint as:

$$v_{cm} = \left(v_{az} + v_{bz}\right)/2. \tag{1-4}$$

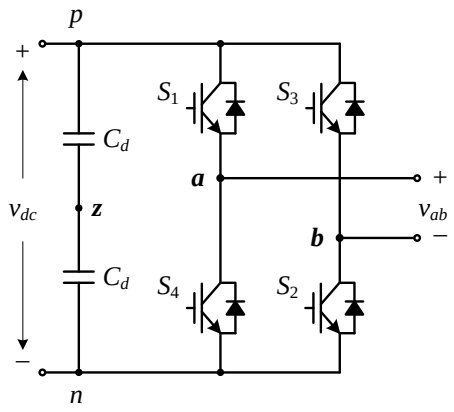


Fig. 1-2 Single-phase full-bridge converter.

With bipolar modulation that simultaneously turns on or off the diagonal switches (S_1 and S_2, S_3 and S_4), the CMV is always kept at zero. However, unipolar PWM generates a stepwise CMV waveform with the values of $\pm v_{dc}/2$ and 0 [73].

The CMVs are essentially zero-sequence components in three-phase systems and equal to zero with a balanced supply and load. Fig. 1-3 illustrates a popular three-leg, three-phase VSC whose CMV is defined by

$$v_{cm} = \left(v_{az} + v_{bz} + v_{cz}\right)/3. \tag{1-5}$$

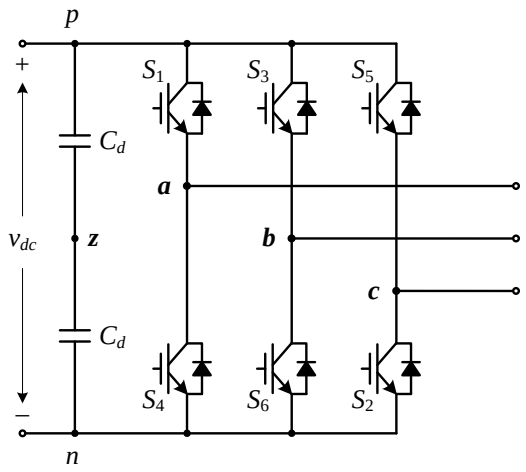


Fig. 1-3 Three-leg, three-phase, two-level voltage-source converter.

This is different from the single-phase full-bridge converter in that the CMV in Fig. 1-3 could never be zero, because the voltages v_{az}, v_{bz} and v_{cz} are either $+v_{dc}/2$ or $-v_{dc}/2$, resulting in the values of $\pm v_{dc}/6$ and $\pm v_{dc}/2$ for the CMV [74]. The research work of this dissertation is focused on the CMVs and their mitigation in three-phase power converter systems.

1.2 Problems Caused by CMVs

1.2.1 CMV Issues In Motor Drives

If CMVs are not mitigated in a motor drive, they will appear on the neutral point of the stator windings with respect to the ground. The motor line-to-ground voltage, which is originally equal to the line-to-neutral (phase) voltage, can be substantially increased, leading to premature failure of the motor winding insulation system. As a result, the motor life expectancy is shortened [1, 14, 15, 75].

The MV drives (2.3 kV–13.8 kV) do not allow their motors to be subjected to any CMVs; otherwise replacement of damaged motors would be very costly in addition to causing loss of production [13]. The CMV stress, on the other hand, is often neglected in low-voltage (LV: ≤ 600 V) drives thanks to the conservative insulation design of LV motors.

However, the other CMV issues induced via the parasitically capacitive couplings inside the motor, including the shaft voltage, ground and bearing currents, exist in both MV and LV drives, and cannot be ignored [5-10, 13, 16-19]. The CM-circuit model of a machine shown in Fig. 1-4 is used to elaborate these problems. C_{sg} is the parasitic capacitance between the stator winding and the grounded frame. C_{sr} is the capacitance between the stator winding and the rotor. C_{rg} is the capacitance between the rotor and the frame. $C_{b\text{-}NDE}$ and $C_{b\text{-}DE}$ are, respectively, the capacitances of lubricant grease films at the nondrive-end (NDE) and drive-end (DE) bearings. Z_{b1} and Z_{b2} denote the bearing and rotor-shaft impedances. The switches, SW_1 and SW_2, are employed to interpret the occurrence of the dielectric breakdown of thin lubricant films [8, 18, 76-78].

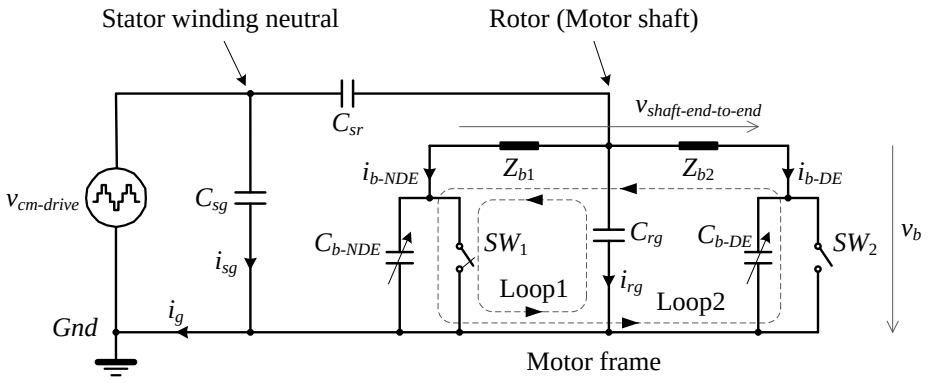


Fig. 1-4 CM-circuit model of a machine.

The stepwise CMV $v_{cm\text{-}drive}$ with a high value of dv/dt that appears on the neutral point of the motor stator windings induces a current i_{sg} leaking from C_{sg}. Due to the impedance ratio of C_{sg} to the capacitances on the rotor side, i_{sg} primarily contributes to the motor ground current i_g, which can arouse conducted EMI [50-52, 54, 71]. Malfunctions of ground-fault protection relays may also occur, especially in large drives (e.g., ≥ 100 kW) with a magnitude of i_g in the order of 15% - 25% of the rated current [19, 20].

The bearing currents and shaft voltage have complex mechanisms which can be explained by the cause-and-effect chains in Fig. 1-5 [19, 20]. Four types of bearing currents have been distinguished:

1) Capacitive bearing current stemming from the shaft-to-frame voltage that is also termed bearing voltage v_b;

2) Electrical discharge machining (EDM) bearing current. At intact lubrication film, v_b mirrors $v_{cm\text{-}drive}$ through a capacitive voltage divider called the “bearing voltage ratio” (BVR):

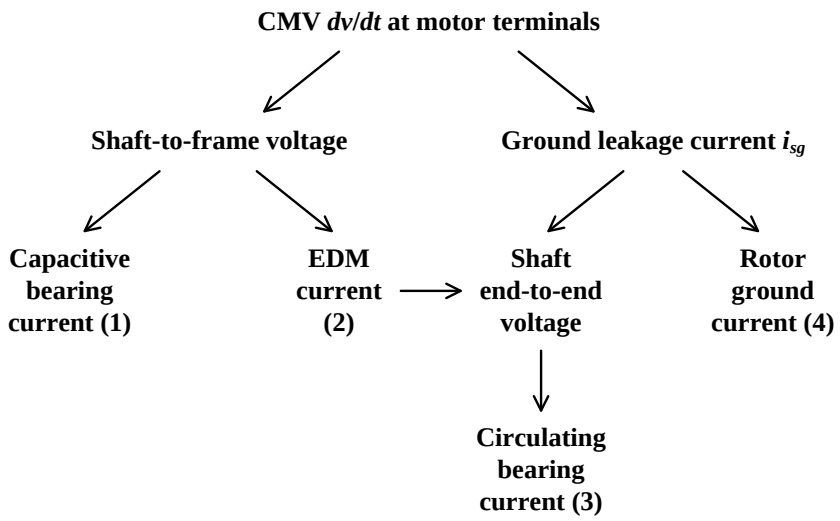


Fig. 1-5 Cause-and-effect chains of the motor bearing currents and shaft voltage.

$$BVR = \frac{v_b}{v_{cm-drive}} = \frac{C_{sr}}{C_{sr} + C_{rg} + \left(C_{b-NDE} + C_{b-DE}\right)}. \tag{1-6}$$

Once v_b exceeds the threshold voltage of the lubricant film between the bearing balls and races, the oil film will break down. This is represented by the closing of switch SW_1 or SW_2, and leads to the voltage collapse of v_b and a high EDM current pulse [7-10, 79].

3) Circulating bearing current along the loop "stator frame-nondrive end-shaft-drive end" shown in Fig. 1-4. This current is driven by the shaft end-to-end voltage which is different from v_b and defined by the voltage difference between the nondrive and drive ends of the shaft. Two reasons for the shaft end-to-end voltage have been revealed in the literature: a circumferential flux surrounding the motor shaft and the breakdown of the lubricating film in one bearing (the NDE bearing in most cases) prior to that in the other [6, 77, 78, 80]. The former is excited by the stator leakage current i_{sg} in the axial direction.

The latter produces an EDM current flowing through C_{rg} and the bearing where the breakdown occurs (Z_{b1} and $C_{b\text{-}NDE}$ in most cases). This EDM current is larger than that in the healthy bearing, i.e., $i_{b\text{-}NDE} > i_{b\text{-}DE}$, due to $C_{rg} >> C_{b\text{-}DE}$, resulting in a shaft end-to-end voltage [77, 78].

4) Rotor ground current passing the bearings, which is only considered when the rotor is connected to the earth potential (e.g., via the mechanical load) with a significantly lower impedance than the grounding of the stator housing.

Among the four, the first capacitive bearing current is small and regarded as harmless, whereas the other three can be reasons for bearing failure and reflected by the shaft voltages including the bearing voltage, v_b, and shaft end-to-end voltage. According to Fig. 1-5, the issues of the bearing currents and shaft voltage originate from the switching CMV. The removal of CMVs from the motor terminals solves the problems of motor winding insulation failure and bearing unreliability [50].

1.2.2 Leakage Current In PV Generation Systems

As a result of the large surface area and small thickness of PV panels, parasitic capacitors exist between the modules and the ground. The capacitance depends on many factors, such as the panel and frame structure, surface of cells and distance between cells, module frame, weather conditions, humidity and dust or salt covering the PV panels [81]. The CMV produced by the inverter is imposed on the capacitors. If there is no galvanic isolation, a CM-circuit loop will be constituted, though which the leakage current flows and charges/discharges the parasitic

capacitors. As a result, severe (conducted and radiated) EMI, grid current distortion and additional losses in the system would be generated.

The leakage current is limited by different standards. For example, the VDE 0126-1-1 standard in Germany requires the PV generation system to be discontented from the grid in 0.3 s, once the ground leakage current exceeds the threshold level of 300 mA [82]. On the other hand, the U.S. *National Electrical Code* (NEC) 690 standard demands that the PV modules should be system grounded and monitored for ground fault [83-85]. The system grounding involves the negative or positive terminal of PV array(s) being connected to the ground. This prevents the widespread application of transformerless PV systems since the grid-side neutral point has been grounded. In PV generation systems with a galvanic isolation, there is no concern with leakage currents.

1.3 Overview of System Grounding and CMV Analysis

The CMV issues and their solutions are closely related to the system grounding, which will be reviewed with the CMV analysis from the perspective of frequency.

Fig. 1-6 shows the grounding diagram of a general motor drive, where the supply and optional isolation transformers are neglected for simplicity. According to the NEC 690 standard, an EMI filter with a solid-ground neutral point is normally inserted between the input harmonic filter and the grid. This line-side harmonic filter should be floating or connected to the neutral line of a five-wire source system, as shown in the figure. If the neutral point of the harmonic filter is grounded, malfunctions of ground-fault protection relays must occur with a sensitive threshold current of 10 mA [83, 86]. The motor-side filter is also connected to the neutral wire of

the supply system to avoid the ground fault current interruption (GFCI), but the motor frame and all other cases must be grounded for safety and protection. The grounding of PV energy systems is very similar to Fig. 1-6, which is not discussed in detail.

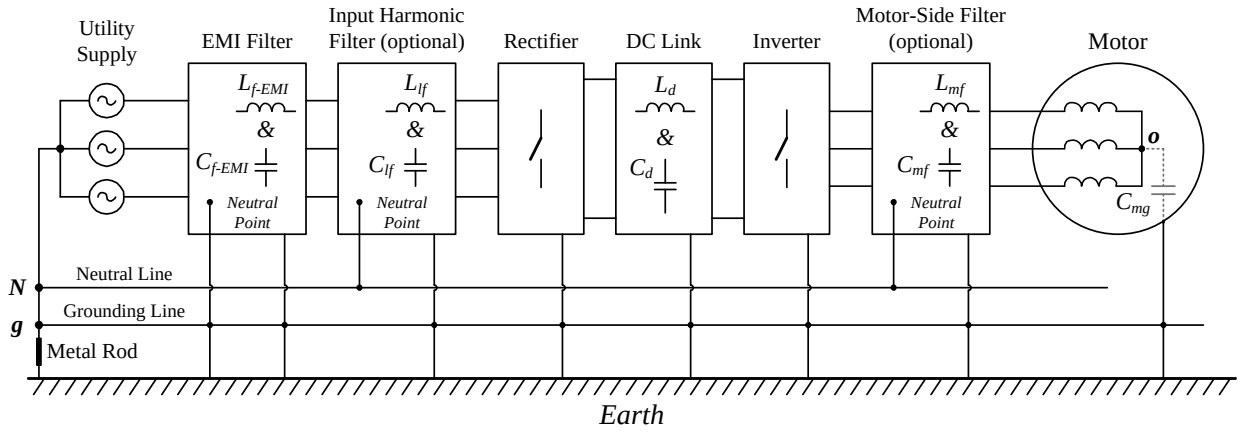


Fig. 1-6 System grounding diagram of a general motor drive.

The EMI filter with a solid-ground neutral point suppresses both the DM and CM interferences. The later is induced by the CMV components at the EMI frequencies that are higher than 150 kHz and up to several MHz. The CMVs produced by power converters can be classified into three frequency ranges: 1) the low frequency range composed of triplen harmonics, 2) the medium frequency range including components around the switching frequency and its integral multiples, and 3) the high EMI frequency range. Research of the EMI filter for suppression CMV components in the high frequency range is beyond the scope of the dissertation. The CMV components within the low and medium switching frequency ranges are dominant in the spectra and will be analyzed and mitigated by different techniques.

1.4 State-of-the-Art Solutions

Besides isolation transformers, lots of solutions to the CMV issues have been proposed, including modified motor and converter configurations, modulation schemes and synchronization, as well as passive filters and CM chokes. The state-of-the-art technologies for CMV mitigation are reviewed.

1.4.1 Isolation Transformers

According to the standard [83], a power converter system, such as a motor drive, must be electrically grounded either on the grid side or on the load side. If the load neutral is grounded, the CMV stress will be imposed on the grid-side transformer, and vice verse. However, the power system usually requires the neutral point of the supply transformer to be grounded. In this case, the CMV stress is imposed on the motor neutral, leading to premature failure of the motor winding insulation.

To solve the problem, an isolation transformer with a floating secondary is installed between the supply transformer and MV drive, as illustrated in Fig. 1-7. Most of the isolation transformers are in Y-Δ connection in North America, but in order to clearly express the intrinsic winding-to-ground capacitance of the transformer, a transformer in Δ-Y connection is adopted in the explanation. In addition, EMI emissions are mainly excited by *dv*/*dt*, including both the DM and CM *dv*/*dt*. In current-source-fed drives, as the large capacitor bank on the ac side filters the high value of *dv*/*dt*, the EMI filter in Fig. 1-6 may be omitted. However, in VSC-based drives, the EMI filter normally exists to satisfy the electromagnetic compatibility (EMC) code. For simplicity, Fig. 1-7 does not show the EMI filter. The CM model of the motor has been reduced

to a lumped stray capacitor with respect to the ground C_{mg} [76, 87]. The capacitance value of C_{mg} is typically much larger than that of C_{tg} in the transformer, e.g., 150 times in high-power MV systems [24]. The latter acts as an electrostatic voltage divider and undertakes the overwhelming majority of CMVs that are thus removed from motor terminals. Accordingly, the CMV issues are mitigated, although some of them, such as the bearing currents and shaft voltage, have not been completely addressed [25].

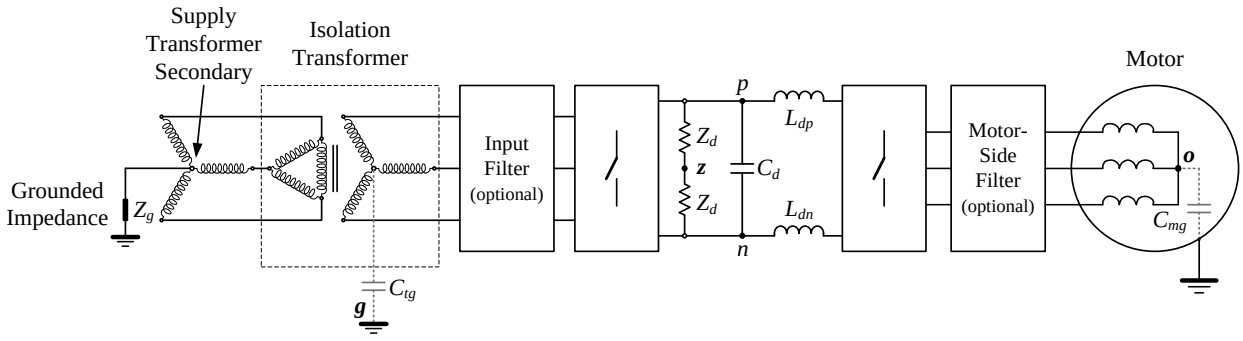


Fig. 1-7 Block diagram of a general MV drive with an isolation transformer.

Although the isolation transformer provides a reliable solution to the CMV issues within the low and medium frequency ranges, it occupies immense space, costs a large amount of money and decreases system efficiency by 1%-2%. Other measures have been proposed and employed.

1.4.2 Motor and Converter Configurations

Many approaches that alter the hardware, i.e., the motor and converter configurations, have been presented to solve the CMV issues. Modifications on the motor construction include:

1) The use of shielded motor cables. This is effective for the rotor ground current when the shaft is grounded, but not for the EDM and circulating bearing currents [16, 19].

2) A second method is insulated bearings that are generally used in dc and large-power motors. All the parasitic bearing currents can be significantly reduced by insulating both bearings, whereas one insulated bearing decreases the circulating bearing and rotor ground currents, but is invalid for the EDM current [26].

3) Hybrid bearings, consisting of steel bearing rings and ceramic bearing balls, suppress all types of bearing currents. Due to their high cost, hybrid ceramic bearings are recommended for small motors that suffer from the EDM bearing current [27].

4) The addition of conductive agents to the grease or oil reduces the equivalent impedance of the bearing capacitive effect and thus attenuates the bearing currents. However, this approach is only successful for a short time, because of the separation of conductive additives, particularly in high-speed operation [13, 16].

5) Grounding the rotor shaft by installing contact brushes to bearings makes the shaft voltage equal to zero and is effective in eliminating bearing currents. The hardware is relatively easy to implement and low-cost, but requires extra space and regular maintenance. In addition, it may be unacceptable in certain hazardous environments [16].

6) The electrostatic shielded induction motor (ESIM) has an internally mounted Faraday shield to diminish the coupling between the stator and rotor (reducing C_{sr}), which does not affect the electromagnetic torque. The ESIM has been proved effective in eliminating the rotor shaft voltage and bearing currents, but it is difficult and expensive to retrofit a machine with this shield [88].

All these motor constructions only focused on the shaft voltage and bearing currents. Premature failures of the stator winding insulation and the ground leakage current i_g have not

been addressed. It was proposed to change the converter and/or system configurations for elimination of the CMV at its source.

Fig. 1-8 presents a dual-bridge inverter drive that is controlled to generate balanced excitations for a standard three-phase dual-voltage (double-winding) induction motor [28]. The switches in the two inverter bridges are triggered in the reverse order to each other. The CMV is defined by

$$v_{cm} = \left(v_a + v_b + v_c + v_{a'} + v_{b'} + v_{c'}\right)/6. \tag{1-7}$$

It is easy to make the CMV be zero by setting v_a = -$v_{a'}$, v_b = -$v_{b'}$ and v_c = -$v_{c'}$. Since this configuration needs twice the number of semiconductor devices as that of the conventional configuration, a reduced-switch dual bridge inverter was developed based on the two-leg three-phase inverter topology with split dc-link capacitors [29]. This inverter topology also eliminates the CMV, but still has more switches.

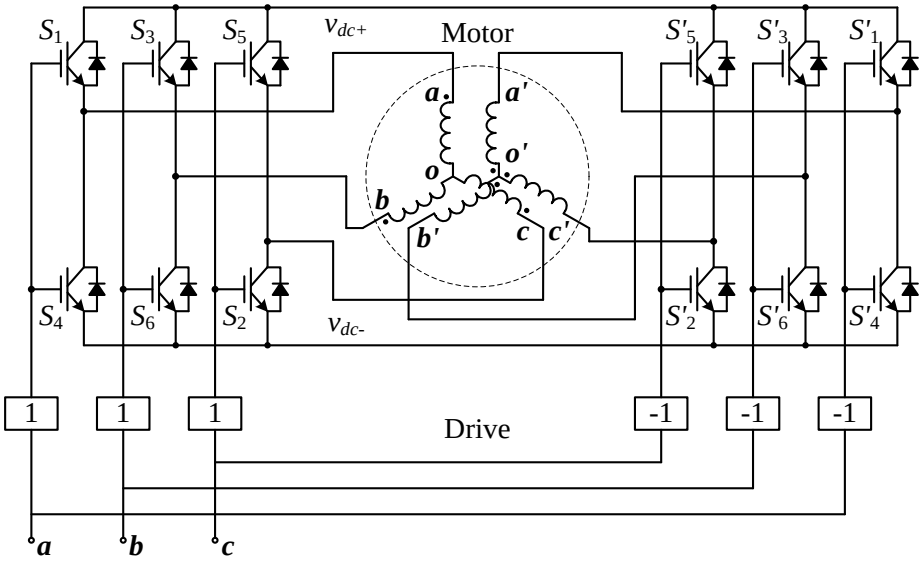


Fig. 1-8 Dual-bridge inverter drive for double-winding motors.

In a similar way, four-leg inverters can also be controlled to reduce or eliminate the CMV by balancing the switches between the positive and negative dc rails [30, 31]. Accordingly, four-leg inverters are commonly used to feed unbalanced loads or compensate for power quality [89-93]. If the four-leg inverters are applied to a general motor drive for CMV cancellation, the extra switching devices will not only increase the cost, but also complicate the system control and lower the reliability.

Furthermore, six- and seven-pole inverters were suggested to cancel or reduce the CMV [32, 33]. Whereas the six-pole inverters drive six-phase motors, six legs of the seven-pole inverters are fed to a three-phase load with every two in parallel and the seventh leg realizes the active cancellation of CMVs with the filter inductance equal to half of those in the other legs. Besides the necessity for more power electronic devices, another drawback of such systems is the resonances that could be easily excited through the switches, filter inductance and capacitance in series on the additional pole [33].

A CM active filter shown in Fig. 1-9 consists of a push-pull emitter follower using transistors, a CM transformer, a Y-connected capacitor bank to detect the CMV and two dc capacitors to prevent a dc current from flowing into the CM transformer. The emitter follower acts as a voltage-controlled voltage source with a unity gain, high-input and low-output impedance. In terms of the winding polarities of the CM transformer, a compensating voltage with the same amplitude as, but opposite polarity to the CMV would be generated. The CMV is consequently cancelled before motor terminals by the active filter. Nonetheless, the lack of complimentary transistors with high-voltage ratings (e.g., $\geq$ 600 V) and the complex circuitry limit the use of this technique [34, 35, 94].

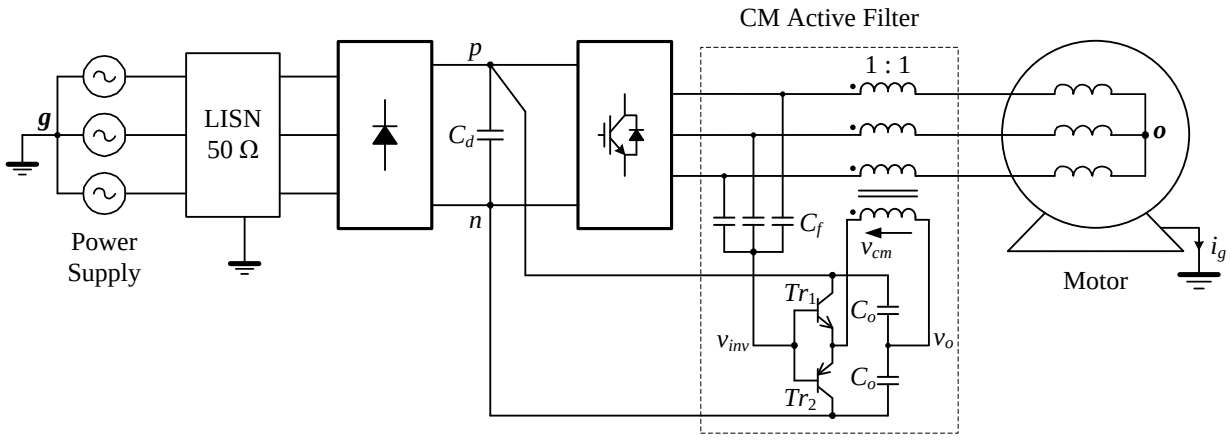


Fig. 1-9 CM active filter in a PWM VSI drive.

The approaches of modifying the motor and converter configurations add hardware, increase the cost, and complicate the system construction and control. Modulation schemes and synchronization, on the other hand, reduce or eliminate the CMV at its origin, and do not require extra hardware.

1.4.3 PWM Techniques and Synchronization

As mentioned earlier, the CMV in a two-level three-phase VSC consists of the values of $\pm v_{dc}/6$ and $\pm v_{dc}/2$. Table 1-1 lists the relationship between all the switching states and CMV values. As demonstrated, the CMV peak values are produced by zero vectors.

Several modulation schemes have been proposed to constrain the CMV magnitude within $\pm v_{dc}/6$ by avoiding zero vectors, such as active-zero-state (AZS) modulation, remote-three-state (RTS) modulation and nearest-three-state (NTS) modulation. The first modulation replaces the zero vectors with two complementary active states in the voltage reference synthesis. Since a

total of three pairs of active vectors can be used, there are three specific techniques [36]. In the second modulation, three odd and/or even active vectors approximate the voltage reference. Although the methods make the CMV constant or vary only between $\pm v_{dc}/6$, the modulation index range is reduced a lot, leading to a lager dc-link voltage [37]. The last scheme synthesizes the voltage reference with the nearest three active states, which requires the modulation index between 2/3 and 1 [38, 39, 48]. The limitation for the modulation index in the last two methods and the increase in harmonic distortion due to the absence of zero vectors prevent these modulation techniques from being practical in VSCs. In addition, even with these CMV mitigation methods, the dead time can still produce short CMV pulses with high values. The dead-time effect on CMVs should be compensated [95, 96].

Table 1-1 Relationship between the VSC switching states and CMV values.

Type	Zero vector		Active vector					
Space vector	$\vec{V}_0$	$\vec{V}_7$	$\vec{V}_1$	$\vec{V}_2$	$\vec{V}_3$	$\vec{V}_4$	$\vec{V}_5$	$\vec{V}_6$
Switching state	[0, 0, 0]	[1, 1, 1]	[1, 0, 0]	[1, 1, 0]	[0, 1, 0]	[0, 1, 1]	[0, 0, 1]	[1, 0, 1]
On-state switches	S_4, S_6, S_2	S_1, S_3, S_5	S_1, S_6, S_2	S_1, S_3, S_2	S_4, S_3, S_2	S_4, S_3, S_5	S_4, S_6, S_5	S_1, S_6, S_5
v_{cm}	$-v_{dc}/2$	$+v_{dc}/2$	$-v_{dc}/6$	$+v_{dc}/6$	$-v_{dc}/6$	$+v_{dc}/6$	$-v_{dc}/6$	$+v_{dc}/6$

In the VSI-fed motor drives with an active-front end, the system CMV is determined by the switching states of both the PWM voltage-source rectifier (VSR) and inverter as well as by their synchronization. Table 1-2 presents the correspondence between the system CMV values and switching states of the converters. Synchronous modulation between the VSR and VSI with identical switching frequencies avoids the CMV pulses at $\pm v_{dc}$ [97].

Table 1-2 Correspondence between the CMV values and voltage vectors of the VSR and VSI.

		Inverter voltage vectors			
		$\vec{V}_1, \vec{V}_3, \vec{V}_5$	$\vec{V}_2, \vec{V}_4, \vec{V}_6$	$\vec{V}_0$	$\vec{V}_7$
Rectifier voltage vectors	$\vec{V}_1, \vec{V}_3, \vec{V}_5$	0	$+v_{dc}/3$	$-v_{dc}/3$	$+2v_{dc}/3$
	$\vec{V}_2, \vec{V}_4, \vec{V}_6$	$-v_{dc}/3$	0	$-2v_{dc}/3$	$+v_{dc}/3$
	$\vec{V}_0$	$+v_{dc}/3$	$+2v_{dc}/3$	0	$+v_{dc}$
	$\vec{V}_7$	$-2v_{dc}/3$	$-v_{dc}/3$	$-v_{dc}$	0

The CMV magnitude can be further restricted so that it is not larger than $v_{dc}/3$ by shifting an active voltage vector of the inverter in a control period and aligning an inverter switching point to one of the rectifier switching points [46, 47]. So the combinations of the specific active vectors and zero vectors, which produce CMV pulses at the values of $\pm 2v_{dc}/3$, are prevented.

Moreover, since the rms value of the motor ground current is proportional to the number of current pulses and accordingly the CMV pulses, another objective could be the reduction of the number of CMV pulses. Redistribution of zero vectors drops the number of CMV pulses by 1/3, resulting in a theoretical 18% decrease of the rms motor ground current [46]. Although these methods play a role in mitigating the CMV issues, they increase the harmonic distortion and do not eliminate the CMV in a two-level, three-phase VSC system [98].

The CMVs in multilevel VSCs can be further reduced or eliminated with more flexibility and at lower cost in harmonic distortion and linear modulation region [40-45]. For example, this can be seen in a popular neutral-point clamped (NPC) three-level VSC whose CMV values corresponding to the switching states are summarized in Table 1-3. The CMV magnitude can be easily lowered from $v_{dc}/2$ to $v_{dc}/3$ by avoiding the zero states of [1, 1, 1] and [-1, -1, -1]. The redundancy of small voltage vectors provides a possible method to limit the CMV within $\pm v_{dc}/6$,

but brings inconvenience to the neutral-point voltage control. To an extreme extent, only employing medium voltage vectors and [0, 0, 0] produces a zero CMV, while three voltage levels of the NPC converter regress to two levels with the maximum modulation index decreased to $\sqrt{3}/2$ and deteriorated harmonic distortion [44]. Fig. 1-10 demonstrates the conventional and reduced voltage vector diagrams of a three-level converter, as well as the reduced voltage vector diagram of a five-level VSC which is linked to that of a three-level VSC [41].

Table 1-3 CMV values corresponding to the switching states in a NPC VSC.

Voltage vector type	switching states	CMV values
Medium voltage vectors	[1, 0, -1] [0, 1, -1] [-1, 1, 0] [-1, 0, 1] [0, -1, 1] [1, -1, 0]	0
Large voltage vectors	[1, -1, -1] [1, 1, -1] [-1, 1, -1] [-1, 1, 1] [-1, -1, 1] [1, -1, 1]	$\pm v_{dc}/6$
Small voltage vectors	[1, 0, 0] [0, 1, 0] [0, 0, 1] [-1, 0, 0] [0, -1, 0] [0, 0, -1]	$\pm v_{dc}/6$
	[1, 1, 0] [1, 0, 1] [0, 1, 1] [-1, -1, 0] [-1, 0, -1] [0, -1, -1]	$\pm v_{dc}/3$
Zero voltage vectors	[0, 0, 0]	0
	[1, 1, 1] [-1, -1, -1]	$\pm v_{dc}/2$

In multilevel converters, a compromise is sometimes made between the CMV reduction and loss of voltage levels, harmonic distortion as well as modulation index range. It is possible to omit the isolation transformer in MV drive systems, particularly for the VSCs with seven levels or higher [99]. The transformerless multilevel VSC-based drives have entered the commercial market. One product is called Pyramid, manufactured by Converteam, and the other is ACS 2000

from ABB which uses active NPC (ANPC) converter topologies [100]. Besides modulation schemes, these transformerless MV drives usually employ a CM choke to suppress the CM voltage/current [100-103].

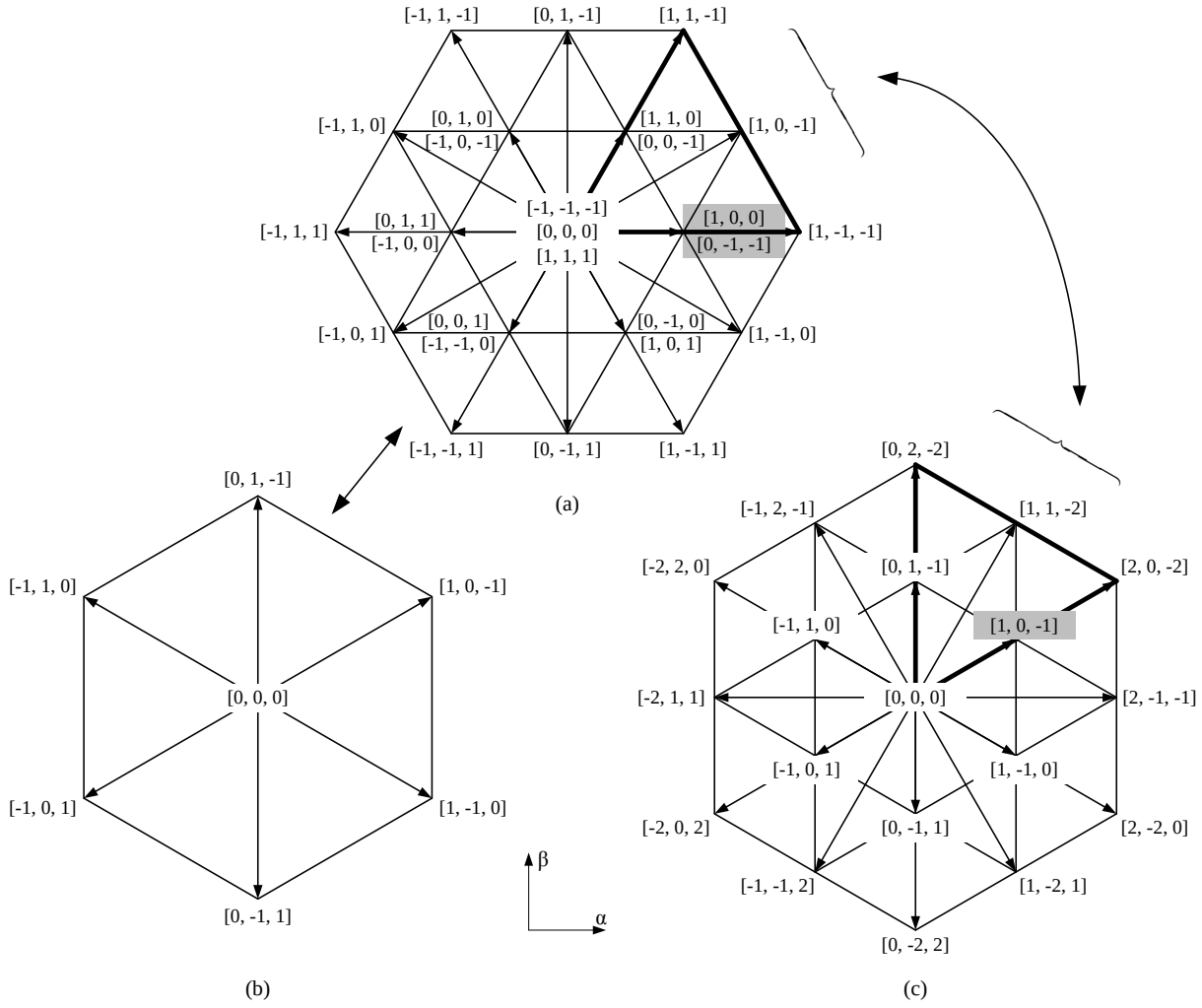


Fig. 1-10 Linkage between voltage vector diagrams. (a) Conventional three-level VSC. (b) Reduced three-level converter with a zero CMV. (c) Five-level converter with a zero CMV.

1.4.4 Passive Filters and CM Chokes

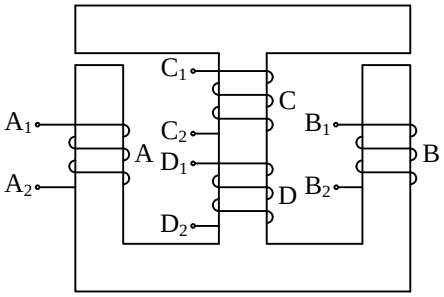
As shown in Fig. 1-6, passive filters are comprehensively used in power converter systems to deal with the harmonic distortion and EMI issues. Various types of filter configurations based on inductors, capacitors, damping resistors and even diodes, have been presented [11, 49, 50]. A series of passive filters consisting of both DM and CM filters were proposed to suppress the CM voltage/current in low-power motor drives. The filters were installed on both the rectifier and inverter sides. The configurations required access to the motor neutral point to make the filter smaller in size and more effective in attenuating the CMV issues [51-54, 77, 94].

In high-power drive systems, the CMV stress, ground current and shaft voltage can be mitigated by installing CM chokes. As previously stated, the CM chokes facilitates the implementation of transformerless configurations [99-103]. Without an isolation transformer, the CMV is supposed to appear on the motor side, but the insertion of CM chokes takes the most CMV from motor terminals and thus addresses the issues. This requires high impedance for the CM choke.

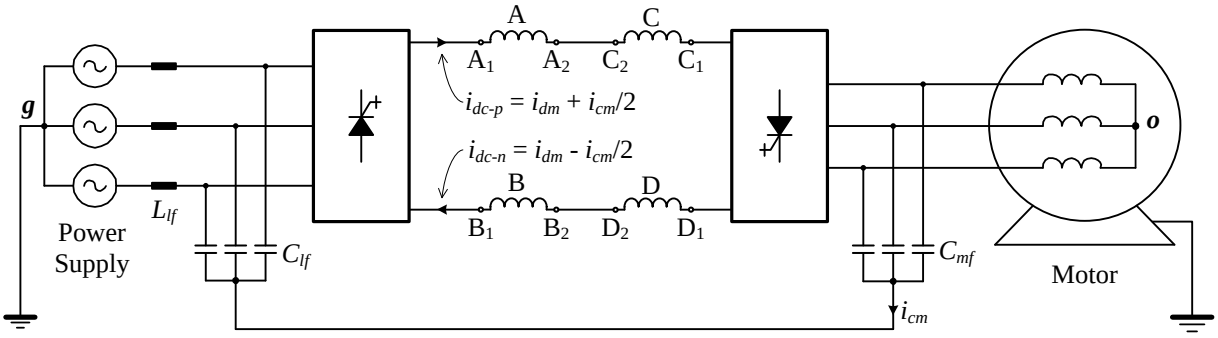
If the CM choke is incorporated into a DM reactor, such as the inductor in a *dv*/*dt* filter at the output of the inverter or the inductor in a grid-side harmonic filter, there will be a considerable decrease in size and weight of the passive components. This can significantly lower costs and improve efficiency, in particular when compared to converter systems with an isolation transformer [68, 69].

There have been inventions in magnetic integration, but most of them are for single-phase or dc systems [60-64]. Fig. 1-11 shows an example of the integrated dc-link choke and its connection diagram in transformerless MV CSI drives that are products of Rockwell, PowerFlex

7000 [104]. According to the DM and CM current directions and fluxes induced in the core, only coils A and B contribute to the DM inductance, whereas all four coils take part in the CM inductance generation. The DM and CM inductance can be adjusted independently. With the same number of turns for all four coils, a CM-to-DM inductance ratio of 2.25 is obtained. To eliminate the CMV from motor terminals, the neutral points of the motor- and grid-side capacitor banks are shorted and kept floating. The CM current flows through converters, the integrated choke and filter capacitor banks, excluding the motor and grid neutral point. The CM impedance of the integrated choke limits the CM current [66, 67].



(a)



(b)

Fig. 1-11 Structure of the integrated dc-link choke and its connection diagram in transformerless MV CSI drives (PowerFlex 7000: Rockwell). (a) Integrated dc-link choke. (b) Connection diagram.

Only two types of multi-phase integrated chokes have been proposed. Unfortunately they were specific for mitigating long-cable effects at the inverter output and attenuating circulating currents in parallel VSCs. They were neither structure-optimized designs yet, nor able to facilitate the implementation of transformerless configurations in high-power MV systems [68-70].

In fact, passive filters are practical solutions to the CMV issues. The concept of the DM and CM integration in one magnetic device offers great benefits in saving the cost and size of the passive components. The design and use of integrated chokes are based on comprehensive CMV analyses, and in coordination with grounding techniques and modulation schemes.

1.5 Dissertation Objectives

In view of the features and limitations of previous technologies, the research motivation for this dissertation is to develop reliable, more functional and cost-effective solutions to the CMV issues. Elimination of the isolation transformer is one of the objectives. Due to the high cost, complexity and unreliability, modifications of the motor/converter configurations do not fall in the scope of the research. The modulation schemes and synchronization between converters that reduce the CMV magnitude cannot eliminate CMVs in the most popular two-level, three-phase converter systems, and degrade the DM performance. However, these techniques have been employed in multilevel VSCs to implement transformerless configurations with CM chocks. In terms of reliability and practicality, passive filters and CM chokes are superior to the other types of CMV mitigation methods. They solve the CMV issues from the spectrum point of view, rather than from the magnitude as PWM schemes.

The prior art of filters and CM chokes were mostly designed for the CM *dv*/*dt* effects and EMI in LV VSC systems. They have not been general solutions to the CMV issues yet, which also include the voltage stress and premature failures of the motor insulation system [49-54, 56, 57]. Moreover, the DM and CM magnetic integration in passive filters has demonstrated advantages in cost and size savings, attracting attention and research effort. This dissertation is dedicated to the development and use of integrated chokes that mitigate the CMVs at their dominant frequencies in both VSC (in the medium frequency range) and current-source converter (CSC) systems (in the low frequency range).

In VSC systems, there has been no integrated choke invented for CMV suppression in general. In CSI-fed drives, although, the integrated dc-link choke was proposed, its application has not been combined with modern SVM, which brings more flexibility in system control and optimization than conventional SHE modulation [105-115]. Meanwhile SVM generates a larger CMV magnitude. Development of new SVM schemes, in coordination with the integrated dc-link choke, is another initiative of the research to keep the compact design for the choke.

The main tasks and objectives of this dissertation are listed as follows.

1) Analysis of CMVs in power converters.

As mentioned in the review of existing solutions, the CMV magnitudes and values in various VSCs were investigated in the literature [36-48], but the spectra have not been analyzed. Furthermore, the CMVs in CSC systems have not been studied in both facets of magnitude and frequency. In order to propose more effective and economic techniques, the CMVs need to be analyzed comprehensively in commonly used power converters with different modulation schemes. The first objective of the research is to fill the gaps in the analysis of CMVs.

2) Invention and design of a novel integrated ac choke.

The separate CM choke has been used in EMI filters and transformerless VSC systems, such as MV motor drives and PV generation systems [11, 49-54, 56-59, 94, 101-103]. Since a DM filter inductor is usually indispensible on the grid side, the CM blocking function can be incorporated into the DM inductor to compose a three-phase integrated choke, mitigating the CMV issues in the medium frequency range. The second important objective of the dissertation is to propose and design a novel integrated ac choke that saves the iron and copper materials, decreases the volume and weight of passive components, improves the system efficiency and reduces the cost. The Finite element analysis (FEA) and effect tests of a prototype will be conducted to verify the concept of magnetic integration.

3) Modeling and analysis of VSC systems using the integrated choke.

Not only does the CM suppression performance of the integrated choke depend on the structure design, but it is also closely related to the core material characteristics, system grounding and other CM-circuit components, such as CM capacitors and parasitic parameters. The specific converter systems where the integrated choke is employed should be investigated, including the circuit configurations and grounding concepts. The third objective of the research work is to identify the applications of the integrated choke and analyze the VSC systems with the choke by CM-circuit modeling and simulation.

4) New SVM schemes for CMV mitigation in medium-voltage CSCs.

Whereas the integrated ac choke can be utilized in VSI drives with appropriate modulation and system grounding to realize transformerless configurations, the product of CSI-fed drives without an isolation transformer has appeared with the invention of the integrated dc-link choke

[66, 67, 104]. Although SVM provides CSI drive systems with more flexibility to implement the active damping control and optimize the dc-link current for a high or unity input power factor [109-115], it generates the CMV with a larger magnitude than conventional SHE methods. A higher CM inductance is thus required for the integrated choke in the system with SVM. In order to maintain the choke's compact design, the last objective of the dissertation is to propose new SVM schemes which limit the CMV magnitude to no larger than that produced by SHE techniques.

1.6 Dissertation Outline

The dissertation is composed of six chapters and organized as follows.

Chapter 1 presents the background and introduction of the research, providing a comprehensive review of undesirable issues caused by CMVs and state-of-the-art solutions.

Chapter 2 reveals the CMV characteristics in various power converters including the diode and SCR rectifiers, VSC and CSC systems. As the CMV magnitudes and values in VSCs have been studied with different modulation schemes, the analysis of spectrum within the low and medium frequency ranges is emphasized. Both the magnitude and spectrum of the CMVs generated by trapezoidal PWM, SHE and SVM in a CSC are analyzed. The investigation of CMV characteristics paves the way for the development of effective mitigation methods.

Chapter 3 proposes a novel three-phase integrated choke used on the grid side of VSC systems. Not only does the choke filter the DM harmonics, but it also suppresses the CMV in the medium frequency range. Magnetic integration and design optimization significantly decrease

the size and weight, improve the system efficiency and save the cost. The validation of the proposed choke is supported by FEA simulations and experimental results of a prototype.

Chapter 4 identifies applications of the proposed choke in PV generation systems, medium-voltage and low-voltage drives. The CM behaviors of these VSC systems with the integrated choke, appropriate system grounding and other filter components, such as CM capacitors and damping resistors, are analyzed by CM-circuit modeling and simulation.

Chapter 5 develops modified SVM schemes with lower CMV magnitudes in CSI drives. The use of these CMV mitigation methods in active damping control and dc current optimization for a high or unity input power factor remains the size of the integrated dc-link choke as small as with conventional SHE modulation. New switching patterns for the proposed modulation schemes are designed for the purposes of lower switching frequencies and superior harmonic performance. Simulations and experiments are carried out to verify the modulation schemes.

Chapter 6 concludes the dissertation, summarizes the main contributions and presents the possible future work.

Chapter 2

Analysis of Common-Mode Voltages in Power Converters

The common-mode voltages (CMVs) are determined by power converter topologies and switching patterns. In order to propose more effective mitigation methods, this chapter will investigate the CMV magnitude and spectrum characteristics in commonly used power converters with different modulation schemes. The converter topologies considered in the chapter include diode and silicon controlled rectifiers (SCRs), two-level and multilevel voltage-source converters (VSCs) as well as current-source converters (CSCs).

This chapter is organized as follows: first, the CMVs are described in a generic converter block diagram, and then specifically analyzed in diode and SCR rectifiers from both the magnitude and spectrum points of view. Besides reviewing the CMV magnitudes in VSC systems, the spectra in the low and medium frequency ranges are explored with different modulation methods. Moreover, the CMVs in CSCs are discussed by simulation and theoretically. Not only does the investigation reveal some principles of the state-of-the-art techniques to mitigate the CMV, but it points out directions for the novel solutions proposed in following chapters.

2.1 General Description of CMVs

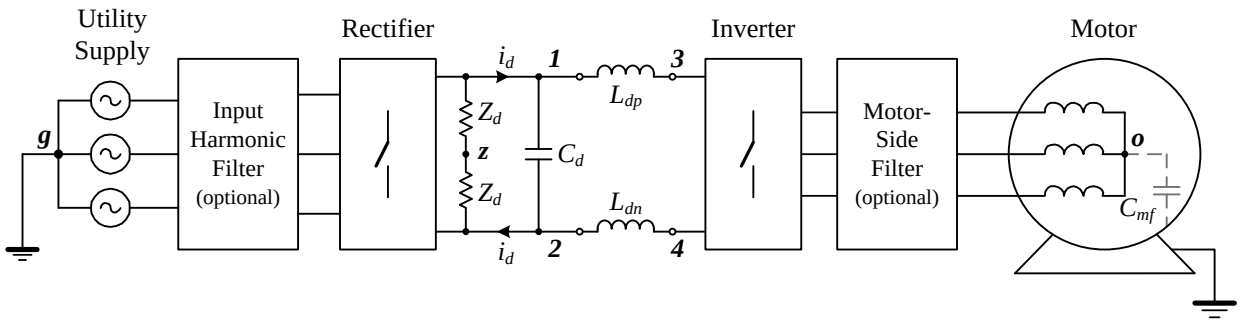
Fig. 2-1 illustrates a generic block diagram of the voltage-source- or current-source-fed motor drive. The front end could be a diode, SCR, pulse-width modulated (PWM) voltage-source or current-source rectifier (VSR or CSR). The motor-side converter is a two-level or multilevel voltage-source inverter (VSI), or current-source inverter (CSI). Fig. 2-1 omits the transformer and EMI filters, but shows the optional differential-mode (DM) filters on both line and motor sides. The dc-link configuration depends on the type of inverter topology: for VSI-fed drives, the capacitor C_d is sufficiently large and the dc-link chokes, L_{dp} and L_{dn}, are not required, whereas for CSI-based drives, the dc inductance should be large enough and C_d is not needed. Two fictitious impedances Z_d are employed to obtain a dc-link midpoint and may not physically exist in the system. Accordingly, the CMV produced by the rectifier can be represented by the dc-link midpoint voltage to the ground of the utility supply:

$$v_{cm-rec} = v_{zg} = \frac{v_{1g} + v_{2g}}{2}, \tag{2-1}$$

where v_{1g} and v_{2g} are the voltages of positive and negative dc points 1 and 2 on the rectifier side to the ground. Similarly, the CMV of the inverter is derived from

$$v_{cm-inv} = -\frac{v_{3o} + v_{4o}}{2}, \tag{2-2}$$

where v_{3o} and v_{4o} are the voltages of positive and negative dc points 3 and 4 on the inverter side to the load neutral point [74].



For voltage-source-fed drives: C_d is sufficiently large and $L_{dp} = L_{dn} = 0$;

For current-source-fed drives: $L_{dp} = L_{dn}$, are large enough, and $C_d = 0$;

Fig. 2-1 Generic block diagram of a voltage-source- or current-source-fed motor drive.

In CSI-fed drives, due to the existence of dc-link chokes, the CMV of the inverter $v_{cm\text{-}inv}$ is not equal to the voltage between the load neutral point and the dc-link midpoint that is on the rectifier side, v_{oz}. The voltage drops on the dc reactors are given by

$$v_{31} = -L_{dp} \cdot \frac{di_d}{dt}; \tag{2-3}$$

$$v_{42} = L_{dn} \cdot \frac{di_d}{dt}, \tag{2-4}$$

where i_d denotes the dc-link current flowing through the inductors.

The voltage of the motor neutral point to the utility ground, which is defined as the CMV of the whole system, is calculated by

$$v_{og} = v_{1g} + v_{31} - v_{3o}; \tag{2-5}$$

$$v_{og} = v_{2g} + v_{42} - v_{4o}. \tag{2-6}$$

By combining (2-1)–(2-4), the addition of (2-5) and (2-6) gives the total CMV:

$$v_{cm-sys} = v_{og} = v_{cm-rec} + v_{cm-inv} + \left(\frac{L_{dn} - L_{dp}}{2} \right) \cdot \frac{di_d}{dt} . \tag{2-7}$$

In VSI-fed drives, the dc inductance is 0, i.e., $L_{dp} = L_{dn} = 0$, whereas in CSI-based systems, in order to reduce the CMV, the inductance on the positive rail should be set equal to that on the negative rail, i.e., $L_{dp} = L_{dn}$. Hence, the system CMV can be simplified as

$$v_{cm-sys} = v_{cm-rec} + v_{cm-inv} . \tag{2-8}$$

The additive effect in (2-8) means an increase in total CMV magnitude. In particular, during some intervals when the CMVs $v_{cm\text{-}rec}$ and $v_{cm\text{-}inv}$ present identical polarities, the maximum CMV of the drive system could be the sum of the peak values of $v_{cm\text{-}rec}$ and $v_{cm\text{-}inv}$ [14].

The voltage stress imposed on motor terminals is evaluated by the phase-to-ground voltage. As an example of phase *a*, the voltage value of the phase terminal to the ground is

$$v_{ag} = v_{ao} + v_{og} = v_{ao} + v_{cm-sys} , \tag{2-9}$$

where v_{ao} is the phase-to-neutral voltage of the motor. It is demonstrated in (2-9) that the CMV increases the motor voltage stress and may damage the stator winding insulation, especially in medium-voltage (MV) drives [1, 14, 15, 74]. Furthermore, the steep change of CMVs or CM *dv*/*dt* added to the motor phase-to-ground voltage leads to the shaft voltage, ground and bearing currents [5, 7-10, 16, 19]. These problems can be solved by the mitigation of CMVs from motor

terminals [50], which needs a comprehensive investigation into the CMV magnitude and spectrum characteristics.

2.2 CMVs in Diode and SCR Rectifiers

As the names of diode and SCR rectifiers indicate, these types of converters consist of uncontrollable and semi-controllable devices: power diodes and thyristers without PWM. The CMVs can be derived according to the switches' conduction which lies on the imposed voltage and flowing current.

2.2.1 CMV of a Diode Rectifier

Fig. 2-2 illustrates the circuit diagram of a six-pulse diode rectifier with a resistive load. The conduction of the diodes is determined by three-phase source voltages. Only one diode in the top half of the bridge and one in the bottom are forward-biased simultaneously (excluding commutation intervals), and either is conducted for 120˚ of the supply cycle [1]. Since balanced three-phase voltages of the supply also have a 120˚ phase angle difference between each other, the waveform of the CMV defined by (2-1) repeats itself every 120˚.

With the definition of three-phase voltages of the supply:

$$\begin{cases} e_{ug} = \sqrt{2} \cdot V_g \sin(\omega t) \\ e_{vg} = \sqrt{2} \cdot V_g \sin(\omega t - 120°) \\ e_{wg} = \sqrt{2} \cdot V_g \sin(\omega t + 120°) \end{cases}, \tag{2-10}$$

where V_g is the rms value of the phase voltage and ω is the supply angular frequency, given by $\omega = 2\pi f_1$ (f_1 is the fundamental frequency of the grid voltage.). The CMVs of the diode rectifier are listed in Table 2-1 during every 60˚ interval of a supply cycle. The CMV waveform can be represented by

$$v_{cm} = -\frac{\sqrt{2}}{2} \cdot V_g \sin\theta, \tag{2-11}$$

where θ has been specified in Table 2-1 in terms of ωt and each phase angle. According to (2-11) and Table 2-1, it is clear that the main CMV frequency is three times the supply frequency, and the maximum value is $\left(\sqrt{2}/4\right)V_g$.

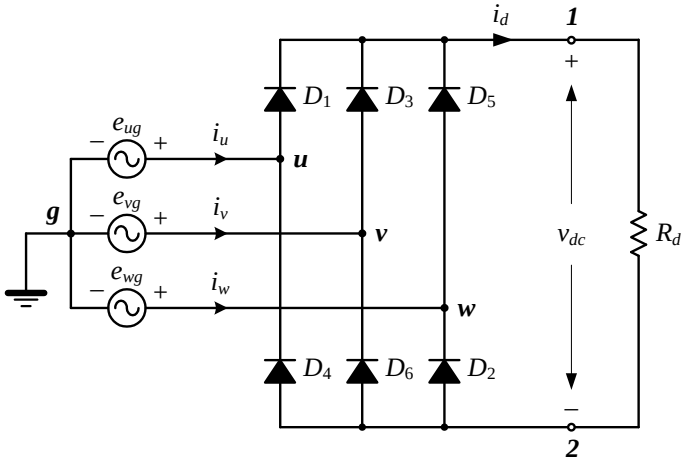


Fig. 2-2 Circuit diagram of a six-pulse diode rectifier with a resistive load.

A 1MVA/4160V diode rectifier with a 2.0 pu dc resistive load was simulated in MATLAB/Simulink. Fig. 2-3 shows the simulation results of the three-phase voltages, the voltages of positive and negative dc-link points 1 and 2 to the ground, the CMV and its fast

Fourier transform (FFT) analysis. The abscissa axis in Fig. 2-3 (b) is represented by *n*, the frequency ratio of the CMV components to the supply (60 Hz). It is observed from the figures that the CMV is dominant at three times the supply frequency, i.e., 180 Hz, and the maximum value is 849.1 V (0.35 pu), equal to $\left(\sqrt{2}/4\right)V_g$. The previous theoretical calculations are thus verified.

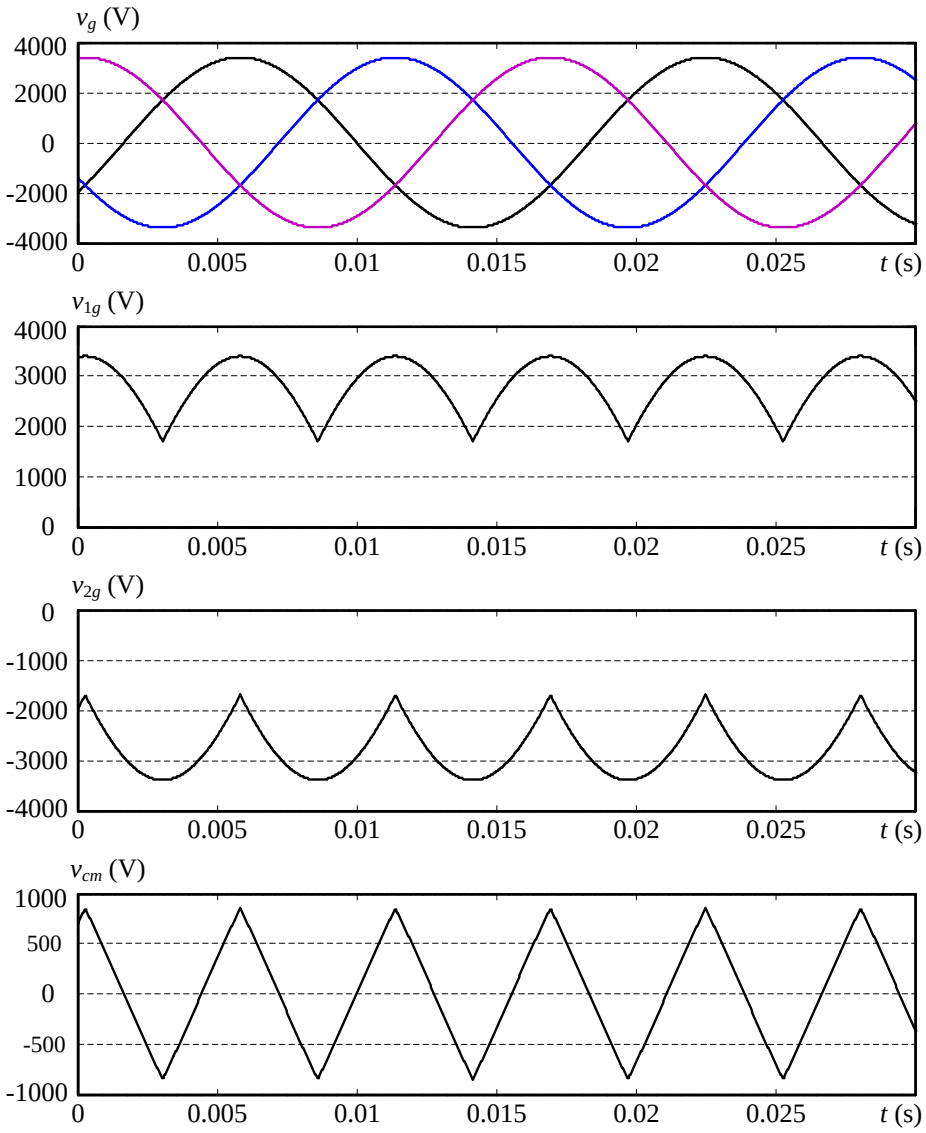
Table 2-1 CMVs of a diode rectifier during every 60˚ interval of a supply cycle.

ωt	[30˚, 90˚)	[90˚, 150˚)	[150˚, 210˚)	[210˚, 270˚)	[270˚, 330˚)	[330˚, 360˚) & [0˚, 30˚)
v_{cm}	$-e_{wg}/2$	$-e_{vg}/2$	$-e_{ug}/2$	$-e_{wg}/2$	$-e_{vg}/2$	$-e_{ug}/2$
θ in (2-11)	[150˚, 210˚)	[-30˚, 30˚)	[150˚, 210˚)	[-30˚, 30˚)	[150˚, 210˚)	[-30˚, 30˚)

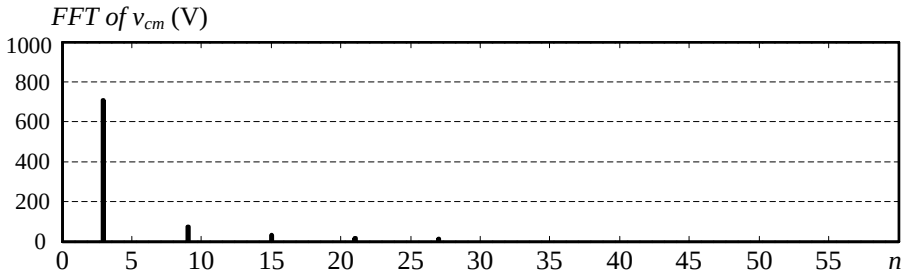
As diode rectifiers are usually employed in VSI-fed drives [1, 75], the simulation with a capacitive load should be more practical, but becomes complicated in CMV analysis. Fortunately, a capacitive load mitigates the CMV, as shown in Fig. 2-4, where the magnitude has been reduced to 560 V (0.23 pu) with a 5.0 pu dc capacitor and 2.0 pu resistor in parallel.

2.2.2 CMV of a SCR Recitifier

SCR rectifiers are mainly used as the front end of CSI-fed drives [1]. An inductive load is accordingly supposed in the dc link. In order to obtain a ripple-free dc current I_{dc}, the inductance is ideally infinite, as demonstrated in Fig. 2-5. In this case, the firing angle could be in the full range of 0˚–180˚, which means the SCR rectifier can regenerate power to the supply, operating in an inverting mode.

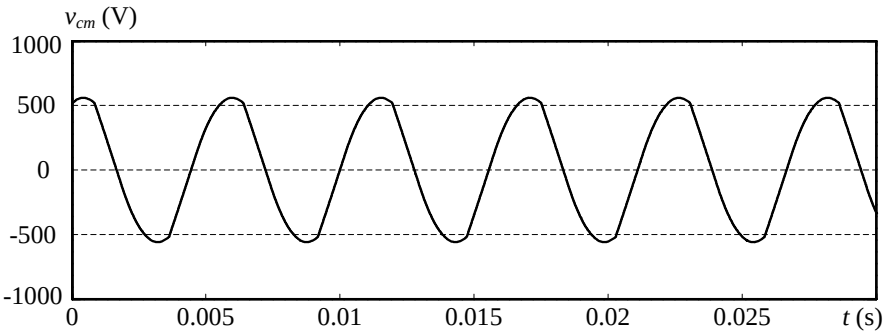


(a)

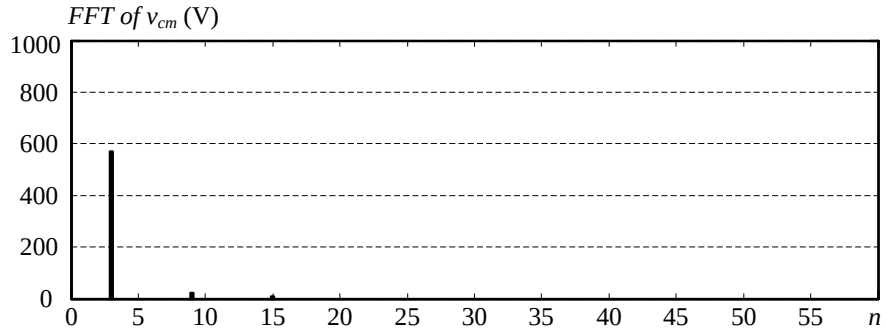


(b)

Fig. 2-3 Simulation results of a 1MVA/4160V diode rectifier with a 2.0 pu resistive load. (a) From top to bottom: three-phase supply voltages v_g, voltages of the positive and negative dc-link points to the ground v_{1g} and v_{2g}, and CMV v_{cm}. (b) FFT of v_{cm}.



(a)



(b)

Fig. 2-4 CMV waveform and its spectrum of the 1MVA/4160V diode rectifier with a capacitive load (5.0 pu dc capacitor and 2.0 pu resistive load in parallel). (a) CMV v_{cm}. (b) FFT of v_{cm}.

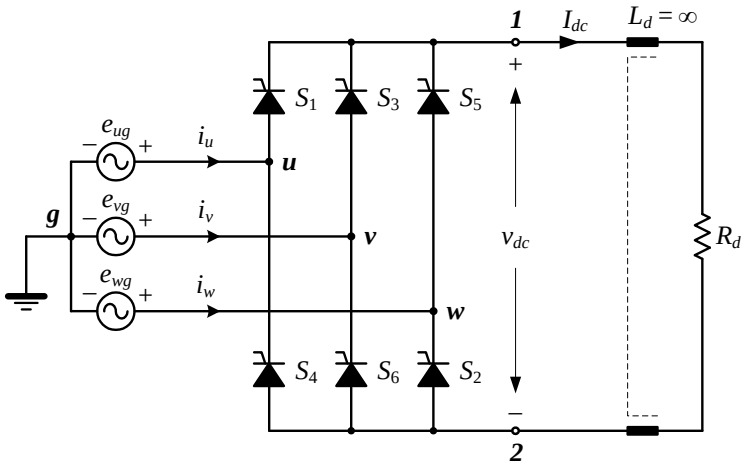


Fig. 2-5 Circuit diagram of a six-pulse SCR rectifier with an inductive load ($L_d = \infty$).

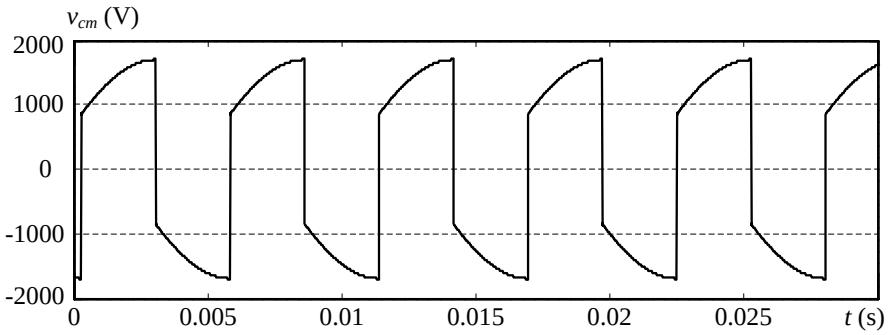
The firing angle α determines the conduction of thyristors. With a sufficiently large dc inductance, every switch is turned on for a 60˚ interval. The operation of the SCR rectifier is similar to that of the diode rectifier, except that the conduction of thyristors is delayed for a firing angle α. In other words, the CMV analysis is identical for the diode and SCR rectifiers when α = 0˚.

According to the derivation in diode rectifiers and considering an arbitrary firing angle α, Table 2-2 lists the CMVs of a SCR rectifier in every 60˚ interval. The CMV function can also be given by (2-11), where θ is related to α and impacts the CMV magnitude. When α falls in the range of 60˚–120˚, the maximum CMV is achieved at half the peak value of the phase voltage.

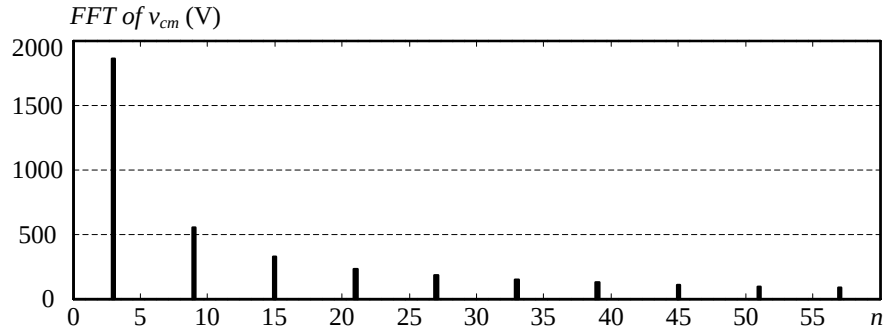
Table 2-2 CMVs of a SCR rectifier in every 60˚ interval.

ωt	[α+30˚, α+90˚)	[α+90˚, α+150˚)	[α+150˚, α+210˚)	[α+210˚, α+270˚)	[α+270˚, α+330˚)	[α-30˚, α+30˚)
v_{cm}	$-e_{wg}/2$	$-e_{vg}/2$	$-e_{ug}/2$	$-e_{wg}/2$	$-e_{vg}/2$	$-e_{ug}/2$
θ in (2-11)	[α+150˚, α+210˚)	[α-30˚, α+30˚)	[α+150˚, α+210˚)	[α-30˚, α+30˚)	[α+150˚, α+210˚)	[α-30˚, α+30˚)

Fig. 2-6 shows the CMV waveform and its FFT analysis in a simulated 1MVA/4160V SCR rectifier with a firing angle α = 60˚. The CMV magnitude reaches 1698.3 V (0.71 pu), half the peak value of the phase voltage. The CMV spectrum is still mainly distributed at three times the supply frequency, but more other triplen components are introduced by the angle delay α, compared to that of a diode rectifier.



(a)



(b)

Fig. 2-6 Simulation results of a 1MVA/4160V SCR rectifier with an inductive load and a firing angle α = 60˚. (a) CMV v_{cm}. (b) FFT of v_{cm}.

2.3 Analysis of CMVs in Voltage-Source Converters

Fig. 2-7 shows a simplified diagram of VSI-fed drives, where Z_{lf} and Z_{mf} are, respectively, the line- and motor-side filter impedance. According to the definition and general description in 2.1, the CMVs of the rectifier, inverter and balanced three-phase system are

$$v_{cm-rec} = v_{zg} = -\frac{v_{uz} + v_{vz} + v_{wz}}{3}, \tag{2-12}$$

where v_{uz}, v_{vz} and v_{wz} are the rectifier ac voltages to the dc-link midpoint; and

$$v_{cm-inv} = v_{oz} = \frac{v_{az} + v_{bz} + v_{cz}}{3}, \tag{2-13}$$

where v_{az}, v_{bz} and v_{cz} denote the inverter output voltages to the dc-link midpoint; and the total CMV of the drive system is calculated by

$$v_{og} = v_{cm-rec} + v_{cm-inv} = \frac{v_{az} + v_{bz} + v_{cz}}{3} - \frac{v_{uz} + v_{vz} + v_{wz}}{3}. \tag{2-14}$$

It is noted that the minus sign in (2-14) does not mean a reduction of the total CMV. In fact, asynchronization between the rectifier and inverter can increase the CMV as in (2-8) [46, 47].

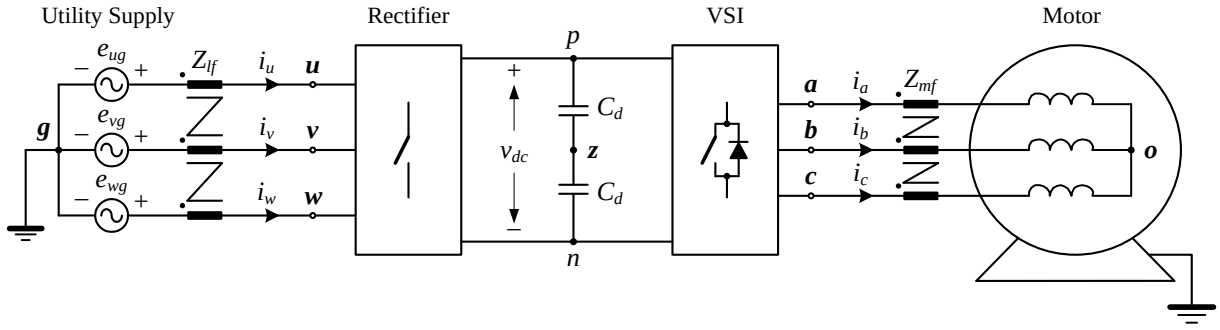


Fig. 2-7 Simplified circuit diagram of VSI-fed drives.

2.3.1 CMV of a Single Converter

The CMV characteristics of the single two-level and multilevel VSCs will be revealed with an emphasis on the spectrum by simulation.

2.3.1.1 Two-Level VSCs

For a two-level VSI shown in Fig. 2-8, a binary-logic switching function is defined per the switching requirements,

$$s_i = \begin{cases} 1 & \text{when the upper switches } (S_1,\ S_3 \text{ and } S_5) \text{ turn on;} \\ 0 & \text{when the lower switches } (S_4,\ S_6 \text{ and } S_2) \text{ turn on,} \end{cases} \tag{2-15}$$

where i = a, b and c, signifying three phases. According to the CMV derivation in (2-13), the CMV of the VSI can be further explicated by the switching functions:

$$v_{cm} = \frac{v_{az} + v_{bz} + v_{cz}}{3} = \frac{v_{dc}}{3}\left(s_a + s_b + s_c\right) - \frac{v_{dc}}{2}. \tag{2-16}$$

where v_{dc} is the dc-link voltage [74].

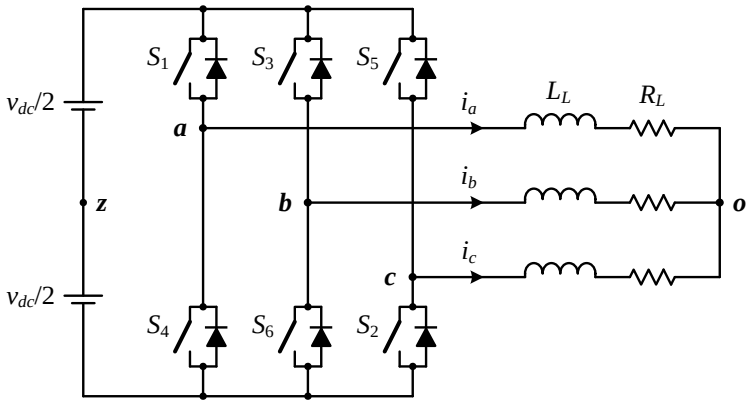


Fig. 2-8 Circuit diagram of a two-level VSI with a three-phase *RL* load.

The CMV is determined by the switching functions and with the values of $\pm v_{dc}/6$ and $\pm v_{dc}/2$, as indicated in Table 1-1. The VSI in Fig. 2-8 was simulated with sinusoidal pulse-width modulation (SPWM) and space vector modulation (SVM) to study the CMV waveforms and spectra. Table 2-3 lists the simulation parameters. In the simulations of the high-power VSI, the switching frequencies were designated low and to be integer multiples of the fundamental frequency (synchronous PWM), i.e., f_{sw} = 900 Hz for SPWM, and f_{sw} = 720 Hz for SVM. The

frequency modulation indices, which are defined by the ratio of the switching frequency to the fundamental frequency ($m_f = f_{sw}/f_1$), are correspondingly m_f = 15 (SPWM) and m_f = 12 (SVM). The simulated VSI was required to output a 4160-V line-to-line voltage (rms value). For SPWM, the definition of amplitude modulation index is the ratio of the peak values of the modulating wave to carrier wave, equivalent to that of the output phase voltage magnitude to half the dc voltage, i.e., $\hat{V}_{ao}/(v_{dc}/2)$. On the other hand, the modulation index in SVM is defined by the ratio of the line-to-line voltage magnitude to the dc voltage, i.e., $\hat{V}_{ab}/v_{dc}$. The different modulation index definitions result in different dc voltage utilization [1]. Therefore, the dc-link voltage was set a little different for SPWM and SVM with the same amplitude modulation index of m_a = 0.9.

Table 2-3 Simulation parameters of a VSI with SPWM and SVM.

Rated power	1 MVA	DC voltage source, v_{dc}	7548.1 V – SPWM
Rated voltage (line-to-line, rms)	4160 V		6536.8 V – SVM
Fundamental frequency, f_1	60 Hz	Switching frequency, f_{sw}	900 Hz (m_f =15) – SPWM
Modulation index, m_a	0.9		720 Hz (m_f =12) – SVM
Load resistance, R_L	0.9 pu	Load inductance, L_L	0.44 pu

A. Sinusoidal Pulse-Width Modulation

Fig. 2-9 shows the simulation results with SPWM, including the modulation waveforms, inverter output ac voltages to the dc-link midpoint, v_{az}, v_{bz} and v_{cz}, the CMV and its spectrum. As previously mentioned, the CMV waveform is stepwise with the values of $\pm v_{dc}/6$ and $\pm v_{dc}/2$. The

FFT analysis only shows the CMV distributions up to $n = m_f = 60$, or 3600 Hz, in the medium frequency range. Other trivial components at higher frequencies have been omitted. It is seen from the figure that the component at the carrier frequency f_{sw} = 900 Hz ($n = m_f = 15$) dominate the CMV spectrum and achieves 2689.3 V (1.12 pu) with $m_a = 0.9$. There are also minor CMV distributions at the carrier frequency's integer multiples and their sidebands, but no triplen component in the low frequency range is produced. This is an important feature of the CMV characteristics in VSIs with SPWM.

B. Space-Vector Modulation

The simulated CMV waveform and its FFT analysis with SVM are provided in Fig. 2-10. As reviewed in Chapter 1, the CMV peak values at $\pm v_{dc}/2$ are produced by the zero vectors and can be decreased to $\pm v_{dc}/6$ by using nonzero-state modulation, which, however, pays the penalty of DM performance degradation, such as a shrunken linear modulation region and increased harmonic distortion [36-39].

The CMV waveforms generated by SVM and SPWM are similar, but the former has smaller staircase values thanks to higher dc voltage utilization. This can be considered a small advantage in the CMV magnitude and is attributed to the triplen harmonic injection in SVM. On the other hand, the triplen harmonic injection leads to the corresponding CMV components in the low frequency range, i.e., at the third and ninth fundamental frequencies, etc., as demonstrated in the spectrum of Fig. 2-10 (b). The CMV component at the triple fundament frequency is 597.84 V (0.25 pu) with $m_a = 0.9$ and f_{sw} = 720 Hz ($m_f = 12$), which includes the injected third harmonic in SVM plus the side-band harmonic of the dominant CMV component at the low switching frequency. This amount of CMV in the low frequency range is non-negligible for suppression.

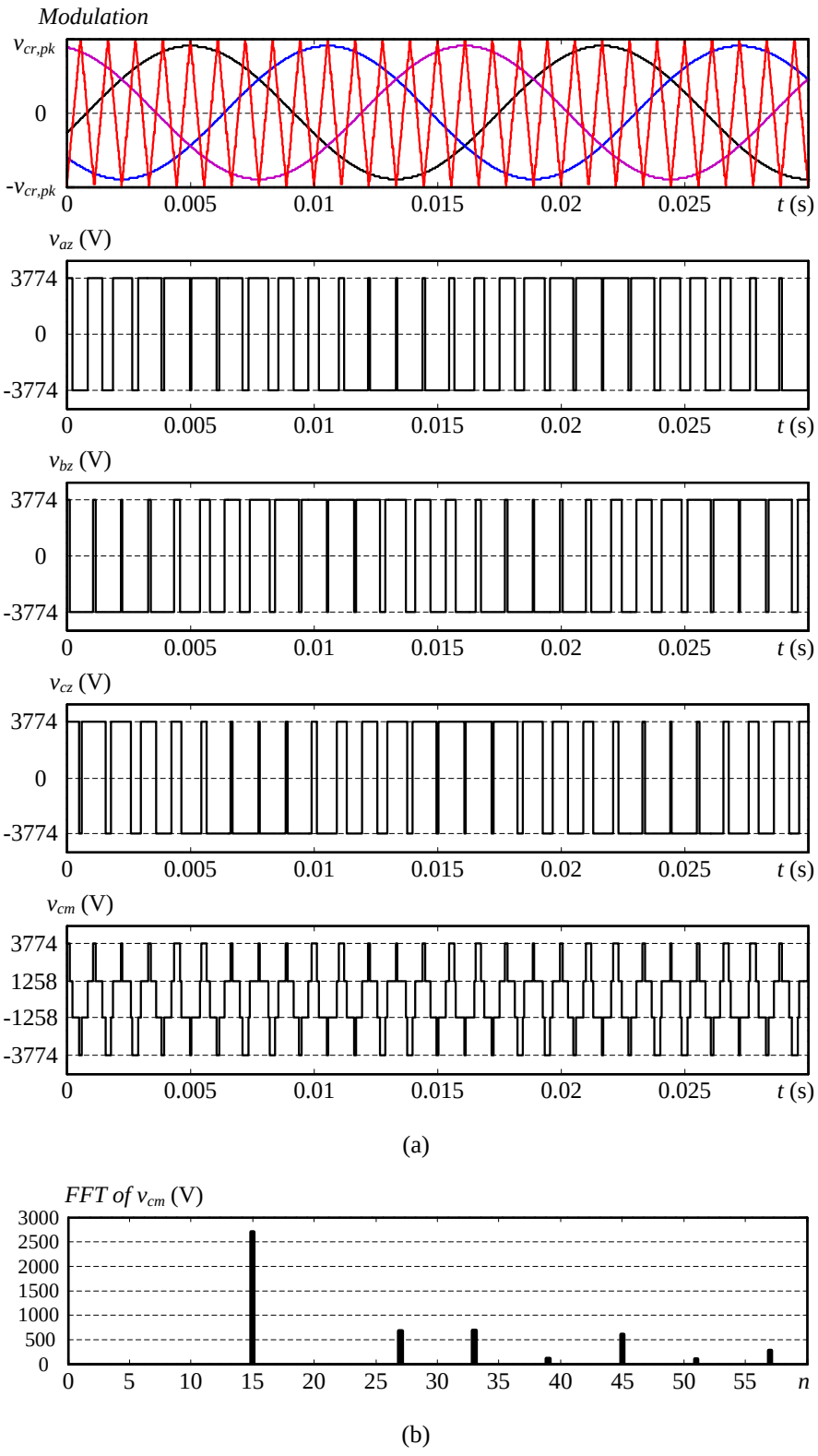
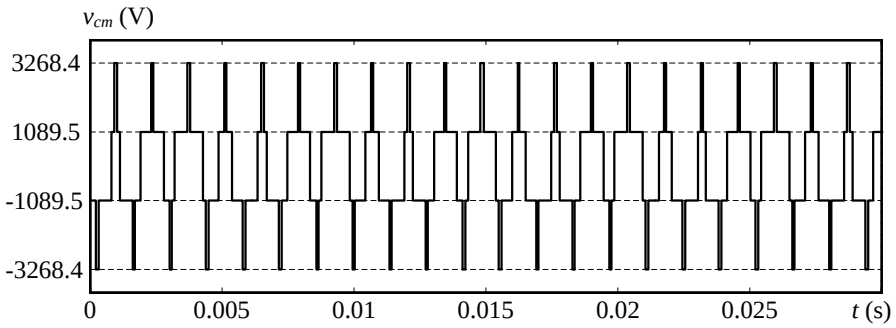
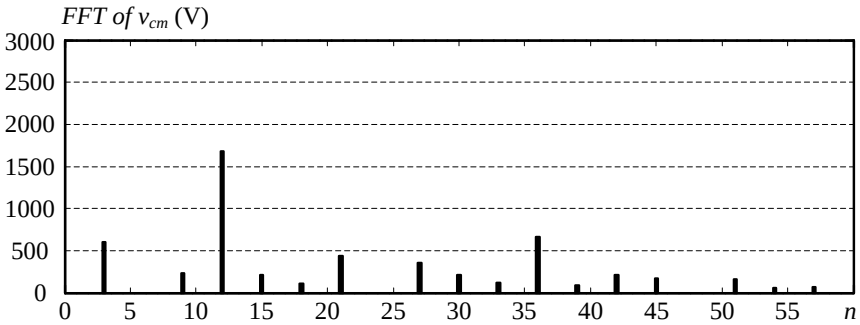


Fig. 2-9 Simulation results of a 1MVA/4160V VSI with SPWM operating at m_a = 0.9 and f_{sw} = 900 Hz ($m_f = f_{sw}/f_1$ = 15). (a) From top to bottom: the modulation waveforms, inverter output voltages to the dc-link midpoint, v_{az}, v_{bz} and v_{cz}, and CMV v_{cm}. (b) FFT of v_{cm}.



(a)



(b)

Fig. 2-10 Simulation results of the 1MVA/4160V VSI with SVM operating at m_a = 0.9 and f_{sw} = 720 Hz ($m_f = f_{sw}/f_1$ = 12). (a) CMV waveform v_{cm}. (b) FFT of v_{cm}.

2.3.1.2 Multilevel VSCs

Multilevel converters have been widely applied to the industry with the benefits of eliminating switching devices in series, lower *dv*/*dt* and a better total harmonic distortion (THD) profile with smaller device switching frequencies [116-119]. Moreover, they also provide the modulation redundancy to reduce or eliminate CMVs from the perspective of magnitude [40-45]. This has been reviewed in Chapter 1.

It is the same as in two-level VSCs that SVM introduces triplen components in the low frequency range to the CMV of multilevel converters, whereas SPWM does not. For example, a popular neutral-point clamped (NPC) inverter illustrated in Fig. 2-11 was simulated with an in-phase disposition (IPD) level-shifted modulation scheme [1]. The parameters were the same as those of the previous two-level VSI with SPWM except for a carrier frequency at f_{sw} = 1080 Hz (m_f = 18). Fig. 2-12 shows the CMV and its spectrum. The CMV waveform has a magnitude of 2516 V (1.05 pu) that is equal to $v_{dc}/3$, and five staircase values of 0, $\pm v_{dc}/6$ and $\pm v_{dc}/3$. The CMV peak values of $\pm v_{dc}/2$ in Table 1-3 are essentially eliminated by the carrier-based PWM scheme without the third-order harmonic injection. As observed in Fig. 2-12 (b), the CMV is distributed at the carrier frequency and its integer multiples as well as their sidebands, with no triplen component in the low frequency range. The value at f_{sw} = 1080 Hz ($n = m_f$ = 18) is dominant and reaches 1535.5 V (0.64 pu).

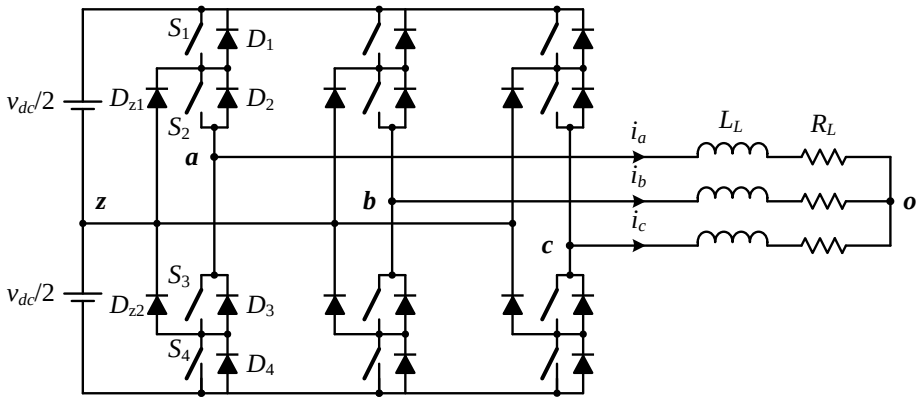


Fig. 2-11 Circuit diagram of a neutral-point clamped VSI with a *RL* load.

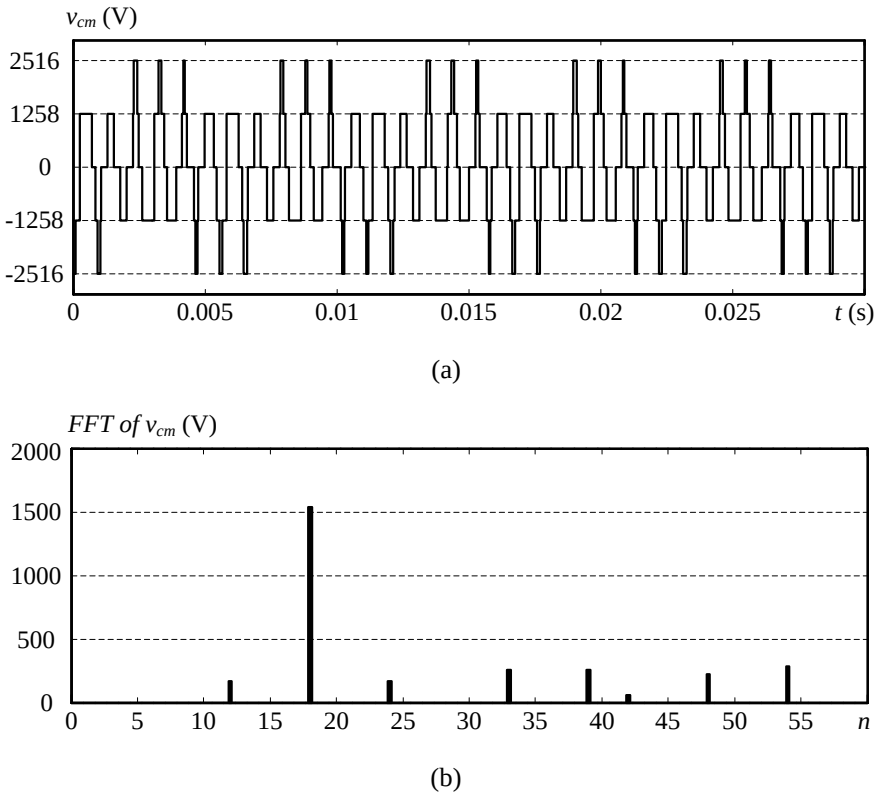


Fig. 2-12 Simulation results of a 1MVA/4160V NPC VSI with in-phase disposition level-shifted modulation operating at m_a = 0.9 and f_{sw} = 1080 Hz ($m_f = f_{sw}/f_1$ = 18). (a) CMV waveform v_{cm}. (b) FFT of v_{cm}.

2.3.2 CMVs in Voltage-Source-Fed Drives

As stated earlier, the CMVs of a voltage-source-fed drive can be calculated from those of the rectifier and inverter, and depend on the converter topologies, modulation techniques as well as operating conditions of the drive [46, 47, 97]. In this section, two configurations are simulated as examples to explore the CMV characteristics in VSI-fed drives: 1) diode-front end + VSI with SPWM; 2) PWM VSR + VSI with SVM on both sides. With two-level VSCs in the simulation, the system ratings were lowered to the medium-power scale (50HP/460V) with a fixed switching frequency at any motor speed ($m_f = f_{sw}/f_m$ may not be an integer, and noncharacteristic harmonics are generated [1].). Open-loop constant Voltage/Frequency (V/F) control is applied to the

inverter. The system ratings, key parameters and steady-state operating conditions are listed in Tables 2-4 and 2-5. As load conditions exert no influence on the CMVs of the voltage-source-fed drives, no load is imposed on the machine [50].

Table 2-4 System ratings of the voltage-source-fed drives.

Rated power	37.285 kW (50 HP)
Supply voltage (line-to-line, rms)	480 V
Line-side fundamental frequency, f_1	60 Hz
Motor rated voltage (line-to-line, rms)	460 V
Motor rated speed	1780 rpm

Table 2-5 Simulation parameters and steady-state operating conditions of the VSI-fed drives.

System parameters	Diode-front end + VSI with SPWM	PWM VSR + VSI with SVM on both sides	
Motor speed (with no load)	1200 rpm	600 rpm	
Inverter output frequency, f_m	40 Hz	20 Hz	
DC voltage, v_{dc}	678.8 V	723 V	
Switching frequency, f_{sw}	5 kHz – VSI	5 kHz – VSR	5 kHz – VSI (syn.)
			4 kHz – VSI (asyn.)
Inverter modulation index at the steady state, $m_{a\text{-}inv}$	0.74	0.3	

2.3.2.1 Diode-Front End + VSI with SPWM

The VSI-fed drive with a diode-front end shown in Fig. 2-13 was simulated without any DM or CM filter. Fig. 2-14 provides simulation results of the CMVs generated by the diode rectifier, VSI with SPWM and the whole drive system, as well as the FFT analysis of the total CMV.

Because of the different fundamental frequencies of the rectifier and inverter, the abscissa axis of the CMV spectrum in Fig. 2-14 (b) is changed to the absolute frequency, rather than the ratio. As previously indicated, the CMVs produced by the diode-front end and PWM inverter are distributed separately at the triple line frequency (180 Hz) and the carrier frequency of f_{sw} = 5 kHz as well as sidebands of its integer multiples. The non-overlapping spectra make the total CMV be a direct addition of the rectifier's and inverter's CMVs. This is not only verified by the FFT analysis in Fig. 2-14 (b), but also manifested in the time-domain waveforms of Fig. 2-14 (a). The CMV of the whole drive system is the stepwise waveform plus a fluctuation at the triple line frequency, i.e., the waveform superposition of individual converters. The maximum total CMV is 391.8 V (1.48 pu), equal to the algebraic sum of the CMV peak values generated by the diode rectifier and VSI, which are, respectively, 52.4 V (0.2 pu) with 5.0 pu dc-link capacitance and 339.4 V (1.28 pu), or v_{dc}/2.

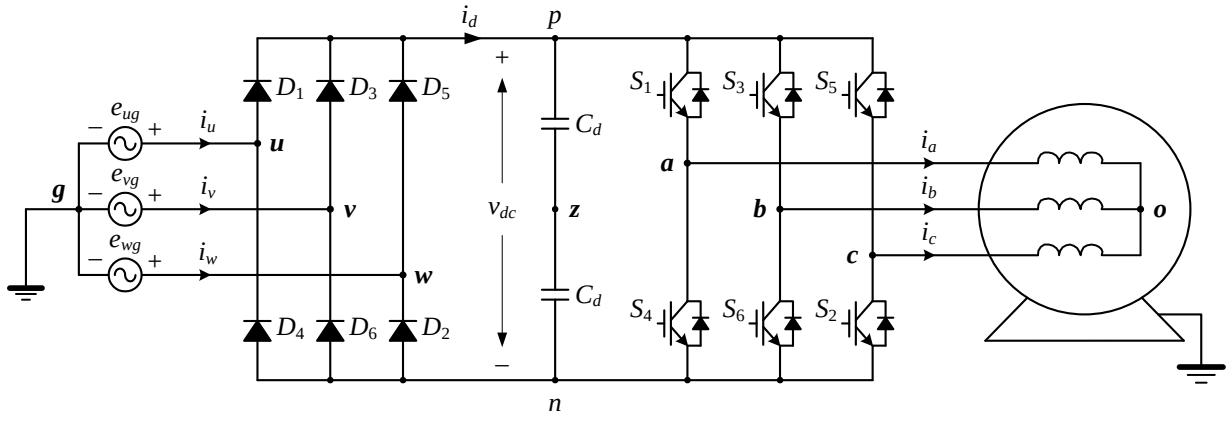
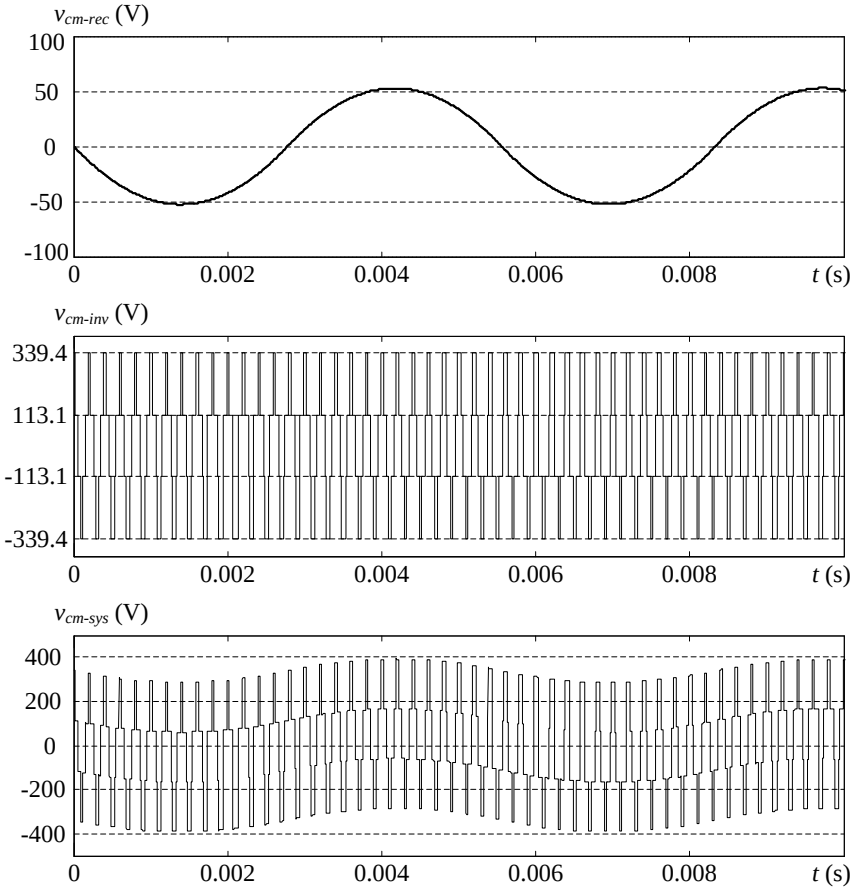


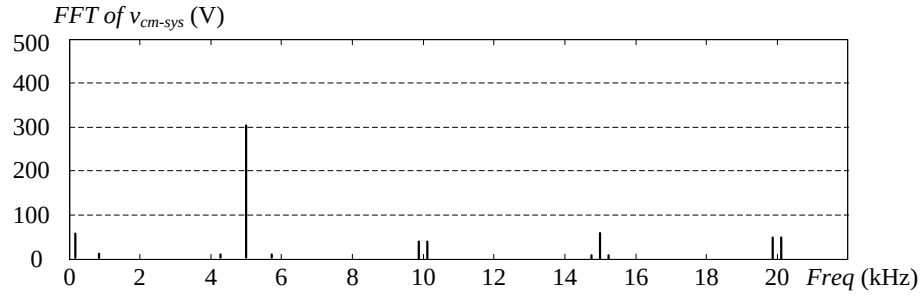
Fig. 2-13 Circuit diagram of the simulated VSI-fed motor drive with a diode-front end.

Similar to the previous FFT analysis, Fig. 2-14 (b) also only covers the CMV spectrum up to the sideband of four times the inverter switching frequency, i.e., 22 kHz, in the medium

frequency range. The distributions at higher frequencies are trivial and easier to filter. The frequency of 22 kHz will be the upper bound of the FFT analysis in the rest of this section.



(a)



(b)

Fig. 2-14 Simulation results of a 50HP/460V motor drive with a diode-front end and VSI with SPWM operating at a motor speed of 1200 rpm (inverter output frequency f_m = 40 Hz). (a) From top to bottom: CMV waveforms of the diode rectifier, VSI and the whole drive system, $v_{cm\text{-}rec}$, $v_{cm\text{-}inv}$ and $v_{cm\text{-}sys}$. (b) FFT of $v_{cm\text{-}sys}$.

2.3.2.2 PWM VSR + VSI with SVM on Both Sides

A motor drive composed of back-to-back PWM VSCs is shown in Fig. 2-15, where the CMVs produced by SVM in both the rectifier and inverter were analyzed and simulated as an illustration. By extending the definition of the switching function in (2-15) and CMV calculation in (2-16) to the active-front end, the total CMV of the drive system can be derived from (2-14):

$$v_{cm} = \frac{v_{dc}}{3}\left[\left(s_a + s_b + s_c\right) - \left(s_u + s_v + s_w\right)\right], \tag{2-17}$$

where s_u, s_v and s_w are the switching functions of phase *u*, *v* and *w* of the rectifier. In terms of the combination of switching functions in (2-17) or voltage vectors, the possibilities of all CMV values include 0, $\pm v_{dc}/3$, $\pm 2v_{dc}/3$ and $\pm v_{dc}$, which have been listed in Table 1-2 [46, 47].

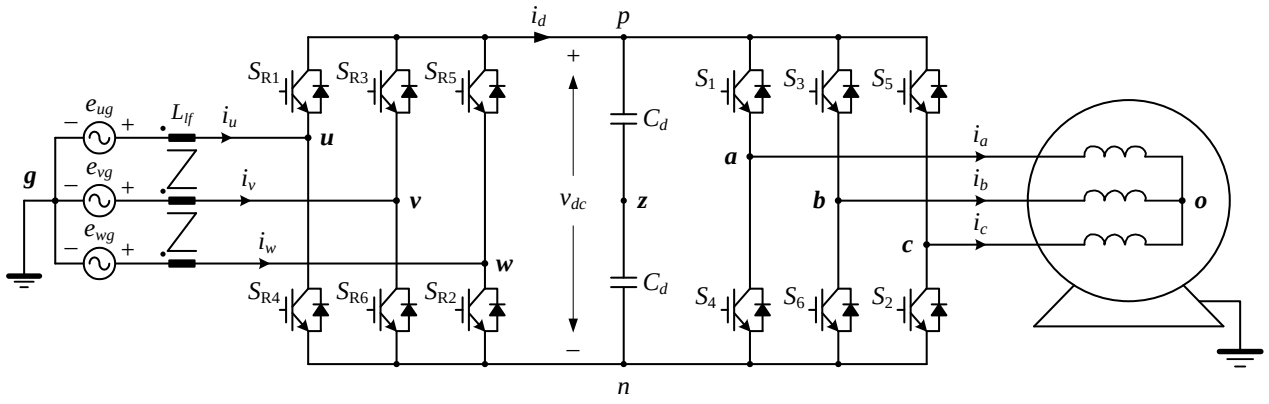


Fig. 2-15 Back-to-back PWM VSC-based motor drive.

Chapter 1 presented a review of the CMV values under different operating conditions and mitigation techniques [97]. With synchronous modulation between the rectifier and inverter, the maximum values of $\pm v_{dc}$ would not appear in the total CMV waveform, as shown in Fig. 2-16 (a)

which provides the CMVs of the PWM VSR, VSI and the whole drive system with the same switching frequency of f_{sw} = 5 kHz. In the simulation, the motor speed was only set to 600 rpm so that a low fundamental frequency and modulation index of the inverter were designated by the controller at f_m = 20 Hz and $m_{a\text{-}inv}$ = 0.3. This large amount of modulation index difference between the back-to-back converters ($m_{a\text{-}rec}$ = 0.94, calculated from the supply voltage of 480 V and the dc-link voltage setup at v_{dc} = 723 V), makes the CMVs of ±482 V (1.81 pu), i.e., $\pm 2v_{dc}/3$, be apparent in the total CMV waveform. The appearances and pulse widths of the CMV values at $\pm 2v_{dc}/3$ increase with the growth of the modulation index difference between the rectifier and inverter [53].

In the spectrum of the total CMV in Fig. 2-16 (b), the components in the medium frequency range are still dominant. In the low frequency range, since the inverter and rectifier operate at different fundamental frequencies of 20 Hz and 60 Hz respectively, separate triple components of the CMV are produced, i.e., 26.65 V (0.1 pu) at 60 Hz and 83.62 V (0.31 pu) at 180 Hz. These values are proportional to their individual ac-side voltages, or modulation indices.

With different fundamental frequencies, it is similar to the analysis in 2.3.2.1 that the spectrum of the total CMV is the direct superposition of non-overlapped CMV spectra of the VSR and VSI in the low frequency range. Only in a special case at the rated motor speed, the low-frequency CMV spectra overlap and the triplen components of the total CMV, e.g. at 180 Hz, might be reduced. This is because of the same fundamental frequency of 60 Hz for the back-to-back converters. The CMV reduction at low triplen frequencies also depends on the initial angle of the supply voltage. On the other hand, the total CMV distributions in the medium frequency range are the overlapping consequence of the CMV spectra generated by the PWM VSR and VSI

that were synchronously modulated at 5 kHz. These CMV components have been mitigated, corresponding to the elimination of $\pm v_{dc}$ from the CMV waveform.

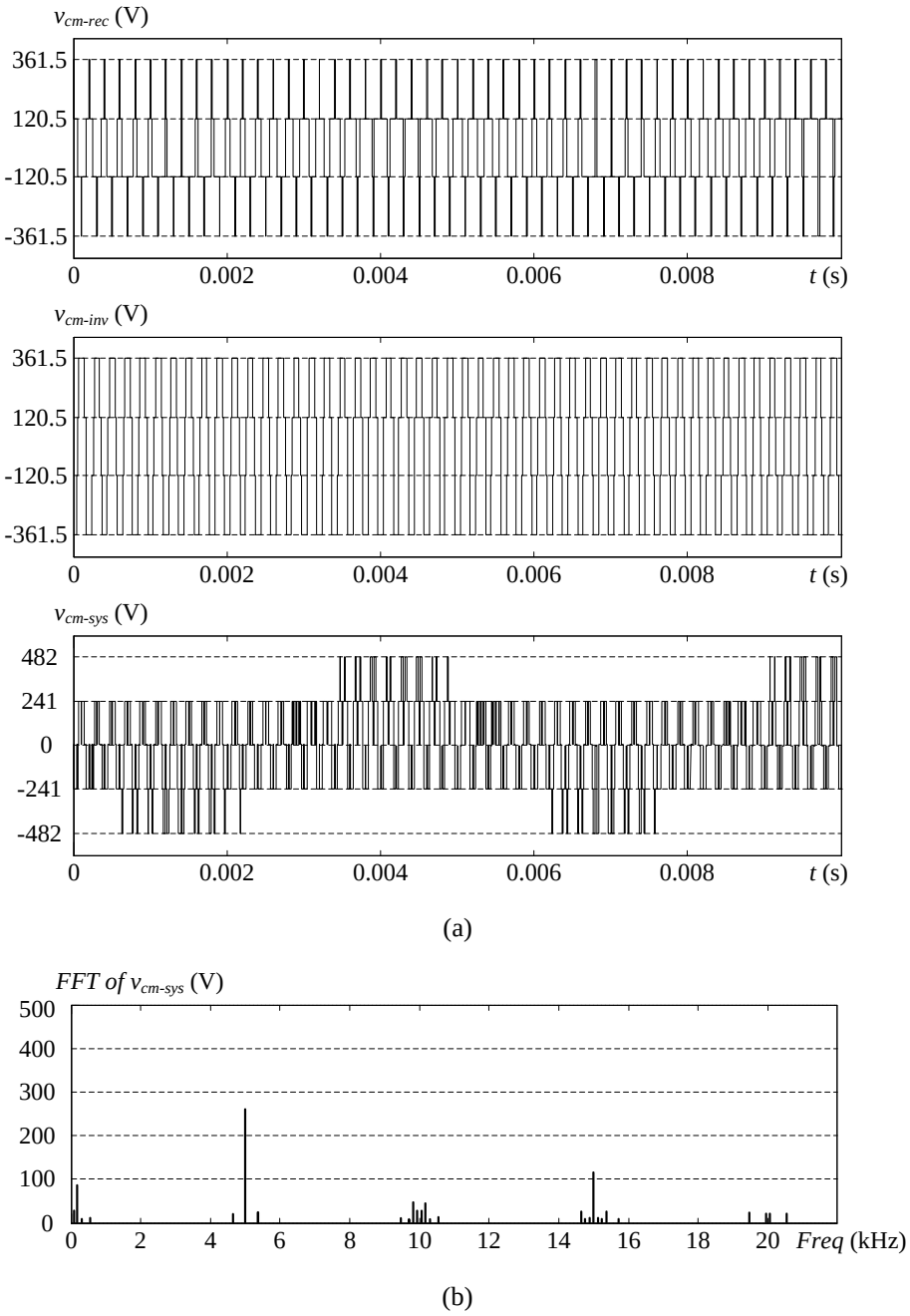


Fig. 2-16 Simulation results of a 50HP/460V motor drive with synchronous SVM between the PWM VSR and VSI operating at a motor speed of 600 rpm (inverter output frequency f_m = 20 Hz). (a) From top to bottom: CMV waveforms of the rectifier, inverter and the whole drive system, $v_{cm\text{-}rec}$, $v_{cm\text{-}inv}$ and $v_{cm\text{-}sys}$. (b) FFT of $v_{cm\text{-}sys}$.

The CMV spectra of the PWM back-to-back converters can also be non-overlapped in the medium frequency range, when asynchronous modulation or different switching frequencies are applied to the rectifier and inverter. In this situation, the CMV magnitude and components are increased [97]. Fig. 2-17 shows the CMVs of the VSR at a switching frequency of $f_{sw\text{-}rec}$ = 5 kHz, the VSI modulated at $f_{sw\text{-}inv}$ = 4 kHz and the whole drive system, as well as the FFT analysis of the last waveform. The motor speed is kept at 600 rpm with an unchanged modulation index at 0.3 for the inverter. The maximum values of $\pm v_{dc}$ appear in the total CMV waveform. The distributions in the medium frequency range are separated. Whereas the low-frequency spectra are almost the same in Figs 2-16 (b) and 2-17 (b), that in the medium frequency range in Fig. 2-17 (b) demonstrates the values of 424.6 V (1.6 pu) at the inverter switching frequency of $f_{sw\text{-}inv}$ = 4 kHz and 163.4 V (0.62 pu) at the rectifier switching frequency of $f_{sw\text{-}rec}$ = 5 kHz, compared to the CMV component of 259.5 V (0.98 pu) at the same switching frequency of f_{sw} = 5 kHz for both converters in Fig. 2-16 (b).

Corresponding to the non-overlapped spectra of top two CMV waveforms in Fig. 2-17 (a), the longer the duration of zero vectors, or the smaller the modulation index, the larger the CMV component at the switching frequency. This qualitatively explains the CMV contents at the switching frequencies in Fig. 2-17 (b) with the modulation indices of the inverter and rectifier, respectively, at $m_{a\text{-}inv}$ = 0.3 and $m_{a\text{-}rec}$ = 0.94. On the other hand, in Fig. 2-16 (b), the partial cancellation of CMV components at f_{sw} = 5 kHz for both converters leads to the lower total value.

Various modulation combinations, such as synchronous or asynchronous modulation between converters, SPWM and SVM, etc., impact the CMV spectrum characteristics. This chapter only provides the analysis at a constant motor speed. The CMVs will be described dynamically with the motor speed changing in Chapter 4 for a VSR-VSI-fed drive with

synchronous SPWM between the converters, which is favorable for the following proposed integrated choke, as no CMV component in the low frequency range will be generated.

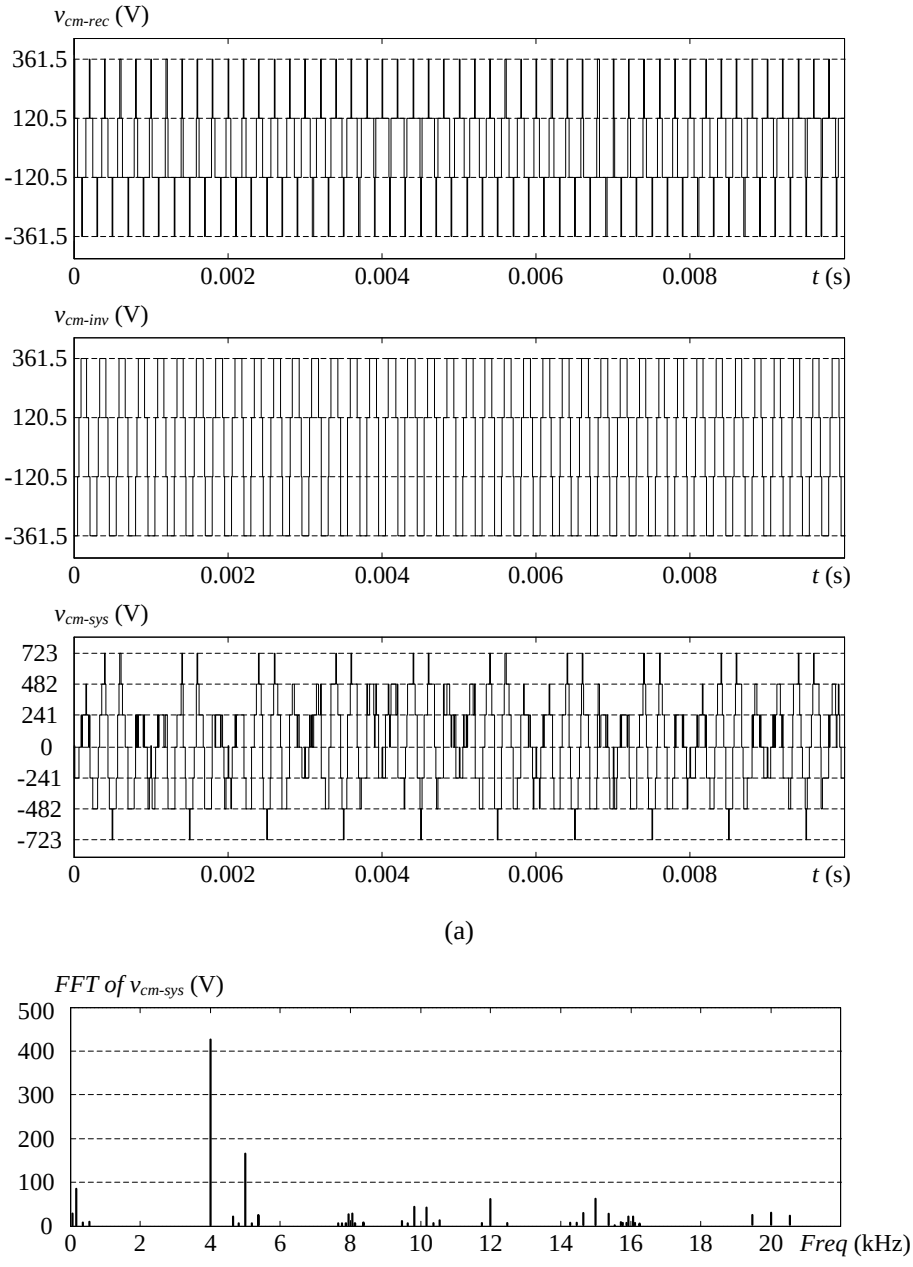


Fig. 2-17 Simulation results of the 50HP/460V motor drive with asynchronous SVM between the PWM VSR and VSI at different switching frequencies of $f_{sw\text{-}rec}$ = 5 kHz and $f_{sw\text{-}inv}$ = 4 kHz. (a) From top to bottom: CMV waveforms of the rectifier, inverter and the whole drive system, $v_{cm\text{-}rec}$, $v_{cm\text{-}inv}$ and $v_{cm\text{-}sys}$. (b) FFT of $v_{cm\text{-}sys}$.

2.4 Analysis of CMVs in Current-Source Converters

The CSC-based motor drive is another attractive topology for high-power applications and also suffers from the CMV stress as its voltage-source-fed counterparts [14, 15, 74]. However, the CMVs are distinct in CSCs and VSCs. A PWM CSI shown in Fig. 2-18 was simulated with different modulations to study the CMV waveforms and their spectra. Table 2-6 lists the simulation parameters of a 1MVA/4160V CSI which operates at the output frequency of f_1 = 60 Hz and feeds a 1.0 pu three-phase *RL* load with a power factor of 0.9 and filter capacitance of 0.4 pu. According to the definition in (2-2), the CMV of the CSI was measured by calculating the average of the voltages of the load neutral point with respect to the positive and negative dc rails.

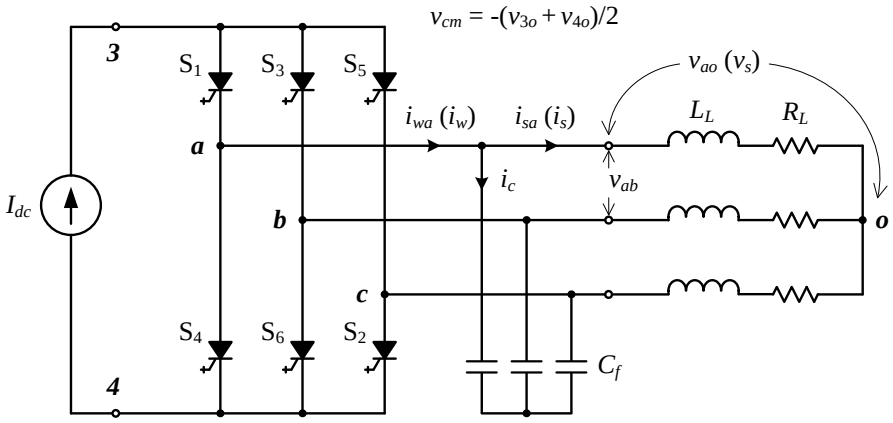


Fig. 2-18 PWM CSI with an ideal dc current source and three-phase *RL* load.

Fig. 2-19 (a) demonstrates waveforms of the ac output and common-mode (CM) voltages with trapezoidal pulse-width modulation (TPWM). In the simulation, the modulation index, which is defined by the ratio of the peak values of the modulating wave to carrier wave, was set to 0.85 for the minimization of the output harmonic distortion [1]. The device switching

frequency was f_{sw} = 540 Hz. It is observed that the CMV peak values are 1680 V (0.7 pu), approximately equal to half the phase voltage magnitude. The FFT analysis in Fig. 2-19 (b) indicates that the CMV is primarily distributed at three times the fundamental frequency, i.e., 180 Hz, besides some trivial components at higher triplen frequencies.

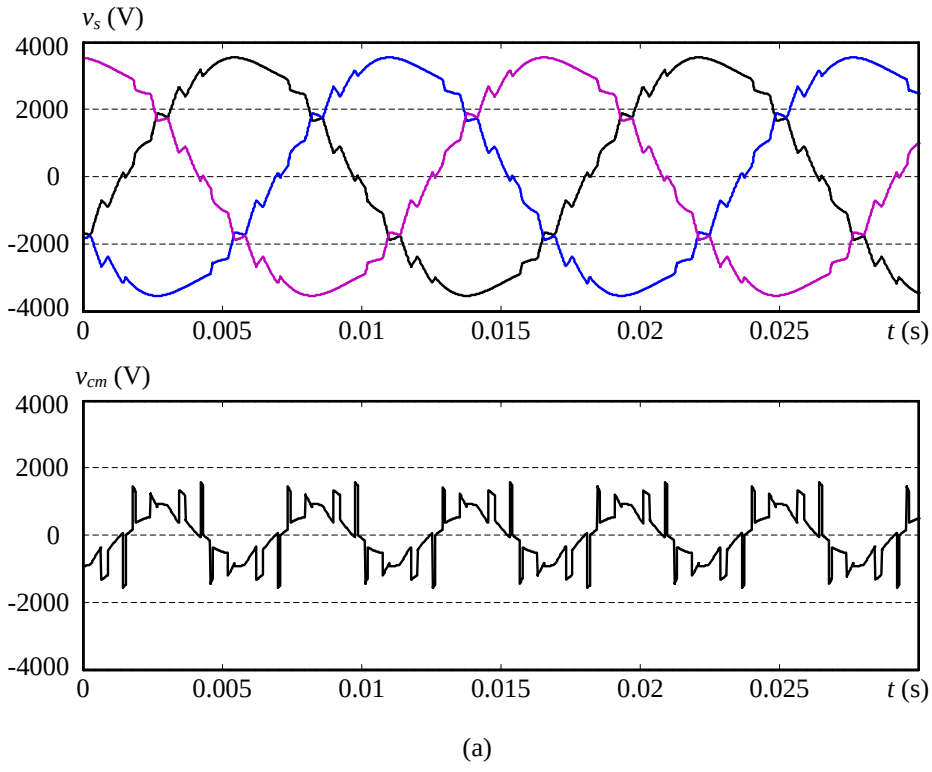
Table 2-6 Simulation parameters of a 1MVA/4160V CSI with TPWM, SHE and SVM.

System parameters	TPWM	SHE	SVM
DC current source, I_{dc}	220.7 A	183.8 A	218.1 A
Modulation index, m_a	0.85	1.0	0.9
Number of pulses per half cycle of the PWM current i_w, N_p	9	7	9
Device switching frequency, f_{sw}	540 Hz	420 Hz	540 Hz (Sampling *freq.* f_{sp} = 1080 Hz)

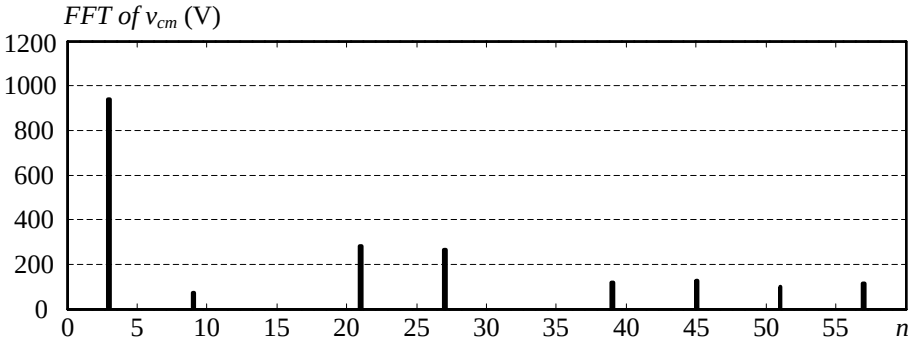
Fig. 2-20 shows the simulation results with selective harmonic elimination (SHE) modulation, in which the fifth, seventh and eleventh harmonics have been eliminated. The switching frequency was f_{sw} = 420 Hz. The SHE method also produces a CMV waveform that does not exceed half the phase voltage magnitude and a spectrum similar to that generated by TPWM, with the majority of the CMV at the triple fundamental frequency.

Fig. 2-21 (a) provides the output and CM voltages, as well as gating signals for S_1 and S_4 of the CSI with space vector modulation (SVM). High spikes are seen in the CMV waveform, which has a maximum value of 3390 V (approximately 1.41 pu), close to the phase voltage amplitude. The CMV spectrum shown in Fig. 2-21 (b) presents a larger component at three times the fundamental frequency and more even distributions throughout the triplen frequencies than those in Figs. 2-19 (b) and 2-20 (b). It should be noted that the dc-link current in the simulations

has been adjusted for almost the same output voltage at 4160 V (line-to-line rms value) with different modulation indices. For SVM, the definition of amplitude modulation index is the ratio of the peak value of the fundamental-frequency component in PWM current to the dc current, i.e., $\hat{I}_{w1}/I_{dc}$. In this situation, the CMV magnitude generated by SVM is twice as large as those generated by the TPWM and SHE schemes.



(a)



(b)

Fig. 2-19 Simulation results of a 1MVA/4160V CSI with TPWM operating at m_a = 0.85 and f_{sw} = 540 Hz. (a) The upper: three-phase output voltages v_s; the lower: CMV v_{cm}. (b) FFT of v_{cm}.

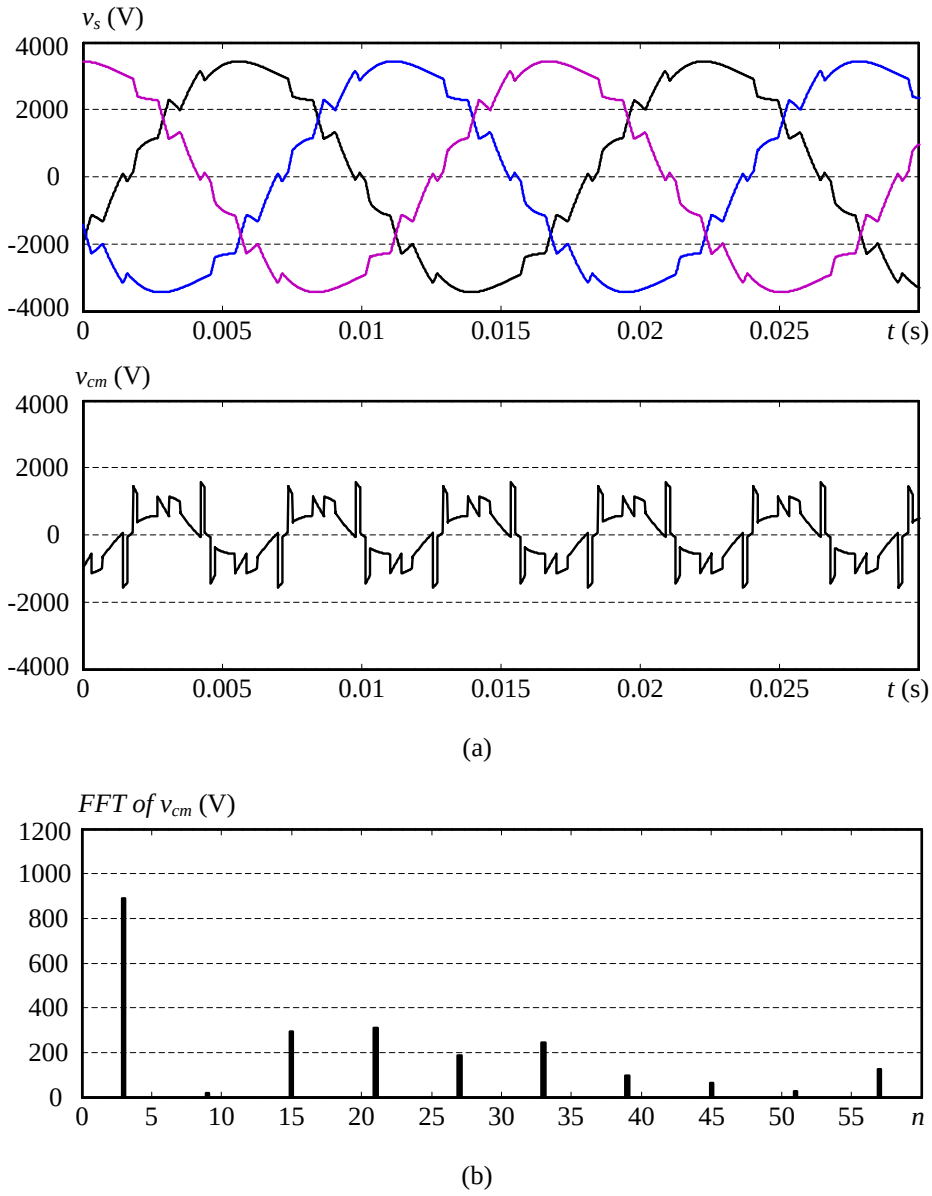


Fig. 2-20 Simulation results of the 1MVA/4160V CSI with SHE modulation eliminating the fifth, seventh and eleventh harmonics. (a) The upper: three-phase output voltages v_s; the lower: CMV v_{cm}. (b) FFT of v_{cm}.

What causes the CMV spikes in Fig. 2-21 (a)? Why does the CMV of a CSC distribute primarily at the triple fundamental frequency, rather than at the higher switching frequency as that of a VSC? These two questions will be answered in the following sections.

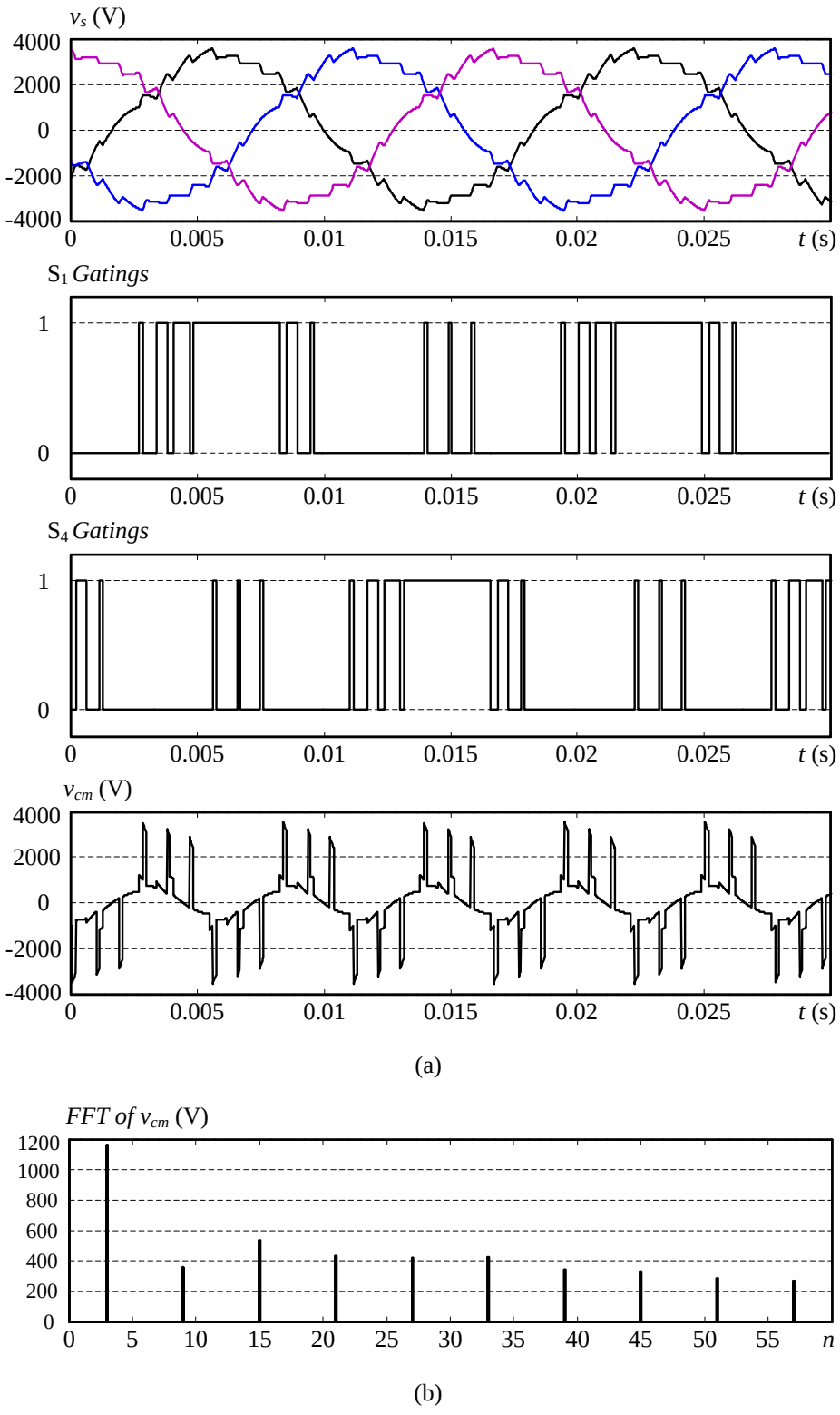


Fig. 2-21 Simulation results of the 1MVA/4160V CSI with SVM operating at m_a = 0.9 and f_{sw} = 540 Hz. (a) From top to bottom: three-phase output voltages v_s, gating signals for S_1 and S_4, and the CMV v_{cm}. (b) FFT of v_{cm}.

2.4.1 Anlysis of CMV Magnitude

The CMV waveforms through Figs 2-19 (a) to 2-21 (a) look messy compared to those in VSCs. The latter are constituted by fractions of the dc voltage, whereas the former can be derived by substituting the switching states into (2-2). Table 2-7 lists the CMV values at all switching states in a balanced three-phase CSI. The zero states produce the CMVs with full phase voltages, whereas the CMVs at the active states equal half the phase voltages. The chopped three-phase voltages make up the messy CMV waveforms in CSCs. TPWM and conventional SHE modulation schemes do not involve zero states. On the other hand, Fig. 2-21 (a) manifests the consistency between high spikes of the CMV and zero states of SVM. However, it is not always true that the zero states produce the CMV peak values. As instantaneous values, the active-state CMVs are not necessarily smaller than those at the zero states. The operating conditions of a CSI drive also play a role in the CMV magnitude.

Table 2-7 Relationship between the CMV values and CSI switching states.

Type	Zero states			Active states					
Switching state	[1, 4]	[3, 6]	[5, 2]	[6, 1]	[1, 2]	[2, 3]	[3, 4]	[4, 5]	[5, 6]
On-state switches	S_1, S_4	S_3, S_6	S_5, S_2	S_6, S_1	S_1, S_2	S_2, S_3	S_3, S_4	S_4, S_5	S_5, S_6
Space vector	$\vec{I}_0$			$\vec{I}_1$	$\vec{I}_2$	$\vec{I}_3$	$\vec{I}_4$	$\vec{I}_5$	$\vec{I}_6$
$v_{cm\text{-}inv}$	$-v_{ao}$	$-v_{bo}$	$-v_{co}$	$v_{co}/2$	$v_{bo}/2$	$v_{ao}/2$	$v_{co}/2$	$v_{bo}/2$	$v_{ao}/2$

The inverter PWM current i_w is adjusted by bypassing the dc-link current via shoot-through operation of the appropriate phase leg. The shoot-though operation is normally inserted in the long conducting duration of the switching devices. Thus, the zero states are located around the

peak of the output current, or in the vicinity of the 90˚ position of i_w [105, 120, 121]. When the angle φ_w between the phase voltage v_s (v_{ao}, for example) and i_w (i_{wa}, in this case) is out of a certain range, the CMV values produced by the zero states could be smaller than those at the active states. Let us consider a light-load condition given in Fig. 2-22 (a) for an induction motor drive. While the flux excitation is kept almost constant, the required steady-state torque is quite small, making the machine's power factor very low [107, 113, 122]. The resultant large value of φ_w may lead to the zero-state CMVs smaller than the active-state ones. This means the active vectors would generate the CMV peaks, which rise with the increase of the angle φ_w, but never exceed half the phase voltage amplitude. The situation is similar to that with TPWM and SHE schemes.

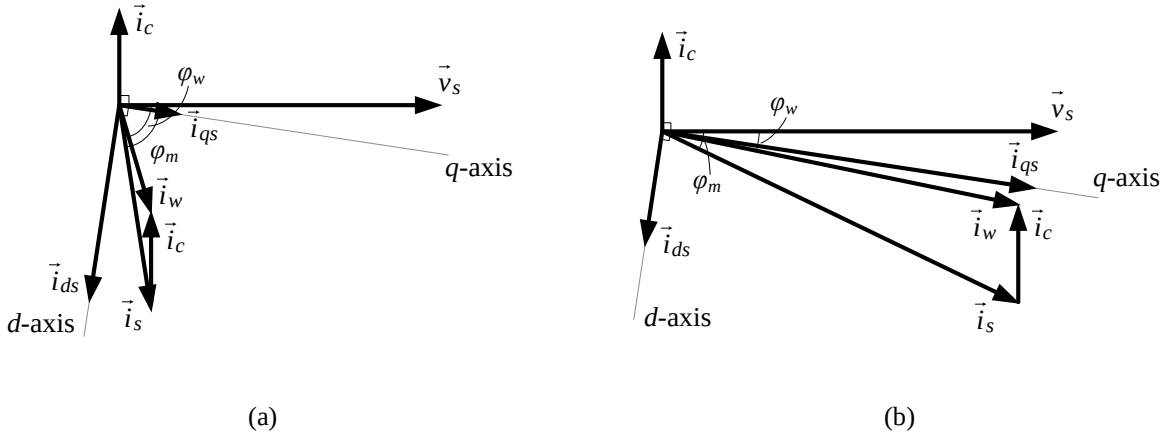


Fig. 2-22 Operating conditions of a CSI-fed motor drive. (a) Light-load condition. (b) Heavy-load condition (high load power factor).

As the filter capacitor compensates for the load lagging reactive current, the previously described situation is an extreme case. On the other hand, a more common situation in CSI-fed drives is that the zero states of SVM produce the CMV peaks. This is guaranteed by $|\varphi_w| \le 60°$.

As illustrated in Fig. 2-22 (b), when a larger torque is required, the drive operates under a heavier load condition, meaning a relatively high load power factor. With the compensation effect of the capacitor current i_c, the angle φ_w easily falls in the range of $|\varphi_w| \le 60°$. In the worst case, the CMV peaks produced by the zero vectors could be as large as the phase voltage amplitude, i.e., twice the values for TPWM and SHE schemes.

The aforementioned analysis focused on the inverter of a current-source-fed drive, but it can be extended to the PWM rectifier. Considering a near-unity power factor for the CSR, the PWM current should lag behind the grid voltage, because it has to compensate for the leading capacitive current. However, with the normal filter capacitance in the range of 0.3–0.6 pu, the angle between the PWM current and grid phase voltage would make the SVM zero states produce the maximum value of the CMV in the CSR.

2.4.2 Analysis of CMV Spectrum

The switching constraints for CSCs lead to identical pulse patterns for all the switching devices, and a 60˚ interval of the fundamental cycle between the pulse patterns of two switches that are adjacently numbered per Fig. 2-18 [1, 123, 124].

It is assumed that the angle φ_w between the phase voltage v_s and PWM current i_w is constant in steady state, and the fundamental components of the PWM currents are

$$\begin{cases} i_{wa,1} = \sqrt{2} \cdot I_{w1} \sin(\omega t) \\ i_{wb,1} = \sqrt{2} \cdot I_{w1} \sin(\omega t - 120°) \\ i_{wc,1} = \sqrt{2} \cdot I_{w1} \sin(\omega t + 120°) \end{cases}, \tag{2-18}$$

where I_{w1} denotes the rms fundamental-frequency current. By filtering the harmonics, the ac phase voltages are ideally written as:

$$\begin{cases} v_{ao} = \sqrt{2} \cdot V_s \sin\left(\omega t + \varphi_w\right) \\ v_{bo} = \sqrt{2} \cdot V_s \sin\left(\omega t + \varphi_w - 120°\right), \\ v_{co} = \sqrt{2} \cdot V_s \sin\left(\omega t + \varphi_w + 120°\right) \end{cases} \tag{2-19}$$

where V_s is the rms phase voltage.

Considering the duration of ωt = 0˚–60˚, no matter what the modulation scheme is, the adopted active switching states are [5, 6] and [6, 1], and the zero state is [3, 6] if there is (for SVM). Referring to Table 2-7, the respective CMV values are $v_{cm} = v_{ao}/2$, $v_{co}/2$ and $-v_{bo}$. When ωt = 120˚–180˚ and the switching states [1, 2], [2, 3] and the optional zero state [2, 5] are selected, the CMV values are $v_{cm} = v_{bo}/2$, $v_{ao}/2$ and $-v_{co}$, respectively. During ωt = 240˚–300˚, the employment of switching states [3, 4], [4, 5] and [1, 4] generates the CMV values at $v_{cm} = v_{co}/2$, $v_{bo}/2$ and $-v_{ao}$. According to the sequential order of identical pulse patterns for the switches and the phase sequence of the voltages, switching states [5, 6], [1, 2] and [3, 4] in the durations of 0˚–60˚, 120˚–180˚ and 240˚–300˚ would produce the same CMVs. The equality of CMV values also occurs at the other corresponding states. These situations are similar when 60˚ ≤ ωt < 120˚, 180˚ ≤ ωt < 240˚ and 300˚ ≤ ωt < 360˚. Table 2-8 lists all the circumstances in which the equal CMVs are represented by the sinusoidal voltage expressions of (2-19) with the defined angle $\theta = \omega t$ in the range of 0˚–120˚.

Table 2-8 CMV values and their equality at all switching states in different 60˚ intervals of a fundamental cycle.

ωt duration	Switching state	CMVs	CMV values	CMV values with $0^\circ \le \theta < 120^\circ$
0˚–60˚	[5, 6]	$v_{ao}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w\right)$
	[6, 1]	$v_{co}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w+120^\circ\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w+120^\circ\right)$
	[3, 6]	$-v_{bo}$	$-\sqrt{2}\cdot V_s \sin\left(\omega t+\varphi_w-120^\circ\right)$	$-\sqrt{2}\cdot V_s \sin\left(\theta+\varphi_w-120^\circ\right)$
60˚–120˚	[6, 1]	$v_{co}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w+120^\circ\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w+120^\circ\right)$
	[1, 2]	$v_{bo}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w-120^\circ\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w-120^\circ\right)$
	[1, 4]	$-v_{ao}$	$-\sqrt{2}\cdot V_s \sin\left(\omega t+\varphi_w\right)$	$-\sqrt{2}\cdot V_s \sin\left(\theta+\varphi_w\right)$
120˚–180˚	[1, 2]	$v_{bo}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w-120^\circ\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w\right)$
	[2, 3]	$v_{ao}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w+120^\circ\right)$
	[2, 5]	$-v_{co}$	$-\sqrt{2}\cdot V_s \sin\left(\omega t+\varphi_w+120^\circ\right)$	$-\sqrt{2}\cdot V_s \sin\left(\theta+\varphi_w-120^\circ\right)$
180˚–240˚	[2, 3]	$v_{ao}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w+120^\circ\right)$
	[3, 4]	$v_{co}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w+120^\circ\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w-120^\circ\right)$
	[3, 6]	$-v_{bo}$	$-\sqrt{2}\cdot V_s \sin\left(\omega t+\varphi_w-120^\circ\right)$	$-\sqrt{2}\cdot V_s \sin\left(\theta+\varphi_w\right)$
240˚–300˚	[3, 4]	$v_{co}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w+120^\circ\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w\right)$
	[4, 5]	$v_{bo}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w-120^\circ\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w+120^\circ\right)$
	[1, 4]	$-v_{ao}$	$-\sqrt{2}\cdot V_s \sin\left(\omega t+\varphi_w\right)$	$-\sqrt{2}\cdot V_s \sin\left(\theta+\varphi_w-120^\circ\right)$
300˚–360˚	[4, 5]	$v_{bo}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w-120^\circ\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w+120^\circ\right)$
	[5, 6]	$v_{ao}/2$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\omega t+\varphi_w\right)$	$\left(\sqrt{2}/2\right)\cdot V_s \sin\left(\theta+\varphi_w-120^\circ\right)$
	[2, 5]	$-v_{co}$	$-\sqrt{2}\cdot V_s \sin\left(\omega t+\varphi_w+120^\circ\right)$	$-\sqrt{2}\cdot V_s \sin\left(\theta+\varphi_w\right)$

The conclusion from Table 2-8 is that the CMV has a period of one third the fundamental cycle. In other words, the triple frequency is the fundamental frequency of the CMV. This has been observed in the waveforms through Figs. 2-19 (a) to 2-21 (a). Hence, dissimilar to the CMVs in VSCs, the majority of the CMVs in CSCs are distributed at the triple fundamental frequency and it is almost impossible to avoid the components in the low frequency range. This is determined by the CMV composition and switching constraints for CSCs, regardless of the applied modulation methods.

2.5 Summary

This chapter provided a comprehensive analysis of the common-mode voltages in various power converters including diode and SCR rectifiers, two-level and multilevel voltage-source converters, voltage-source-fed drives, and current-source converters.

The characteristics of both the magnitude and spectrum were revealed theoretically and by simulation. In diode and SCR rectifiers, the CMV magnitudes are determined by three-phase ac voltages and the CMV components at the triple fundamental frequency dominate the spectra. The common-mode voltages in VSCs are stepwise waveforms with fractional values of the dc voltage. They are mainly distributed in the medium frequency range, i.e., at the switching frequency and sidebands of its integral multiples. The CMV components in the low frequency range are generated by the low-order triplen harmonic injection in modulation, e.g. space-vector modulation. The lowest CMV distribution with sinusoidal pulse-width modulation is at the switching frequency, which is favorable for the filter and choke design. Synchronous modulation between the rectifier and inverter in a back-to-back PWM VSC-based motor drive can reduce the

CMV magnitude and the primary component at the switching frequency. As a result of the switching constraints for current-source converters, the common-mode voltages are dominant at the third and other triplen fundamental frequencies (in the low frequency range). Due to the zero states, the CMV magnitude with SVM could be twice the value with trapezoidal PWM and conventional SHE modulation schemes under normal operating conditions.

Chapter 3

An Integrated AC Choke for CMV Suppression in Voltage-Source Converters

As analyzed in Chapter 2, common-mode voltages (CMVs) in voltage-source converter (VSC) systems are dominant around the switching frequency and its integral multiples, in the medium frequency range. No triplen CMV component in the low frequency range is generated by sinusoidal pulse-width modulation (SPWM). As also pointed out in Chapter 1, the deterioration in harmonic distortion and the shrinkage of the linear modulation region come along with the CMV magnitude reduction by modulation schemes. Moreover, the elimination of CMVs in two-level, three-leg VSCs is almost impossible [36-39, 48]. Therefore, common-mode (CM) chokes, in coordination with other filter components, provide a reliable and effective solution to the CMV issues from the facet of spectrum, rather than magnitude.

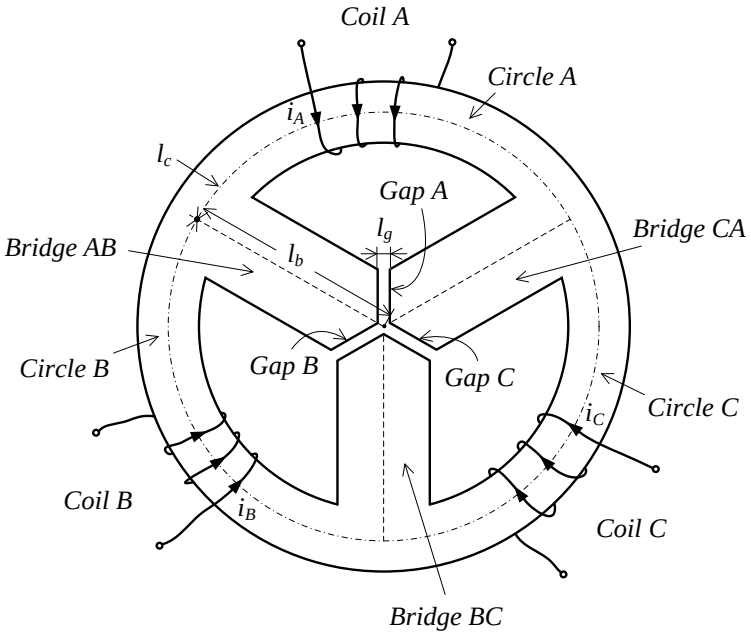
Since a differential-mode (DM) inductor is normally indispensable on the grid side of a VSC system, it is desirable to incorporate the CM choke's suppression function into the DM reactor for size and cost savings [3, 68, 69]. A novel integrated ac choke is proposed in this chapter, which not only filters the DM waveforms, but also blocks the CMV in the medium frequency range. The structure-optimized design saves the iron and copper materials, reduces the weight and cost, and improves the system efficiency. The integrated choke is tailor-made for the special

applications with stringent space and weight requirements, e.g., the electric systems on airplanes [2].

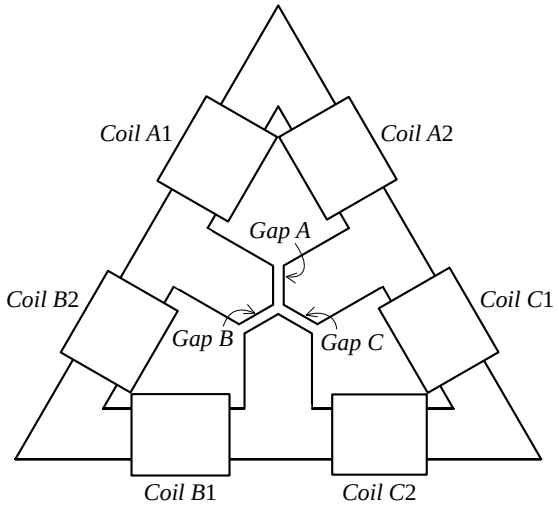
Following the description of proposed configurations of the integrated choke, this chapter analyzes the magnetic equivalent circuit and calculates the DM and CM fluxes and inductances. An equation-solving-based approach is then applied to the weight-minimized design. A minor core loss produced in the choke confirms the heat dissipation capability. The existence and uniqueness of the optimization are proven by a design example. The benefits of magnetic integration are identified via a comparison between the proposed choke and separate DM and CM inductors. The integrated choke is modeled and simulated by the finite element method (FEM) in Ansoft/Maxwell, which tunes the design parameters and verifies the concept. Finally, the experimental results of a prototype in a VSC validate the effectiveness of the integrated choke.

3.1 Proposed Structures

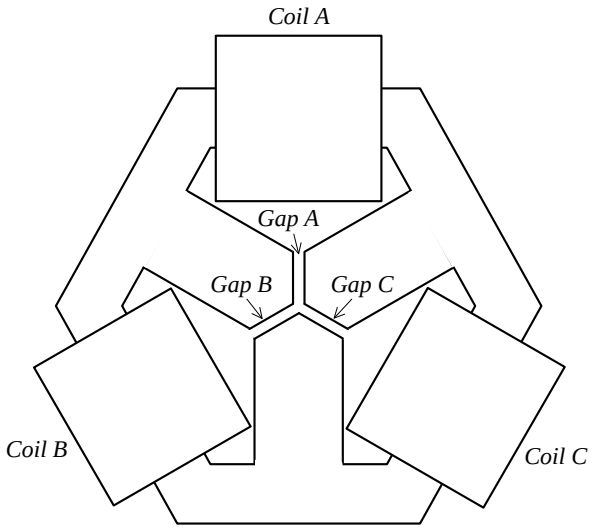
The proposed magnetic structures are illustrated in Fig. 3-1, where the circular mechanical outline is the most compact assembly with the smallest size and weight, compared to its triangular and hexagonal counterparts. In Fig. 3-1 (a), the core of the circular choke is composed of a ring (periphery) and three evenly distributed bridge legs. The three-phase coils are wound on the divided parts of the circumference in the same direction. Air gaps are located in the centre in order to be exclusive to their own phases and to avoid mechanical instability when the choke is running.



(a)



(b)



(c)

Fig. 3-1 Mechanical outlines of the integrated choke. (a) Circular-shaped structure. (b) Triangular assembly. (c) Hexagonal construction.

For high-power systems with a large current rating, winding on the circular-shaped core may not be convenient without a regular bobbin. Alternatives of the triangular- and hexagonal-shaped cores are shown in Fig. 3-1 (b) and (c). The triangular configuration with split coils for each phase simplifies the fabrication, and the hexagonal assembly offers mounting ease for the choke. However, owing to the low window utilization, the triangular and hexagonal constructions are only considered in high-power converter systems, whereas the circular integrated choke is particularly suitable for low- and medium-power applications.

Although various assemblies have different geometric parameters, their principles remain the same. The following magnetic analyses, design, simulations and experimental verification will be focused on the circular integrated choke.

3.2 Magnetic Analysis

3.2.1 Equvilent Circuit

Fig. 3-2 shows the equivalent magnetic circuit of the circular integrated choke. The shape and symbols are consistent with those in Fig. 3-1 (a). Ni_A, Ni_B and Ni_C are three magnetomotive forces (MMFs) in the circuit, where N is the number of turns of the coils; i_A, i_B and i_C are three-phase currents including both the DM and CM parts. $\Re_{c-A}$, $\Re_{c-B}$ and $\Re_{c-C}$ are the reluctances of *Circle A*, *Circle B* and *Circle C*, each of which is one third the circular core in Fig. 3-1 (a). These reluctances are represented by

$$\Re_{c-A} = \Re_{c-B} = \Re_{c-C} = \frac{\Re_c}{3} = \frac{l_c}{3\mu_0\mu_r \cdot A_c}, \tag{3-1}$$

where $\Re_c$ is the reluctance of the whole circular core; l_c and A_c are the mean circumference and cross-sectional area of the circle; μ_0 and μ_r denote the absolute permeability of free space and relative permeability of the core material. The reluctances of the inner legs, *Bridge AB, Bridge BC* and *Bridge CA* are calculated by

$$\Re_{b-AB} = \Re_{b-BC} = \Re_{b-CA} = \Re_b = \frac{l_b}{\mu_0 \mu_r \cdot A_b}, \tag{3-2}$$

where l_b and A_b are the length and cross-sectional area of the bridge legs. The reluctances of the gaps are

$$\Re_{g-A} = \Re_{g-B} = \Re_{g-C} = \Re_g = \frac{l_g}{\mu_0 \cdot \left(A_b / \sqrt{3}\right)}, \tag{3-3}$$

where l_g is the air-gap length.

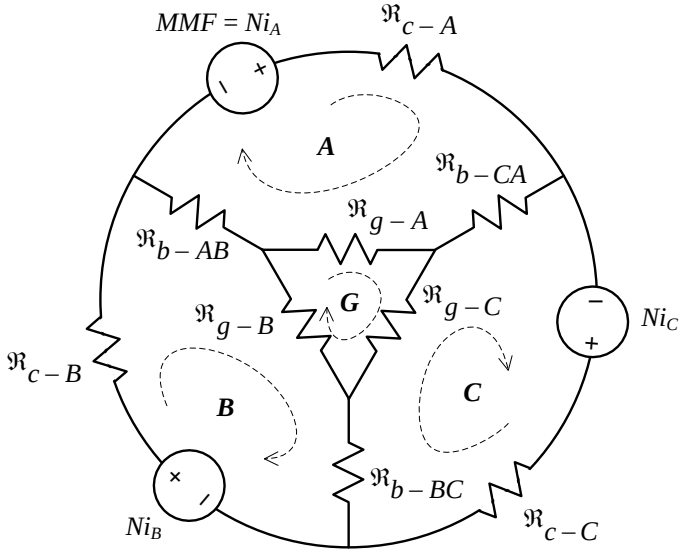


Fig. 3-2 Equivalent magnetic circuit of the circular-shaped integrated choke.

There are a total of four meshes in the equivalent circuit. Meshes *A*, *B* and *C* correspond to the three-phase magnetic paths and mesh *G* represents the air-gap loop. With the MMFs and reluctances, fluxes all over the circuit can be solved using a mesh method.

3.2.2 Flux Calculation

With the directions assumed in Fig. 3-2, a matrix equation can be listed below,

$$\Re \cdot \Phi = F\,, \tag{3-4}$$

where the flux matrix is $\Phi = \begin{bmatrix} \Phi_A & \Phi_B & \Phi_C & \Phi_G \end{bmatrix}^T$, the MMF matrix is $F = \begin{bmatrix} Ni_A & Ni_B & Ni_C & 0 \end{bmatrix}^T$, and the reluctance matrix is

$$\Re = \begin{bmatrix} \left(\Re_c/3 + 2\Re_b + \Re_g\right) & -\Re_b & -\Re_b & -\Re_g \\ -\Re_b & \left(\Re_c/3 + 2\Re_b + \Re_g\right) & -\Re_b & -\Re_g \\ -\Re_b & -\Re_b & \left(\Re_c/3 + 2\Re_b + \Re_g\right) & -\Re_g \\ -\Re_g & -\Re_g & -\Re_g & 3\Re_g \end{bmatrix}. \tag{3-5}$$

The flux matrix is then obtained by solving the equation,

$$\Phi=\begin{bmatrix}\Phi_A\\ \Phi_B\\ \Phi_C\\ \Phi_G\end{bmatrix}=\begin{bmatrix}\dfrac{Ni_A\left(\Re_c/3+\Re_b+\Re_g/3\right)}{\left(\Re_c/3\right)\cdot\left(\Re_c/3+3\Re_b+\Re_g\right)}+\dfrac{Ni_B\left(\Re_b+\Re_g/3\right)}{\left(\Re_c/3\right)\cdot\left(\Re_c/3+3\Re_b+\Re_g\right)}+\dfrac{Ni_C\left(\Re_b+\Re_g/3\right)}{\left(\Re_c/3\right)\cdot\left(\Re_c/3+3\Re_b+\Re_g\right)}\\ \dfrac{Ni_A\left(\Re_b+\Re_g/3\right)}{\left(\Re_c/3\right)\cdot\left(\Re_c/3+3\Re_b+\Re_g\right)}+\dfrac{Ni_B\left(\Re_c/3+\Re_b+\Re_g/3\right)}{\left(\Re_c/3\right)\cdot\left(\Re_c/3+3\Re_b+\Re_g\right)}+\dfrac{Ni_C\left(\Re_b+\Re_g/3\right)}{\left(\Re_c/3\right)\cdot\left(\Re_c/3+3\Re_b+\Re_g\right)}\\ \dfrac{Ni_A\left(\Re_b+\Re_g/3\right)}{\left(\Re_c/3\right)\cdot\left(\Re_c/3+3\Re_b+\Re_g\right)}+\dfrac{Ni_B\left(\Re_b+\Re_g/3\right)}{\left(\Re_c/3\right)\cdot\left(\Re_c/3+3\Re_b+\Re_g\right)}+\dfrac{Ni_C\left(\Re_c/3+\Re_b+\Re_g/3\right)}{\left(\Re_c/3\right)\cdot\left(\Re_c/3+3\Re_b+\Re_g\right)}\\ \dfrac{Ni_A}{\Re_c}+\dfrac{Ni_B}{\Re_c}+\dfrac{Ni_C}{\Re_c}\end{bmatrix}. \tag{3-6}$$

The fluxes of the meshes, Φ_A, Φ_B and Φ_C, are equal to those filling in each one-third part of the circular core, $\Phi_{c\text{-}A}$, $\Phi_{c\text{-}B}$ and $\Phi_{c\text{-}C}$, respectively. Based on the solution, we can further calculate the fluxes in the bridge legs and air gaps through

$$\begin{cases}\Phi_{b-AB}=\Phi_A-\Phi_B=\dfrac{N\left(i_A-i_B\right)}{\left(\Re_c/3+3\Re_b+\Re_g\right)}\\ \Phi_{b-BC}=\Phi_B-\Phi_C=\dfrac{N\left(i_B-i_C\right)}{\left(\Re_c/3+3\Re_b+\Re_g\right)},\\ \Phi_{b-CA}=\Phi_C-\Phi_A=\dfrac{N\left(i_C-i_A\right)}{\left(\Re_c/3+3\Re_b+\Re_g\right)}\end{cases} \tag{3-7}$$

and

$$\begin{cases}\Phi_{g-A}=\Phi_A-\Phi_G\\ \Phi_{g-B}=\Phi_B-\Phi_G\\ \Phi_{g-C}=\Phi_C-\Phi_G\end{cases}. \tag{3-8}$$

Because of the complexity, (3-8) has not been fully expressed in its general form, but the separate DM and CM fluxes will be considerably simplified. The inductance can also be calculated by substituting the respective excitations and using the relationships of the three-phase currents as follows.

3.2.3 Differential-Mode Inductance

With balanced three-phase DM currents, $\begin{cases} i_{dm,A} = I_{ac,peak} \cdot \sin(\omega t) \\ i_{dm,B} = I_{ac,peak} \cdot \sin(\omega t - 120°) \\ i_{dm,C} = I_{ac,peak} \cdot \sin(\omega t + 120°) \end{cases}$, which have a relationship of $i_{dm,A} + i_{dm,B} + i_{dm,C} = 0$, the DM fluxes are simplified as,

$$\begin{cases} \Phi_{dm,c-A} = \Phi_{dm,g-A} = \dfrac{Ni_{dm,A}}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} = \dfrac{NI_{ac,peak} \cdot \sin(\omega t)}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} \\ \Phi_{dm,c-B} = \Phi_{dm,g-B} = \dfrac{Ni_{dm,B}}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} = \dfrac{NI_{ac,peak} \cdot \sin(\omega t - 120°)}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} \\ \Phi_{dm,c-C} = \Phi_{dm,g-C} = \dfrac{Ni_{dm,C}}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} = \dfrac{NI_{ac,peak} \cdot \sin(\omega t + 120°)}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} \end{cases}, \quad (3\text{-}9)$$

and

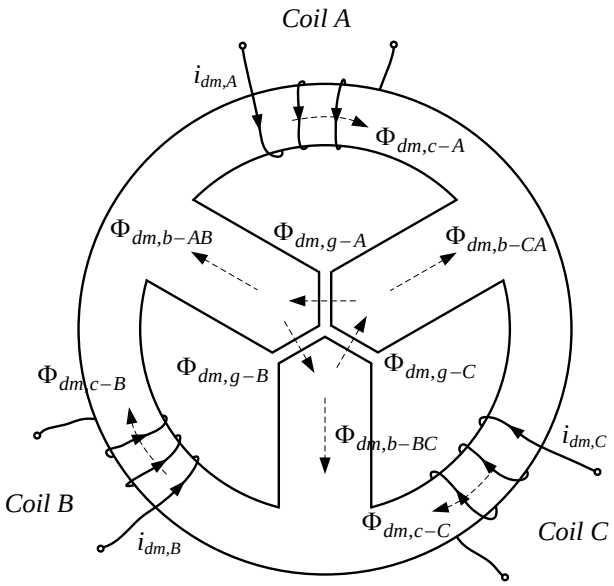
$$\begin{cases} \Phi_{dm,b-AB} = \dfrac{N\left(i_{dm,A} - i_{dm,B}\right)}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} = \dfrac{N\sqrt{3}I_{ac,peak}\cdot\sin\left(\omega t + 30°\right)}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} \\ \Phi_{dm,b-BC} = \dfrac{N\left(i_{dm,B} - i_{dm,C}\right)}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} = \dfrac{N\sqrt{3}I_{ac,peak}\cdot\sin\left(\omega t - 90°\right)}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} \\ \Phi_{dm,b-CA} = \dfrac{N\left(i_{dm,C} - i_{dm,A}\right)}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} = \dfrac{N\sqrt{3}I_{ac,peak}\cdot\sin\left(\omega t + 150°\right)}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} \end{cases}. \quad (3\text{-}10)$$

According to (3-9) and (3-10), the DM fluxes filling in one-third part of the ring core and the air gaps are only induced by the corresponding phase current, called the "phase flux". On the other hand, the flux in the bridge legs is the difference between two adjacent phase fluxes and is named the "bridge flux." Fig. 3-3 (a) displays the DM magnetic flux distributions.

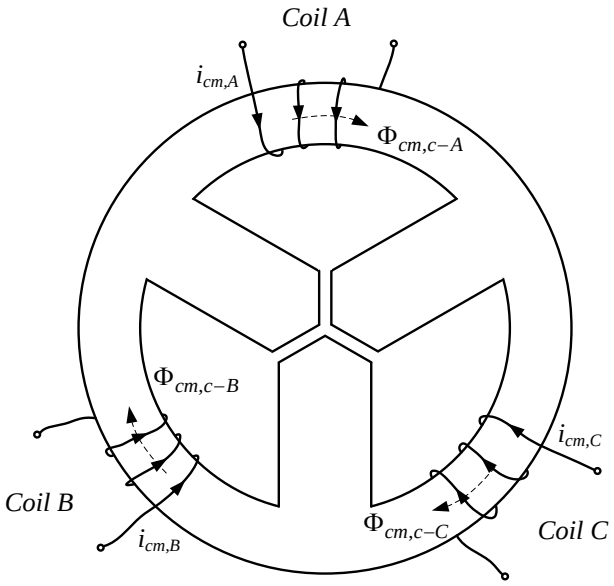
The DM inductance per phase is then derived from its definition and the previous flux calculations:

$$L_{dm} = \frac{N\Phi_{dm,c}}{i_{dm}} = \frac{N^2}{\left(\Re_c/3 + 3\Re_b + \Re_g\right)} \approx \frac{N^2\mu_0\cdot\left(A_b/\sqrt{3}\right)}{l_g}, \quad (3\text{-}11)$$

where $\Phi_{dm,c}$ and i_{dm} represent the DM flux in any one-third part of the ring core and the corresponding phase current. The approximation in (3-11) is made by choosing a core material whose relative permeability: $\mu_r >> 1$. This means the DM inductance primarily depends on the air-gap geometries rather than any other core parts.



(a)



(b)

Fig. 3-3 Magnetic flux distributions. (a) Produced by DM currents. (b) Produced by CM currents.

3.2.4 Common-Mode Inductance

Substitution of CM currents, $i_{cm,A} = i_{cm,B} = i_{cm,C} = i_{cm}/3$ (assuming that the balanced three phases which are connected in parallel for the CM analysis equally share the total current i_{cm}), into (3-6) through (3-8) generates the CM fluxes,

$$\Phi_{cm,c-A} = \Phi_{cm,c-B} = \Phi_{cm,c-C} = \Phi_{cm} = \frac{Ni_{cm}}{\Re_c}; \tag{3-12}$$

$$\Phi_{cm,b-AB} = \Phi_{cm,b-BC} = \Phi_{cm,b-CA} = 0; \tag{3-13}$$

and

$$\Phi_{cm,g-A} = \Phi_{cm,g-B} = \Phi_{cm,g-C} = \Phi_{cm} - \Phi_G = 0. \tag{3-14}$$

As illustrated in Fig. 3-3 (b), the CM fluxes in the peripheral core have the same polarity, and those in the bridge legs and air gaps cancel each other out, which then equals zero.

Hence, the CM inductance of each phase is

$$L_{cm,ep} = \frac{N\Phi_{cm}}{i_{cm}/3} = \frac{3N^2}{\Re_c} = \frac{3N^2}{l_c}\mu_0\mu_r \cdot A_c, \tag{3-15}$$

and the whole CM inductance is one-third of (3-15)

$$L_{cm,w} = \frac{L_{cm,ep}}{3} = \frac{N^2}{l_c}\mu_0\mu_r \cdot A_c. \tag{3-16}$$

3.3 Methodology of Design Optimization

For the proposed grid-side filter application, the integrated choke should be designed to achieve the required DM inductance and sufficiently large CM inductance. The former is typically between 0.05 and 0.2 pu in a VSC, while the latter attenuates the CM current as an impedance, which is also proportional to the frequency. In the following analysis, the CM blocking function will be investigated only at the switching frequency (f_{sw}) where the CMV (v_{cm}) component is dominant in PWM VSCs. By ignoring the other trivial impedances in the CM loop for simplification, we have

$$L_{cm,w} = \frac{v_{cm}}{2\pi f_{sw} \cdot i_{cm}}. \tag{3-17}$$

The design optimization of a DM inductor is normally aimed at the minimization of its volume and weight. The maximum flux density should accordingly be set close to the saturation value. Similar to a transformer, a CM reactor requires no energy storage capability. The total loss is minimized for the CM choke optimization, requiring a minor operating flux density at the relatively high switching frequency [125, 126].

If a traditional design approach for the DM inductor is applied to the integrated choke based on magnetic circuit calculation, special attention must be paid to the power loss and heat dissipation issues in this weight-minimized design. The CM core loss at the switching frequency might be the main concern [125-127].

Note that the peripheral core of the choke is shared by both the DM and CM phase fluxes. The following equations are derived from the inductance calculation in which the peak flux densities are considered to avoid the core saturation:

$$\begin{cases} NA_c = L_{dm} \cdot I_{ac,peak} \big/ B_{dm,c\_peak} \\ NA_c = L_{cm,w} \cdot i_{cm,\max} \big/ B_{cm,c\_peak} \end{cases}, \tag{3-18}$$

where B_{dm,c_peak} and B_{cm,c_peak} are the peak values of the DM and CM flux densities in the circular part of the core, and $i_{cm,max}$ is the maximum magnetizing CM current. Because of the common number of turns and cross-sectional area, a certain ratio between the peak CM and DM flux densities exists only in terms of the electrical parameters:

$$\frac{B_{cm,c\_peak}}{B_{dm,c\_peak}} = \frac{L_{cm,w} \cdot i_{cm,\max}}{L_{dm} \cdot I_{ac,peak}} = \frac{\left(v_{cm,\max} \big/ 2\pi f_{sw}\right)}{L_{dm} \cdot I_{ac,peak}}, \tag{3-19}$$

and the sum of the flux densities has to be smaller than the saturation B_{sat},

$$B_{cm,c\_peak} + B_{dm,c\_peak} \le B_{sat} \cdot \tag{3-20}$$

Equations (3-19) and (3-20) indicate that within the definite saturation, the higher the switching frequency, the smaller the CM flux density. This relationship confirms the heat dissipation capability of the weight-minimized design because a reasonably small CM core loss will always be generated. When the core loss that is mainly contributed by the switching-frequency CM flux is as small as the copper ohmic loss with particular parameters, the CM-part

optimization is regarded as achieved and the total loss of the integrated choke approaches the minimum value, although the gap loss of the core has not been taken into account [125].

The design, based on magnetic circuit calculation, essentially uses an equation-solving method. Once the solution is acquired at the minimum-weight point, the DM inductance will be determined primarily by the air-gap geometries, whereas the CM inductance will be fixed and largely dependent on the permeability of the core material that varies with the frequency and operational point of the *B*-*H* curve. To obtain a sufficiently large CM inductance, a highly permeable material should be selected.

Laminated silicon steel is a common core material for the grid-side filter inductor in medium- and high-power systems. Take an example of the integrated choke designed for a 5kW/208V VSC using SPWM at the carrier frequency of f_{sw} = 5 kHz and the DM inductance is set to 0.12 pu, i.e., L_{dm} = 2.76 mH. For silicon steel, there is a drop in permeability at 5 kHz, compared to the dc magnetization curve. This may degrade the CM suppression performance of the integrated choke. Other materials with a stable permeability at high frequencies, such as the amorphous and nano-crystalline iron alloys, are more favorable, but in high-power applications, these materials are costly and unnecessarily used due to the lower switching frequency [125-129]. On the other hand, the high-frequency CM fluxes are superimposed on the fundamental-frequency DM fluxes in the periphery core of the choke, and at least two of the three-phase DM fluxes fall in the linear region of the *B*-*H* curve. The real CM inductance is consequently calculated from the incremental permeability, rather than the values given in manufactures' datasheets. This CM inductance, in fact, is the incremental inductance and is normally larger than the apparent inductance [130]. The determination of an accurate CM inductance is complicated by the material characteristics, which, however, are not the emphasis of this research. In the design

example, laminated silicon steel is used as the core material to validate the proposed structure and design of the integrated choke.

For simplicity, an initial relative permeability of μ_r = 4250 is assumed. Fig. 3-4 plots the choke weight tracking versus the CM-to-DM inductance ratio, where W_{tfe}, W_{tcu} and W_{tc} are weights of the core, copper and the whole choke, respectively. The minimum total weight appears around the point of $W_{tfe} = W_{tcu}$, corresponding to the inductance ratio of $L_{cm,w}/L_{dm} \approx$ 36.74 or $L_{cm,w}$ = 101.4 mH (4.41 pu). At this point, all parameters of the weight-optimized choke can be obtained from the detailed design in Appendix A. Table 3-1 lists the parameters that have been adjusted to leave margins and for prototype manufacture. The core and copper losses, as well as the temperature rising, directly prove the heat dissipation capability of the choke.

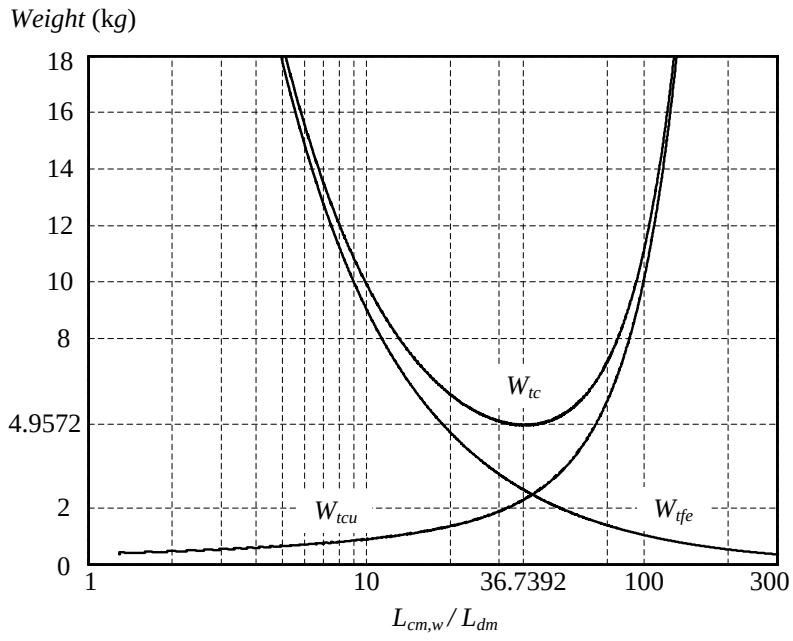


Fig. 3-4 Curves of the core, copper and total weights versus the CM-to-DM inductance ratio.

Table 3-1 Design parameters of the weight-optimized integrated choke for prototype manufacture.

Core data: 50W310 silicon steel, 0.5 mm thickness		Coil data: AWG#11	
Core sheet number	88	Number of turns, N (designed)	96
Ring width, a	1.7 cm	Number of turns, N (tuned)	88
Ring inner radius, r	4.6 cm	Mean length per turn, MLT	19.60 cm
Bridge leg width, b	2.5 cm		
Air-gap length, l_g (designed)	2.5 mm		
Air-gap length, l_g (tuned)	7.5 mm		
Weight		**Maximum losses and temperature rising**	
Copper, W_{tcu}	2.15 kg	Copper ohmic loss	41.23 W
Ring core	2.00 kg	CM core loss	22.60 W
Bridge legs	1.09 kg	DM core loss	2.16 W
Total core, W_{tfe}	3.09 kg	Total core loss	24.76 W
Total, W_{tc}	5.24 kg	Temperature rising	52.59˚C

In this design example, the minimum point of the total weight curve is taken, as shown in Fig. 3-4. However, if the converter system specified a more stringent CM current requirement, the integrated choke would have to increase in weight along the curve such that the inductance ratio could be improved. Due to the sole minimum point on the curve, the weight-optimized design that satisfies a demanded CM inductance must exist and is unique.

In terms of CM blocking function, the integrated choke is almost infinitely superior to a reactor using a three-phase EI core, because the latter has no CM impedance, except for the leakage inductance. Compared to another type of reactors composed of three single-phase inductors, which are usually employed in low-power applications, the designed integrated choke also has a better CM suppression effect by 36.74 times ($L_{cm,w}/L_{dm} \approx 36.74$ or $L_{cm,w} = 4.41$ pu and $L_{dm} = 0.12$ pu), since the CM inductance of the separate single-phase reactor is equal to its DM inductance (0.12 pu).

3.4 Comparison to Separate Inductors

As a substitute for the isolation transformer, the integrated choke undoubtedly has the advantages with a smaller size and higher efficiency. Even compared to separate DM and CM inductors, the enhancements of the integrated choke in weight and loss are still significant. Following is a quantitative comparison between the integrated choke and separate inductors under identical conditions and criteria.

The reactor with a three-phase EI core can be used as the separate DM inductor which is designed to minimize the volume and weight. The CM reactor is constructed to obtain an inductance close to that of the integrated choke with the same permeability assumption. Its total loss should also be minimized within the selection of a standard EI core from manufactures' datasheets [127]. The design parameters of the separate DM and CM reactors are listed in Appendix B. Table 3-2 extracts the comparable design data of the integrated choke and separate inductors. The improvements brought by magnetic integration are summarized as follows:

1) A 40% decrease in copper weight;
2) The same proportional (approximately 40%) copper ohmic loss reduction;
3) A 60% iron weight decline;
4) A 40% drop in CM core loss due to the less CM-part iron weight;
5) An almost 50% total weight decrement.

The copper weight and ohmic loss reduction are the result of using only one set of coils in the integrated choke. The cross-sectional area of the ring core is shared by distinct magnitudes of the CM and DM flux densities at the carrier and fundamental frequencies, respectively. Sufficient

utilization of the core saves the iron material, and the CM core loss is also lowered as a result of the lower CM-part core weight. The fact that the CM flux density in the integrated choke approaches the optimized value in the separate inductor offers further evidence of the reasonably small CM core loss.

Table 3-2 Comparison of design data between the integrated choke and separate reactors.

Comparable index	Inductor type		
	Integrated choke	Separate reactors	
		DM	CM
Max flux density (T)	0.8 (total); 0.1 (CM)	0.9	0.07
Inductance (mH)	2.76 (DM); 101.4 (CM)	2.76	101.3
Copper weight (kg)	2.15	1.68	1.96
		3.64	
Core weight (kg)	3.09	3.67	3.56
		7.23	
Total weight (kg)	5.24	5.35	5.53
		10.88	
Copper loss (W)	41.23	28.12	41.76
		69.88	
Core loss (W)	2.16 (DM); 22.60 (CM)	5.34	35.64
		40.98	

3.5 Finite Element Analysis

In the equation-solving-based design, non-linear characteristics have not been taken into account. For example, in this particular configuration, the fringing effect that would magnify the DM inductance could not be evaluated by empirical equations. As a result of the 120º angle between two bridge legs, the equivalent air-gap length is shortened more than that of typical EI cores. The fringing effect is exacerbated [126, 130, 131]. The FEA is thus necessary in tuning the design parameters with which a prototype can be implemented. Moreover, the FEM is also a

useful simulation tool to verify the electromagnetic design. Ansoft/Maxwell 13.0 will be utilized in the FEA simulation.

3.5.1 FEA Modeling

In the FEA of the integrated choke, a three-dimensional (3-D) magnetostatic model is first built to tune the design parameters. This type of solution is accurate and features adaptive meshing, ensuring convergence of the iterative calculation. With the nonlinear dc magnetization curve, static simulations validate the integrated choke by computing the magnetic flux density distributions and induced inductances. The estimation of the maximum core losses is verified by transient simulations whose meshing is linked to the previous magnetostatic model. Fig. 3-5 illustrates a 3-D image of the integrated choke model in Ansoft/Maxwell 13.0. It is worth noting that the FEA simulation differs from practical operations in that the CM current is used as excitations instead of voltage, since the latter causes a short circuit in the simulation [131].

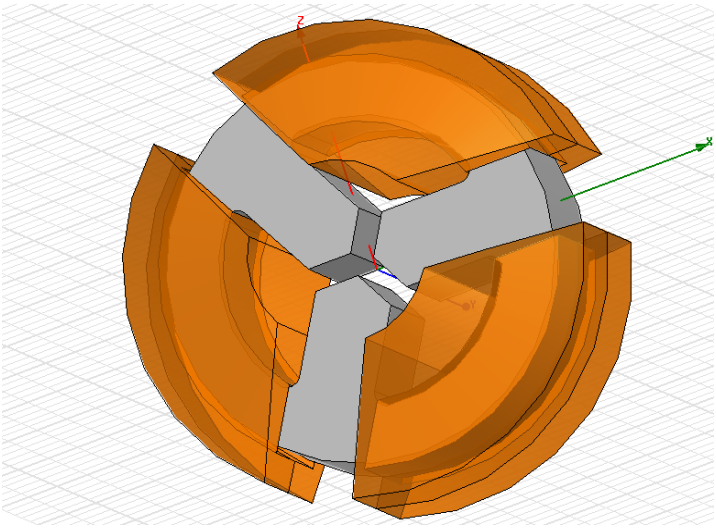


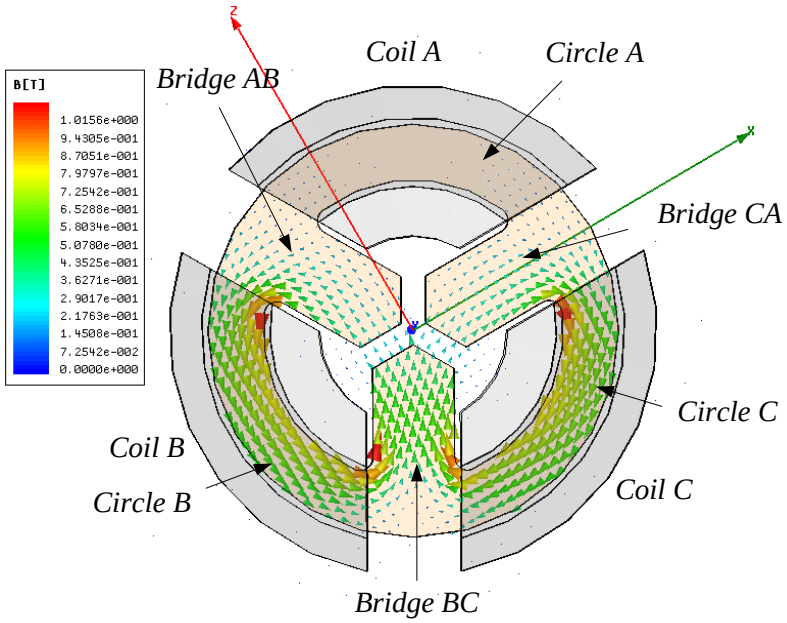
Fig. 3-5 3-D image of the integrated choke model in Ansoft/Maxwell 13.0.

3.5.2 Magnetostatic Simulations

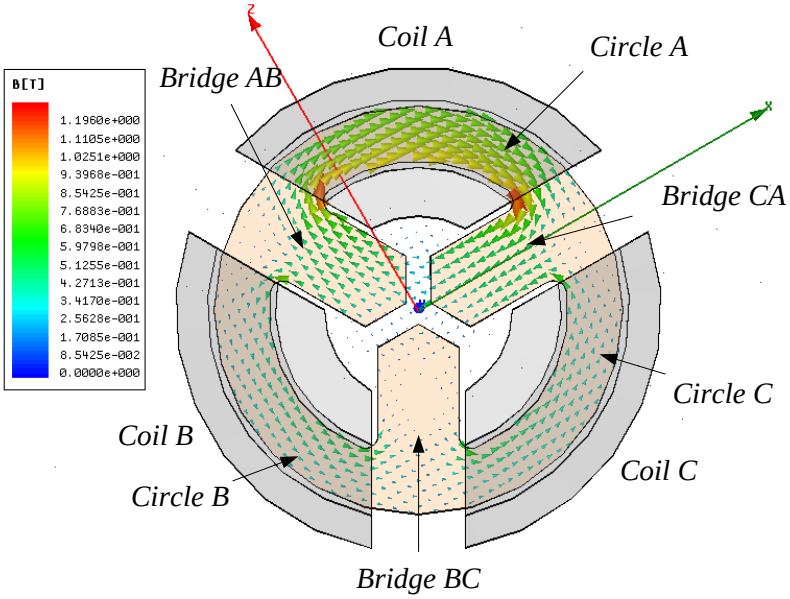
With only the DM excitations and inductance calculation, the design parameters are tuned, including a prolonged air-gap length and reduced number of turns as given in Table 3-1. Fig. 3-6 displays the flux density distributions of the choke with corrected parameters and excited by three-phase DM currents at ωt = 0º and 90˚. In the illustrations, the colour gradients of the magnetic lines denote the flux density magnitude and the arrows point out the direction. At ωt = 0º of the DM excitations, the flux density in Fig. 3-6 (a) is zero in the peripheral part *Circle A* and decreases from the inner to outer portion in the other parts of the ring core along the radial orientation. At the same time, the leg *Bridge BC* arrives at its mean maximum flux density. In Fig. 3-6 (b) at ωt = 90º, the flux density in *Circle A* achieves the maximum value and that in *Bridge BC* equals zero. The flux density values appear periodically in the circular parts and bridge legs of the core, conforming to the three-phase sinusoids. Fig. 3-6 verifies the theoretical calculation in (3-9) and (3-10). The maximum flux density is lower than the saturation. In the magnetostatic simulations, the DM inductances are calculated around 2.8 mH (0.12 pu), which coincides with the designed value.

Fig. 3-7 exhibits the maximum CM flux density distributions that are the same in all three parts of the circle and almost equal zero in the bridge legs. The magnetizing current is preset to i_{cm} = 60.12 mA (only 0.0043 pu) in terms of the designed CM inductance and the CMV that was assumed to be its magnitude of $v_{cm,max}$ = 191.5 V (1.6 pu) at f_{sw} = 5 kHz in a 5kW/208V VSC with the modulation index m_a = 0.9. The reduced number of turns would decrease the CM inductance, whereas the equivalently enlarged cross-sectional area at the connection of the peripheral core and bridge legs (see the extension of the magnetic lines to the centre through the

bridge legs in Fig. 3-7) increases the inductance. The synthetic effect results in the simulated CM inductance: $L_{cm,w}$ = 93.2 mH (4.05 pu).



(a)



(b)

Fig. 3-6 Flux density distributions (B) produced by pure DM excitations. (a) At ωt = 0°. (b) At ωt = 90°.

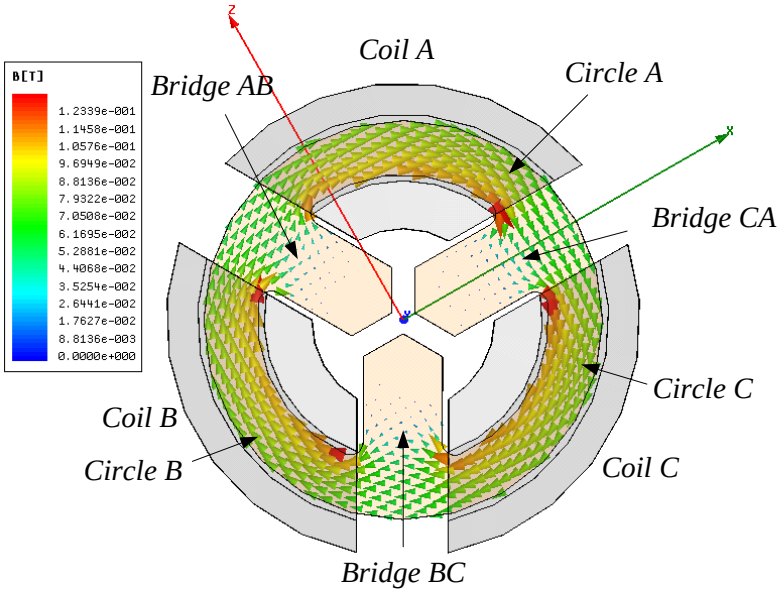
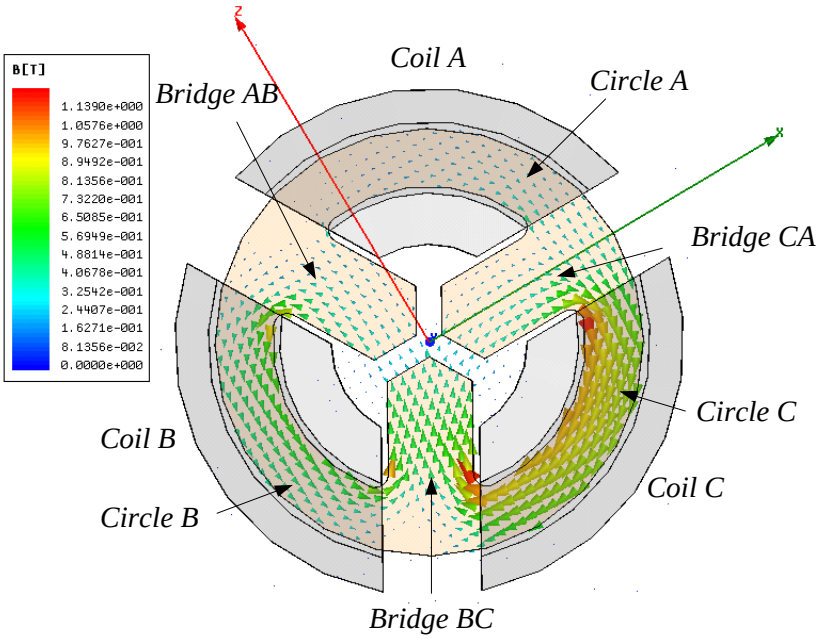
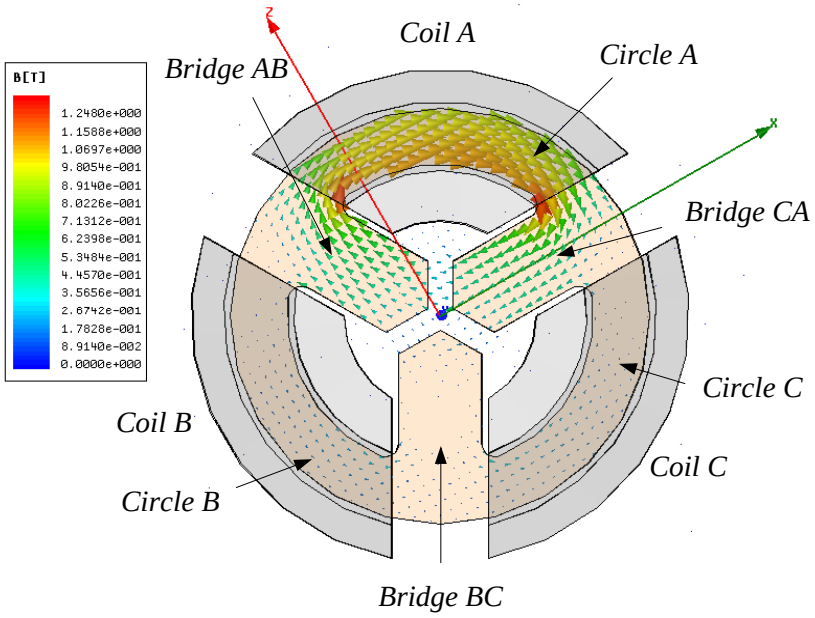


Fig. 3-7 Flux density distribution (*B*) produced only by the CM magnetizing current preset at i_{cm} = 60.12 mA (0.0043 pu).

The integrated flux densities shown in Fig. 3-8 are excited by both the DM currents, at ωt = 0º and 90˚, respectively, and the maximum CM magnetizing current. In Fig. 3-8 (a), the flux density distributions in *Circle C* and *Circle B* are no longer symmetrical as those in Fig. 3-6 (a). The superimposed flux density in *Circle C* is intensified by the DM and CM components having the same direction, but the contrary polarities of the DM and CM components in *Circle B* reduce the resultant flux density. The actual switching frequency of CM flux densities generates a rapid exchange between *Circle C* and *Circle B*. Fig. 3-8 (b) shows the maximum flux density in *Circle A*, which is the superposition of the DM and maximum CM components and achieves a mean value of 1.0 T approximately, which is below saturation.



(a)



(b)

Fig. 3-8 Flux density distributions (B) produced by both DM currents and the maximum CM magnetizing current. (a) At ωt = 0º. (b) At ωt = 90º.

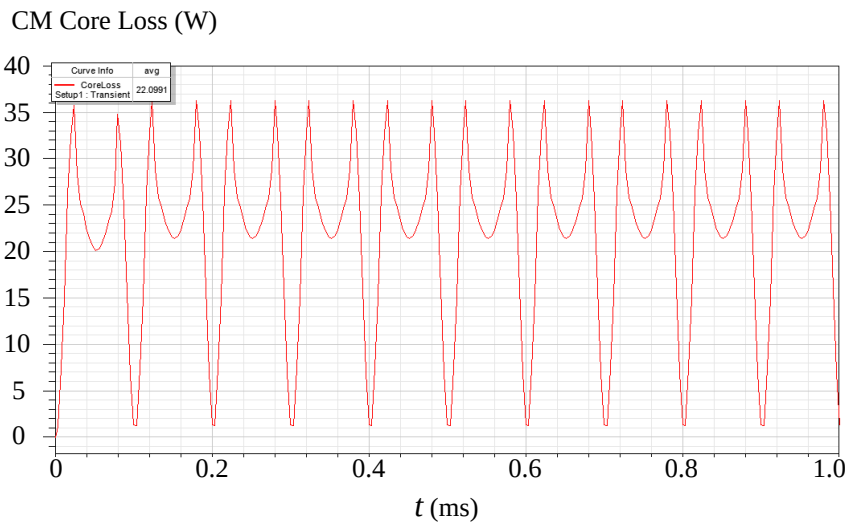
3.5.3 Loss Verification

Although it has been proven that the core loss does not result in thermal issues in the integrated choke, an equivalently parallel resistance that is attributed to the core loss exerts great influence on the CM impedance and performance. The maximum CM and DM core losses are calculated by the FEA with transient simulations. Fig. 3-9 shows the CM core loss curve with a supposed sinusoidal excitation whose magnitude is i_{cm} = 60.12 mA, and the DM core loss. Their average values are 22.1 W and 2.21 W respectively, close to the evaluation in Table 3-1. In addition, the transient simulations can provide animation for the flux density distributions, giving visible verification of the choke design at every operational point.

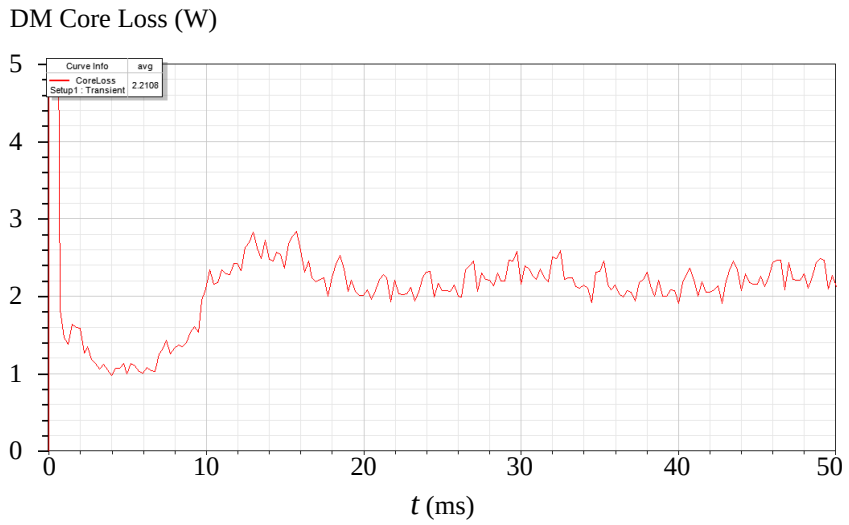
3.6 Experimental Verification

3.6.1 Prototype Setup

A prototype of the designed choke is built with silicon steel for validation. Fig. 3-10 shows photographs of the laminated core and integrated choke after winding, compared with a ballpoint pen. For the 5kW/208V VSC system, the size of the integrated choke is obviously smaller than that of separate DM and CM inductors.

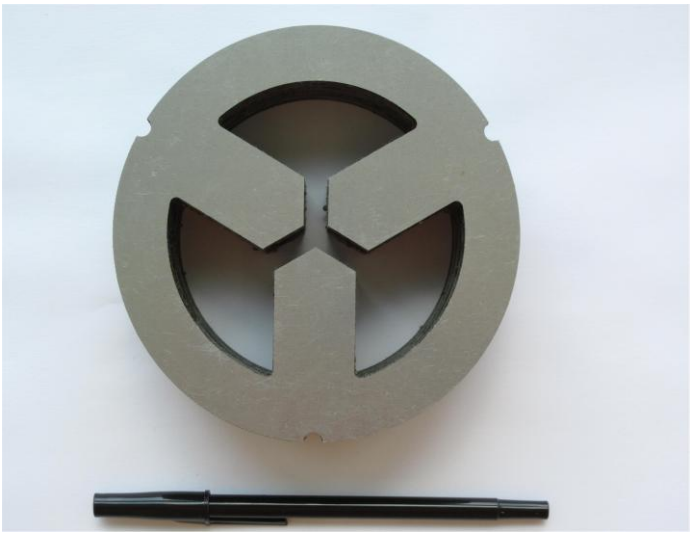


(a)

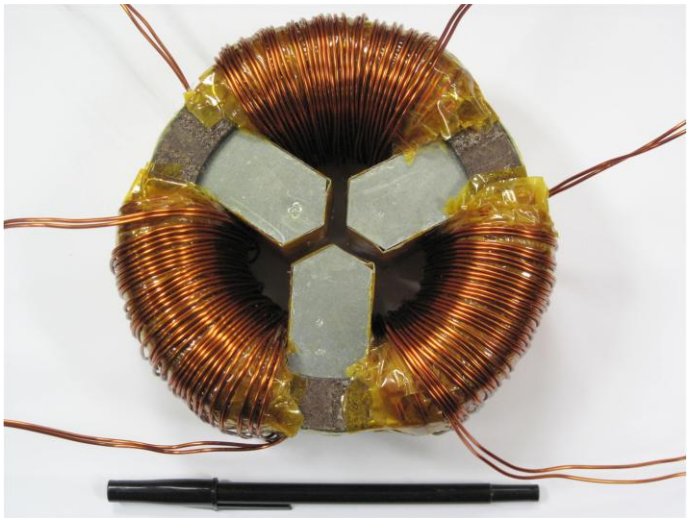


(b)

Fig. 3-9 Core loss curves from the transient simulations in Ansoft/Maxwell. (a) Maximum CM core loss. (b) DM core loss.



(a)



(b)

Fig. 3-10 Photographs of the integrated choke prototype compared with a ballpoint pen. (a) Laminated core before winding. (b) Choke after winding.

3.6.2 Inductance Measurement

As opposed to the simulations in which the choke was excited by currents, the DM and CM inductances of the prototype were measured by imposing three-phase balanced voltages and a

common ac voltage as the respective excitations. For measurement of the CM inductance at the switching frequency, because a large current is drawn by the core-loss-caused resistance in parallel with the inductor, an excessive voltage beyond the limit of the ac power supply may have to be imposed. Hence, the CM inductance was practically measured at a relatively lower frequency, e.g., 1 kHz. In order to correctly evaluate the inductances, the copper and core losses must be factored into the calculation, and the voltage and current waveforms are observed to be sinusoidal to avoid the core saturation [130, 132]. The measured three-phase DM inductances are $L_{dm,A}$ = 2.72 *mH*, $L_{dm,B}$ = 2.71 *mH* and $L_{dm,C}$ = 2.78 *mH* (all around 0.12 pu); the whole CM inductance is $L_{cm,w}$ = 95.1 *mH* (4.13 pu), demonstrating a good agreement with the designed and simulated values, as summarized in Table 3-3.

Table 3-3 Inductances of the design, simulation and measurement.

	L_{dm} (mH)	$L_{cm,w}$ (mH)
Design	2.76	101.4
Simulation	2.8	93.2
Measurement	2.74	95.1

3.6.3 Experimental Results

Fig. 3-11 shows a SPWM VSI powered by a dc supply, v_{dc}, and loaded by a three-phase resistance, R_L, on which the integrated choke prototype was tested. When the switch *SW* is open, the CMV, v_{cm}, could be measured between the ac-side neutral and dc-link midpoint of the converter, i.e., $v_{cm} = v_{oz}$. Fig. 3-12 shows the CMV waveform and its FFT analysis at m_a = 0.9. As the simulation results in Chapter 2, the CMV is a stepwise waveform with the values of $\pm v_{dc}/6$ and $\pm v_{dc}/2$. The spectrum is mainly distributed at the carrier frequency of f_{sw} = 5 kHz and

sideband of its integral multiples. The small triple component (at 180 Hz) is produced by the regular sampling of SPWM and the dead time. In this VSC setup rated at 5kW/208V, the dc-link voltage is 383 V (3.19 pu) and the rms value of the CMV component at f_{sw} = 5 kHz is approximately 100 V (0.83 pu).

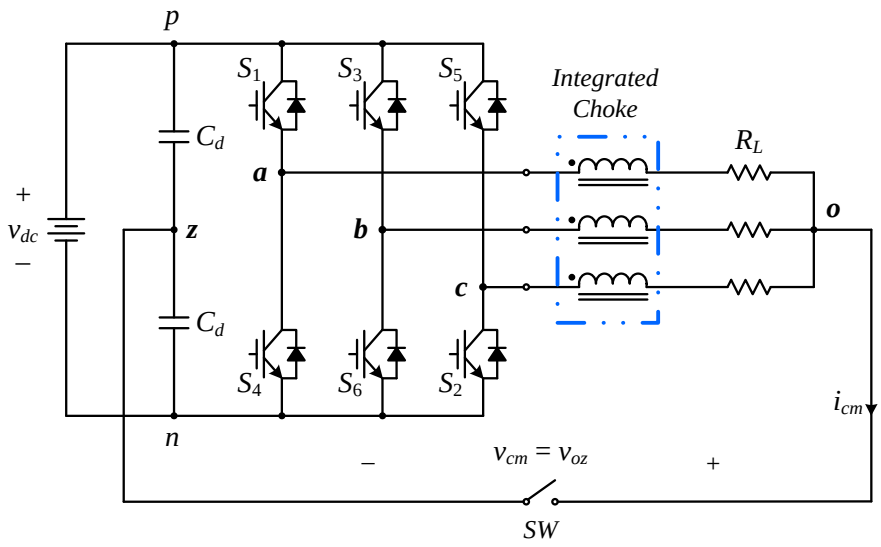


Fig. 3-11 SPWM VSI for test of the integrated choke.

When the switch *SW* is closed, the CM current, i_{cm}, in the VSI with the integrated choke can be obtained in Fig. 3-13. The magnitude of the CM current is confined with 0.8 A (0.058 pu). From its spectrum, the rms value at the carrier frequency is less than 0.36 A (0.026 pu). However, it is noted that the third-order fluctuation in the current waveform is non-negligible, although the triple CMV component is small. This means the integrated choke does not perform well in blocking the CMV components in the low frequency range. If the CMV has large triplen harmonics, the width of the ring core will have to be broader to avoid saturation, increasing the volume and weight of the choke. In order to keep its cost advantage, the integrated choke is

designed and used only for the CM suppression in the medium frequency range. The application of the choke in VSC systems will be investigated and analyzed in the next chapter.

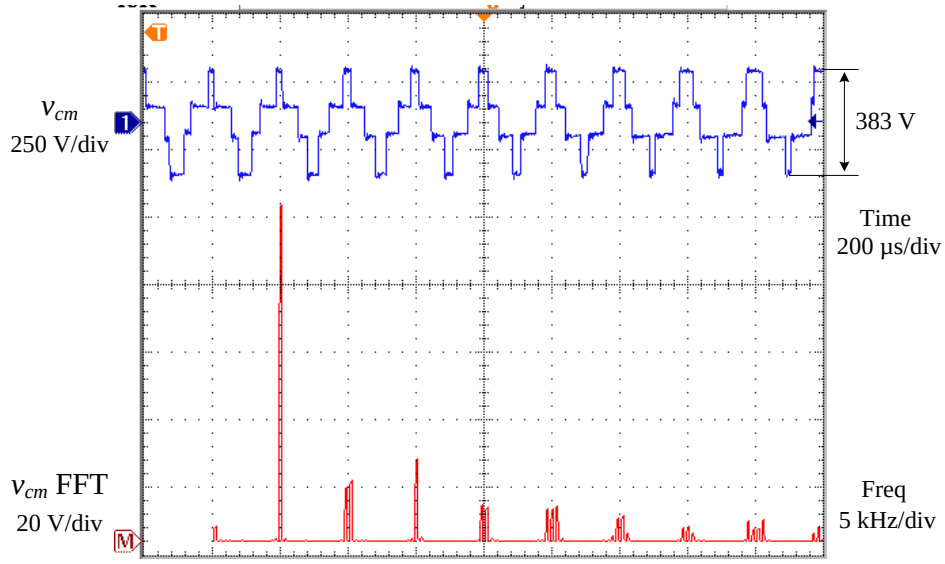


Fig. 3-12 CMV waveform of the VSI with SPWM and its FFT analysis.

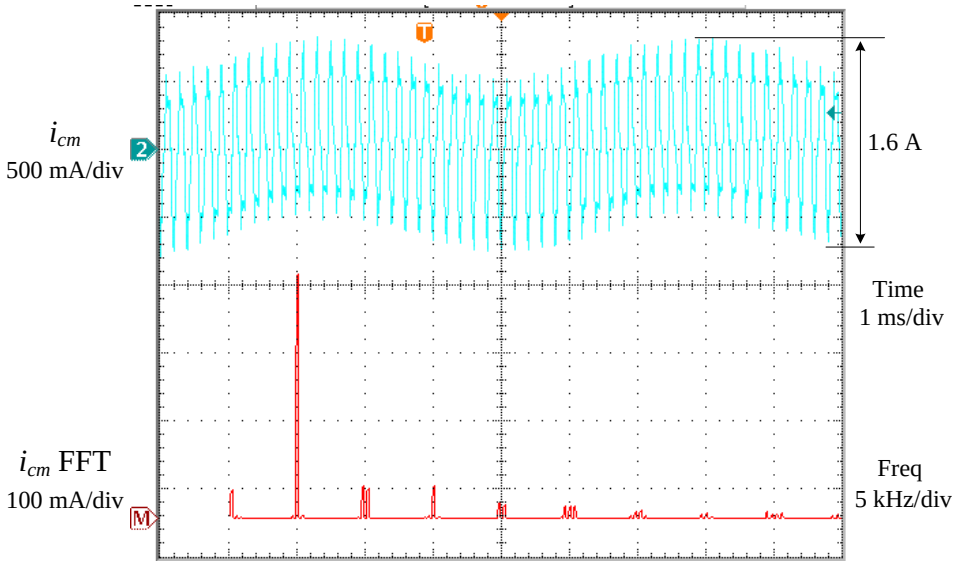
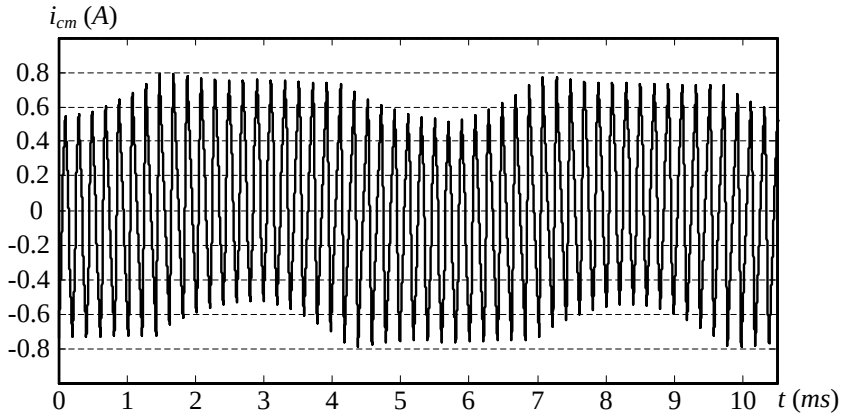
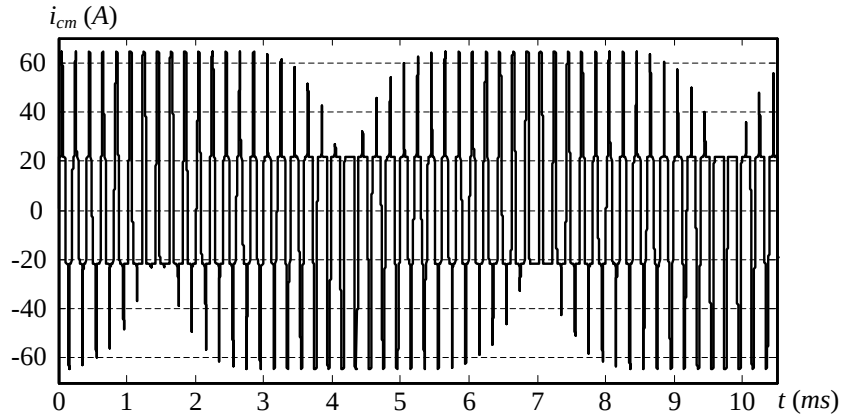


Fig. 3-13 Experimental CM current and its spectrum in the neutral-connected VSI using the integrated choke.

The neutral-connected converter was also simulated with and without the integrated choke. By taking the core loss of the choke into simulation, the attenuated CM current that is shown in Fig. 3-14 (a) is close to the experimental result. On the other hand, in the VSI with the switch *SW* closed and the integrated choke removed, the CM current magnitude becomes very high and, as shown in Fig. 3-14 (b), exceeds 60 A (i.e., 4.33 pu) which could destroy the experimental setup. Such a large CM current is due to little impedance in the CM loop, except for the load resistance and line impedance.



(a)



(b)

Fig. 3-14 Simulated CM current waveforms in a neutral-connected VSC. (a) With the integrated choke. (b) Without the integrated choke.

By comparing the resultant CM currents with and without the integrated choke in Figs. 3-13 and 3-14, the CM blocking function of the integrated choke has been well verified, although the CM current was not attenuated to the small extent in terms of the designed CM inductance and voltage. As mentioned earlier, there are two reasons for the performance degradation: 1) the permeability drop of silicon steel at 5 kHz and 2) the core loss at the carrier frequency that reduces the CM impedance. The amorphous and nano-crystalline magnetic core materials, which have a stable permeability and less loss at high frequencies, can be applied to the integrated choke for performance improvement [125-129], but silicon steel has been adequate in the research to validate the effectiveness of the proposed integrated choke.

3.7 Summary

A novel three-phase choke that incorporates the CM suppression and DM filtering functions in one magnetic device were proposed in this chapter. The integrated ac choke provides a reliable and cost-effective solution to the CMV issues from the spectrum point of view, facilitating the implementation of a transformerless configuration in voltage-source converter systems.

Different magnetic paths in the novel structure of the proposed choke generate the required high CM-to-DM inductance ratio. Compared to separate inductors, the integrated choke reduces the total weight by 50% and drops the loss by 40%. Although the integrated choke was designed for minimization of the weight, the reasonably small CM core loss proves the heat dissipation capability.

The parameters designed based on magnetic circuit calculation were further tuned by the 3-dimentional finite element analysis. Magnetostatic and transient simulations verify the flux

density distributions, inductances and core losses of the choke. The effectiveness in blocking the CM voltage/current was validated by the experimental results of a prototype in a voltage-source converter. The CM suppression performance depends not only on the choke design but also on the core material characteristics including permeability and loss. Other circuit components, such as CM filter capacitors, can be employed in coordination with the integrated choke to mitigate the CMV issues. Applications of the proposed choke will be identified and analyzed in Chapter 4 by CM-circuit modeling and simulation.

Chapter 4

CM-Circuit Modeling and Analysis of VSC Systems Using the Integrated Choke

The objective of this chapter is to identify applications of the integrated choke proposed in Chapter 3 and to analyze the voltage-source converter (VSC) systems using the choke by common mode-(CM) circuit modeling and simulation. The substitution of the integrated choke for an isolation transformer in medium-voltage (MV) drive and photovoltaic (PV) generation systems significantly reduces the system size and cost, and improves the efficiency [16, 21-25, 66]. In low-voltage (LV) drives that may not need an isolation transformer, the choke could also be employed to mitigate ground leakage and bearing currents as well as shaft voltage [11, 49-53, 62, 71, 94]. Appropriate system grounding and filter components, such as CM capacitors and damping resistors, should be coordinated with the integrated choke for a better CM voltage/current suppression effect [99].

This chapter first investigates the choke's application in various configurations of transformerless PV generation systems and motor drives. The CM circuits of typical VSC systems using the integrated choke are then modeled, followed by the evaluation of parameters, including the common-mode voltage (CMV) sources, impedance of the integrated choke, and CM capacitances. Finally, simulation results are provided to verify the modeling and analysis of the VSC systems with the integrated choke.

4.1 Applications of the Integrated Choke

The integrated choke suppresses the CMV components in the medium frequency range, which are dominant in the spectrum in VSC systems. The applications of the proposed choke include PV energy systems and motor drives.

4.1.1 Applications in PV Energy Systems

As introduced in Chapter 1, if there is no galvanic isolation, the CMV of the power converter in PV generation systems may produce impermissible amplitude of ground leakage currents via the parasitic capacitances between PV panels and the ground. In single-phase systems, besides bipolar pulse-width modulation (PWM), half-bridge and neutral-point clamped (NPC) converters, a number of solutions to the leakage currents, e.g., Highly Efficient and Reliable Inverter Concept (HERIC) and H5 topologies, as well as their variants, have been proposed and applied to commercial products [72, 73, 85, 133-138]. On the other hand, most of three-phase systems still use the galvanic isolation, either in the form of a high-frequency transformer in the dc-dc converter, or as a bulky low-frequency transformer at the ac output of the PV inverter. In addition to an increase in size and cost, both of the transformers also drop system efficiency, which is considered a crucial factor of the converter circuit used in PV energy systems [81]. A transformerless configuration is an ideally high-efficient PV generation system [21-23].

The galvanic isolation of a three-phase PV inverter can be eliminated by using the proposed integrated choke for both differential-mode (DM) harmonic filtering and CM current suppression. Whereas the transformer cuts off the path through which the leakage current flows, the choke inserts a large impedance to constrain the current. However, with only the integrated choke, the

residual leakage current can still circulate through the parasitic capacitance of PV panels. The amplitude may not satisfy the strict standards [82-84].

Fig. 4-1 illustrates a complete solution to this leakage current issue, where a pair of CM capacitors C_{cm} is added between the output terminals of the PV array(s) and the ground [22]. In order to generate little leakage current through the parasitic capacitance C_E, it is required that $C_{cm} >> C_E$. The transformerless PV system could be either a single-stage or two-stage configuration. In Fig. 4-1, the optional dc-dc converter is not shown for simplicity.

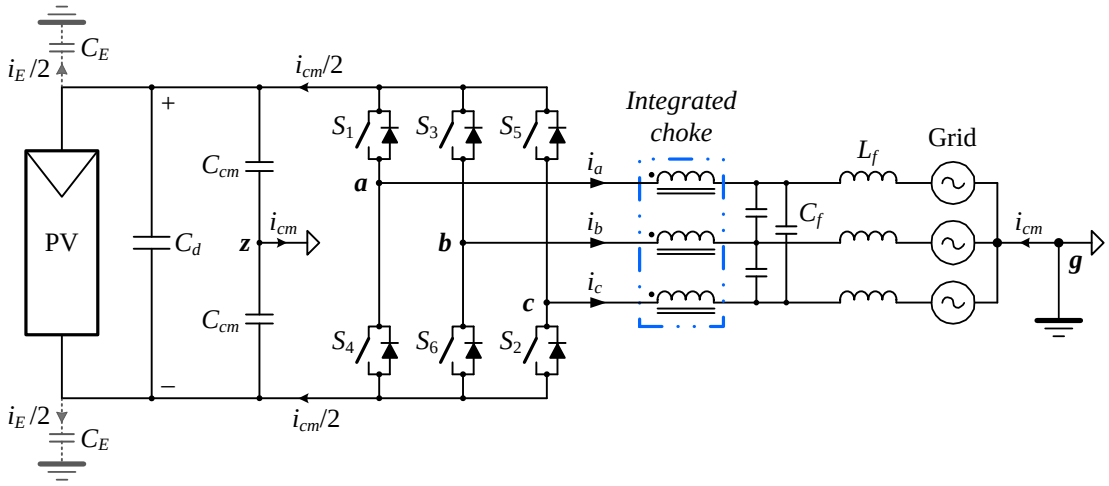


Fig. 4-1 Transformerless PV inverter using the integrated choke and CM capacitors.

It is worth pointing out that the requirements for system grounding and ground fault monitoring in NEC 690 standard prevent the implementation of the transformerless PV energy system [83, 84]. However, the configuration in Fig. 4-1 can be applied in Europe, satisfying the local code [82]. A Δ-connected capacitor bank is illustrated in the figure for the grid-side *LCL* filter. Without consideration of the neutral-grounded EMI filter and ground fault current interruption (GFCI), the filter capacitors could also be in Y connection with its neutral point

grounded via an added CM capacitor or directly. This will reduce the CM current flowing into the grid, if the CM impedance of the capacitors is set to be much smaller than the line impedance. This concept is the same as in MV motor drives.

4.1.2 Applications in Motor Drives

Chapter 1 indicated that the shaft voltage, ground and bearing currents all stem from the CMVs through parasitic capacitive couplings of motor drives [5-10]. These issues are common in both MV and LV systems, and can be solved by removing the CMV from motor terminals [16, 50]. On the other hand, whereas the CMV stress is often ignored in LV motor drives, it is regarded as a main challenge to the motor winding insulation in MV drives [1, 14, 15].

An extra isolation transformer is traditionally installed in MV drives to mitigate the motor CMV stress and isolate the interference to the grid [24, 25, 99]. By reviewing the grounding concepts in MV grids, the application of the integrated choke will be identified to implement a transformerless configuration. Although LV drives may not need an isolation transformer, the integrated choke can be combined with other filter components to address the issues of shaft voltage, ground and bearing currents [11, 49, 51-53]. In addition, the choke's special applications, such as in the electric system on airplanes and machine tools, are also discussed [2].

4.1.2.1 MV Drive Systems

Fig. 4-2 demonstrates the utilization of the integrated choke in the new generation of MV (2.3 kV–13.8 kV) drives with an active-front end and featured by four-quadrant operation [100]. Similar to the isolation transformer that was explained in Chapter 1, the integrated choke provides a much higher CM impedance than that of the motor windings to the ground. The

majority of the CMV is accordingly transferred to the choke, but only using the choke does not completely solve the CMV problems. A Y-connected capacitor bank $C_{cm\text{-}mf}$ and series resistors $R_{d\text{-}mf}$ that damps any possible DM and CM resonances are installed between the motor and its *dv*/*dt* filter.

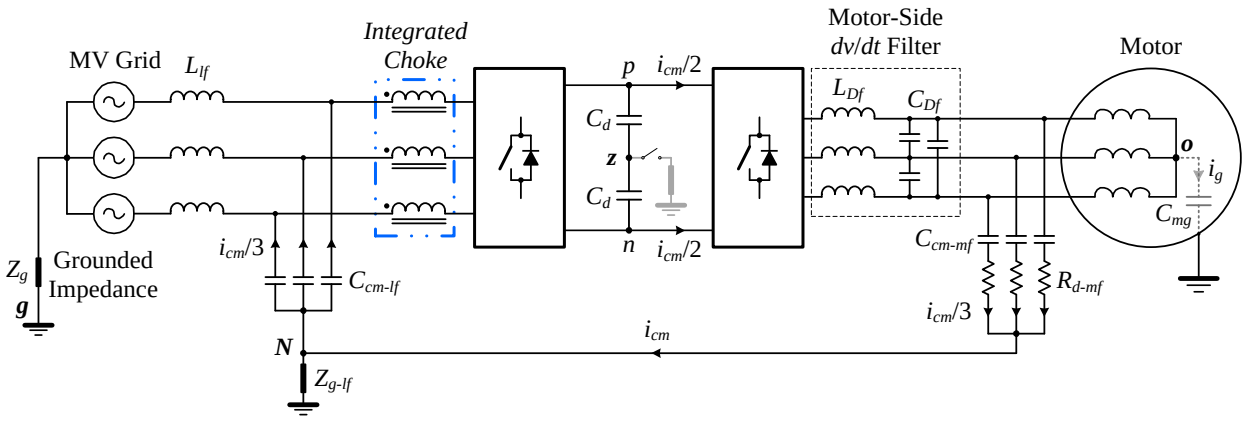


Fig. 4-2 Transformerless MV voltage-source-fed drive with the integrated choke and new system grounding.

The grounding concepts in MV distribution grids up to 15 kV include [139]:

1) low impedance grounding (to limit ground-fault current between 100 A and 1000 A);

2) high impedance grounding (to limit the resistor current to typically 10 A or less);

3) reactance grounding (if the desired current magnitude is several thousand amperes);

4) resonant grounding (ground-fault neutralizer).

The CM effects have been studied for low- and high-impedance grounded systems which are two extremes in regards of the impedance [99]. To prevent the CM current from flowing in the direction of the grid, the grounding of the MV drive systems is moved from the historically preferred dc-link midpoint to the neutral point of the line-side CM capacitor bank $C_{cm\text{-}lf}$, as

shown in Fig. 4-2. $Z_{g\text{-}lf}$ signifies the grounding impedance of the line-side filter. It was obviously concluded in [99] that high-impedance grounding constrains the CM current flowing into the MV grid more effectively than low-impedance grounding.

Fig. 4-2 shows shorted neutral points of the motor-side CM network ($C_{cm\text{-}mf}$ and $R_{d\text{-}mf}$) and line-side CM capacitor bank $C_{cm\text{-}lf}$. With no ground fault, this neutral point ***N*** is virtually grounded. The purpose of the CM *RC* network on the motor side is to bypass the motor parasitic circuit to the ground shown in Fig. 1-4, which has been simplified to a stray capacitor C_{mg}. This demands the former have a much lower impedance than the latter, i.e., $(Z_{Ccm\text{-}mf} + Z_{Rd\text{-}mf}) << Z_{Cmg}$. The CM current will flow primarily through $C_{cm\text{-}mf}$ and $R_{d\text{-}mf}$, rather than leaking from C_{mg} as the ground leakage current. Moreover, $C_{cm\text{-}mf}$ and $R_{d\text{-}mf}$ in parallel with C_{mg} could considerably decrease the motor-side total impedance and the ratio to that of the integrated choke, resulting in a smaller CMV imposed on the motor terminals [11, 25].

4.1.2.2 LV Drives

The neutral point of LV (≤ 600 V) distribution grids is usually solid grounded. As shown in Fig. 4-3, the application of the integrated choke in LV drive systems is similar to that in MV drives, but the shorted neutral points of the motor-side CM network and line-side CM capacitor bank are kept floating. The integrated choke, in coordination with $C_{cm\text{-}lf}$, $C_{cm\text{-}mf}$ and $R_{d\text{-}mf}$, mitigates the ground and bearing currents as well as shaft voltage by removing the CMV from motor terminals. The CM current in the grid and supply transformer (not shown in the figure for simplicity) is also prevented, avoiding the possible core saturation and reducing losses [11, 53, 54].

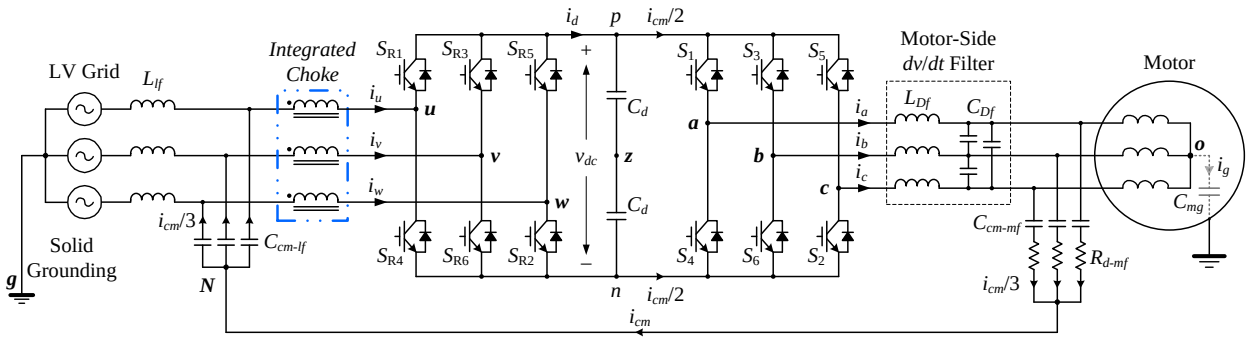


Fig. 4-3 Low-voltage VSI-fed motor drive with the integrated choke, line- and motor-side CM capacitors and damping resistors.

It is noted that the integrated choke design may not be suitable for motor drives with a diode-front end. The reason is that a diode rectifier produces the CMV dominantly at the triple supply frequency, which saturates the choke; otherwise, as discussed in Chapter 3, the width of the ring core has to be much broader, increasing the weight and cost of the choke.

Fig. 4-3 provides a typical LV drive configuration and filter circuit with the integrated choke [11], which, in fact, have many variants. Two special applications of the choke are illustrated in Figs. 4-4 and 4-5. The former is the drive system on a More-Electric Aircraft (MEA), for which the integrated choke is tailor-made. In order to avoid corona discharges under low pressure at high altitudes, any point-to-ground potential of the electric system on airplanes is not allowed to exceed 270 V. The dc-link midpoint is thus required to be grounded, splitting the CMVs generated by the rectifier and inverter [140, 141]. As a result, two integrated chokes need to be used on both sides. It is worth pointing out that the choke applied to the MEA should be redesigned with the specifications different from general drives and materials with less loss, e.g., the amorphous and nano-crystalline iron alloys, because the choke is on the generator/motor side,

rather than grid-tied, and the switching frequency has been increased to reduce the passive components' size in aerospace applications.

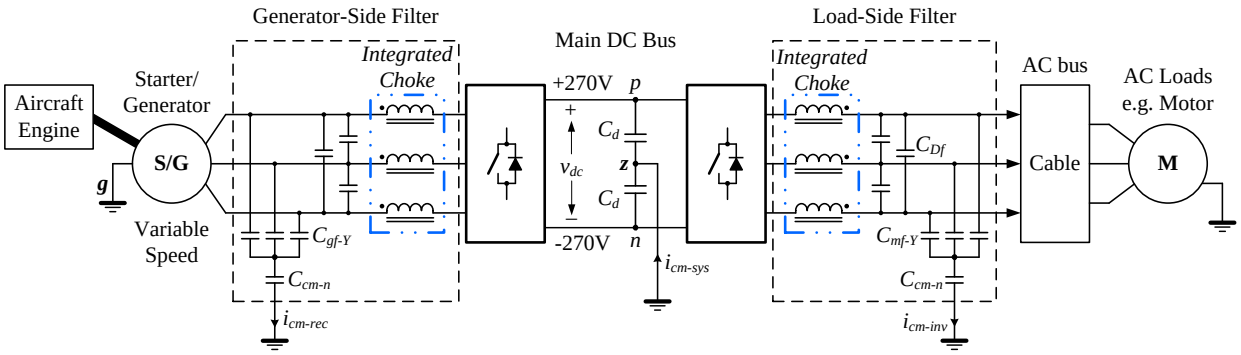


Fig. 4-4 Drive system on a More-Electric Aircraft with its dc-link midpoint grounded, integrated chokes on both sides and CM capacitors on the neutral line.

The filter circuits shown in Fig. 4-4 add CM capacitors $C_{cm\text{-}n}$ on the neutral line, while the Y-connected capacitor banks $C_{mf\text{-}Y}$ and $C_{gf\text{-}Y}$ function as a part of both DM and CM filters. The machine CMV issues are addressed by setting the total CM filter capacitance much larger than the machine parasitic capacitance.

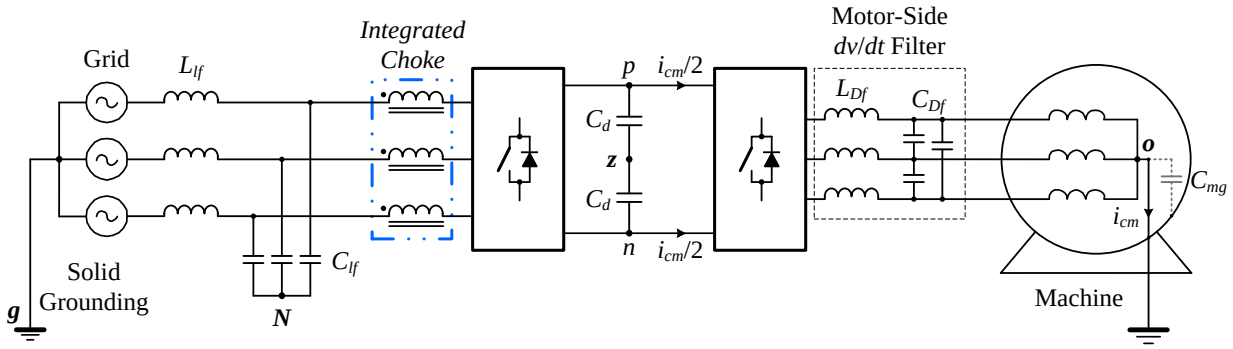


Fig. 4-5 Drive of machine tools with the integrated choke and grounded neutral point of the motor windings.

Fig. 4-5 presents the drive of machine tools with the integrated choke, where the motor winding neutral point must be grounded for safety. As a zero CMV has been forced at motor terminals, the motor-side CM capacitors $C_{cm\text{-}mf}$ can be omitted. The CM current will flow through the motor winding neutral point to the ground. The shaft voltage and bearing currents will be zero due to the stator neutral grounding.

On the other hand, as a result of the solid grounding in LV distribution grids, the CM current that has been attenuated by the integrated choke cannot be excluded from the grid or supply transformer. In Fig. 4-5, a line-side filter capacitor bank C_{lf} is shown with a floating neutral point. According to the system grounding standard, the neutral point $\boldsymbol{N}$ could be grounded to decrease the grid CM current. The reduction depends on the impedance ratio of the grid-side filter inductor L_{lf} to the capacitor C_{lf}.

All these described drives share a common trait that the neutral point of the motor side is connected to that of the line side or ground, either via an extra CM capacitor bank (Figs. 4-3 and 4-4) or through the machine windings directly (Fig. 4-5). Such systems are called neutral-connected drives. These configurations efficiently facilitate the CM voltage/current suppression of the integrated choke.

4.2 CM-Circuit Models

The CM behaviors of the transformerless PV inverters and neutral-connected motor drives are modeled. The CM-circuit models and their parameter evaluation analyze the effect and performance of the integrated choke in these VSC systems.

4.2.1 Modeling of PV Inverters

Fig. 4-6 shows the circuit model of the transformerless PV inverter in Fig. 4-1, where the dc link is represented by a virtual point ***z'***, and the voltage sources are the average of each-phase voltage with respect to the positive and negative dc rails, i.e., $v_{az'} = (v_{ap} + v_{an})/2$, $v_{bz'} = (v_{bp} + v_{bn})/2$ and $v_{cz'} = (v_{cp} + v_{cn})/2$. In Fig. 4-6, L_g denotes the CM inductance between the ground connections of the inverter and the grid. C_{ag}, C_{bg} and C_{cg} express the stray capacitances between the inverter output terminals and the ground, but their influence on the CM effects will be ignored owing to their small values [21-23].

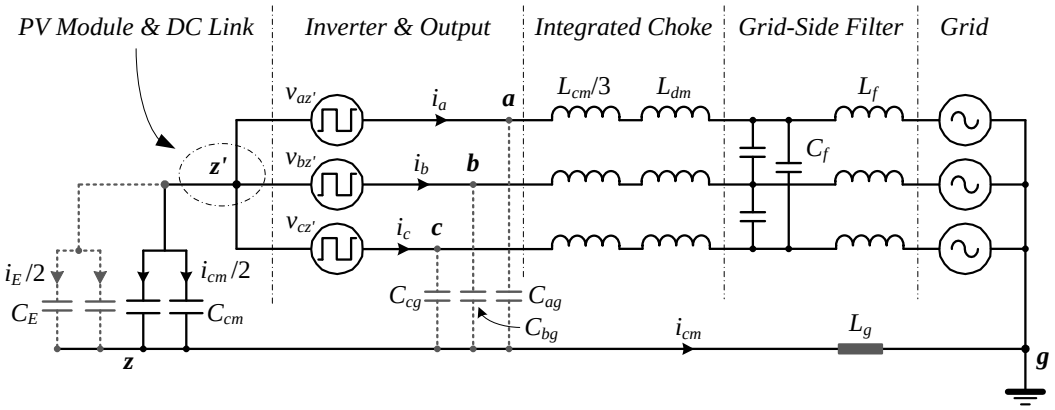


Fig. 4-6 Circuit model of the transformerless PV inverter in Fig. 4-1.

The simplified CM model of the transformerless PV inverter is derived in Fig. 4-7, where Z_g expresses grounding impedance of the grid, and $3C_f$ in the dashed frame is the optional Y-connected grid-side filter capacitance. If the filter capacitors are in the Δ connection, $3C_f$ would not exist in the CM-circuit model.

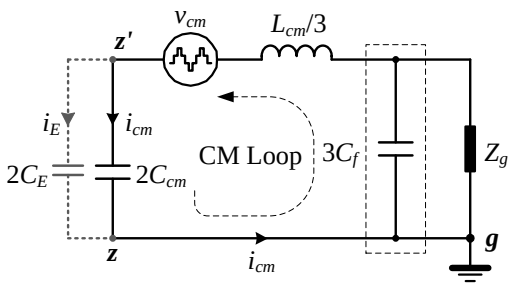


Fig. 4-7 Simplified CM model of the transformerless PV inverter.

4.2.2 Modeling of Neutral-Connected Motor Drives

The CM-circuit models of the previously described neutral-connected motor drives, through Figs. 4-2 to 4-5, are derived. Whereas similar models are obtained for the typical MV and LV drives in Figs. 4-2 and 4-3, the different filter configurations and grounding techniques in Figs. 4-4 and 4-5 result in changes in their CM-circuit models.

As indicated earlier, the integrated choke, with appropriate system grounding and filter components, is supposed to remove the CMV from motor terminals. For circuit analysis of the neutral-connected drives with the integrated choke, the complex CM model of the motor in Fig. 1-4 is reduced to a series-parallel capacitor network, shown in Fig. 4-8. According to the figure, a machine can be represented by a single lumped capacitor to the ground in the CM-circuit models:

$$C_{mg} = C_{sg} + \left[\frac{C_{sr} \cdot \left(C_{rg} + 2C_b \right)}{C_{sr} + C_{rg} + 2C_b} \right]. \tag{4-1}$$

This simplification has been exhibited in the earlier plots of the drive systems. C_{mg} is dominated by the stator winding-to-ground capacitance C_{sg}, because C_{sg} is much larger than the other parasitic capacitances on the rotor side [25, 87].

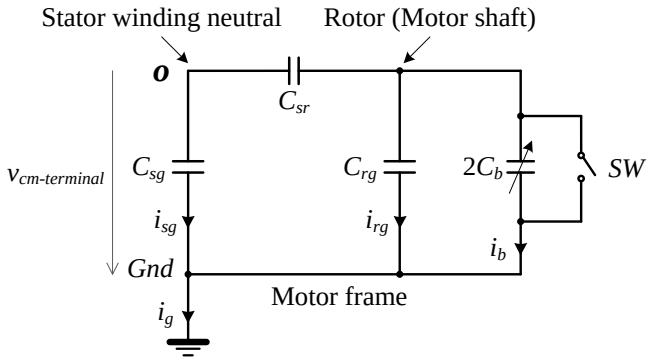


Fig. 4-8 Reduced CM-circuit model of a machine (series-parallel capacitor network).

For the MV and typical LV drives in Figs. 4-2 and 4-3, the power ratings do not make any difference in the CM-circuit modeling. The power converter topologies are modeled as CMV sources whose waveforms and spectra have been investigated in Chapter 2. The solid grounding in LV distribution grids can also be regarded as an extreme case of low impedance grounding in Fig. 4-3. Without ground fault, the shorted neutral points of the motor- and line-side CM filters are virtually grounded in both MV and LV drives.

Based on the analysis, the CM model of Figs. 4-2 and 4-3 are derived almost the same in Fig. 4-9, where the dashed lines between the neutral points ***N*** and the ground ***g*** represent virtual grounding of the CM capacitor network. The CM model of the motor is simplified to the stray capacitor C_{mg}, and Z_g signifies the grounding impedance of the grid, which equals zero for LV motor drives. As stated in the PV inverter modeling, the parasitic capacitances between the ac

outputs, dc-link rails and the ground have been omitted. The CMVs generated by the rectifier and inverter can be merged into one voltage source in terms of their synchrony. According to the system grounding and requirements for the CM capacitances, the motor ground current i_g and CM current flowing into the grid $i_{cm\text{-}grid}$ should be sufficiently small and ignored in the CM loop. The CM impedance of the integrated choke will constrain the system CM current and primarily undertake the CMV.

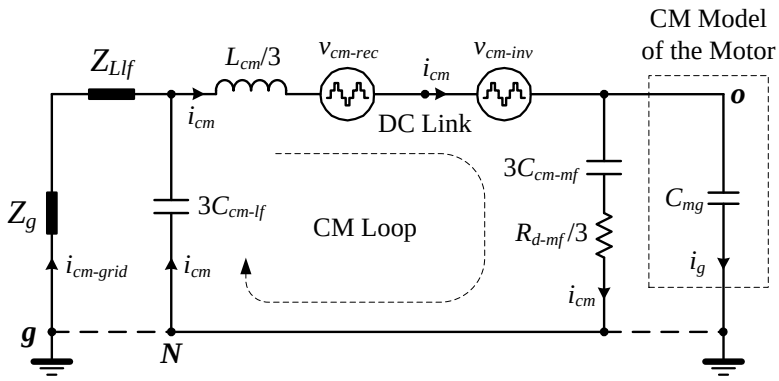


Fig. 4-9 CM model of the MV and typical LV motor drives shown in Figs. 4-2 and 4-3.

Fig. 4-10 shows the CM-circuit model of a drive system on airplanes corresponding to Fig. 4-4. With the grounded dc-link midpoint, this model can be easily split into two identical circuits with individual integrated chokes. The CMV sources generated by the rectifier and inverter should be separately analyzed without consideration of their synchrony. This simplifies the parameter evaluation and CM-behavior study of the MEA drives using the integrated chokes.

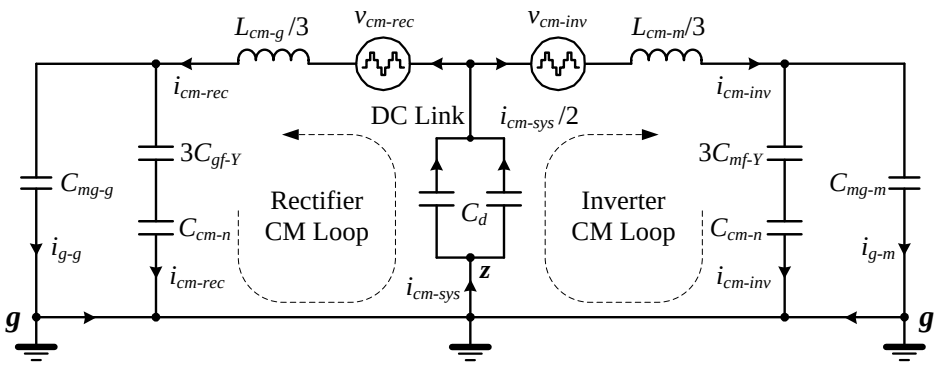


Fig. 4-10 CM-circuit model of a drive system on More-Electric Aircrafts corresponding to Fig. 4-4.

The grounding of the motor winding neutral point in a drive of machine tools bypasses the parasitic capacitances inside the motor, reducing the system CM circuit to that displayed in Fig. 4-11. The motor neutral grounding, integrated choke and line-side filter impedance Z_{Llf} constitute the CM loop, which would also include the filter capacitance $3C_{lf}$, if the neutral point of the capacitor bank is grounded. This situation is expressed by the capacitor in a dashed frame in the figure. Without CM capacitors on the motor side, the CM behavior of the drive has been simplified and will not be analyzed further.

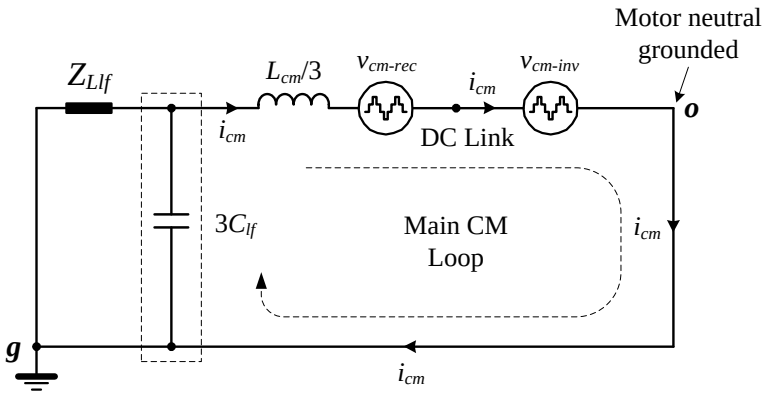


Fig. 4-11 CM model of the drive for machine tools in Fig. 4-5.

4.3 CM-Model Parameters

The parameters of the CM models in Figs. 4-7 and 4-9, including the CMV sources, impedance of the integrated choke and CM capacitance, are evaluated to clarify the applications and effects of the integrated choke in VSC systems.

4.3.1 Analysis of CMV Sources

The magnitude and spectrum of CMVs in typical power converters were studied in Chapter 2 by simulation, but their characteristics versus operating conditions, such as the motor speeds and modulation indices, have not been analyzed. In the following, the CMV components will be plotted in the medium frequency range under various conditions. In the simulation for analysis of the CMV sources, a 5kW/208V system is set for consistency with the integrated choke design example in Chapter 3. Only sinusoidal PWM (SPWM) at f_{sw} = 5 kHz is employed in the VSC system, because space-vector modulation (SVM) introduces triplen CMV components in the low frequency range. These low-frequency CMV components also vary with the load operation and are not the objective of the proposed choke designed to solve.

Fig. 4-12 shows the CMV waveform over half the dc-link voltage ($0.5v_{dc}$) and the fast Fourier transform (FFT) analysis with a typical modulation index of m_a = 0.9 in a single VSC. This spectrum can be found consistently in Fig. 4-13, which depicts the ratio of the peak values of CMV components to $0.5v_{dc}$ versus the modulation index. The frequency of the CMV components is up to $4f_{sw} \pm 3f_1$, where f_1 is kept at 60 Hz. The distributions at higher frequencies are smaller than 0.1 and out of the medium frequency range. In the spectra, the CMV component at the switching frequency is dominant and decreases monotonically with the increase of m_a.

This is because a smaller m_a corresponds to a longer duration of $\pm v_{dc}/2$ in the stepwise CMV waveform. Moreover, the CMV components at $2f_{sw} \pm 3f_1$ and $3f_{sw} \pm 6f_1$ rise with m_a increasing, and those at $3f_{sw}$ and $4f_{sw} \pm 3f_1$ are not monotonous. The maximum values of the CMV components at $2f_{sw} \pm 3f_1$ and $3f_{sw}$ appear at the maximum and minimum modulation indices, respectively. Generally, $m_a = 0$ is the worst case in terms of the CMV spectra.

The ac output voltage of grid-tied PV inverters is constant, whereas its dc-link voltage could be either variable in a single-stage configuration or constant with a dc-dc converter [22]. For transformerless single-stage PV inverters, the dc-link voltage can be adjusted up to the open-circuit voltage of PV panels, which needs a smaller m_a. As per Fig. 4-13, a higher dc-link voltage and lower m_a both raise the dominant CMV components, requiring a larger CM inductance of the integrated choke and therefore increasing the size and cost. On the other hand, for two-stage PV generation systems, maximum power point tracking (MMPT) control is implemented in the front-end dc-dc converter. The dc-link voltage and modulation index of the inverter are constant. Accordingly, certain CMV components can be obtained from Fig. 4-13.

The CMV source is also analyzed in a voltage-source rectifier (VSR) and inverter-(VSI) fed motor drive with synchronous SPWM at f_{sw} = 5 kHz for both converters. In the simulation, the power and voltage ratings are set to 5kW/208V and the dc-link voltage is kept at 383 V (3.19 pu). The rated speed of the motor is 1750 rpm. The VSR has a constant frequency and modulation index of f_1 = 60 Hz and m_a = 0.9, whereas with the open-loop constant Voltage/Frequency (V/F) control, the inverter output voltage and modulation index are proportional to the frequency. Fig. 4-14 shows the CMV waveform of the whole drive system and its spectrum at the inverter output frequency of f_m = 40 Hz. The variation of CMV components over the inverter output frequency is plotted in Fig. 4-15.

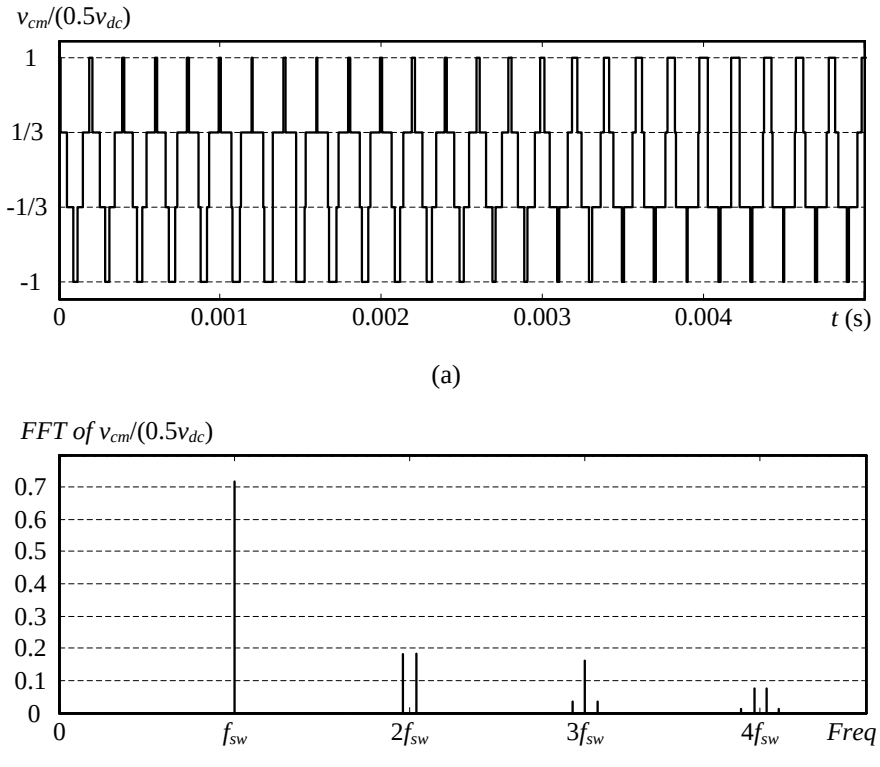


Fig. 4-12 Simulation results of a single VSC with SPWM at m_a = 0.9. (a) Waveform of the CMV over half the dc-link voltage $v_{cm}/(0.5v_{dc})$. (b) FFT of $v_{cm}/(0.5v_{dc})$.

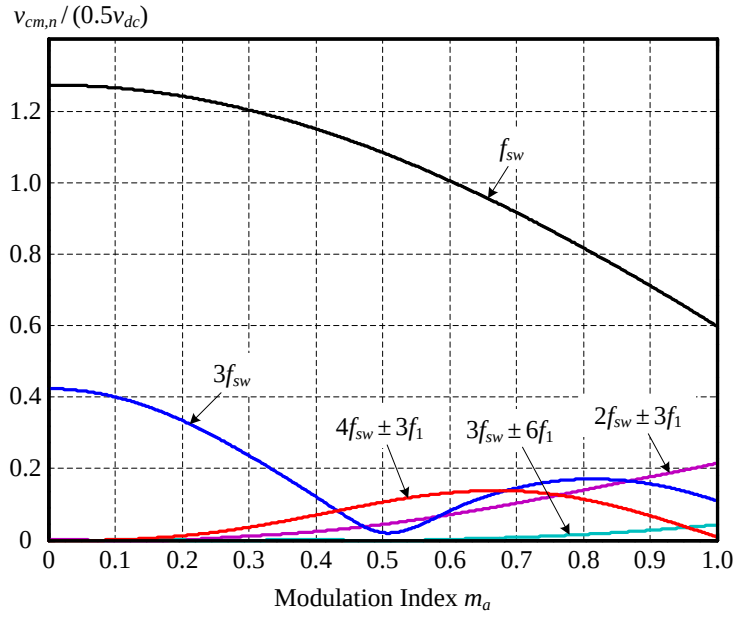
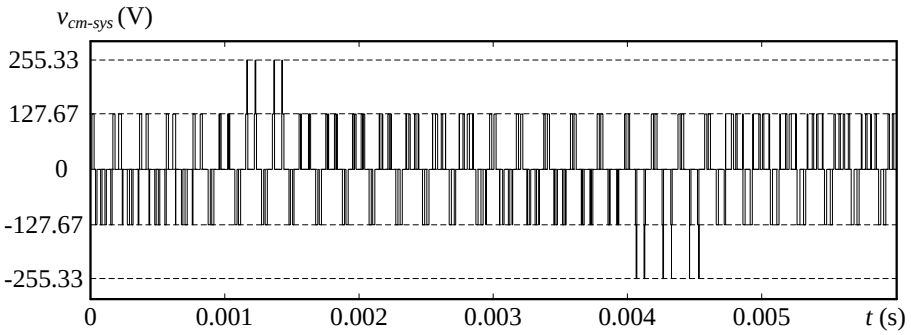
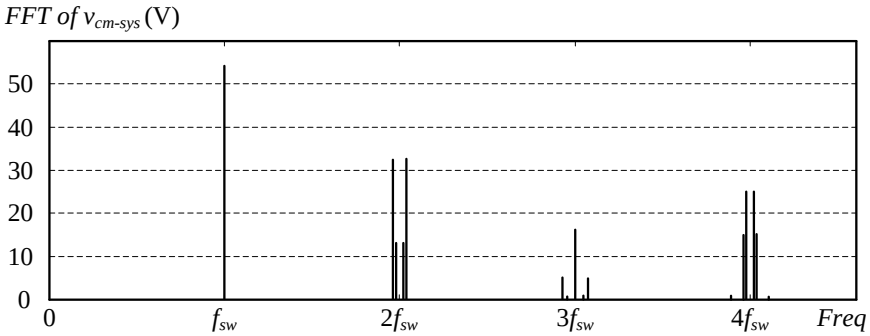


Fig. 4-13 Ratio of the peak values of CMV components to half the dc-link voltage ($v_{cm,n}/(0.5v_{dc})$) versus the modulation index in a single VSC.



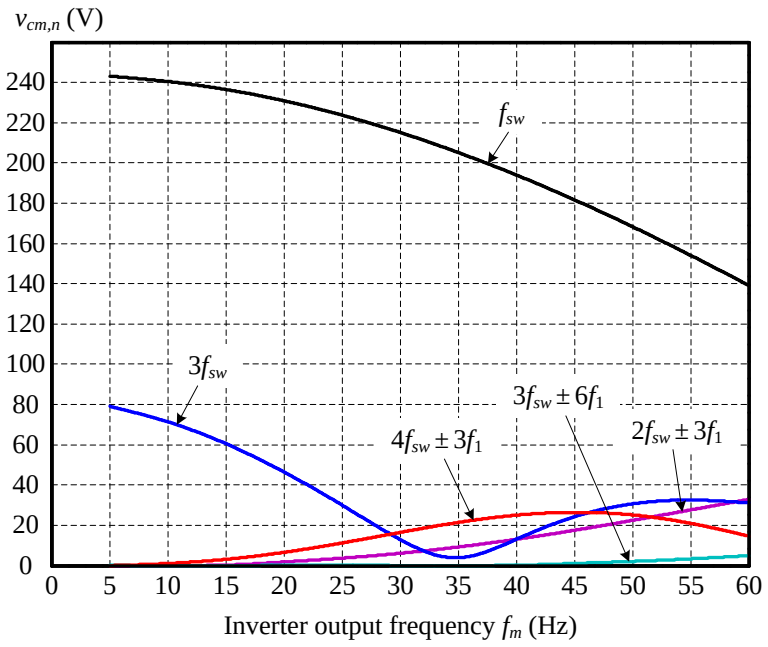
(a)



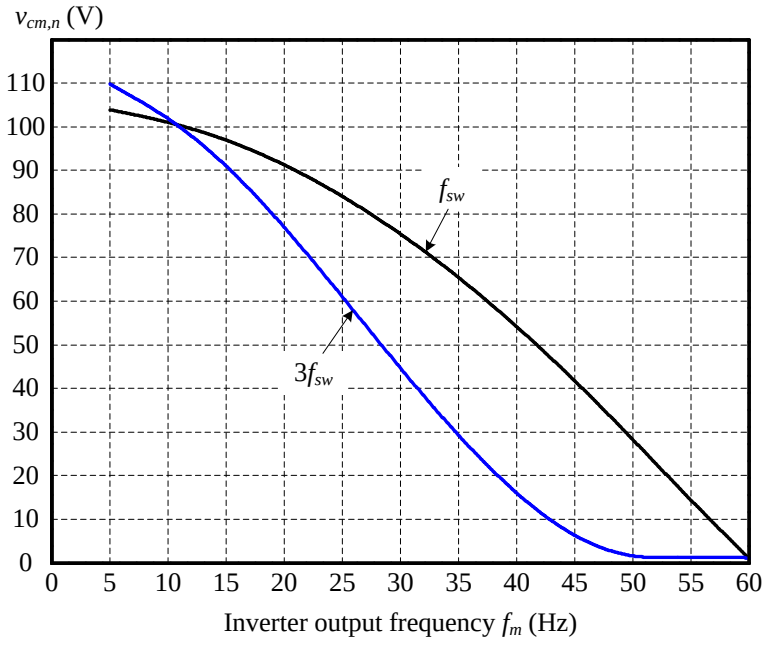
(b)

Fig. 4-14 Simulation results of a VSR-VSI-fed motor drive with synchronous SPWM for both converters at f_{sw} = 5 kHz and f_m = 40 Hz. (a) CMV waveform of the whole drive system $v_{cm\text{-}sys}$. (b) FFT of $v_{cm\text{-}sys}$.

Fig. 4-15 (a) shows the CMV components produced only by the inverter. The curves are similar to those in Fig. 4-13. The worst case is the zero- or low-speed operation, corresponding to a small m_a. With synchronous SPWM, the CMVs of the VSR and VSI have no triplen distributions in the low frequency range. The CMV components that overlap at the switching frequency and its integral multiples (i.e., 5 kHz and 15 kHz in this simulation example) are reduced, as shown in the comparison between Fig. 4-15 (a) and (b), and displayed in Fig. 4-14, particularly during high-speed operations of the motor. This is beneficial to the integrated choke to be applied and take effect in motor drives.



(a)



(b)

Fig. 4-15 CMV components over the inverter output frequency of a 5kW/208V motor drive. (a) Produced only by the inverter. (b) CMV components of the drive at f_{sw} and $3f_{sw}$ with synchronous SPWM for both converters.

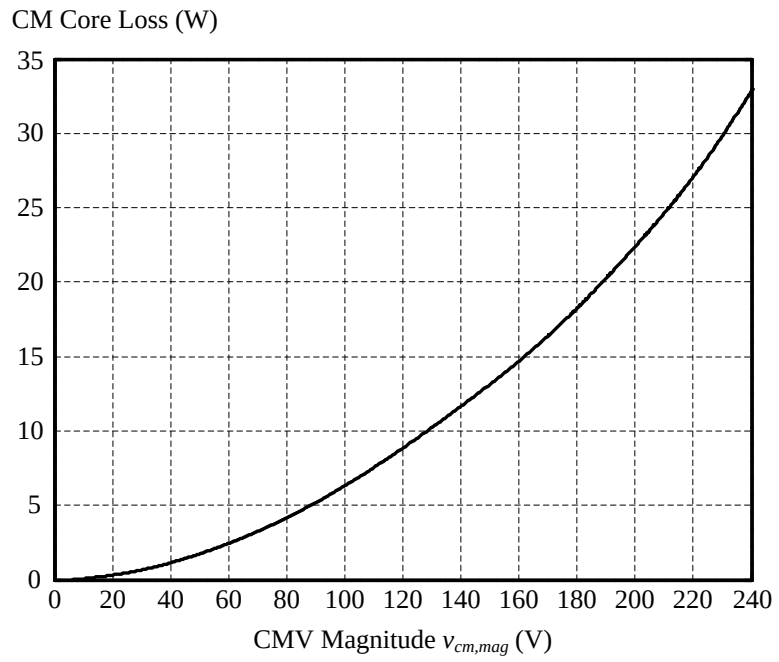
At an inverter output frequency other than 60 Hz (i.e., $f_m \neq 60$ Hz), the side-band CMV components produced by the rectifier and inverter are distributed at different frequencies, and thus cannot cancel each other out. In other words, the CMV components at $2f_{sw} \pm 3f_1$ and $2f_{sw} \pm 3f_m$, $3f_{sw} \pm 6f_1$ and $3f_{sw} \pm 6f_m$, as well as $4f_{sw} \pm 3f_1$ and $4f_{sw} \pm 3f_m$, where $f_1 = 60$ Hz and $0 \text{ Hz} \leq f_m < 60$ Hz, will all appear in the spectra. Their values follow Fig. 4-15 (a) at the corresponding frequencies. Fig. 4-14 displays an example of $f_m = 40$ Hz, where the values of the total CMV FFT analysis are consistent with Fig. 4-15 (a). In another case of $f_m = f_1 = 60$ Hz which is special, the side-band CMV harmonics decrease significantly, similar to those at f_{sw} and $3f_{sw}$. From Fig. 4-15, the distributions at f_{sw} and $3f_{sw}$ dominate in the worst-case CMV spectrum of the motor drive with synchronous modulation between the back-to-back converters.

4.3.2 CM Impedance of the Integrated Choke

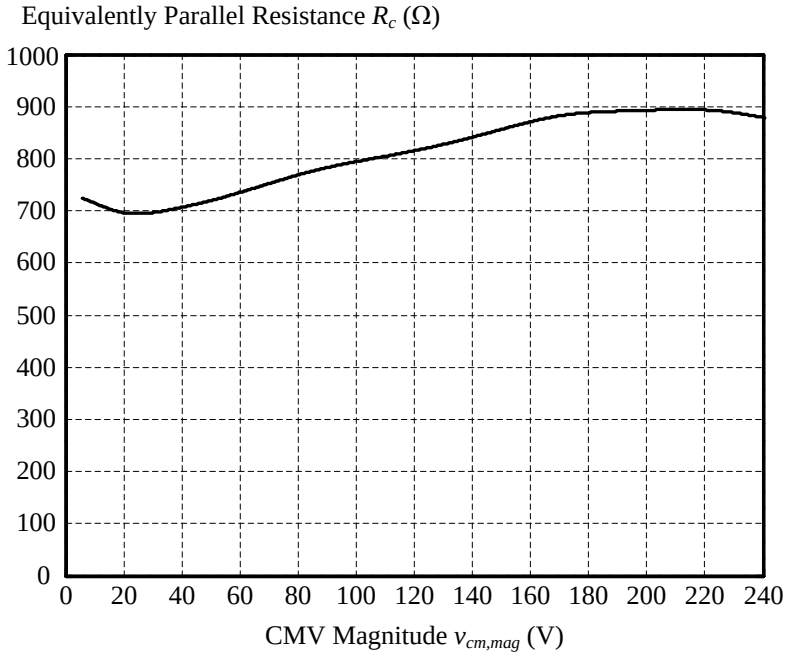
Only inductances are far from describing the DM and CM behaviors of the integrated choke in VSC systems. An equivalent-circuit model of the choke should include the self, mutual and leakage inductances, the series and parallel resistances which respectively present the copper and core losses, and stray capacitances between turns and lays of the windings [126]. The stray capacitances are only taken into account at very high frequencies, e.g., several hundred kHz or MHz. The copper-loss-caused series resistance is usually negligible compared to the CM inductive impedance. However, owing to the equivalently parallel resistance, the core loss might significantly reduce the CM impedance of the integrated choke depending on the core material. Therefore, the CM-circuit model of the choke can be simplified into an inductance in parallel with a resistor.

Take an example of the integrated choke designed in Chapter 3 with laminated silicon steel. At the maximum CMV of $v_{cm,max}$ = 191.5 V (1.6 pu), the CM core loss is 22.1 W, resulting in an equivalent resistance of R_c = 829.7 Ω, whereas the CM inductive impedance is approximately 3 kΩ at f_{sw} = 5 kHz. As a consequence of considering the core loss, the total impedance decreases 4.6 times, which sharply degrades the CM suppression performance. This undesirable situation can be avoided by using the core material of amorphous or nano-crystalline iron alloys with less loss. Fig. 4-16 plots the CM core loss and equivalently parallel resistance of the choke versus the CMV magnitude. The observation indicates that the resistance varies in a narrow range between 700 Ω and 900 Ω, while the CM core loss increases from 0 to 33 W. The total CM impedance of the choke has accordingly declined 4.5 to 5.5 times. The CM suppression performance only changes slightly over the entire CMV range.

It should be noted that the CM core loss, equivalently parallel resistance and CM impedance are all evaluated only at 5 kHz. Consideration of higher frequencies will complicate the analysis. The inductive impedance increases with the frequency rising, but in a nonlinear manner. The higher frequency leads to an exponentially increased CM core loss. However, the flux density has been reduced significantly by the corresponding smaller CMV components and higher inductive impedance, and this decreases the core loss. Based on the estimation of the loss and impedance at 5 kHz, the CM filter capacitances in the system will also be determined at the same frequency.



(a)



(b)

Fig. 4-16 CM core loss and equivalently parallel resistance of the integrated choke versus the CMV magnitude. (a) CM core loss. (b) Equivalently parallel resistance.

4.3.3 CM Capacitances

The CM capacitances C_{cm} in transformerless PV inverters and $C_{cm\text{-}mf}$ in motor drives will be determined as per the parasitic capacitances C_E and C_{mg}, as well as the CM impedance of the integrated choke in the circuit models of Figs. 4-7 and 4-9. The objectives of C_{cm} and $C_{cm\text{-}mf}$ are to bypass C_E and C_{mg}, and decrease the CMV imposed on the PV panels and motor terminals [25]. Since the determination of the grid-side CM capacitance, $C_{cm\text{-}lf}$, has the same principle as that of C_{cm} and $C_{cm\text{-}mf}$, and depends on the line inductance and grounding impedance, it will not be discussed in detail.

4.3.3.1 C_{cm} in PV Energy Systems

The parasitic capacitance of PV modules, influenced by the atmospheric conditions and size/structure of the panels, could be up to 50–150 nF/kWp (crystalline-Si modules) [72, 81, 135]. A value of C_E = 500 nF for each dc-link terminal of the 5kW/208V PV generation system in Fig. 4-1 is chosen to determine the CM capacitance C_{cm}.

In this system, the dc-link voltage is assumed constant at 383 V (3.19 pu) with a dc-dc boost converter, resulting in the modulation index m_a = 0.9. The CM impedance of the integrated choke is approximately 649.95 Ω at f_{sw} = 5 kHz. The CM capacitance is set to C_{cm} = 10 μF (0.03 pu), whose impedance is only 1.59 Ω at 5 kHz. The value of C_{cm} is much larger than C_E. According to the parallel connection of C_{cm} and C_E in the CM-circuit model of Fig. 4-7, the CM current that has been attenuated by the integrated choke will primarily flow through C_{cm}, rather than the PV panel parasitic capacitance. On the other hand, the integrated choke will predominantly undertake the CMV, owing to the high ratio of its CM impedance to that of C_{cm} and C_E in parallel.

In addition, the dc-link capacitor C_d is usually set to 4 to 5 pu for power decoupling and voltage smoothing, e.g., C_d = 1.5 mF in the system [85]. With this value, the DM behavior will not be affected by the added C_{cm}.

4.3.3.2 $C_{cm\text{-}mf}$ in Motor Drives

The parasitic capacitances inside a machine are closely related to its construction [17, 18]. As mentioned before, the CM stray capacitance C_{mg} is approximately equal to the stator winding-to-ground capacitance C_{sg}, and increases with the rise of the motor's power rating [87]. For a 5 kW motor, the typical value of C_{mg} is estimated at 5.14 nF, with $C_{sg} \approx 5$ nF, $C_{sr} \approx 150$ pF, $C_{rg} \approx 1.3$ nF and $C_b \approx 300$ pF, as referred to Fig. 4-8 and (4-1) [17, 18, 51-53, 77, 87]. According to the CM-circuit model of typical neutral-connected motor drives in Fig. 4-9, we set the CM capacitance to $C_{cm\text{-}mf}$ = 0.47 μF (0.006 pu) and conservative damping resistance to $R_{d\text{-}mf}$ = 100 Ω (11.5 pu). With the impedance ratio of the CM filter network ($C_{cm\text{-}mf}$ and $R_{d\text{-}mf}$) to C_{mg} at the CMV dominant frequencies, the motor leakage current should dramatically descend. The total CM impedance of the motor-side capacitors and damping resistors is 55.41 Ω at f_{sw} = 5 kHz. With the CM impedance evaluation of the integrated choke, more than 90% CMV will be transferred from motor terminals to the integrated choke at any motor speed.

4.4 Simulation Verification

A transformerless PV inverter and a motor drive with synchronous SPWM between the converters are simulated in MATLAB/simulink to verify the previous modeling, parameter evaluation and analysis of the integrated choke's effect in these systems.

4.4.1 PV Inverters

In the simulation of a 5kW/208V transformerless PV inverter, a dc voltage source at v_{dc} = 383 V (3.19 pu) was used to represent the PV module output with a dc-dc converter. The modulation index was m_a = 0.9. The simulated system is illustrated in Fig. 4-17, which is very similar to Fig. 4-1, except that only the integrated choke is employed in the simulation to be the grid-side filter. The capacitors of C_E = 500 nF and C_{cm} = 10 µF (0.03 pu) were connected between the dc-link positive and negative rails and the ground. The integrated choke was modeled by a three-phase mutual inductor with consideration of the losses.

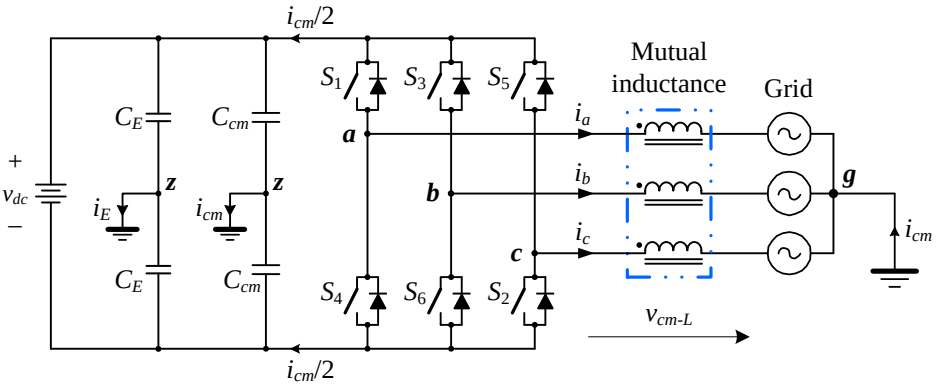


Fig. 4-17 Transformerless PV inverter using the integrated choke and CM capacitors.

Fig. 4-18 provides the simulation results of the CMV imposed on the integrated choke, $v_{cm\text{-}L}$, CM current flowing through C_{cm}, i_{cm}, and ground current leaking from C_E, i_E, respectively, from top to bottom. The waveform of $v_{cm\text{-}L}$ was measured by calculating the average of three-phase voltages on the mutual inductance, i.e., $v_{cm\text{-}L} = (v_{ag} + v_{bg} + v_{cg})/3$, and is observed to be almost the same as Fig. 4-12. This means almost all the CMV has been undertaken by the choke. Furthermore, the integrated choke limits the peak value of i_{cm} to 0.26 A (0.019 pu), whereas the

ground leakage current from the PV panels (i_E) is smaller than 13 mA, only 5% of the former due to the bypass function of C_{cm}. This little value of i_E satisfies the standard for leakage current of PV arrays [21, 82]. It thus can be concluded that the integrated choke, with CM capacitance of C_{cm} = 10 µF (0.03 pu), facilitates the implementation of transformerless PV inverters.

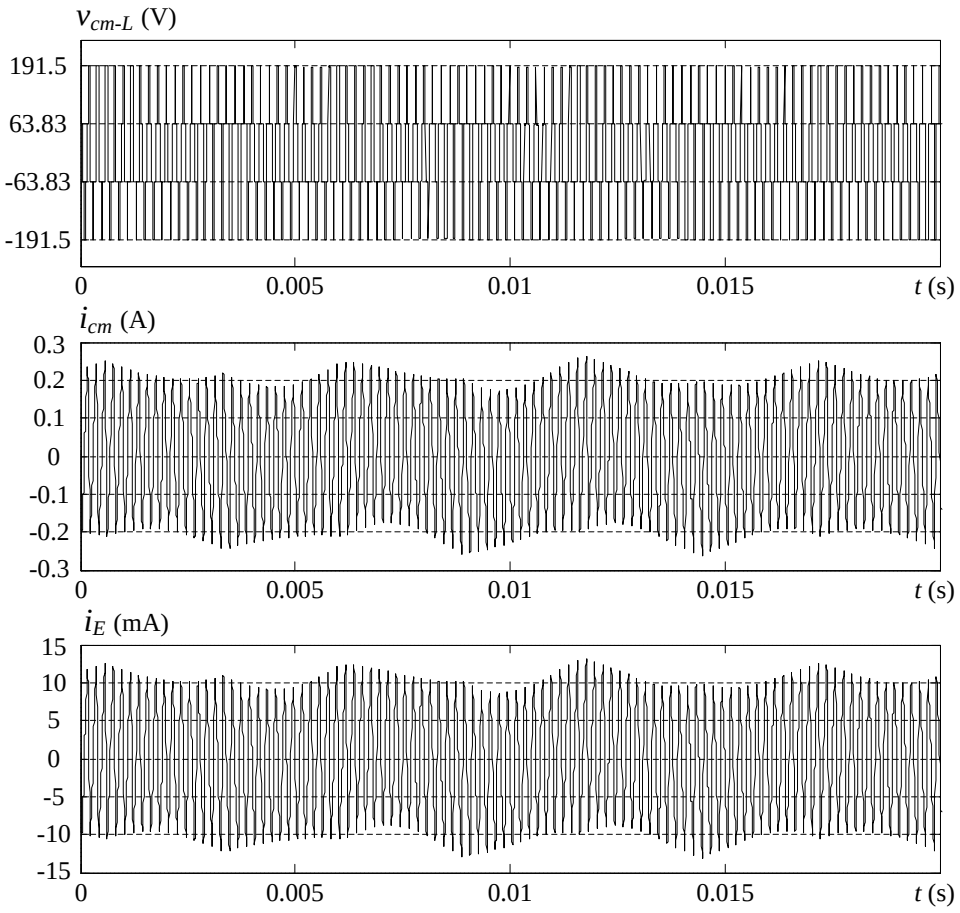


Fig. 4-18 Simulation results of a 5kW/208V PV inverter using the integrated choke and CM capacitors of C_{cm} = 10 µF (0.03 pu) – from top to bottom: the CMV imposed on the integrated choke, $v_{cm\text{-}L}$, CM current flowing through C_{cm}, i_{cm}, and ground current leaking from C_E, i_E.

4.4.2 VSI Drives with Synchornous SPWM Between the Converters

The simulated motor drive shown in Fig. 4-19 employed the voltage oriented control (VOC) and open-loop constant V/F control, respectively, for the PWM VSR and VSI with synchronous SPWM at f_{sw} = 5 kHz. The dc-link voltage was controlled constant at 383 V (3.19 pu). The 208-V, 5-kW, four-pole induction motor was modeled with the parasitic capacitance of C_{mg} = 5.1 nF in the simulation. The motor-side filter was simplified without the DM filter capacitor C_{Df}. The line-side filter components of L_{lf} and $C_{cm\text{-}lf}$ were also ignored for simplicity. The omission of these inessential parameters would exert little influence on the simulation results. Other parameters in the simulation include: L_{Df} = 0.46 mH (0.02 pu), $C_{cm\text{-}mf}$ = 0.47 μF (0.006 pu) and $R_{d\text{-}mf}$ = 100 Ω (11.5 pu). Since the CMV worst case appears at the low-speed operation, the drive was first operated at an inverter output frequency of f_m = 5 Hz. According to the CMV components in Fig. 4-15, an equivalently parallel resistance of 900 Ω was found from Fig. 4-16, and taken into account in the CM modeling of the integrated choke.

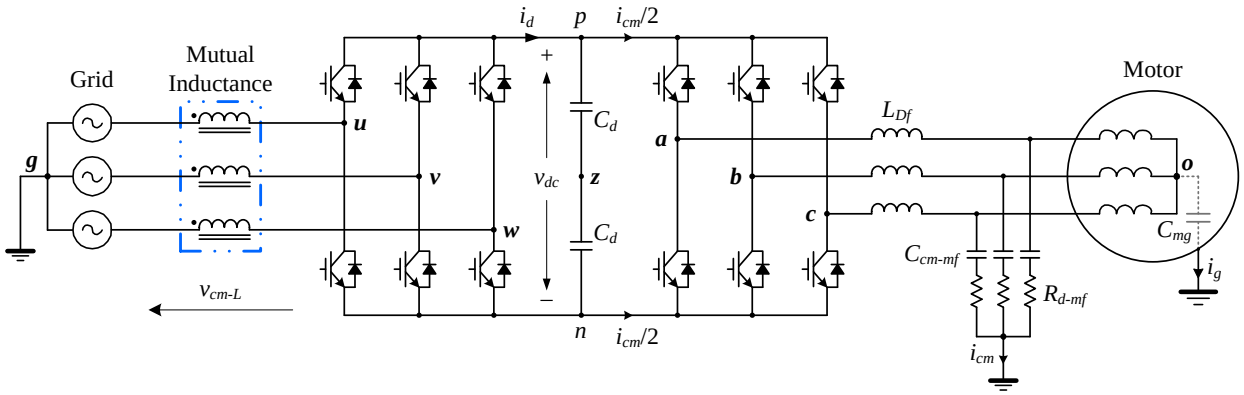


Fig. 4-19 Simulated motor drive with the integrated choke, CM capacitors and damping resistors.

Fig. 4-20 presents, from top to bottom, the steady-state simulation results of the CMV imposed on the integrated choke, $v_{cm\text{-}L}$, CMV appearing at motor terminals, $v_{cm\text{-}m}$, CM current flowing through $C_{cm\text{-}mf}$ and $R_{d\text{-}mf}$, i_{cm}, and the current leaking from the motor capacitor C_{mg}, i_g, respectively. It is the same as in the PV inverter simulation that the waveform of $v_{cm\text{-}L}$ is very close to the real CMV of the drive at f_m = 5 Hz, with the magnitude of $2v_{dc}/3$, or 255.33 V. On the other hand, the peak value of $v_{cm\text{-}m}$ is only 8.6 V (0.07 pu), meaning the overwhelming majority has been removed from the motor terminals. This small value will induce little shaft voltage (< 1 V) and bearing currents, with the motor "bearing voltage ratio" (BVR) usually less than 10% [87]. From the figure, the CM current, i_{cm}, has been constrained within 0.24 A (0.017 pu) by the choke, whereas the large ratio of $Z_{Cmg}/(Z_{Ccm\text{-}mf} + Z_{Rd\text{-}mf})$ leads to the maximum motor ground current, i_g, being only 2.6 mA and negligible.

The motor drive was also operated at a higher inverter frequency of f_m = 40 Hz, and the CM impedance of the integrated choke was accordingly adjusted with an equivalently parallel resistance of 800 Ω as per Figs. 4-15 and 4-16. Fig. 4-21 shows the simulation waveforms of the same voltages and currents as in Fig. 4-20. The magnitude of $v_{cm\text{-}L}$ is still 255.33 V ($2v_{dc}/3$), but its appearances and durations decrease significantly as a result of the higher motor speed. In this situation, the maximum CMV on the motor terminals is lowered to 6.3 V (0.052 pu). The currents flowing through C_{cm} and leaking from the motor, i_{cm} and i_g, are within 0.17 A (0.012 pu) and 2.2 mA, respectively.

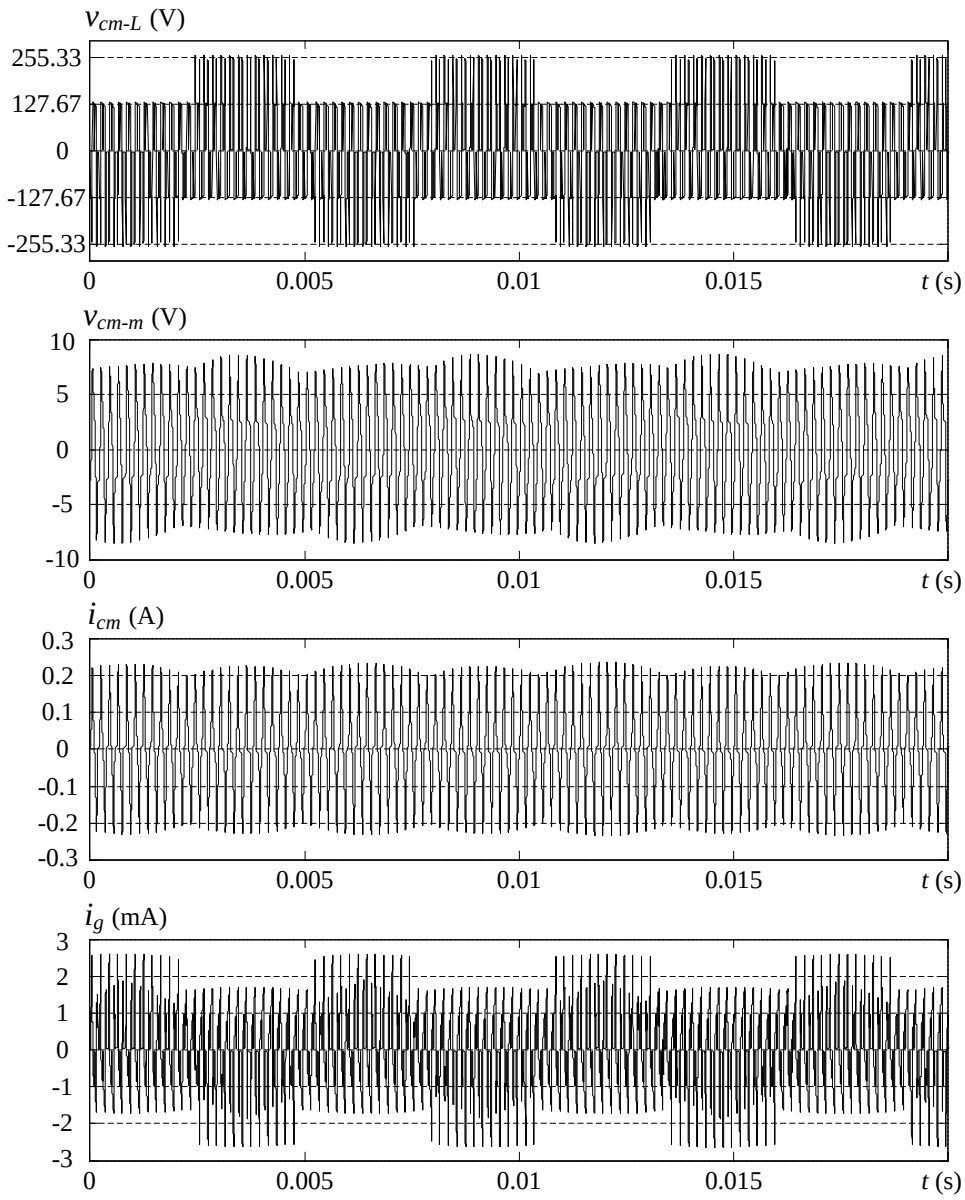


Fig. 4-20 Simulation waveforms of a 5kW/208V motor drive operating at f_m = 5 Hz – from top to bottom: the CMV imposed on the integrated choke, $v_{cm\text{-}L}$, CMV appearing at motor terminals, $v_{cm\text{-}m}$, CM current flowing through $C_{cm\text{-}mf}$ and $R_{d\text{-}mf}$, i_{cm}, and motor ground current, i_g.

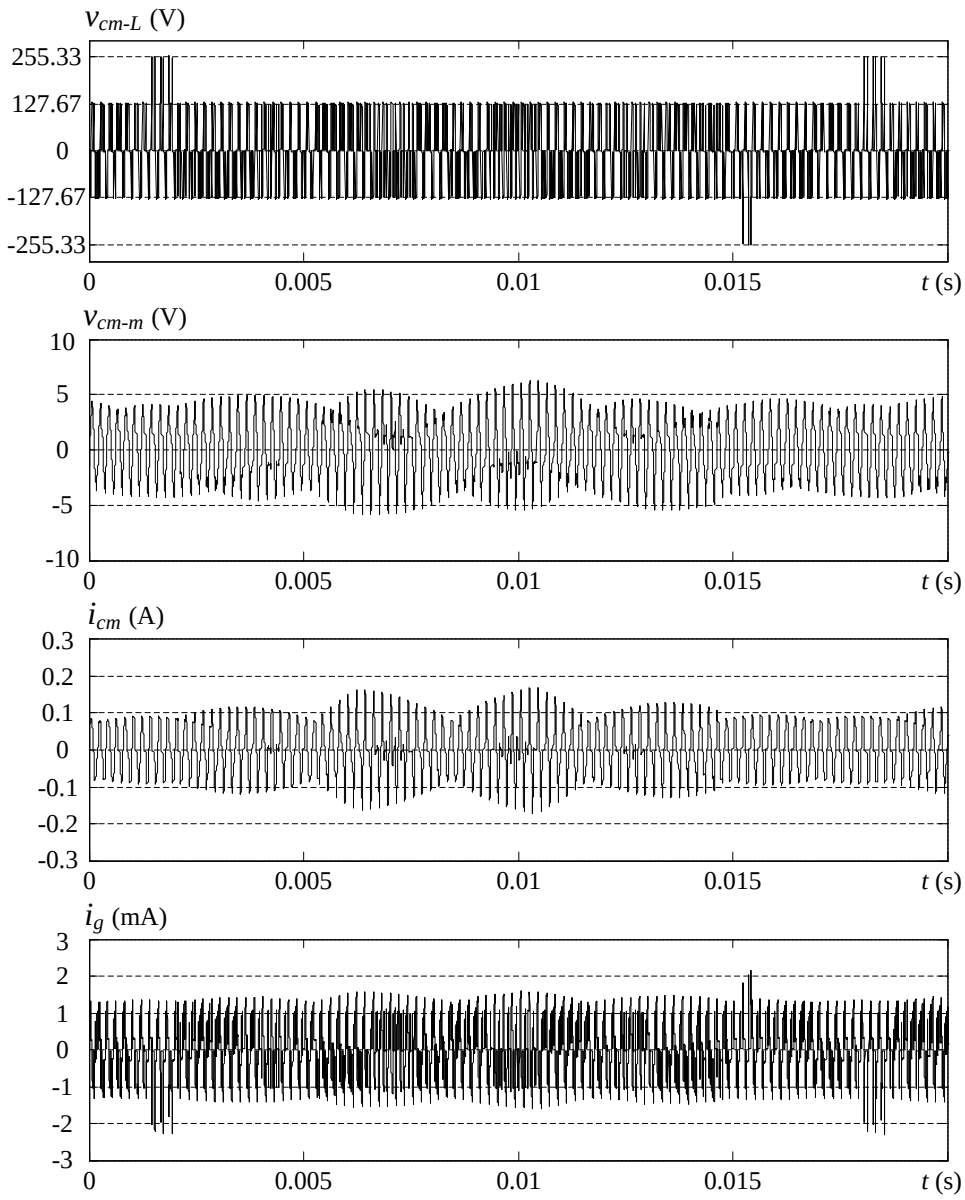


Fig. 4-21 Simulation waveforms of the motor drive operating at f_m = 40 Hz – from top to bottom: the CMV imposed on the integrated choke, $v_{cm\text{-}L}$, CMV appearing at motor terminals, $v_{cm\text{-}m}$, CM current flowing through $C_{cm\text{-}mf}$ and $R_{d\text{-}mf}$, i_{cm}, and motor ground current, i_g.

4.5 Summary

This chapter analyzed the voltage-source converter systems using the integrated choke by CM-circuit modeling and simulation. The transformerless photovoltaic inverters, medium-voltage and low-voltage neutral-connected motor drives were identified as applications of the integrated choke. Appropriate system grounding and filter components, such as CM capacitors and damping resistors, were coordinated with the choke for a better CM voltage/current suppression effect. The drive systems on a More-Electric Aircraft and of machine tools for which the proposed choke is especially suitable were also discussed.

The circuit modeling of the voltage-source converter systems explains their CM behaviors with the integrated choke. With evaluated CM-model parameters that include the CMV sources, impedance of the choke and CM capacitances, both the PV inverter and motor drive were simulated. It is concluded from the observations that the integrated choke undertakes the most common-mode voltages. The ground leakage currents which have been constrained by the choke and decreased further by the bypass function of CM capacitors are negligible in motor drives and satisfy the standard for photovoltaic arrays. These simulation results verify the modeling and analysis of the transformerless PV energy systems and motor drives using the integrated choke.

Chapter 5

CMV Mitigation Methods for Medium-Voltage Current-Source Converters

As pointed out in Chapter 2, the observations following apply: 1) under normal operating conditions of a current-source-fed drive, the common-mode voltage (CMV) magnitude produced by the zero states of space vector modulation (SVM) could be twice as large as those with trapezoidal pulse-width modulation (TPWM) and conventional selective harmonic elimination (SHE) schemes; 2) since the CMVs are composed of chopped three-phase ac voltages depending on the switching states, they are primarily distributed at the third and other triplen frequencies in the low frequency range and it is difficult to mitigate these components by modulation. The integrated dc-link choke that was proposed for medium-voltage (MV) current-source inverter-(CSI) fed drives has been reviewed in Chapter 1 as an example of the CM choke solutions to the CMV issues. A transformerless configuration was accordingly implemented with the CMV stress imposed on the dc-link choke [65-67].

SVM is applied to the active damping control and unity or high input power factor operation. This is because SVM, as an online PWM technique, offers a fast dynamic response and instantaneous regulation of the modulation index [105-115]. However, the CMV stress aggravated by the zero states of SVM requires the integrated choke with higher CM inductance. This will enlarge the passive component, make the drive system oversized and increase the cost.

The main objective of this chapter is to develop modified SVM techniques which can reduce the CMV magnitude and thus keep the compact design of the integrated dc-link choke. Similar to voltage-source converters (VSCs), the modified PWM techniques for current-source converters (CSCs) avoid zero states, called nonzero-state (NZS) modulation. Three NZS modulation techniques are adapted for use in CSCs [36-39]. The switching sequences of suitable methods are designed with the purposes of a low device switching frequency and small low-order (i.e., the fifth and seventh) harmonic distortion. Whereas the nearest-three-state (NTS) modulation sequences perform well with a high modulation index, the combined active-zero-state (AZS) modulation technique can be employed as compensation, when the modulation index is adjusted to a lower level for high input power factor operation. Both simulation and experimental results are provided to verify the CMV reduction effects and harmonic performances of the NTS and combined AZS modulation schemes.

5.1 Nonzero-State Modulation Techniques

The high CMV magnitude generated by SVM can be reduced at least by half using nonzero-state modulation, which, as its name implies, avoids the zero states, but remains the fast dynamic response of SVM. Three types of NZS methods for VSCs that have appeared in the literature [36-39], namely active-zero-state (AZS), remote-three-state (RTS) and nearest-three-state (NTS) modulations, are adapted for use in CSCs.

5.1.1 Active-Zero-State Modulation

AZS modulation maintains the sector divisions and active space vectors as in conventional SVM, but replaces the zero vectors by two opposing active vectors [36]. Based on the selection of the pair of opposing active vectors for substitution, AZS modulation can be classified into three specific methods. With the counterclockwise rotation of the current reference $\vec{I}_{ref}$, AZS1 uses the leading adjacent space vector and its opposite one; AZS2 employs the trailing adjacent and opposite vectors; and AZS3 adopts the remaining pair of opposing vectors.

Fig. 5-1 shows the vector syntheses of the AZS methods with $\vec{I}_{ref}$ falling into Sector I, which is re-named Sector A1 to differentiate between the modified sector divisions in the following NTS method and those in the conventional SVM as well as AZS modulation. As calculated in (5-1), the corresponding dwell times are the same in conventional SVM and AZS methods, except that T_0 is equally shared by the substitute active vectors in AZS modulation:

$$\begin{cases} T_1 = T_s \cdot m_a \cdot \sin\left(\pi/6 - \theta\right) \\ T_2 = T_s \cdot m_a \cdot \sin\left(\pi/6 + \theta\right) \\ T_0 = T_s - T_1 - T_2 \end{cases} \quad \text{for } -\pi/6 \le \theta \le \pi/6, \tag{5-1}$$

where T_s is the sampling period, m_a is the modulation index and θ is the angle between $\vec{I}_{ref}$ and the center of the sector.

Due to the substitution of two opposing active vectors for the zero state, it is difficult for the AZS methods to satisfy the requirement that only two switches occur during the switching state transition. As a consequence, AZS modulation may have higher device switching frequencies than SVM using the zero vectors. The low-order harmonic distortion is another crucial factor for

the application of the AZS methods, because steady-state *LC* resonances can be excited by the low-order harmonics, in particular the fifth and seventh components, which are hardly filtered. Both the switching frequency and low-order harmonics depend on the switching sequence, described later in the chapter.

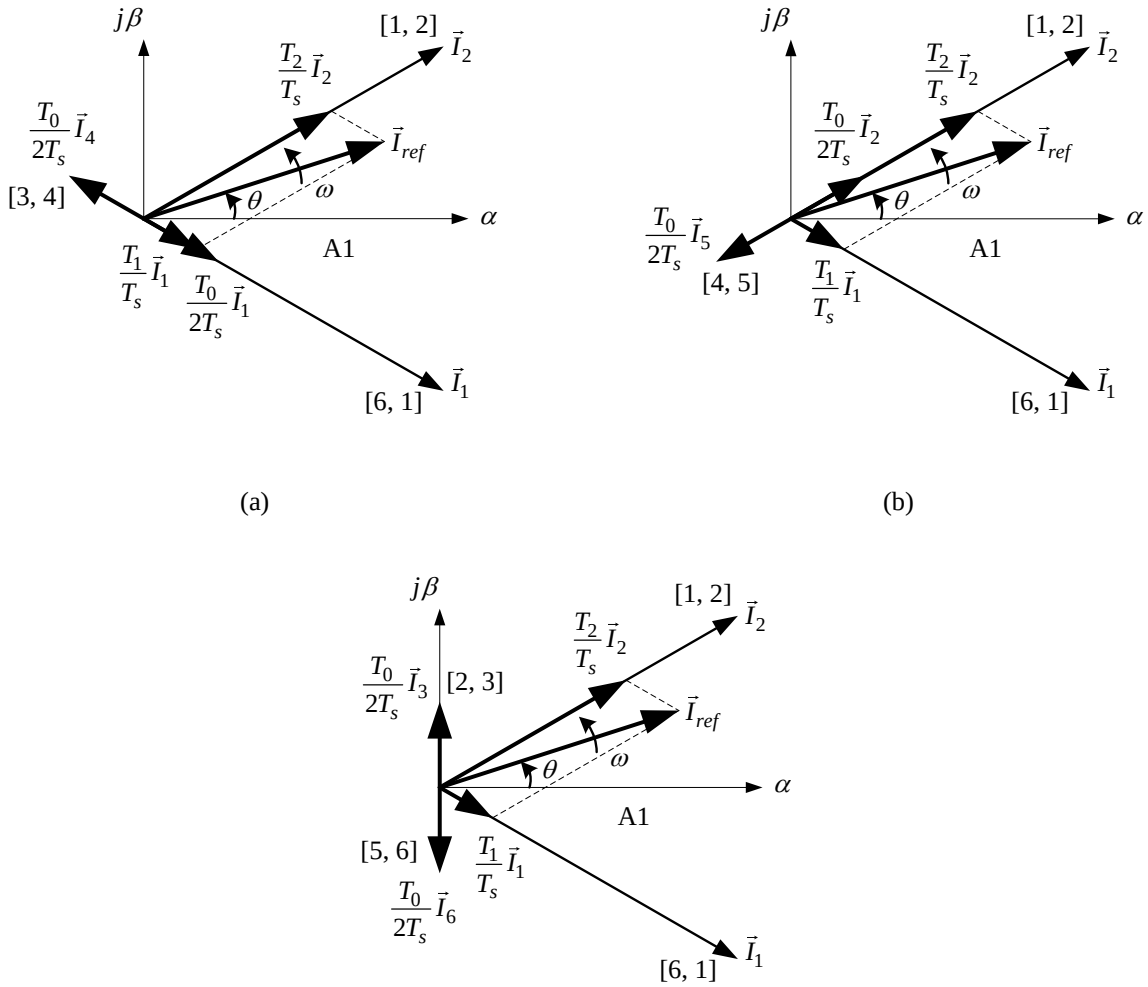


Fig. 5-1 Vector syntheses of the AZS modulation methods in Sector A1. (a) AZS1. (b) AZS2. (c) AZS3.

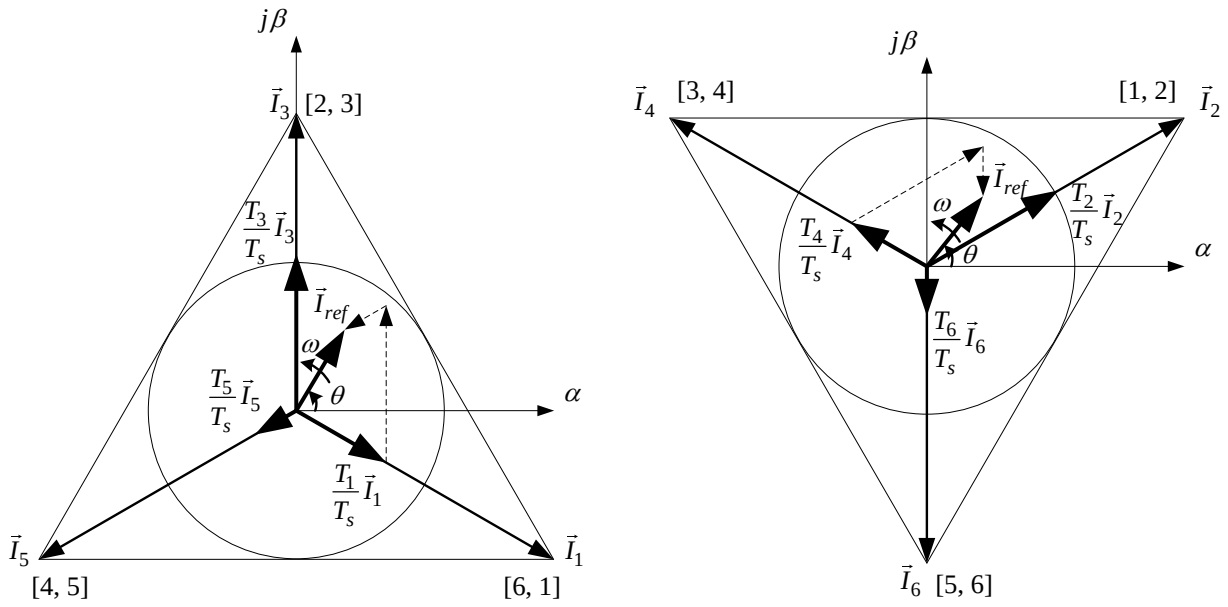
5.1.2 Remote-Three-State Modulation

In RTS modulation, the current reference $\vec{I}_{ref}$ is approximated by three odd and/or even active vectors [37]. In a similar situation to AZS modulation, there are also three RTS schemes in terms of the active vector selection. No matter which sector $\vec{I}_{ref}$ falls in, RTS1 only uses three odd active space vectors ($\vec{I}_1$, $\vec{I}_3$ and $\vec{I}_5$), and RTS2 uses even active vectors ($\vec{I}_2$, $\vec{I}_4$ and $\vec{I}_6$). Their dwell times are calculated by (5-2) and (5-3), respectively:

$$\begin{cases} T_1 = \dfrac{T_s}{3} + T_s \cdot m_a \left(-\dfrac{\sqrt{3}}{6}\sin\theta + \dfrac{1}{2}\cos\theta \right) \\ T_3 = \dfrac{T_s}{3} + \dfrac{\sqrt{3}}{3} T_s \cdot m_a \cdot \sin\theta \\ T_5 = \dfrac{T_s}{3} - T_s \cdot m_a \left(\dfrac{\sqrt{3}}{6}\sin\theta + \dfrac{1}{2}\cos\theta \right) \end{cases} \tag{5-2}$$

$$\begin{cases} T_2 = \dfrac{T_s}{3} + T_s \cdot m_a \left(\dfrac{\sqrt{3}}{6}\sin\theta + \dfrac{1}{2}\cos\theta \right) \\ T_4 = \dfrac{T_s}{3} + T_s \cdot m_a \left(\dfrac{\sqrt{3}}{6}\sin\theta - \dfrac{1}{2}\cos\theta \right) \\ T_6 = \dfrac{T_s}{3} - \dfrac{\sqrt{3}}{3} T_s \cdot m_a \cdot \sin\theta \end{cases} \tag{5-3}$$

where θ is the angle between $\vec{I}_{ref}$ and α-axis, in the range of $0 \le \theta < 2\pi$. Fig. 5-2 illustrates the vector syntheses of RTS1 and RTS2. As a result of the availability of less space vectors, their linear modulation regions have shrunken to the inscribed circle of the triangles. The maximum modulation index is reduced to $1/\sqrt{3}$ or 0.58.



(a) (b)

Fig. 5-2 Vector syntheses and linear modulation regions of RTS1 and RTS2. (a) RTS1. (b) RTS2.

In order to improve the upper bound of the RTS modulation index, the third method RTS3 is proposed by combining RTS1 and RTS2. In RTS3, sectors are identified to determine whether the odd or even vectors will be used. As shown in Fig. 5-3, the corresponding space vectors are taken as the centers of the newly defined sectors B1–B6 which have a 30˚ angle difference from the original sector divisions.

In sectors B1, B3 and B5, $\vec{I}_{ref}$ is synthesized by vectors $\vec{I}_1$, $\vec{I}_3$ and $\vec{I}_5$, the same as in RTS1, whereas in sectors B2, B4 and B6, the synthesis is similar to that in RTS2: $\vec{I}_2$, $\vec{I}_4$ and $\vec{I}_6$ approximate the current reference. The linear region of RTS3 is manifested by the gray circle in Fig. 5-4, with an improved modulation index range from 0 to 2/3 or 0.67.

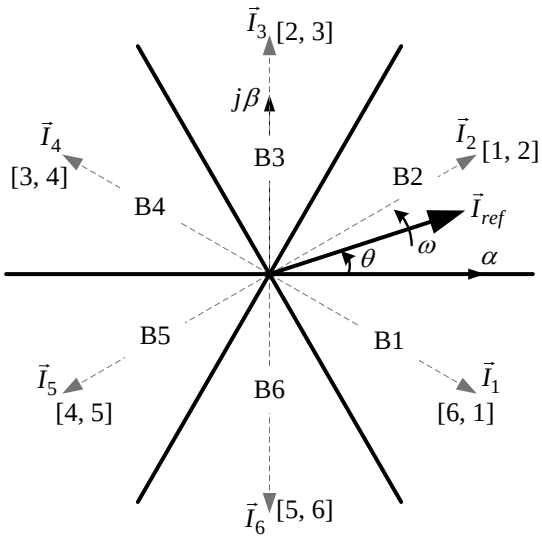


Fig. 5-3 Modified sector divisions: B1 – B6.

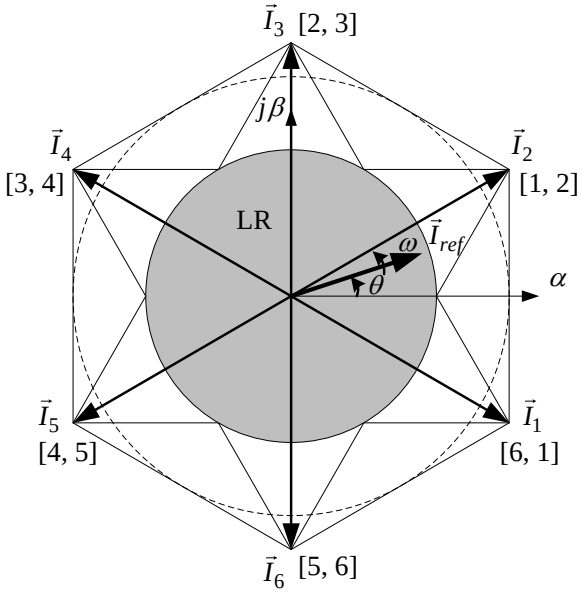


Fig. 5-4 Linear modulation region of RTS3.

The decreased upper bound of the modulation index in RTS modulation will need a higher dc-link current, leading to a larger power loss in the CSI-fed drive system. Similar to AZS modulation, the device switching frequency is also increased in RTS methods. Furthermore, the

remote-state syntheses produce server low-order harmonic distortion, even including the second and ninth harmonics in RTS1 and RTS2, which means neither half-wave nor 3-phase symmetric waveforms [105]. These three disadvantages prevent the application of RTS modulation in high-power CSCs, so they will not be discussed further in the following studies.

5.1.3 Nearest-Three-State Modulation

NTS modulation employs the nearest three active space vectors to synthesize the current reference [38, 39]. The group of three neighboring vectors is identified by dividing the sectors B1–B6, in the same way as in Fig. 5-3. The NTS ampere-second balancing diagram is illustrated in Fig. 5-5 (a) with $\vec{I}_{ref}$ in sector B2. The dwell times are calculated by

$$\begin{cases} T_1 = T_s\left[1 - m_a \sin\left(\theta + \pi/6\right)\right] \\ T_2 = T_s\left(-1 + \dfrac{\sqrt{3}}{2} m_a \sin\theta + \dfrac{3}{2} m_a \cos\theta\right) \\ T_3 = T_s\left(1 - m_a \cos\theta\right) \end{cases} \quad \text{for } 0 \le \theta \le \pi/3, \tag{5-4}$$

where θ is the angle of $\vec{I}_{ref}$ with respect to the leading edge of the sector; T_1, T_2 and T_3, respectively, represent the dwell times of the three vectors in the counterclockwise direction. They cannot assume a negative value. Equation (5-4) would have no solution when $\vec{I}_{ref}$ falls in the shaded hexagon in Fig. 5-5 (b). This requires a modulation index between 2/3 and 1. The gray toroid in Fig. 5-5 (b) indicates the linear region of NTS modulation.

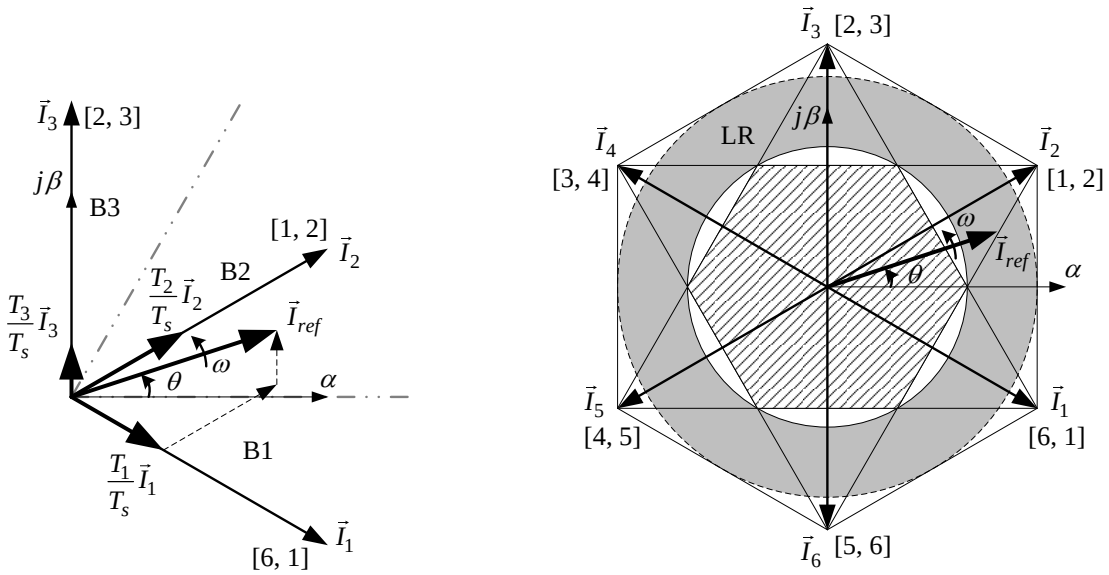


Fig. 5-5 NTS modulation. (a) Vector synthesis in Sector B2. (b) Linear modulation region.

As in the RTS modulation methods, the NTS linear modulation region is also shrunken, but it is the main operating range of a CSC, because a low modulation index is usually avoided for smaller power losses in a high-power motor drive [113, 142]. As the synthesis vectors are adjacent, with carefully designed pulse patterns, the switching frequency and low-order harmonics of NTS modulation may be reduced compared to those of conventional SVM.

5.2 Switching Pattern Development

In terms of the space vector selection and switching sequence development, there are a large number of options in designing a modulation method. However, the device switching frequency and harmonic distortion, especially the low-order components, are two critical criterions that

should be both minimized in high-power CSI-fed drives, since they have significant impacts on the power loss and resonance [106, 109, 111]. Generally, the synthesis with space vectors closest to the reference is superior in the device switching frequency and harmonic performance, which also depend on the switching pattern design [98]. Therefore, the switching sequences of NTS modulation will be developed first. Then, the appropriate AZS pulse patterns will be designed as compensation, when the modulation index is adjusted to below 2/3 with a large dc-link current required for the unity or high input power factor operation.

5.2.1 Switching Sequences for NTS Modulation

Three switching patterns for NTS modulation are demonstrated in Fig. 5-6, where NTS1 and NTS3 are saw-tooth-carrier-based sequences, and NTS2 is based on a triangular carrier. The difference between NTS1 and NTS3 is that the saw-tooth carrier for the former is always upward, whereas the upward and downward carriers alternate in one sector for the latter. When the number of samples in each sector N is larger than 1, more than two switches will occur in NTS1 at the end of the sampling period. NTS2 and NTS3 satisfy the requirement of two switches at all times. The device switching frequencies of NTS1, NTS2 and NTS3 are, respectively, $f_1 \cdot (4N\text{-}1)$, $f_1 \cdot (4N\text{+}1)$ and $f_1 \cdot (2N\text{+}1)$, where f_1 is the converter fundamental frequency.

Considering the worst case for the inverter-side CMV magnitude and synchronous modulation, we chose a rated fundamental frequency f_1 = 60 Hz to investigate the low-order harmonics of the proposed NTS sequences at their reasonable switching frequencies. The numbers of samples in each sector of NTS1, NTS2 and NTS3 are assigned as N = 2, 2 and 4, respectively, such that their switching frequencies are f_{sw} = 420 Hz, 540 Hz and 540 Hz, all

around 500 Hz for a high-power CSC [105, 143]. Fig. 5-7 shows the fifth- and seventh-harmonic contents of the PWM current with the NTS methods, compared to those with conventional SVM at f_{sw} = 360 Hz (N = 2) and 540 Hz (N = 3) in the range of $m_a \geq 0.67$.

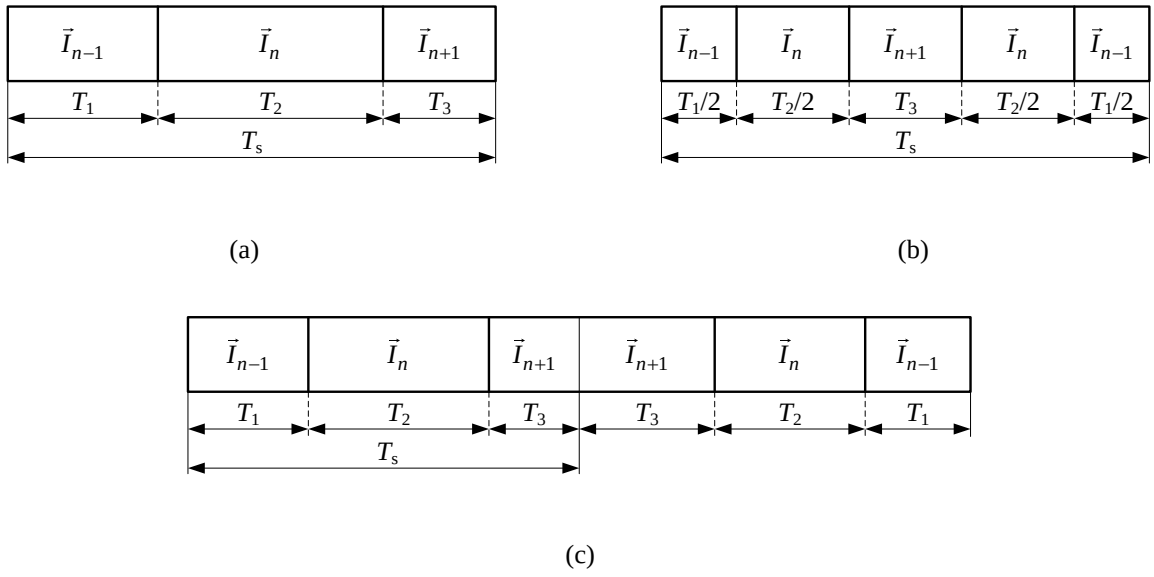
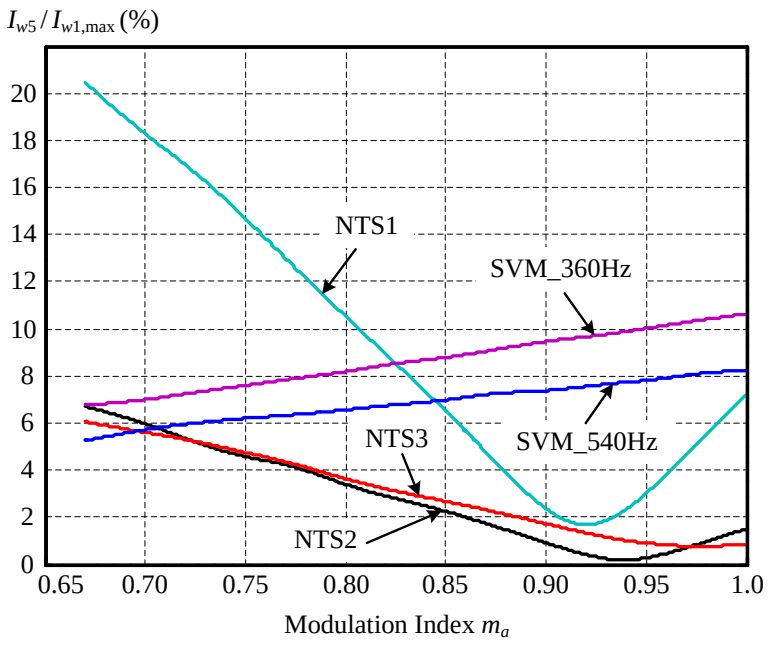
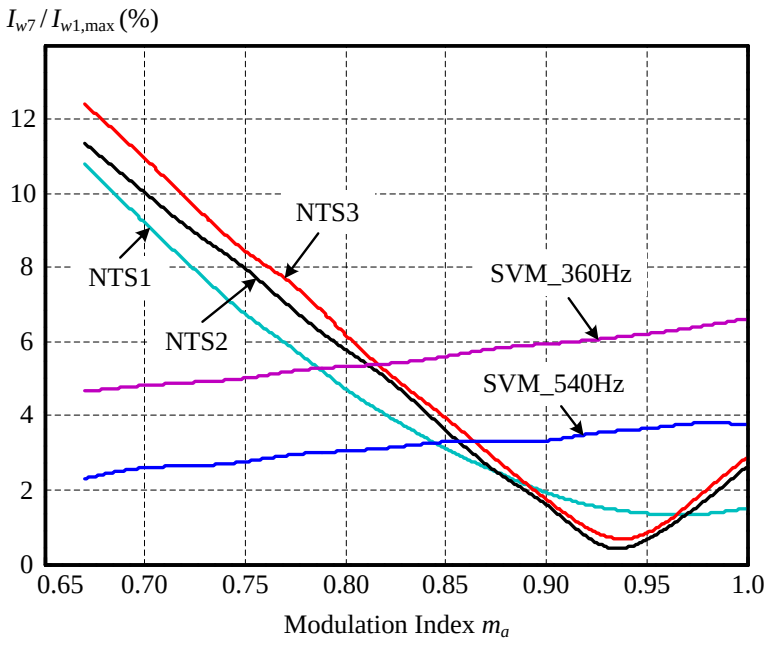


Fig. 5-6 Switching patterns for NTS modulation. (a) NTS1. (b) NTS2. (c) NTS3.

The NTS sequences produce lower fifth- and seventh-harmonic distortions than their conventional SVM counterparts when the modulation index m_a is larger than 0.85. However, NTS1 would not be a practical sequence because of its high fifth-harmonic content with a smaller m_a (i.e., m_a < 0.8). NTS2 and NTS3 are superior in the fifth-harmonic distortion to conventional SVM almost throughout the linear modulation region. Although NTS2 and NTS3 present the worse seventh-harmonic performances with m_a < 0.8, their distortion level is still acceptable. Therefore, NTS2 and NTS3 are the preferred modulation methods due to their CMV reduction while maintaining good low-order harmonic performances and a reasonable switching frequency.



(a)



(b)

Fig. 5-7 Low-order harmonic performances of the PWM current with NTS and conventional SVM sequences. (a) Fifth-harmonic content. (b) Seventh-harmonic content.

As proposed in [106], the modulation strategy is switched from SHE methods to SVM for active damping of the transient *LC* resonance. On the other hand, the dc-link current in high-power CSC-based drives is usually variable and minimized to reduce the system loss [113]. Therefore, during the modulation transition, the dc-link current would also be changed according to the magnitude of the output current. The modulation index of SVM is kept high, probably at 1 [106]. However, the use of SVM increases the CMV magnitude. The CM inductance of the dc-link choke should not be designed for the worst case during transients. The NTS methods can thus be employed to replace conventional SVM in this situation, where a high modulation index within the linear region of NTS modulation is satisfied.

Another application of SVM in CSI-fed drives is the input power factor control. In order to achieve unity or high power factor operation, the dc-link current should be regulated higher than a minimum value, which should be large enough to compensate for the line-side capacitive current. No matter whether SVM is used in the current-source rectifier (CSR) or inverter, the modulation index needs to be adjusted [114, 115]. As a result, the CMV magnitude is aggravated again. In particular, at the rated frequency of the CSI or with SVM adopted in the CSR, the CMV peak value can achieve the rated phase voltage amplitude. NTS modulation has provided a solution when $m_a \geq 0.67$. Once the modulation index is adjusted to a lower value, AZS modulation could be considered to reduce the CMV magnitude.

5.2.2 AZS Pulse Patterns

Based on the conventional SVM sequence shown in Fig. 5-8 (a), Fig. 5-8 (b), (c) and (d), respectively, illustrate the pulse patterns for AZS1, AZS2 and AZS3, where $\vec{I}_{n+3}$ and $\vec{I}_{n+4}$

represent the opposite vectors of $\vec{I}_n$ and $\vec{I}_{n+1}$, and $\vec{I}_{n-1}$ and $\vec{I}_{n+2}$ are opposing vectors. The device switching frequencies of AZS1, AZS2 and AZS3 are $f_1 \cdot (5N+1)$, $f_1 \cdot 5N$ and $f_1 \cdot (5N+1)$, i.e., 660 Hz, 600 Hz and 660 Hz, respectively, for $N = 2$ and the rated fundamental frequency $f_1 = 60$ Hz. As mentioned earlier, the switching frequencies are higher than those of NTS and conventional SVM sequences. This is a drawback of the AZS modulation techniques.

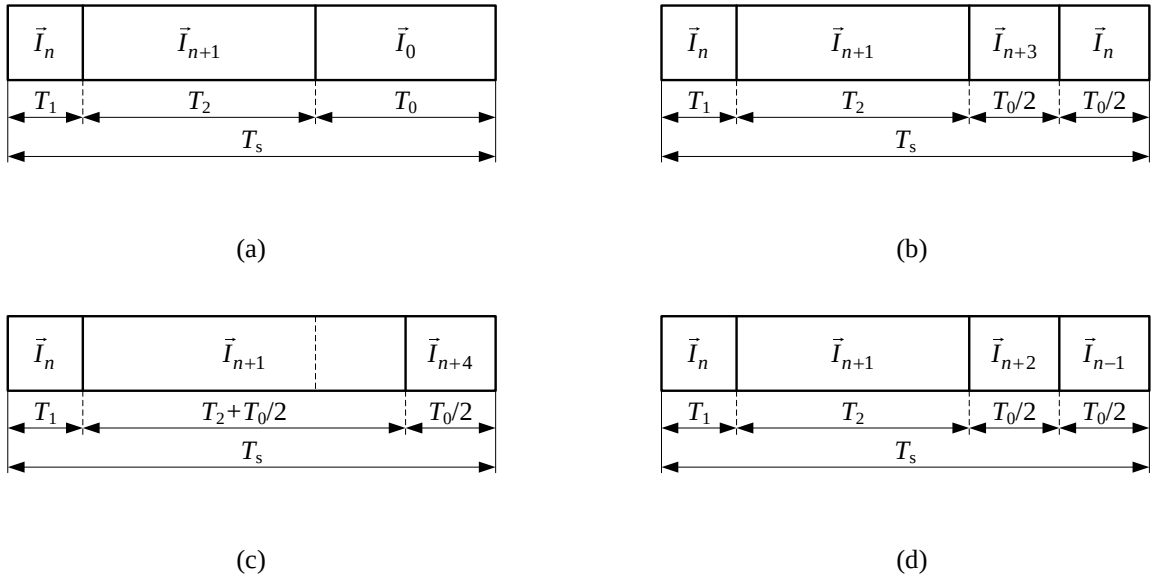
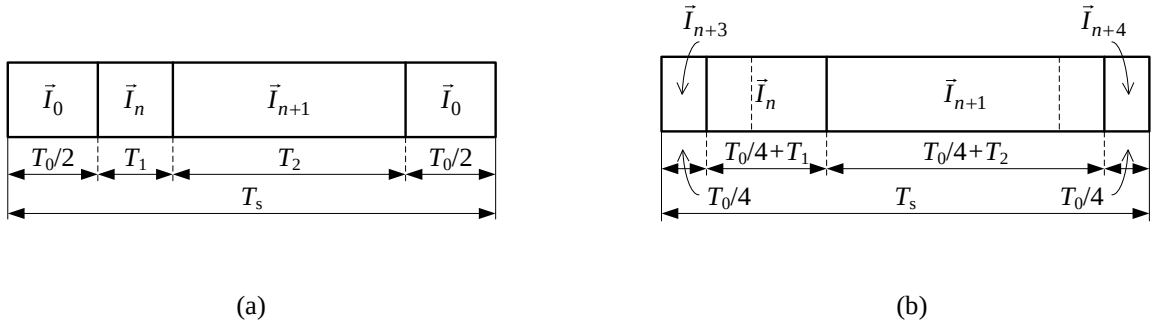


Fig. 5-8 Conventional SVM switching sequence: $\vec{I}_n \rightarrow \vec{I}_{n+1} \rightarrow \vec{I}_0$ and the corresponding AZS modulation pulse patterns. (a) Conventional SVM. (b) AZS1. (c) AZS2. (d) AZS3.

Besides the pulse patterns in Fig. 5-8, a new combined AZS method, called AZS4, is proposed in Fig. 5-9 (b). AZS4 stems from the SVM sequence $\vec{I}_0 \rightarrow \vec{I}_n \rightarrow \vec{I}_{n+1} \rightarrow \vec{I}_0$ shown in Fig. 5-9 (a) and uses the substitute pairs of active vectors in AZS1 and AZS2 in one switching sequence [105, 120, 121]. The switching frequency of AZS4 is $f_1 \cdot (6N\text{-}1)$ or 660 Hz, for $N = 2$ and $f_1 = 60$ Hz. Although the combined method AZS4 does not decrease the switching frequency of AZS modulation, it has a better low-order harmonic performance, especially with a smaller m_a.

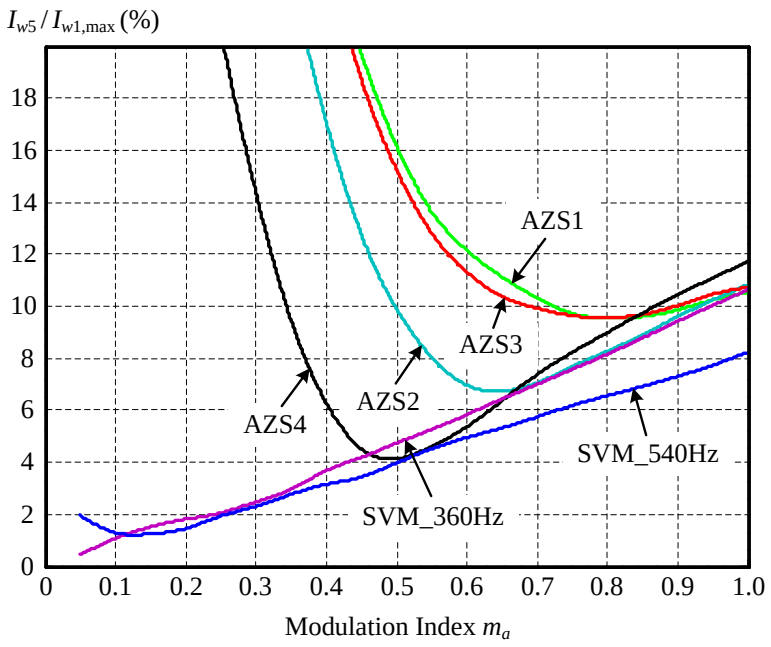
This is demonstrated in Fig. 5-10. The fifth- and seventh-harmonic contents of all AZS methods are close to those of conventional SVM with a high m_a, but they rise steeply with m_a decreasing. AZS4, however, can extend its m_a to 0.4 with acceptable low-order harmonic distortion.



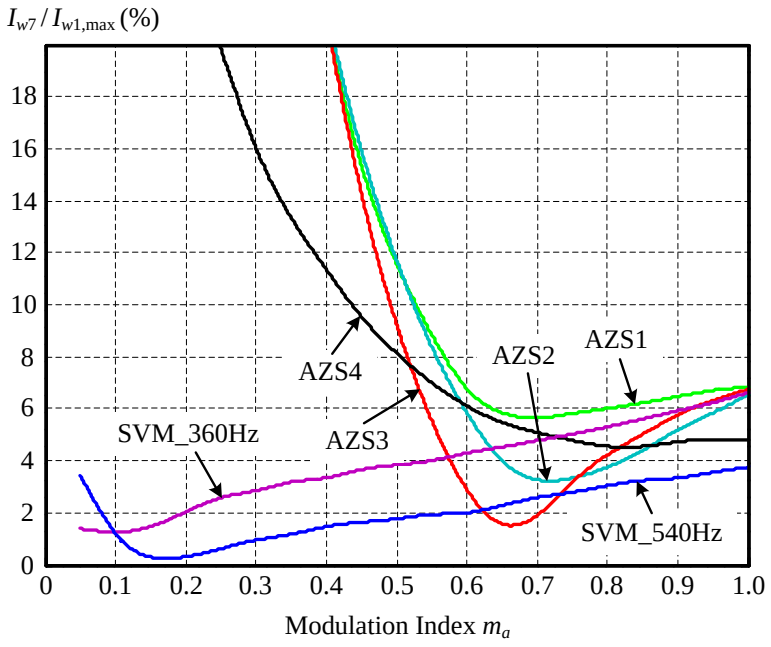
(a) (b)

Fig. 5-9 SVM switching sequence: $\vec{I}_0 \rightarrow \vec{I}_n \rightarrow \vec{I}_{n+1} \rightarrow \vec{I}_0$ and the combined method AZS4. (a) SVM sequence. (b) AZS4.

Fig. 5-11 shows the implementation of the NZS techniques when the modulation index changes. The modulation index is an input to the PWM modulator from the CSR or CSI controller. NZS modulation is realized the same as conventional SVM, except for adding a logic algorithm that is to select a modulation technique according to the value of m_a. If $m_a \geq 0.67$, NTS2 or NTS3 will be adopted; AZS4 can be chosen when $0.4 < m_a < 0.67$. Due to the degradation of the harmonic performances, the proposed PWM methods are not suitable for $m_a <$ 0.4. In fact, the regulation of a variable dc-link current normally avoids low modulation indices in high-power CSI drives even with the high input power factor control; otherwise, large power losses would be generated.



(a)



(b)

Fig. 5-10 Low-order harmonic performances of the PWM current with AZS1–4 and conventional SVM sequences. (a) Fifth-harmonic content. (b) Seventh-harmonic content.

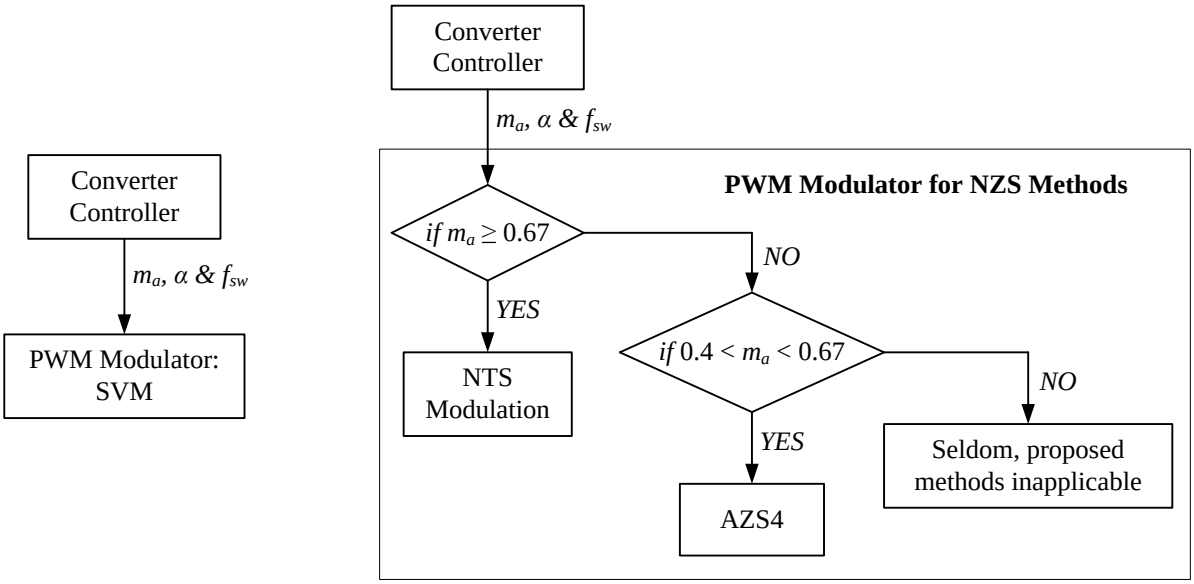


Fig. 5-11 Implementation of conventional SVM and NZS modulation. (a) Conventional SVM. (b) Proposed NZS modulation methods.

5.3 Simulation Varification

Fig. 5-12 illustrates a CSC system with a three-phase *RL* load, where the rectifier supplies a dc-link current. In the simulation, the NZS modulation methods were implemented on the CSI to verify their CMV reduction effects. With the system ratings of 1MVA/4160V, the parameters remained identical to those in Chapter 2, i.e., R_L = 0.9 pu, L_L = 0.44 pu and C_f = 0.4 pu. The fundamental frequency was 60 Hz. For comparison, the ac and CM voltage waveforms generated by conventional SVM are extracted in Fig. 5-13. As observed, the CMV has a maximum value of 3390 V (approximately 1.41 pu), as large as the phase voltage magnitude.

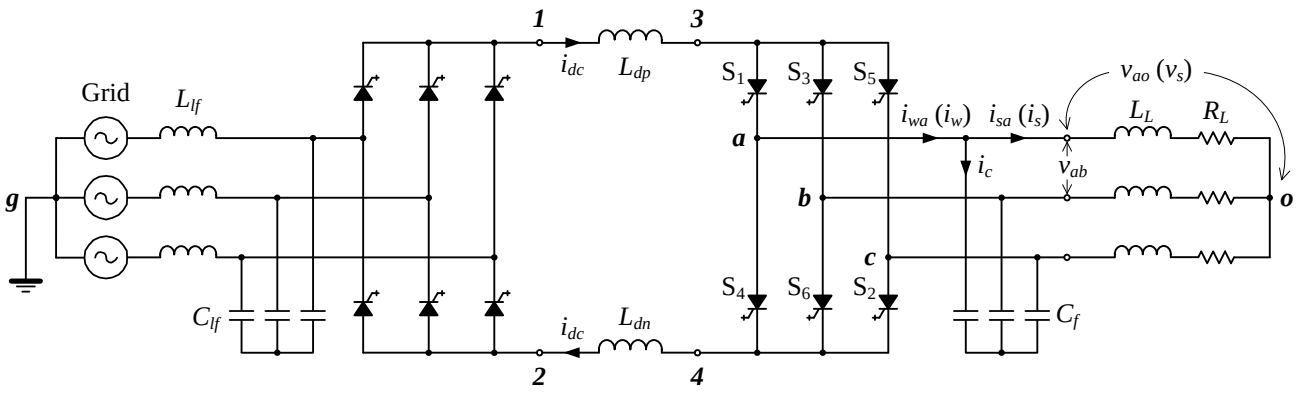


Fig. 5-12 CSC system with a *RL* load.

Fig. 5-14 (a)–(c), respectively, show the CMVs produced by NTS2, NTS3 and AZS4. The modulation index of the first two methods was kept at 0.9, the same as in the simulation of conventional SVM, whereas that of AZS4 was set to 0.5. This value was in the method's applicable range of $0.4 < m_a < 0.67$. The CMV magnitudes in Fig. 5-14 (a)–(c) are all reduced at least by half compared to that in Fig. 5-13.

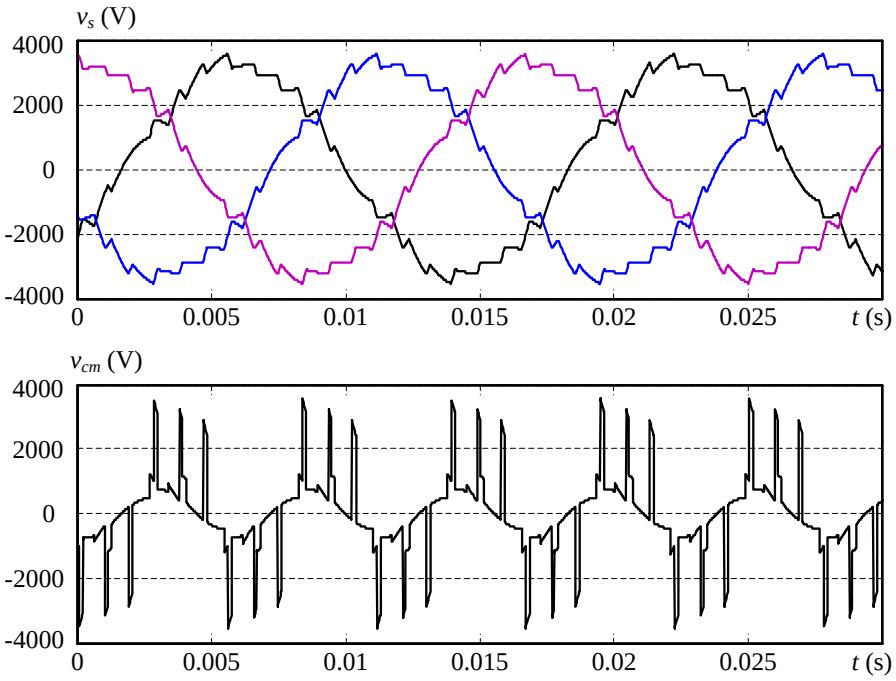
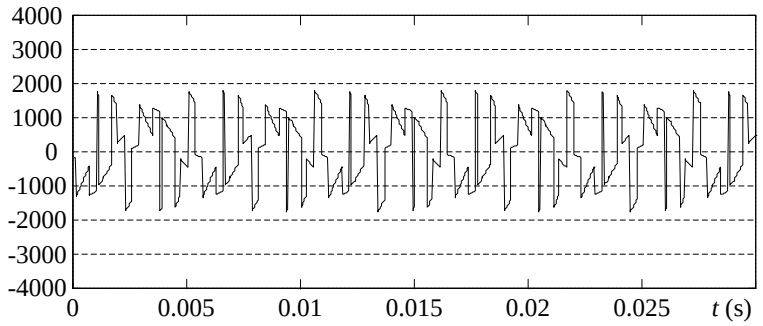
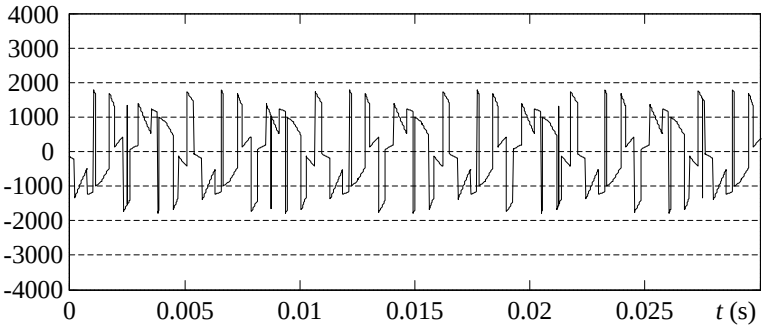


Fig. 5-13 Three-phase ac output and CM voltage waveforms of the 1MVA/4160V CSI with conventional SVM – the upper: three-phase ac voltages v_s; the lower: CMV v_{cm}.

By the same principle of avoiding zero vectors, the modified PWM techniques should have similar performances in CMV reduction. However, it is interesting to note that AZS4 generates a waveform distinct from those of the NTS methods and has a smaller CMV magnitude that is only a little higher than 1000 V (0.42 pu). This is not due to the lower m_a used in the simulation of AZS4; instead, it is the consequence of the nonzero-state implementation and voltage distortion, which also includes the harmonics of orders higher than 5 and 7. Fig. 5-14 (d) displays the CMV waveform of AZS2 with m_a = 0.9. AZS4 and AZS2 have almost the same waveforms and close CMV magnitudes in spite of their different modulation indices. As compared in Fig. 5-14, AZS modulation performs better than the NTS methods in CMV reduction.



(a)



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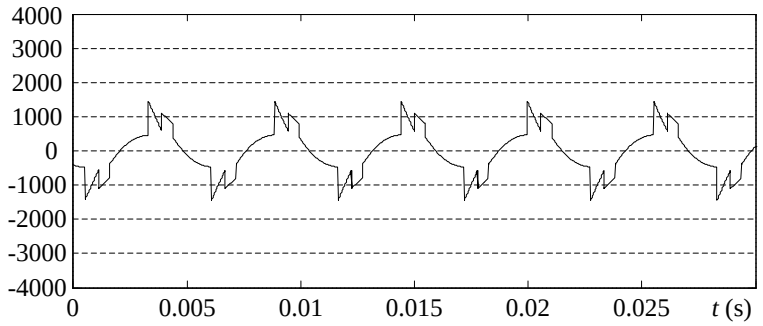
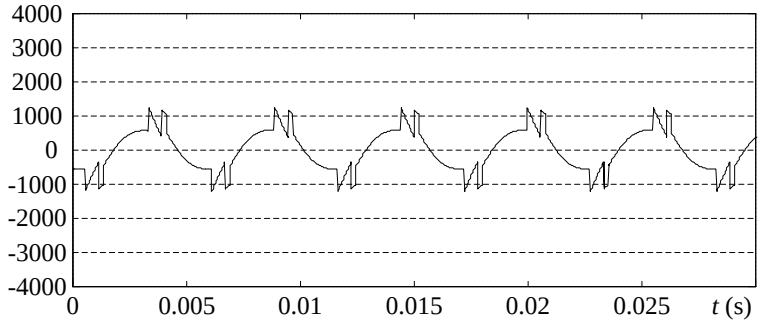


(c)



(d)

Fig. 5-14 CMV waveforms generated by the NZS modulation techniques. (a) NTS2. (b) NTS3. (c) AZS4 with m_a = 0.5. (d) AZS2 with m_a = 0.9.

5.4 Experimental Verification

The experimental setup was established as shown in Fig. 5-12 based on a small-scale gate-turn-off thyristor (GTO) system and DSP-field-programmable gate array (DSP-FPGA) controller. The CSR supplied a variable dc-link current. The NZS modulation techniques were implemented on the CSI with a three-phase *RL* load to verify the CMV reduction effects and harmonic performances. Since NTS2 and NTS3 exhibit similar performances in the simulation, the experiment using only the former method was carried out.

The fundamental frequency of all the experiments was set to 60 Hz. The power factor of the *RL* load was 0.9 and the filter capacitance was 0.4 pu, the same per unit values as in the high-power simulations. For comparison, Fig. 5-15 (a) shows the ac output (*phase a*) and CM voltage waveforms of conventional SVM with f_{sw} = 540 Hz and m_a = 0.9. As observed in the figure, the load condition and filter capacitance locate the zero states near the phase voltage peaks. According to its definition in Chapter 2, the CMV of the CSI was measured by adding the voltages of the three-phase load neutral point with respect to the positive and negative dc points on the inverter side, i.e., $-(v_{3o} + v_{4o})$ referring to Fig. 5-12. The measurement equals twice the real CMV. It is notable that the scale of the CMV measurement is also twice that of the ac output voltage. The waveforms demonstrate that the maximum CMV produced by conventional SVM is approximately the phase voltage amplitude of 100 V (close to 1.41 pu). This is undesirable for the machine winding insulation, especially in MV CSI drives.

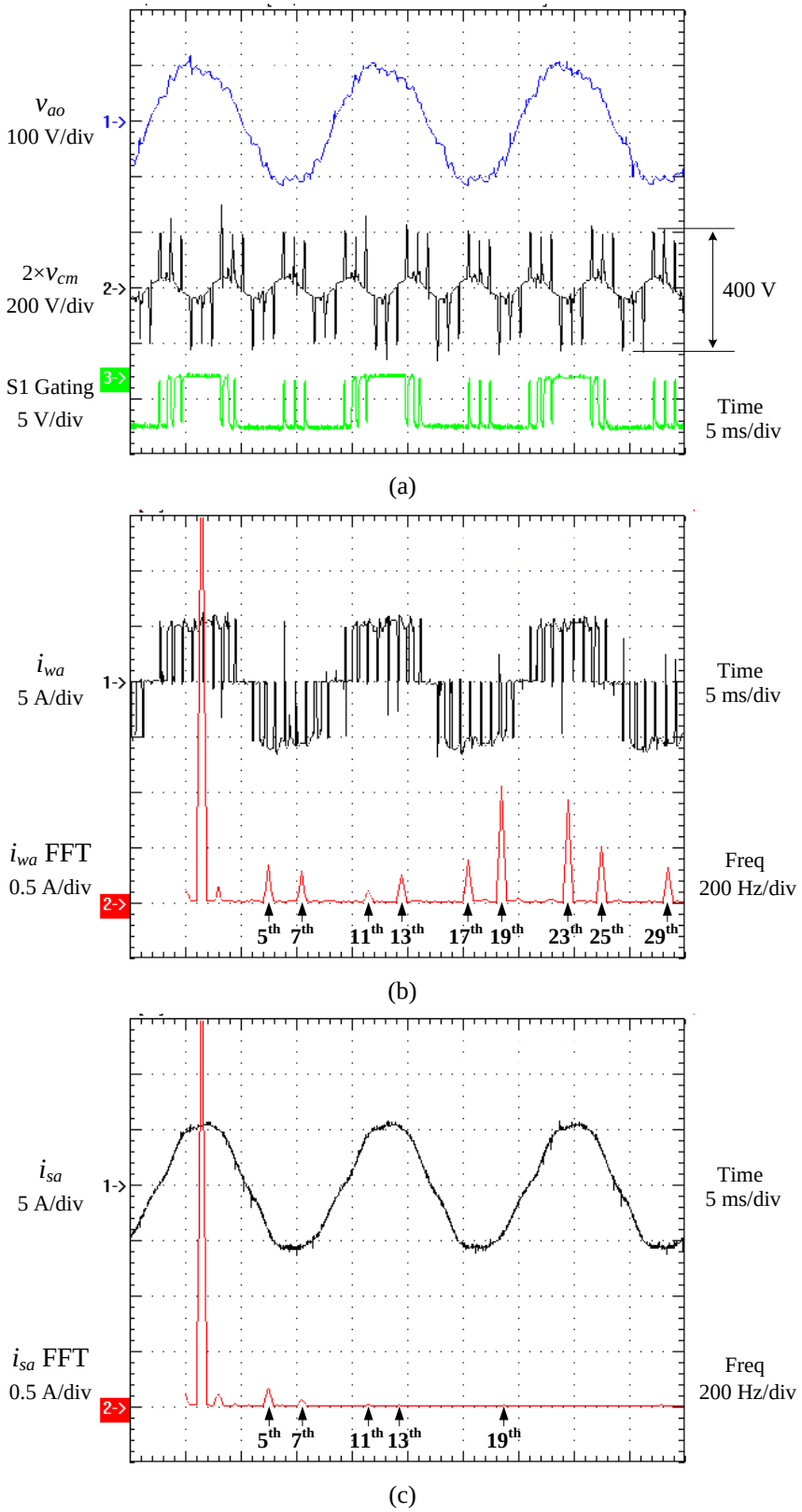


Fig. 5-15 Experimental results of the CSI with conventional SVM. (a) From top to bottom: ac-side phase voltage v_{ao}, twice the CMV $2\times v_{cm}$ ($-(v_{3o} + v_{4o})$) and the gating signal for S1. (b) PWM current i_{wa} and its FFT analysis. (c) Load current i_{sa} and its FFT analysis.

Fig. 5-15 (b) and (c) provide the PWM current, the load current and their spectra. In the FFT analysis of the PWM current, the 19th harmonic has a large value, because it is in the sideband of the sampling frequency, 1080 Hz. With the dc current at 5.65 A (1.41 pu), the fifth- and seventh-harmonic contents are, respectively, $I_{w5}/I_{w1,\max}$ = 7.6% and $I_{w7}/I_{w1,\max}$ = 6.1%, conforming to the simulation results. The minor error is caused by the dc-link current ripple from the CSR. By comparing the spectra of the PWM and load currents, the high-order harmonics of the former are almost completely filtered, whereas the fifth and seventh harmonics are still obviously observed in the latter waveform. This confirms the difficulty of filtering the low-order harmonics, in particular the fifth and seventh components in the PWM current.

The experimental results of NTS2 are shown in Fig. 5-16. The switching frequency and modulation index were kept at f_{sw} = 540 Hz and m_a = 0.9, respectively, which are verified by the number of pulses, PWM and load current waveforms. The CMV waveform shows a 50% decrease in magnitude, compared to that in Fig. 5-15 (a). The fifth- and seventh-harmonic contents of the PWM current are only, $I_{w5}/I_{w1,\max}$ = 2.2% and $I_{w7}/I_{w1,\max}$ = 5.0%. They are lower than those produced by conventional SVM and demonstrate the superiority of NTS modulation in low-order harmonic performance. However, the 11th- and 13th-harmonic contents of the PWM current show a significant increase. This is because the sampling frequency of NTS2 is only 720 Hz, equal to the 12th-harmonic frequency. Fortunately, the filter is effective on the 11th and 13th harmonics, as manifested in Fig. 5-16 (c). The impact of the slightly higher amount of the 11th and 13th components in the load current is on the motor thermal performance, which, however, would be better than that with conventional SVM when taking the fifth and seventh harmonics into account.

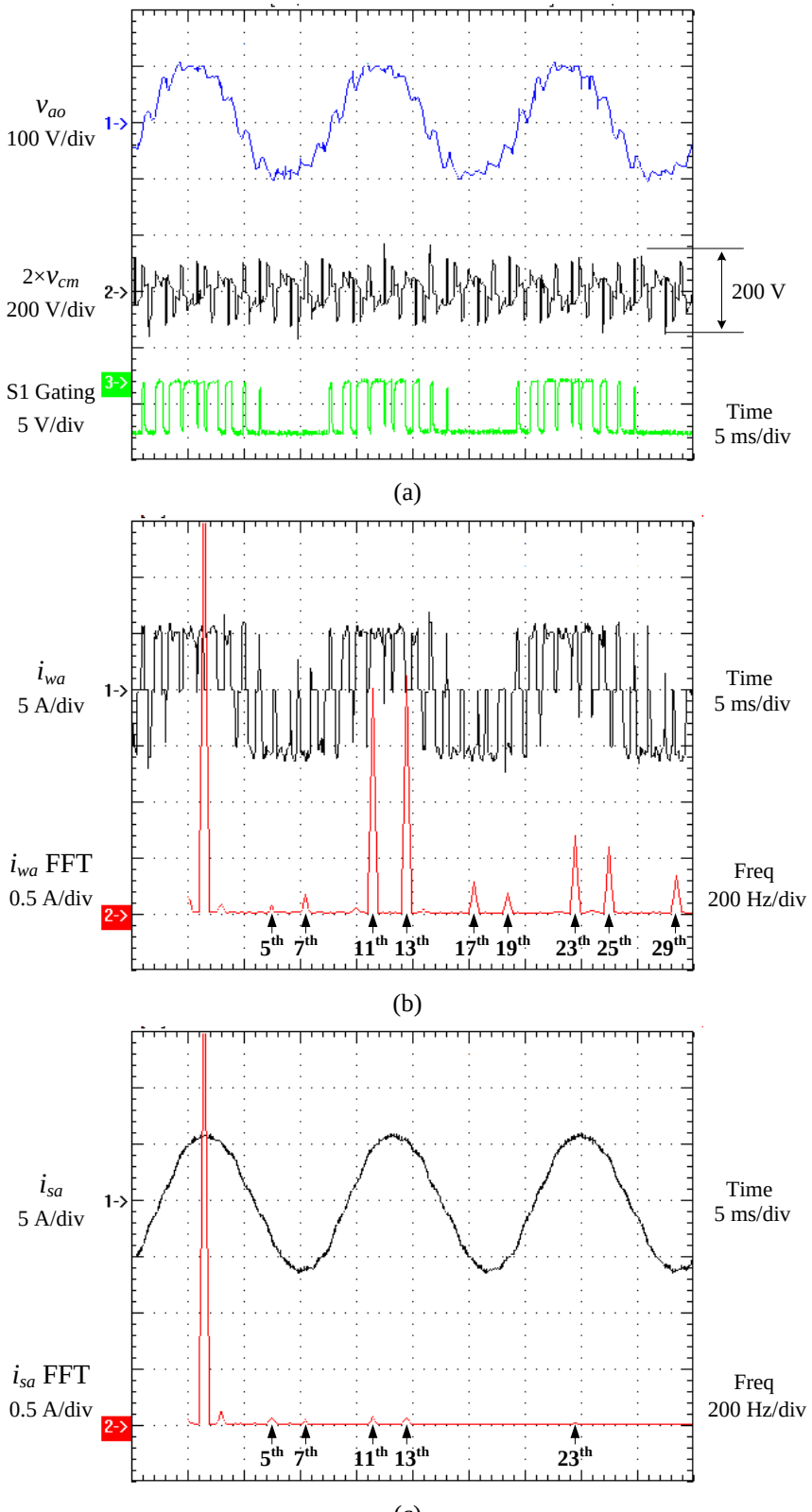


Fig. 5-16 Experimental results with the NTS2 technique. (a) From top to bottom: ac-side phase voltage v_{ao}, twice the CMV $2\times v_{cm}$ ($-(v_{3o} + v_{4o})$) and the gating signal for S1. (b) PWM current i_{wa} and its FFT analysis. (c) Load current i_{sa} and its FFT analysis.

In the experiment with AZS4, the modulation index was decreased to 0.5 for validation of the method's practical use. It is notable that the scales of the PWM current and its FFT analysis in Fig. 5-17 (b) have been doubled compared to those in Figs. 5-15 (b) and 5-16 (b), since the dc-link current was raised to 10.68 A (2.67 pu) for m_a = 0.5 such that the rms value of the output voltage is unchanged with a fixed load. In practice, the grid voltage is always at its rated value even with the m_a control adopted in the CSR for a high power factor. Comparing the CMVs in Figs. 5-16 (a) and 5-17 (a), AZS4 manifests a better mitigation effect, but the expense is the deterioration of the differential-mode harmonic performance. Although the fifth- and seventh-harmonics of the PWM current are acceptable, the sideband harmonic contents of the sampling frequency, i.e., $I_{w11}/I_{w1,\max}$ and $I_{w13}/I_{w1,\max}$, both exceed 100%. The inferior total harmonic distortion (THD) is evidenced by the waveforms of the phase voltage and load current. However, it is seen from the FFT analysis of the load current that the 11^{th}- and 13^{th}-harmonic contents have been reduced to 7.7% and 6.4% respectively after filtering.

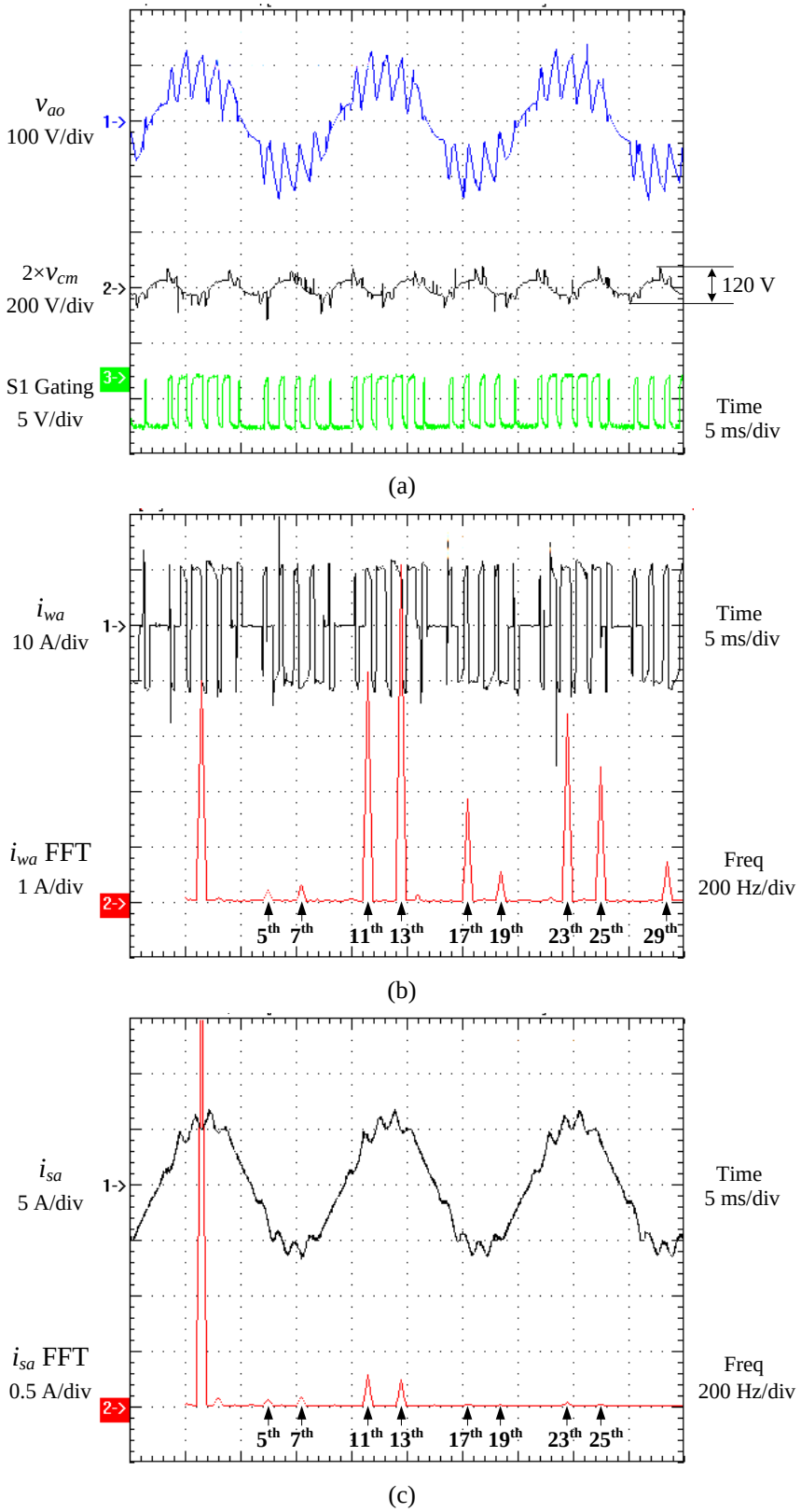


Fig. 5-17 Experimental results with the combined AZS modulation method (AZS4). (a) From top to bottom: ac-side phase voltage v_{ao}, twice the CMV 2×v_{cm} (-(v_{3o} + v_{4o})) and the gating signal for S1. (b) PWM current i_{wa} and its FFT analysis. (c) Load current i_{sa} and its FFT analysis.

5.5 Summary

This chapter adapted three types of nonzero-state modulation techniques for use in current-source converters to reduce the CMV magnitude. By avoiding zero states, the proposed nonzero-state techniques, i.e., active-zero-state, remote-three-state and nearest-three-state modulations, are expected to decrease the CMV magnitude at least by half. Due to the high power loss and severe harmonic distortion produced by remote-three-state modulation, it has been eliminated for high power current-source inverter-fed drives.

Switching patterns for active-zero-state and nearest-three-state modulations were developed. Both simulation and experimental results were provided to validate the CMV reduction effects and harmonic performances of the proposed methods. The research demonstrated that the designed nearest-three-state sequences present superior low-order harmonic performances to that of conventional SVM with a high modulation index and no increase in the switching frequency. The combined active-zero-state technique could be implemented as compensation to reduce the CMV magnitude, when the modulation index is adjusted to a smaller level for high input power factor operation.

Chapter 6

Conclusions

Common-mode voltages (CMVs) that result from the switching action of solid-state devices in power converters lead to undesirable problems, such as motor ground current and bearing damage, premature failure of the stator winding insulation in medium-voltage (MV) drives and leakage currents in transformerless photovoltaic (PV) generation systems. Although various solutions have been presented in the literature, more efforts need to be made to improve the reliability and efficiency, as well as to reduce the system size and cost.

Based on the investigation of CMVs in power converters, this dissertation proposed reliable, practical and more cost-effective methods to mitigate the CMV issues within the low and medium frequency ranges. The contributions include the design and optimization of a novel integrated ac choke, its application and effect analysis in voltage-source converter (VSC) systems, and new space-vector modulation (SVM) techniques to keep the compact design of the integrated dc-link choke in transformerless current-source converter-(CSC) based drives.

6.1 Contributions and Conclusions

The main contributions and conclusions of the research work are summarized as follows.

1) Investigation of CMVs in power converters.

Besides reviewing the magnitudes and values of CMVs in VSCs, the spectrum distributions and the characteristics in other converter topologies, including diode and SCR rectifiers as well as CSCs, have been comprehensively analyzed. The following conclusions are attained:

- The magnitude of CMVs in diode and SCR rectifiers is determined by the three-phase ac voltages and the spectra are at the triplen frequencies in the low frequency range.
- The CMVs in VSCs are primarily distributed in the medium frequency range, i.e., around the switching frequency and its integral multiples. The reason for triplen components of CMVs in the low frequency range is the corresponding harmonic injection in modulation, e.g. SVM. The lowest CMV distribution with sinusoidal pulse-width modulation (SPWM) is at the switching frequency, which is favorable for the filter and choke design.
- Switching constraints for CSCs lead to the CMVs being dominant at the third and other low-order triplen frequencies. Under normal operating conditions, SVM produces a larger CMV magnitude than conventional selective harmonic elimination (SHE) modulation.

2) Proposed and designed a novel three-phase integrated choke.

An integrated ac choke with novel structures has been proposed, designed and optimized. Not only does the proposed choke filter the DM harmonics, but it also suppresses the CM voltage/current in the medium frequency range in VSCs, facilitating the implementation of transformerless system configurations. Compared to separate inductors, the magnetic integration reduces the choke's weight by 50% and copper loss by 40%. The system efficiency is thus improved, and the cost is considerably lowered. Finite element analysis (FEA) simulations and experiments of a prototype were conducted to validate the feasibility of the integrated choke.

3) **Analyzed VSC systems using the integrated choke by CM-circuit modeling and simulation.**

Transformerless PV inverters and neutral-connected motor drives have been identified as applications of the integrated choke. The appropriate system grounding and the coordination with other filter components, such as CM capacitors and damping resistors, were presented. The CM behaviors of these VSC systems were explained by the circuit modeling and simulations with evaluated parameters. The results demonstrated that almost all the CMVs are imposed on the integrated choke and the ground leakage currents are decreased to the level that is negligible in motor drives and satisfies the standard for PV generation systems. These observations verify the CM modeling and effect analysis of the integrated choke in VSC systems.

4) **Development of New SVM schemes for CMV mitigation in MV CSCs.**

Three nonzero-state modulations, namely active-zero-state (AZS), remote-three-state (RTS) and nearest-three-state (NTS) methods, have been proposed to reduce the CMV magnitude at least by half in CSCs with SVM. According to the investigation, only AZS and NTS modulation schemes are suitable and their switching patterns have been designed per the switching frequency and harmonic performances. The conclusions are provided as follows:

- NTS methods present superior low-order harmonic performances with a high modulation index ($m_a \geq 0.67$) and no increase in the switching frequency.
- A combined AZS technique can be implemented as compensation to mitigate the CMV under high input power factor operation with a lower modulation index ($0.4 < m_a < 0.67$).

The CMV reduction effects and harmonic performances have been supported by both simulations and experiments.

6.2 Future Work

The ideas proposed in this dissertation can be extended in the following areas as possible future work:

1) Integrated ac choke with combined core materials.

The amorphous and nano-crystalline magnetic core materials improve the CM blocking performance of the integrated ac choke at high frequencies, but they are expensive. A new integrated choke, whose core is composed of two parts: the circumference made of amorphous or nano-crystalline magnetic materials and the inner legs with powdered iron, can be proposed to keep the CM performance high but reduce system costs.

2) Passive filters with the integrated chokes.

The research in this dissertation was focused on the design and use of the integrated choke, which, in fact, is a part of passive filters. The combination of the choke, CM capacitors and damping resistors in Chapter 4 can be regarded as a specific kind of filters. Based on the proposed choke and aforementioned variety, assorted passive filters for both CMV mitigation and DM filtering could be studied in the future with supported experiments.

3) Modulation and new integrated dc-link chokes for parallel MV CSC-based drives.

As revealed in Chapter 2, the predominant CMV component that is distributed at the triple fundamental frequency in CSCs is hardly mitigated by modulation schemes. However, parallel CSCs provide modulation redundancy, which may inspire new techniques to mitigate the CMV [144]. Moreover, the dc-link inductors of parallel CSC-based drives could be incorporated into one integrated choke to smooth the dc-link current as well as to attenuate the CM and circulating currents. This further reduces the system size, weight and cost.

Appendix A

Design Procedure of the Integrated Choke

Due to the special configuration, the integrated choke could no longer be designed via a straightforward route as standard inductors, but needs an optimization program. The minimum weight point can be tracked either manually or automatically by an intelligent algorithm in the program. This appendix describes the design procedure of the integrated choke step by step.

As shown in Fig. A-1, five basic variables are defined to independently and completely represent the core geometry: w – thickness of the core, a – width of the ring core, r – inner radius of the ring, b – width of the bridge legs, and l_g – length of air gaps, where the former four can be used to calculate the key parameters for reluctances in Chapter 3:

$$l_b = r + a/2\,; \tag{A-1}$$

$$l_c = 2\pi \cdot \left(r + a/2\right); \tag{A-2}$$

$$A_c = a \cdot w \cdot SF\,; \tag{A-3}$$

$$A_b = b \cdot w \cdot SF\,, \tag{A-4}$$

where SF is the stacking factor of laminations and assumed equal to 0.98.

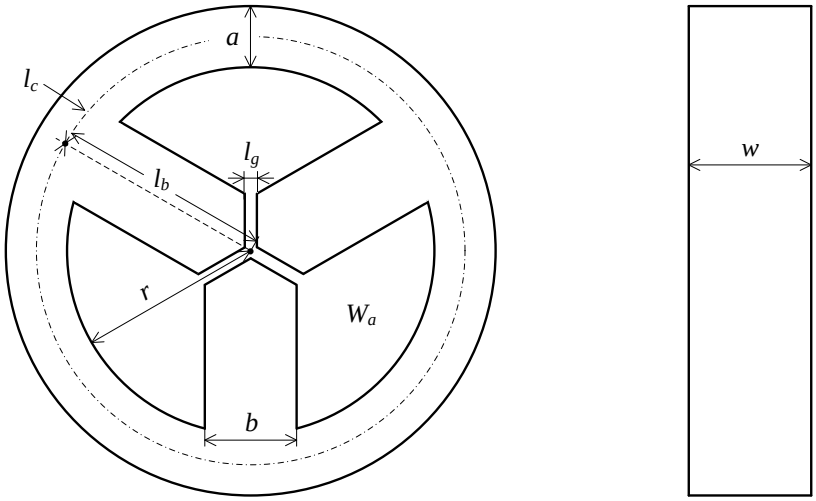


Fig. A-1 Mechanical outline of the circular core of the integrated choke.

Relationships also exist between these basic geometric variables. According to (3-19), there is

$$k_a = \frac{a}{b} = \frac{1}{\sqrt{3}} \cdot \left[1 + \frac{\left(v_{cm,\max} / 2\pi f_{sw} \right)}{L_{dm} \cdot I_{ac,peak}} \right]. \tag{A-5}$$

In addition, it has been found that the ratio of $k_w = w/a$ exerts little influence on the design results. A value of $k_w = 3.0$ is fixed for simplicity with one less variable.

The following two equations are obtained from the magnetic analysis in Chapter 3:

$$N \cdot A_c = v_{cm,\max} / 2\pi \cdot f_{sw} \cdot B_{cm,c\_peak}\,, \tag{A-6}$$

$$B_{cm,c\_peak} = \frac{\Phi_{cm}}{A_c} = \frac{N \cdot i_{cm,\max}}{l_c} \cdot \mu_0 \mu_r\,. \tag{A-7}$$

Substitution of (A-3) and (A-2), respectively, into (A-6) and (A-7) derives the geometry r expressed by a and $i_{cm,max}$,

$$r = \frac{\mu_0 \mu_r \cdot v_{cm,\max} \cdot i_{cm,\max}}{\left(2\pi \cdot B_{cm,c\_peak}\right)^2 \cdot f_{sw} \cdot SF \cdot k_w \cdot a^2} - \frac{a}{2}. \tag{A-8}$$

With r and $a > 0$, the constraints of

$$\left(\frac{2\mu_0 \mu_r \cdot v_{cm,\max} \cdot i_{cm,\max}}{\left(2\pi \cdot B_{cm,c\_peak}\right)^2 \cdot f_{sw} \cdot SF \cdot k_w} \right)^{1/3} > a > 0, \tag{A-9}$$

is imposed on the variable a. Given the specifications reviewed in Table A-1, the integrated choke can be designed by expressing all parameters as functions of a in the domain of (A-9), including the CM inductance $L_{cm,w}$ as well as weights of the core, copper and the whole choke, W_{tfe}, W_{tcu} and W_{tc}.

The design steps of the integrated choke are listed below:

Step 1. Determine the definition domain of a:

In (A-9), except for $i_{cm,max}$ which depends on the CM inductance $L_{cm,w}$, all the other parameters have been know, where B_{cm,c_peak} = 0.0954 T, calculated from (3-19) and (3-20) with the assumption of B_{sat} = 0.8 T. In order to acquire a conservative upper bound of a, a high CM magnetizing current should be designated or we suppose a low CM inductance, e.g., letting $L_{cm,w} = L_{dm}$, which results in 9.50 cm > a > 0. The geometric parameters w and b are both proportional to a, whereas the calculation of r is complex and given in *Step 3*.

Table A-1 Design specifications for the integrated choke.

Converter ratings		Integrated choke specifications	
Rated power	5 kW	Maximum CMV, $v_{cm,max}$	191.5 V
Rated voltage (line-to-line, rms)	208 V	DM inductance, L_{dm}	2.76 mH
Fundamental frequency, f_1	60 Hz	Flux density saturation, B_{sat}	0.8 T
Switching frequency, f_{sw}	5000 Hz	Relative permeability, μ_r	4250
Rated current, I_{ac}	13.88 A	Current density, J	300 A/cm^2
DC voltage, v_{dc}	383 V	Window filling factor, WF	0.4

Step 2. Calculate the number of turns N:

According to(A-6), the number of turns N is a simple function of a

$$N = \frac{v_{cm,\max}}{2\pi f_{sw} \cdot B_{cm,c\_peak} \cdot SF \cdot k_w \cdot a^2}. \tag{A-10}$$

This function is drawn in Fig. A-2, where the number N has been rounded to an integral. It is observed that when $a < 0.5$ cm, the number of turns would be very high, exceeding 1000, which is impractical in manufacture. Hence, we only plot the curve within the range of $1 \le N \le 1000$ for the demonstration with clear values of N. The following figures will also be extracted without loss of the realistic solutions in the similar way.

Step 3. Calculate the inner radius of the ring core r:

The winding area equation of

$$WF \cdot W_a = N \cdot \frac{\sqrt{I_{ac}^2 + \left(i_{cm,\max}/3\right)^2}}{J}, \tag{A-11}$$

where

$$W_a = \left(\pi r^2 - 3rb + \frac{\sqrt{3}}{4} b^2 \right) \Big/ 3, \tag{A-12}$$

provides an implicit function for the geometric parameters r versus a, by omitting another unreasonable solution. Fig. A-3 plots the resultant curve of r with a in its domain.

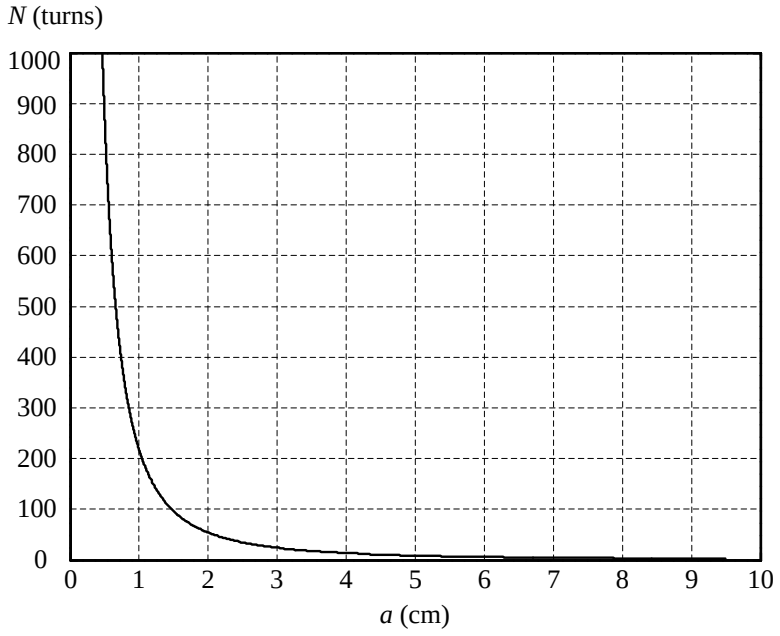


Fig. A-2 Relation curve between the number of turns N and the geometric variable a.

Step 4. Calculate the theoretical air-gap length l_g:

The air-gap length l_g is calculated from the DM inductance requirement:

$$l_g \approx \frac{N^2 \cdot \mu_0 \left(A_b / \sqrt{3} \right)}{L_{dm}}. \tag{A-13}$$

Fig. A-4 shows the change of l_g with a.

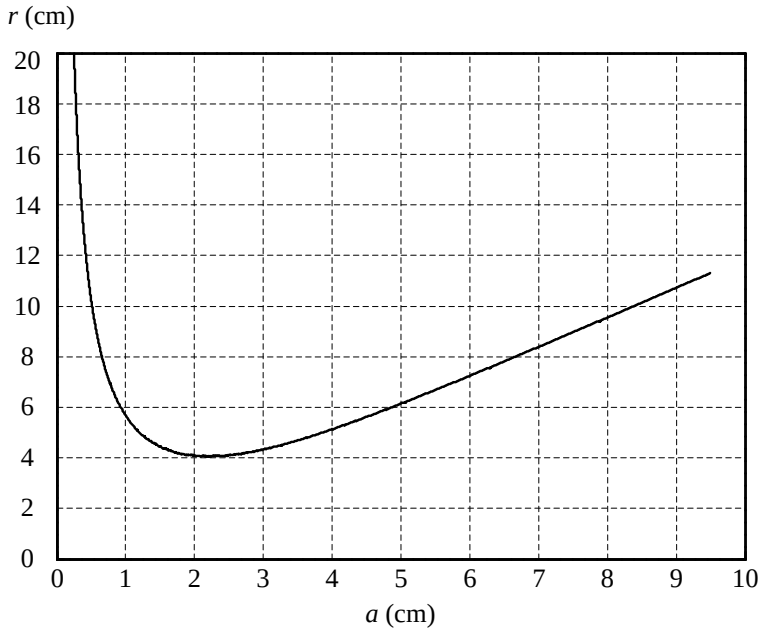


Fig. A-3 Curve of the geometric parameter r as a function of a.

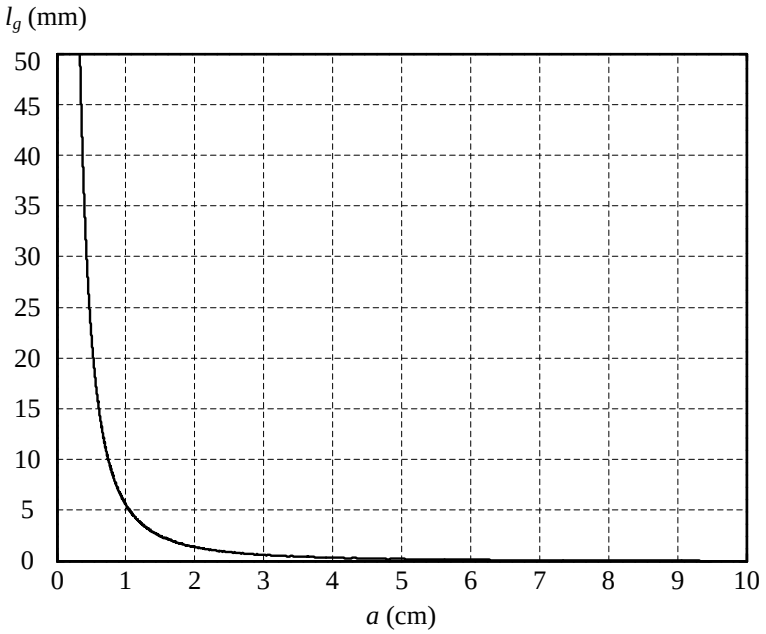


Fig. A-4 Change of the theoretical air-gap length l_g with a.

Step 5. Select a wire from the American Wire Gauge (AWG) Table:

The bare wire size is calculated by

$$A_{w(b)} = \frac{\sqrt{I_{ac}^2 + \left(i_{cm,\max}/3\right)^2}}{J} = 46.327 \times 10^{-3} cm^2 . \qquad \text{(A-14)}$$

We select the wire of AWG #11 that has a copper resistance of 41.4 μΩ/cm at 20˚C and increases the current density a little to J = 333.29 A/cm^2.

Step 6. Calculate the CM inductance $L_{cm,w}$:

Up till now, the CM inductance $L_{cm,w}$ can be calculated by (3-16) from the obtained parameters and shown in Fig. A-5. The CM inductance gives the CM magnetizing current and the CM-to-DM inductance ratio $L_{cm,w}/L_{dm}$ that was regarded an important factor for the integrated choke in Chapter 3.

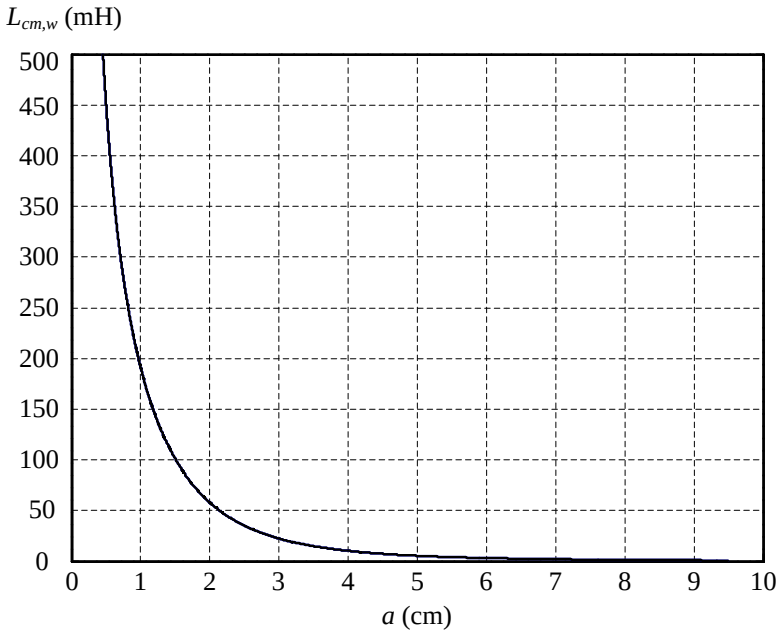


Fig. A-5 Curve of the whole CM inductance $L_{cm,w}$ versus the geometric variable a.

Step 7. Calculate the coil mean length per turn *MLT*:

The mean length per turn *MLT* of coils is estimated by complicated derivations from the core geometric parameters. The curve of *MLT* is plotted in Fig. A-6.

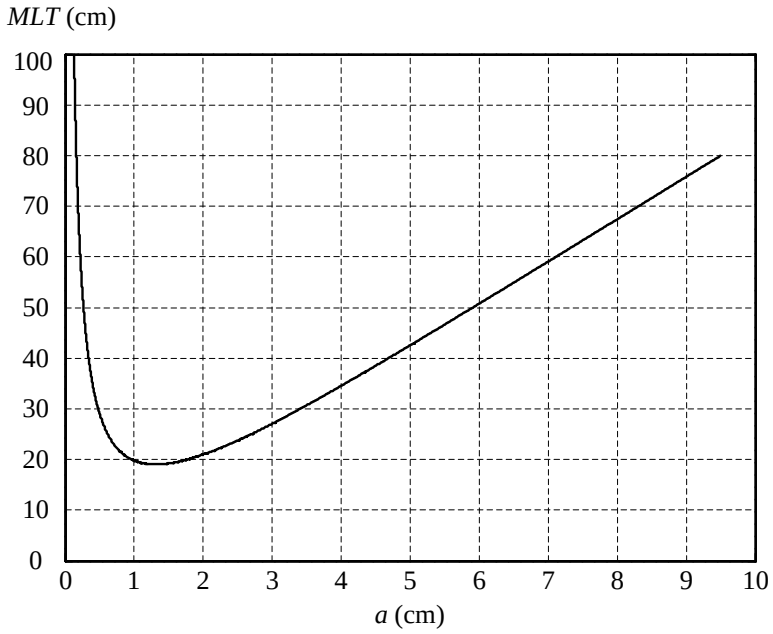


Fig. A-6 Curve of the coil *MLT* changing with *a*.

Step 8. Calculate the weights of the core, copper and the whole choke, W_{tfe}, W_{tcu} and W_{tc}:

The weight of the core is calculated from the iron density and its volume,

$$W_{tfe} = \rho_{fe}\left\{w\cdot\pi\left[\left(r+a\right)^2 - r^2\right] + w\cdot\left(3rb - \sqrt{3}b^2/4\right)\right\}, \tag{A-15}$$

where ρ_{fe} = 7.63 g/cm^3. The weight of the copper is

$$W_{tcu} = 3\rho_{cu}\cdot MLT\cdot W_a\cdot WF\,, \tag{A-16}$$

where ρ_{cu} = 8.89 g/cm^3, and *WF* is adjusted to 0.36 according to the selected wire AWG #11. Fig. A-7 draws the weight tracking versus *a*, from which the minimum total weight of 4.9573 kg is achieved at *a* = 1.5 cm approximately. Substitution of this value throughout the previous steps gives all the design parameters, involving the CM inductance or the CM-to-DM inductance ratio, whose relationship with the choke weights has been shown in Fig. 3-4. Table A-2 lists the optimized parameters.

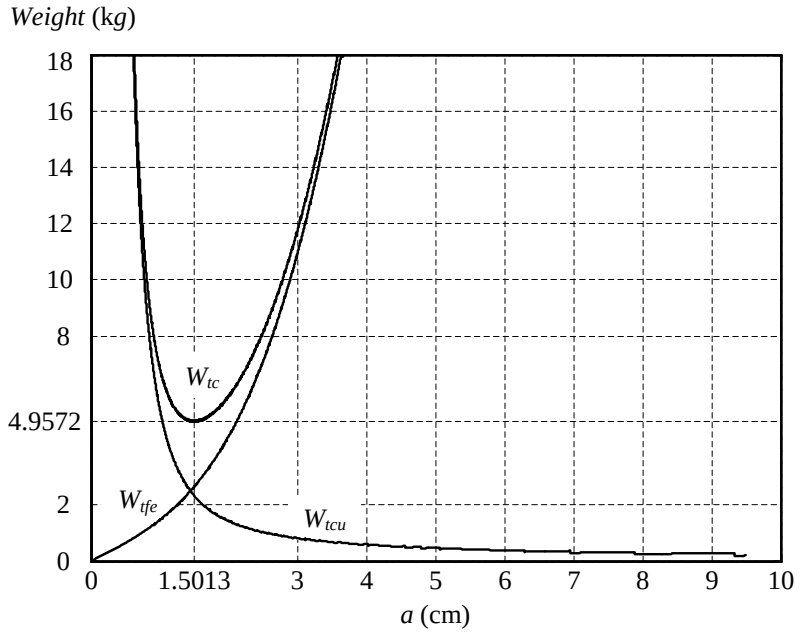


Fig. A-7 Curves of the core, copper and the total weight, W_{tfe}, W_{tcu} and W_{tc} versus the geometric variable *a*.

Table A-2 Optimized parameters of the integrated choke.

Core data: 50W310 silicon steel laminations, μ_r = 4250, *SF* = 0.98, *WF* = 0.36		Coil data: AWG #11, *J* = 333.29 A/cm^2		Weights	
w	4.5039 cm	*N*	96	W_{tcu}	2.3034 kg
a	1.5013 cm	*MLT*	19.2055 cm	W_{tfe}	2.6538 kg
r	4.4415 cm			W_{tc}	4.9572 kg
b	2.2904 cm				
l_g	2.47 mm				

Tuning and adjustment of the parameters are needed to compensate the fringing effect and accommodate the changed flux densities, as done in Chapter 3. With the finally determined parameters, the last step is to check the heat dissipation of the choke.

Step 9. Evaluate the losses and temperature rising:

With N = 88, MLT = 19.60 cm (tuned and adjusted in Chapter 3) and the AWG #11 copper resistance of 41.4 μΩ/cm, the total copper loss is calculated by

$$P_{cu} = 3N \cdot MLT \cdot \frac{\mu\Omega}{cm} \times 10^{-6} \cdot \left(I_{ac}^2 + \left(i_{cm}/3 \right)^2 \right) = 41.2323W .$$

The tuning of number of turns from N = 96 to 88 increases the mean CM flux density to B_{cm,c_peak} = 0.1041 T. The DM flux densities in the circumference and bridge legs also rise with the same proportion. The core losses provided by the manufacture's datasheets are 11.3 W/kg at f_{sw} = 5000 Hz and 0.7 W/kg at f_1 = 60 Hz (at their respective rms flux densities). With the weights of the ring and the whole core, the core losses are estimated as follows:

$$P_{fe,cm} = 11.3 \times 2 = 22.6W ;$$

$$P_{fe,dm} = 0.7 \times W_{tfe} = 2.163W ;$$

$$P_{fe,total} = 22.6 + 2.163 = 24.763W .$$

Considering an air-cooled condition, the average temperature rising T_r can be predicted via an empirical equation and the evaluation of the choke's surface area A_t = 887.2656 cm^2 [125],

$$T_r = 450 \cdot \left(\frac{P_{cu} + P_{fe}}{A_t} \right)^{0.826} = 52.5923°C .$$

It should be mentioned that the gap losses have not been involved in the loss estimation and temperature rising prediction. In fact, the special structure of the choke makes it difficult to calculate the gap losses. However, since no high-frequency CM flux flows through the gaps, the losses should be limited and only make slight contributions to the temperature rising.

Appendix B

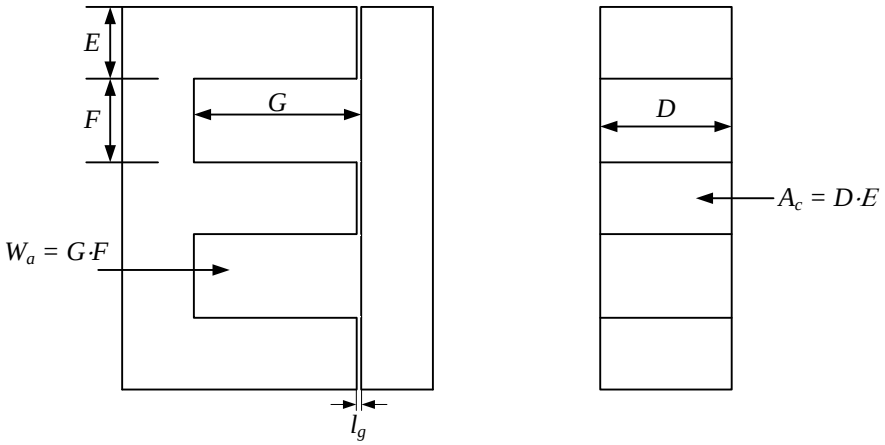
Design Parameters of Separate Inductors

DM and CM separate inductors are both designed by using the area product A_p approach. Whereas the objective of the former is to minimize the size and weight with the maximum flux density close to saturation, the latter should be optimized in terms of the minimum total loss.

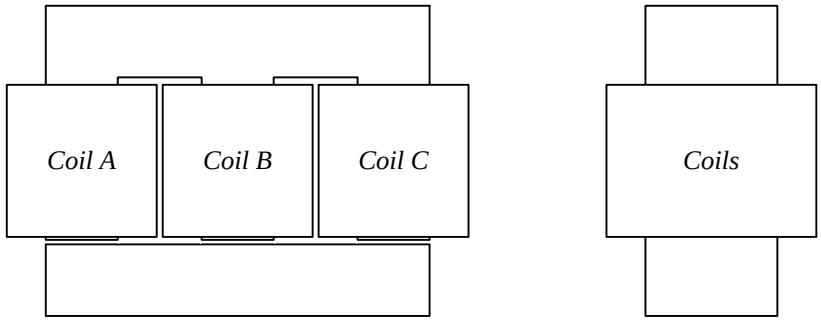
In the separate DM inductor design, the maximum flux density is set the same as that in the integrated choke, i.e., B_{max} = 0.8 T. Table B-1 lists the parameters. The number of turns N has been tuned with an empirical equation for the fringing effect compensation, which leads to an increase in B_{max} to approximately 0.9 T. Fig. B-1 illustrates the outline of the three-phase EI core and the DM inductor assembly [125, 127].

Table B-1 Design parameters of the weigh-minimized three-phase DM inductor.

Core data: three-phase EI laminations, Part No.: 875EI3P - 2, $A_p = 1.5 \cdot W_a \cdot A_c$ = 251.643 cm^4		Coil data: AWG #11	
Stack build, D	4.445 cm	Number of turns, N (designed)	72
Leg width, E	2.223 cm	Number of turns, N (tuned)	64
Window width, F	2.779 cm	Mean length per turn, MLT	18.5 cm
Window height, G	6.111 cm		
Air-gap length, l_g (designed)	2.2 mm		
Weight		Maximum losses and temperature rising	
Copper	1.677 kg	Copper ohmic loss	28.12 W
Core	3.670 kg	Core & gap losses	5.34 W
Total	5.347 kg	Temperature rising	41.15˚C



(a)



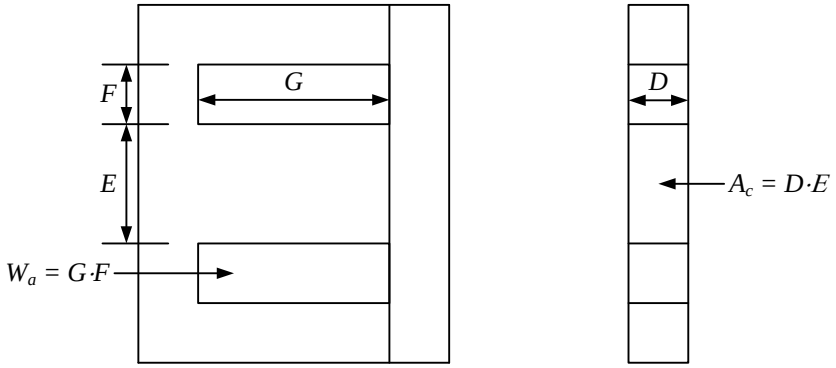
(b)

Fig. B-1 Mechanical outlines of the separate DM inductor. (a) Core of three-phase EI laminations. (b) DM inductor assembly.

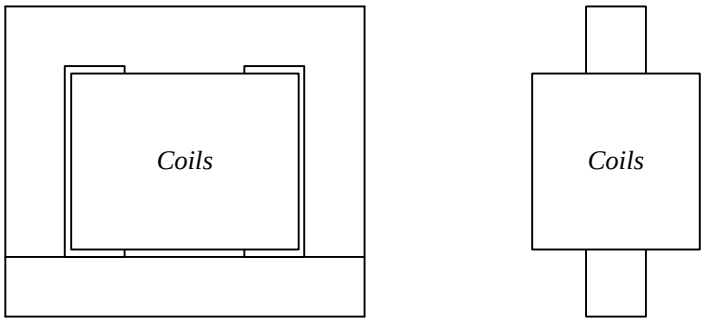
For a fair comparison, another requirement that the CM inductance should be close to that of the integrated choke is imposed on the CM reactor design, besides the loss minimization. A minor CM maximum flux density at $B_{cm,max}$ = 0.07 T is finally determined in the iterative optimization. The same relative permeability μ_r = 4250 as in the integrated choke design is also assumed. As shown in Fig. B-2, the CM choke construction does not contain air gaps. There is thus no need to adjust the parameters. Table B-2 gives the design parameters [125, 127].

Table B-2 Design parameters of the loss-optimized CM choke.

Core data: standard EI laminations, Part No.: 212EI - .5, $A_p = W_a \cdot A_c = 318.275\ \text{cm}^4$		Coil data: AWG#11	
Stack build, D	2.699 cm	Number of turns, N	69
Leg width, E	5.398 cm	Mean length per turn, MLT	25.3 cm
Window width, F	2.699 cm		
Window height, G	8.096 cm		
Weight		**Maximum losses and temperature rising**	
Copper	1.964 kg	Copper ohmic loss	41.76 W
Core	3.564 kg	Core loss	35.64 W
Total	5.528 kg	Temperature rising	65.29˚C



(a)



(b)

Fig. B-2 Outlines of the CM choke. (a) Core of standard EI laminations. (b) CM choke construction.

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Glossary of Acronyms

ABB	Asea-Brown-Boveri
ANPC	Active Neutral-Point Clamped
AZS	Active-Zero-State
BVR	Bearing Voltage Ratio
CM	Common-Mode
CMV	Common-Mode Voltage
CSC	Current-Source Converter
CSI	Current-Source Inverter
CSR	Current-Source Rectifier
DE	Drive-End
DM	Differential-Mode
DSP	Digital Signal Processor
EDM	Electrical Discharge Machining
EMI	Electromagnetic Interference
ESIM	Electrostatic Shielded Induction Machine
FEA	Finite Element Analysis
FEM	Finite Element Method
FFT	Fast Fourier Transform
FPGA	Field-Programmable Gate Array
GFCI	Ground Fault Current Interruption

GTO	Gate Turn-Off Thyristor
HERIC	Highly Efficient and Reliable Inverter Concept
IGBT	Insulated Gate Bipolar Transistor
IPD	In-Phase Deposition
LCL	Inductor, Capacitor and Inductor
LISN	Line Impedance Stabilization Network
LV	Low-Voltage
MEA	More-Electric Aircraft
MMF	Magnetomotive Force
MPPT	Maximum Power Point Tracking
MV	Medium-Voltage (2.3 kV – 13.8 kV)
NDE	Nondrive-End
NPC	Neutral-Point Clamped
NTS	Nearest-Three-State
NZS	Nonzero-State
pu	Per Unit
PV	Photovoltaic
PWM	Pulse-Width Modulation
RC	Resistor and Capacitor
RL	Resistor and Inductor
rms	Root Mean Square
rpm	Revolutions Per Minute
RTS	Remote-Three-State
SCR	Silicon Controlled Rectifier (Thyristor)

SHE	Selective Harmonic Elimination
SPWM	Sinusoidal Pulse-Width Modulation
SVM	Space-Vector Modulation
THD	Total Harmonic Distortion
TPWM	Trapezoidal Pulse-Width Modulation
V/F	Voltage/Frequency
VOC	Voltage Oriented Control
VSC	Voltage-Source Converter
VSI	Voltage-Source Inverter
VSR	Voltage-Source Rectifier